The 555 Timer

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ECE 20007: EE Fundamentals I Lab

Pujary (007)

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Introduction

The 555 Timer integrated circuit was invented in 1971 by Swiss electronics engineer Hans Camenzind while working for Signetics. Hans was tasked with developing a precision timing device, but after coming up with the initial design, he revised the design, and it expanded to become one of the most popular and versatile integrated circuits (IC) in electronics (Atwell 2022).

The 555 timer operates using internal voltage dividers, comparators, and a flip-slop to monitor the charging and discharging of an external capacitor. By controlling these transitions, it generates precis timing pulses or oscillations.

The 555 can operate as a variety of applications including as a timer, pulse generator, oscillator, and flip-flop element. Its simple 8 pin design allows the IC to be reliable, simple, and low cost making its use in electronics widespread from pulse-width modulation (PWM) circuits and frequency generators to time-delay circuits and LED flashers (HowToMechatronics, 2018).

The 555 Timer can operate in multiple configurations, most notably monostable and astable modes. In monostable mode, the circuit produces a single output pulse when triggered by an external input. The length of the pulse, known as a pulse width, is determined by the external resistance and capacitor values. For example, in monostable mode, if the 555 Timer is connected to a circuit with a resistance and capacitance that equals a pulse width of 1 second, when the 555 is triggered by the input source, it outputs a voltage for 1 second and then stops. Every time the 555 is triggered, it will output voltage for 1 second. Changing the circuit's resistance and capacitance will change how long voltage output is for. Monostable mode is commonly used in timers, pulse-width generators, switch debouncers, and delay circuits.

In contrast, in astable mode, the circuit oscillated continuously without requiring an external trigger. This generates a continuous square wave output. The frequency of how quick the 555 triggers on and off a voltage output is determined by resistance and capacitance of the circuit just like in monostable. The circuit uses two resistors, R_A and R_B, and a Capacitor, C_1 to alternatively charge and discharge the capacitor between $\frac{1}{3}$ and $\frac{2}{3}$ of the supply voltage through the internal discharge transistor inside the 555 Timer. There are two calculated values associated with astable mode being frequency and duty cycle. The frequency is the rate at which the periodic output signal repeats. The duty cycle quantifies the proportion of that signal period during which the output remains at a high logic level. In practical terms, a higher duty cycle means the output remains "on" longer relative to its "off" duration. Adjusting R_A, R_B, and C_1 allows fine control of the output waveform. Astable configurations are commonly used for LED blinkers or dimmers, clock pulses, tone generation, and pulse-width modulator circuits.

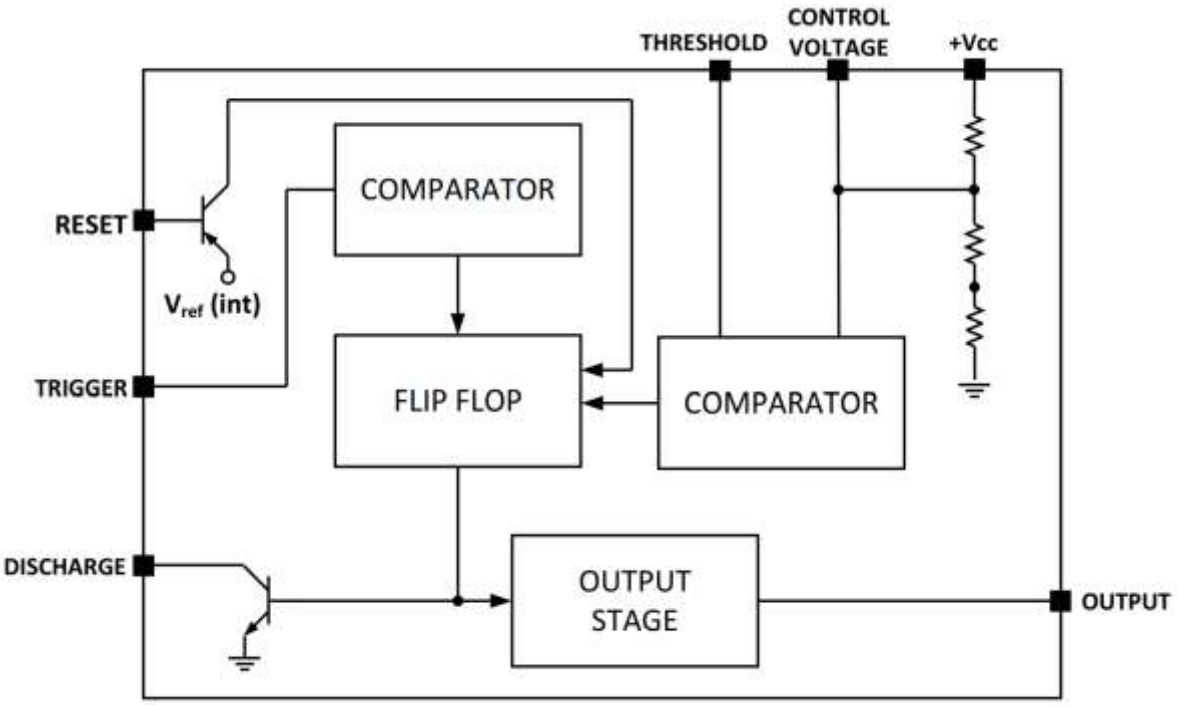
The objective of this project is to experimentally analyze and verify the operations of the 555 Timer in both its monostable and astable configurations. First, this project aims to build knowledge of how each mode operates by designing, simulating, and testing the circuits. The first part involved creating a monostable circuit capable of producing a single pulse of a certain

duration when triggered. Next, switch the 555 Timer to the astable configuration and create an oscillator that continuously produces a square wave signal with specific periods and duty cycles. After building these circuits, analyze the output of each through theoretical calculations, LTSpice simulations, and finally oscilloscope measurements.

The second part of this project requires using the 555 Timer as an application circuit to demonstrate real-world use of the integrated circuit. Similar calculations, simulation, and testing are required in this part. This report will dive into the application of a PWM-based LED brightness controller using the 555 Timer. The particular interest of this application is the fine line between frequency and duty cycle when creating time-based lighting. If the period is too long, the LED will blink instead of lose or gain brightness. So instead of building a dimmable lighting system, a flashing light is created which is not the intended effect. Instead, careful calculations and circuit set up are needed to allow the 555 Timer to control LED brightness. This complex relationship of frequency and duty cycle in astable mode and careful understanding of this IC and its surrounding components is why an LED brightness controller holds particular interest in this project.

Theory

The 555 Timer is a precision integrated circuit that is capable of generating timed outputs. It is composed of a voltage divider network, two comparators, a flip-flop, a discharge transistor, and an output stage. These internal components function together to monitor and control the voltage across an external capacitor when produced a stable timing behavior on its output pin.



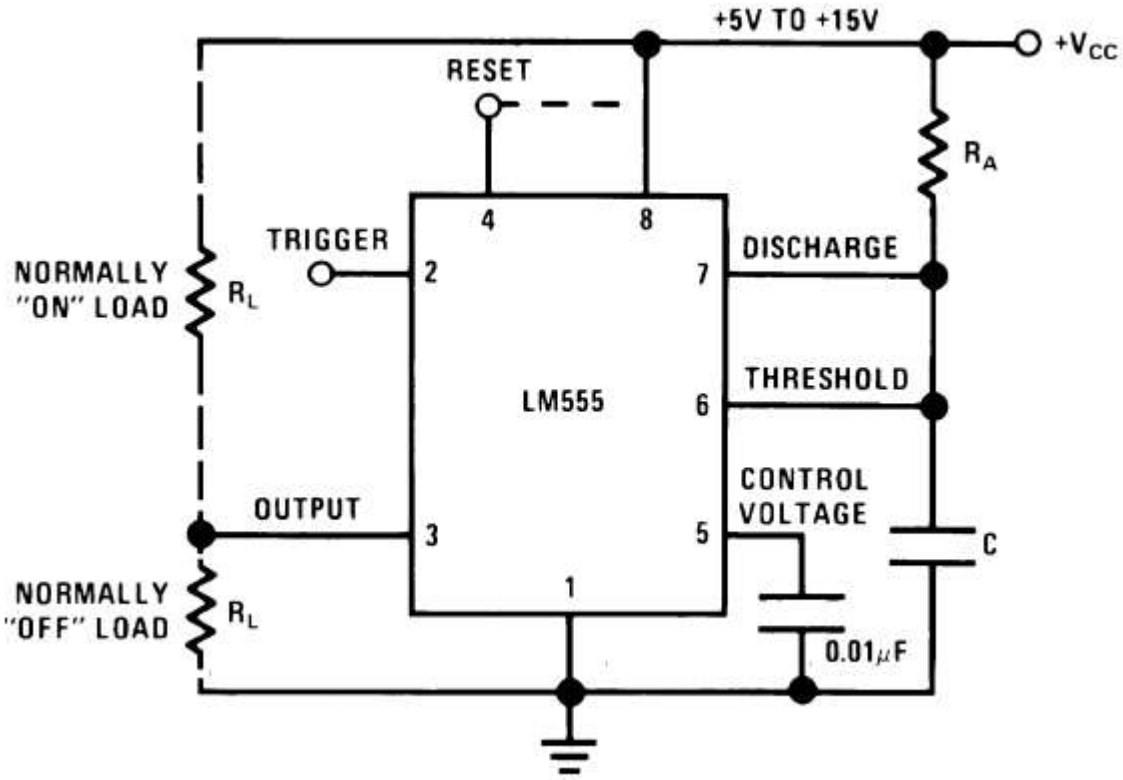
Internal Block Diagram of the 555 Timer. Adapted from LM555 Precision Timer Datasheet (Rev. D) by Texas Instruments, 2022, p. 3 (https://www.ti.com/lit/ds/symlink/lm555.pdf).

Overview of the 555 Timer

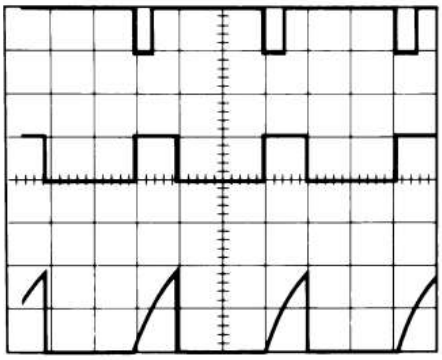
- The voltage dividers consist of three equal resistors, typically 5 kΩ, that are connected in series between the supply voltage, V_{CC} and ground. This configuration divides the input voltage into reference levels of $\frac{1}{3}V_{CC}$and $\frac{2}{3}V_{CC}$, which are used by the comparators to set and reset the flip-flop.
- Comparator 1, which is connected to the trigger pin, compares the voltage on the trigger pin (Pin 2) with $\frac{1}{3}V_{CC}$. When the trigger voltage drops below $\frac{1}{3}V_{CC}$, the compactor output sets the flip-flop to turn the output high (on).
- Comparator 2 monitors the threshold pin (Pin 6) and resets the flip-flop when the external capacitor voltage exceeds $\frac{2}{3}V_{CC}$. This drives the output low and activates the discharge transistor.
- The flip-flop stores the logic state of the output and is set by the trigger comparator and reset by the threshold comparator or the external reset pin (Pin 4).
- The discharge transistor (Pin 7) discharges the external timing capacitor to ground when the flip-flop output goes low.
- The output stage (Pin 3) is a push-pull amplifier that can source or sink the circuit enabling the timer to drive LEDs, speakers, and logic inputs directly.
- The control voltage (Pin 5) provided external access to $\frac{2}{3}V_{CC}$ reference level, allowing for modulation of the timing interval. Usually, it is bypassed with a small capacitor (0.01 μF) to ground for noise stability.
- Finally, the reset pin (Pin 4) overrides all internal functions and forces the output to a low state, when triggered. In most applications, the pin is tied to the supply voltage to disable manual reset.
- Overall, the 555 Timer's operation is governed by charging and discharging an external capacitor through resistive elements, with the internal comparators determining when to switch the output state based on voltage thresholds.

Monostable Mode of Operation

In the monostable configuration, the 555 Timer produces a single pulse of predetermined width when triggered. It is referred to as "one-shot" mode because the circuit returns to its stable (low) state after the output pulse completes (Texas Instruments, 2022).



General Circuit of 555 Timer in Monostable Mode. Adapted from LM555 Precision Timer Datasheet (Rev. D) by Texas Instruments, 2022, p. 3 (https://www.ti.com/lit/ds/symlink/lm555.pdf).



V_{CC} = 5 V
TIME = 0.1 ms/DIV.
R_A = 9.1 kΩ
C = 0.01 μF

Top Trace: Input 5V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 2V/Div.

Voltage Signal Timing Diagram for 555 Timer in Monostable Mode. Adapted from LM555 Precision Timer Datasheet (Rev. D) by Texas Instruments, 2022, p. 3 (https://www.ti.com/lit/ds/symlink/lm555.pdf).

The external resistor R and capacitor C are connected between the discharge pin (Pin 7), threshold pin (Pin 6), and ground. When a negative trigger pulse is applied to Pin 2 (causing the voltage to drop below $\frac{1}{3}V_{CC}$), the lower comparator sets the flip-flop. The output at Pin 3 immediately transitions to high, and the discharge transistor is turned off, allowing the capacitor to charge through R. When the capacitor voltage reaches $\frac{2}{3}V_{CC}$, the upper comparator resets the flip-flop, forcing the output low and discharging the capacitor via the discharge transistor. The circuit remains in its stable state (output low) until another trigger pulse is applied. The timing relationship of the monostable circuit is the most important calculation when using a 555 Timer in monostable mode. This determines when the circuit is triggered, how long the output is high for.

Key equations:

The duration of the high pulse output is determined by the RC time constant:

$$T = 1.1 \times R \times C$$

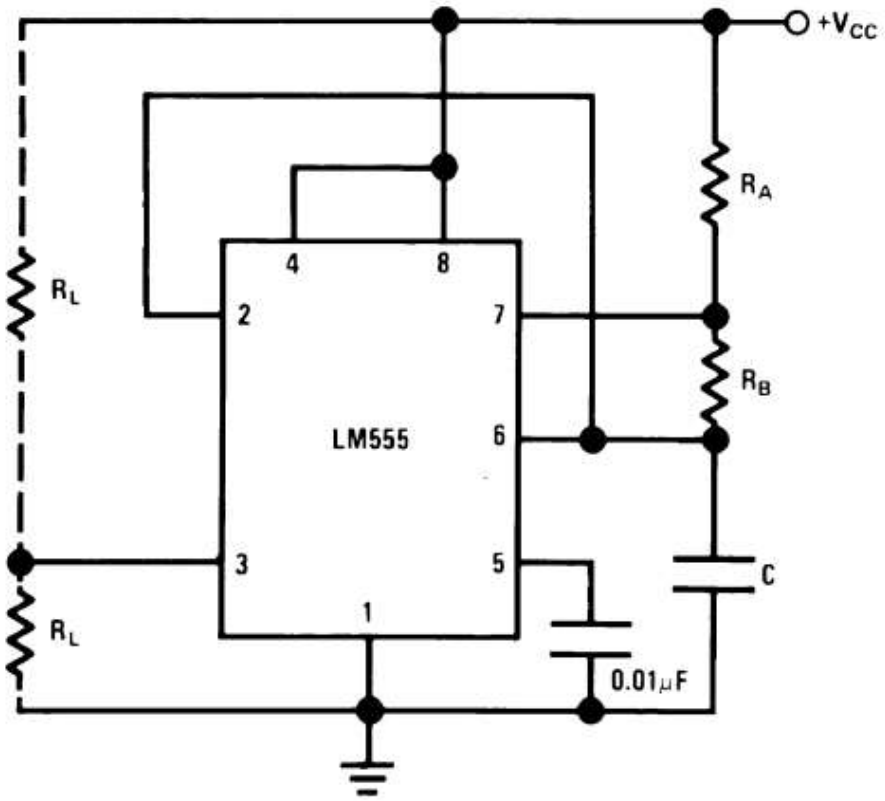
Where:

- T = output pulse width (seconds)
- R = external timing resistance (Ω)
- C = external timing capacitance (F)

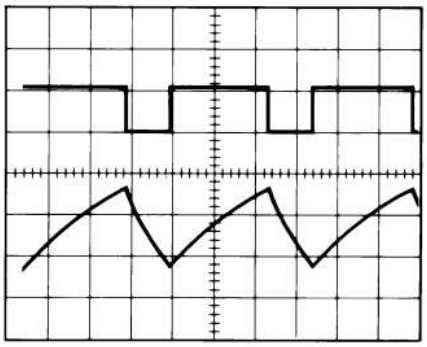
The equation accounts for the capacitor charging from 0 V to $\frac{2}{3}V_{CC}$.

Astable Mode of Operation

In astable mode, the 555 Timer produces a continuous square wave output. The circuit has no stable state, meaning it constantly alternates between charging and discharging the capacitor (Texas Instruments, 2022).



General Circuit of 555 Timer in Astable Mode. Adapted from LM555 Precision Timer Datasheet (Rev. D) by Texas Instruments, 2022, p. 3 (https://www.ti.com/lit/ds/symlink/lm555.pdf).



V_{CC} = 5 V
TIME = 20μs/DIV.
R_A = 3.9 kΩ
R_B = 3 kΩ
C = 0.01 μF

Top Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 1V/Div.

Voltage Signal Timing Diagram for 555 Timer in Astable Mode. Adapted from LM555 Precision Timer Datasheet (Rev. D) by Texas Instruments, 2022, p. 3 (https://www.ti.com/lit/ds/symlink/lm555.pdf).

Two resistors, $R_A$and R_B, and one capacitor C_1 determine the frequency and duty cycle. During the charging phase, the capacitor charges through both $R_A$and R_B. Once the voltage across the capacitor reaches $\frac{2}{3}V_{CC}$, the upper comparator resets the flip-flop, turning on the discharge transistor and pulling Pin 7 to ground. The capacitor discharges through $R_B$until its voltage drops below $\frac{1}{3}V_{CC}$, setting the flip-flop again, turning off the discharge transistor, and restarting the charging phase.

Key Equations:

- Time High:

$$T_{High} = 0.693 \times (R_A + R_B) \times C$$

- Time Low:

$$T_{Low} = 0.693 \times R_B \times C$$

- Total Period:

$$T = T_{High} + T_{Low} = 0.693 \times (R_A + 2R_B) \times C$$

- Frequency:

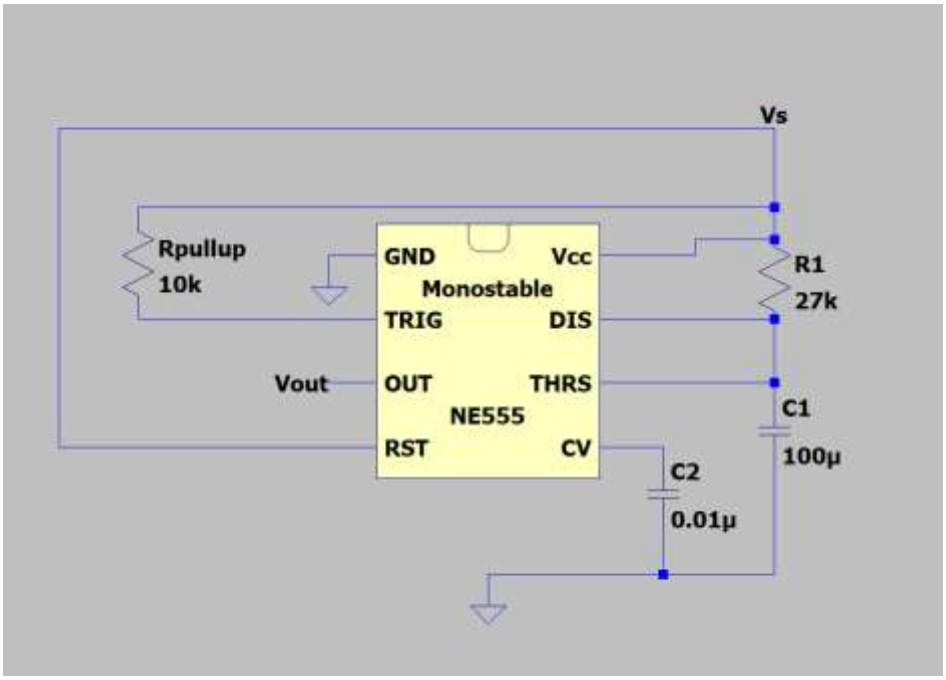
$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B) \times C}$$

- Duty Cycle:

$$D = \frac{THigh}{T} \times 100 = \frac{R_A + R_B)}{(R_A + 2R_B)} \times 100$$

Experimental Procedure

Monostable Mode



Monostable 555 Timer Circuit Schematic (3 second period)

3s Monostable Circuit Parameter Calculations:

$$T = 1.1 \times R \times C$$

T = 3 seconds, choose C_1 to be 100 µF.

$3s = 1.1 \times R \times 100\mu F$

$R \sim 27\ k\Omega$

Check:

T = 1.1 × 27k Ω × 100 µF = 2.97 seconds ≈ 3 seconds

Parameter	Calculated Value	Equation/ Reasoning
R_1	27 kΩ	$T = 1.1 \times R \times C$
C_1	100 µF	$T = 1.1 \times R \times C$
C_2	0.01 µF	General value for control voltage pin

$R_{Pull-up}$	10 kΩ	General value for a pull-up resistor

Parameter Calculations for Monostable 555 Timer Circuit (3 second period)

Procedure to set up this monostable circuit:

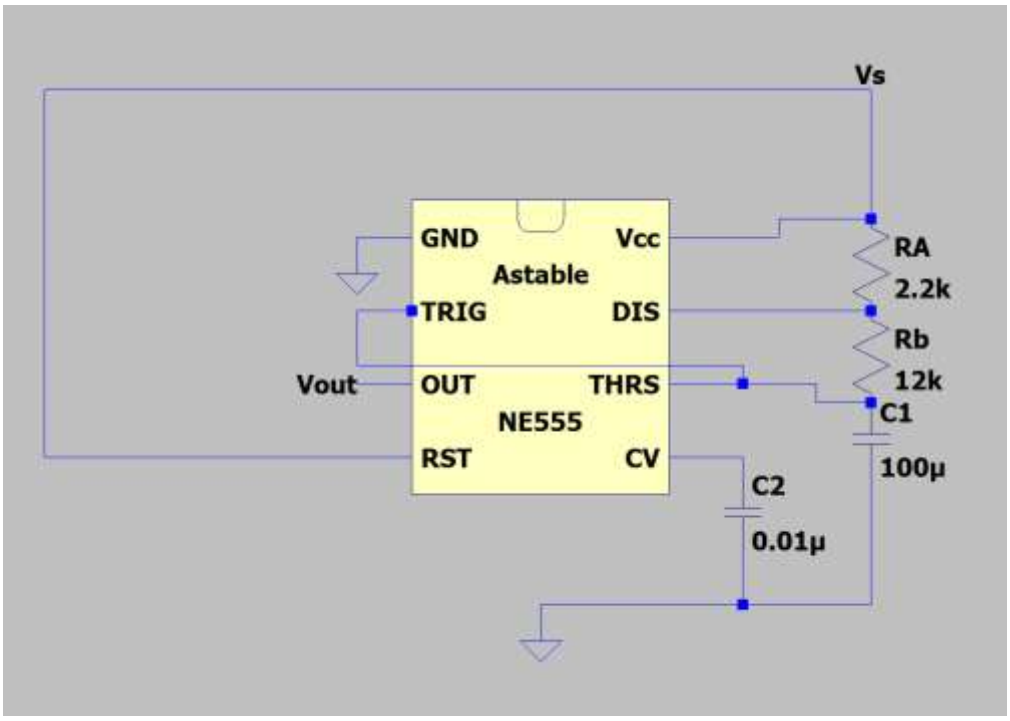
Using the standard 8-pin 555 pin numbering (pin-1 GND at upper left, pin-8 VCC upper right when notch faces up).

1. Power and ground
    a. Pin 1 → GND.
    b. Pin 8 → +5 V (VCC).
2. Reset
    a. Pin 4 (RESET) → +5 V (tie high so reset is disabled).
3. Control voltage
    a. Pin 5 → connect C_2 = 0.01 µF from pin 5 to ground
4. Timing network
    a. Pin 6 (THRESHOLD) → Node A.
    b. Pin 7 (DISCHARGE) → Node A.
    c. One side of C_1 (100 µF) → Node A; the other side of C_1 → GND.
5. Trigger (Pin 2) and pull-up
    a. Pin 2 (TRIGGER) → to +5 V via R_pullup = 10 kΩ (pull-up).
    b. Also connect push button between pin 2 and GND. When the button is pressed, pin 2 is pulled to ground → trigger event.
6. Output
    a. Pin 3 → Output node. Attach an oscilloscope probe to the output pin and ground the probe with another wire.

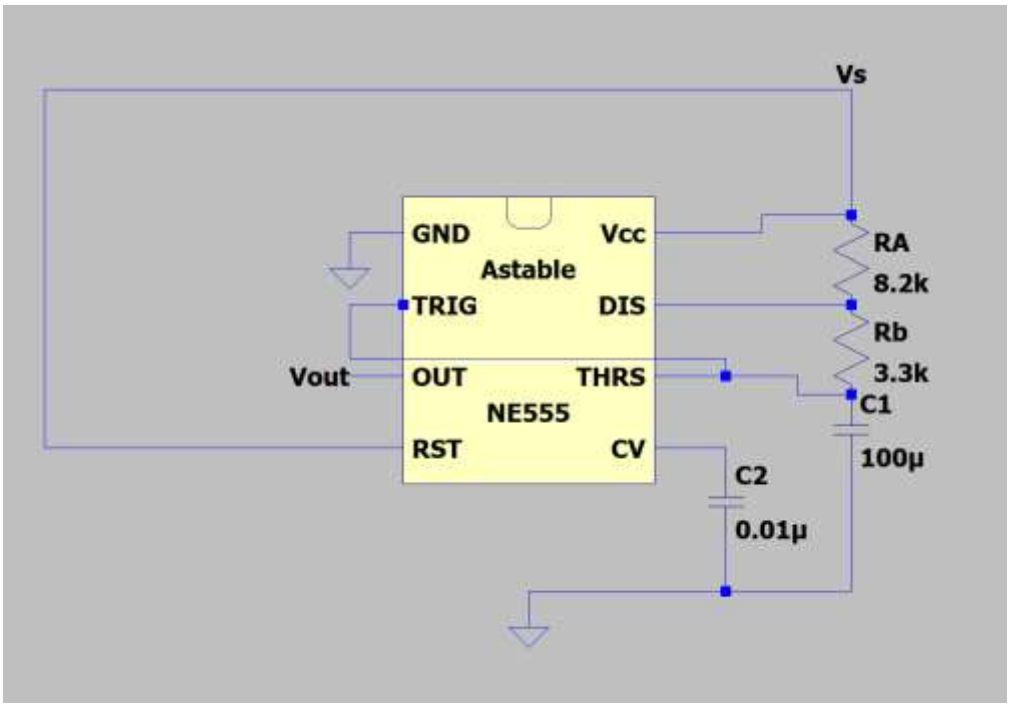
Testing:

With nothing pressed, output should be low. Press the push button (trigger). On release, the circuit should produce a single high pulse at pin 3 of approximately 3.0 s and then return low. Use the oscilloscope to capture this pulse for analysis.

Astable Mode



Astable 555 Timer Circuit Schematic (2 second period, 60% Duty Cycle)



Astable 555 Timer Circuit Schematic (1 second period, 75% Duty Cycle)

2s Astable Circuit Parameter Calculations:

$$T = T_{High} + T_{Low} = 0.693 \times (R_A + 2R_B) \times C$$

$$D = \frac{THigh}{T} \times 100 = \frac{R_A + R_B)}{(R_A + 2R_B)} \times 100$$

$$T_{High} = 0.693 \times (R_A + R_B) \times C$$

Choose C = 100 μF, then R_A = 2.2 kΩ, R_B = 12.2 kΩ.

$$T = 0.693(2200 + 2(12200)) \times (0.0001) = 1.843 \text{ s} \approx 2 \text{ s}$$

$$D = (2200 + 12200) \div (2200 + 2(12200)) = 54.1\% \approx 60\ \%$$

$$T_{High} = 0.693 \times (2200 + 12200) \times 0.0001 = 1.000 \text{ s}$$

$$T_{Low} = T - T_{High} = 1.843 - 1.000 = 0.843 \text{ s}$$

Parameter	Calculated Value	Equation/ Reasoning
R_A	2.2 kΩ	$T = T_{High} + T_{Low} = 0.693 \times (R_A + 2R_B) \times C$
R_B	12.2 kΩ	$T = T_{High} + T_{Low} = 0.693 \times (R_A + 2R_B) \times C$
C_1	100 μF	$T = T_{High} + T_{Low} = 0.693 \times (R_A + 2R_B) \times C$
C_2	0.01 μF	General value for control voltage pin

Parameter Calculations for Astable 555 Timer Circuit (2 second period)

1s Astable Circuit Parameter Calculations:

$$T = T_{High} + T_{Low} = 0.693 \times (R_A + 2R_B) \times C$$

$$D = \frac{THigh}{T} \times 100 = \frac{R_A + R_B)}{(R_A + 2R_B)} \times 100$$

$$T_{High} = 0.693 \times (R_A + R_B) \times C$$

Choose C = 100 μF, then R_A = 8.2 kΩ, R_B = 3.3 kΩ.

$$T = 0.693(8200 + 2(3300)) \times (0.0001) = 1.026 \text{ s} \approx 1 \text{ s}$$

$$D = (8200 + 3300) \div (8200 + 2(3300)) = 77.7\% \approx 75\ \%$$

$$T_{High} = 0.693 \times (8200 + 3300) \times 0.0001 = 0.797 \text{ s}$$

$T_{Low} = T - T_{High} = 1.026 - 0.797 = 0.229$ s

Parameter	Calculated Value	Equation/ Reasoning
R_A	8.2 kΩ	$T = T_{High} + T_{Low} = 0.693 \times (R_A + 2R_B) \times C$
R_B	3.3 kΩ	$T = T_{High} + T_{Low} = 0.693 \times (R_A + 2R_B) \times C$
C_1	100 µF	$T = T_{High} + T_{Low} = 0.693 \times (R_A + 2R_B) \times C$
C_2	0.01 µF	General value for control voltage pin

Parameter Calculations for Astable 555 Timer Circuit (1 second period)

Procedure to set up these astable circuits:

Using the standard 8-pin 555 pin numbering (pin-1 GND at upper left, pin-8 VCC upper right when notch faces up).

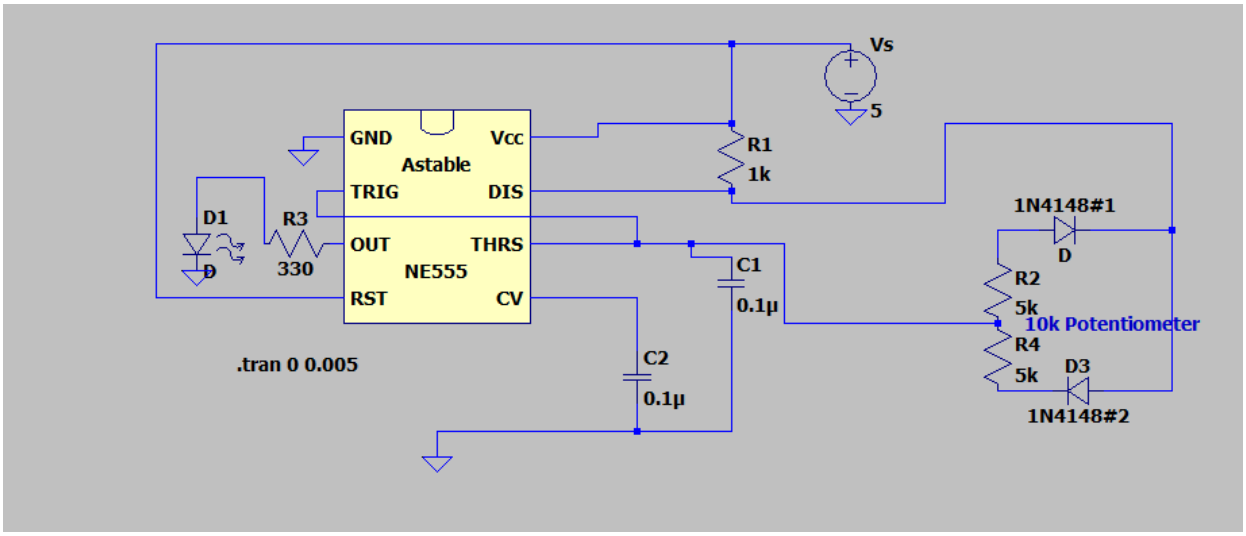
1. Power and ground
    a. Pin 1 → GND.
    b. Pin 8 → +5 V (VCC).
2. Reset
    a. Pin 4 (RESET) → +5 V (tie high so reset is disabled).
3. Control voltage
    a. Pin 5 → connect C_2 = 0.01 µF from pin 5 to ground
4. Timing network
    a. Connect Pin 2 (TRIGGER) directly to Pin 6 (THRESHOLD)
    b. R_A → between Pin 8 (VCC) and Pin 7 (DISCHARGE).
    c. R_B → between Pin 7 (DISCHARGE) and Node A (Pins 2 & 6).
    d. C = 100 µF → between Node A (Pins 2 & 6) and GND (negative terminal to ground).
5. Output
    a. Pin 3 → Output node. Attach an oscilloscope probe to the output pin and ground the probe with another wire.

Testing:

Attaching the oscilloscope probe to the output pin, and supplying the circuit with +5V, the circuit should produce a continuous square wave that alternate between 0 V and ~5 V. The period at which the voltage is high and low should be similar to the theoretical calculations of T_{High}, T_{Low}, and the duty cycle.

Application of 555 Timer

Pulse-width modulation (PWM) is a technique widely used to control the brightness of LEDs, the speed of DC motors, and more. In this application, the 555 Timer operates in astable mode to generate a PWM signal that drives an LED. By adjusting the duty cycle of the output waveform, the average voltage applied to the LED changes, which in turn varies its brightness without altering the peak voltage. This creates a circuit that when adjusting the resistance through a 10 kΩ potentiometer, the brightness of the LED changes. Decreasing the resistance through the potentiometer increases the duty cycle which, in turn, increases the brightness of the LED.



LED Dimmer Astable 555 Timer Circuit Schematic

LED Dimmer Parameter Calculations:

Choose R_1 = 1 kΩ, R_2= 10 kΩ Potentiometer (Low = 330 Ω, High =10.3 kΩ)

C_1 and C_2 = 0.1 µF, R_{Load} = 330 Ω

$$T_{High} = 0.693 \times (R_{charge} + R_A) \times C$$

$$T_{Low} = 0.693 \times R_{discharge} \times C$$

Parameter	Calculations
Time High	0.693 × (10.33 kΩ + 1 kΩ) × 0.1µF = 0.785 ms
Time Low	0.693 × 330 Ω × 0.1µF = 0.023 ms

Time Values for Full LED Brightness

Parameter	Calculations

Time High	$0.693 \times (330\ \Omega + 1\ k\Omega) \times 0.1\mu F = 0.092$ ms
Time Low	$0.693 \times 10.33k\Omega \times 0.1\mu F = 0.716$ ms

Time Values for Minimum LED Brightness

Parameter	Calculations
Time High	$0.693 \times (5.33\ k\Omega + 1\ k\Omega) \times 0.1\mu F = 0.438$ ms
Time Low	$0.693 \times 5.33\ k\Omega \times 0.1\mu F = 0.369$ ms

Time Values for Medium LED Brightness

Potentiometer Position	R_{charge} (kΩ)	$R_{discharge}$ (kΩ)	Time High (ms)	Time Low (ms)	Duty Cycle	Brightness
Min	0.33	10.33	0.092	0.716	11.4%	Dim
Mid	5.33	5.33	0.438	0.369	54.3%	Medium
Max	10.33	0.33	0.785	0.023	97.2%	Bright

Parameters for LED Dimmer

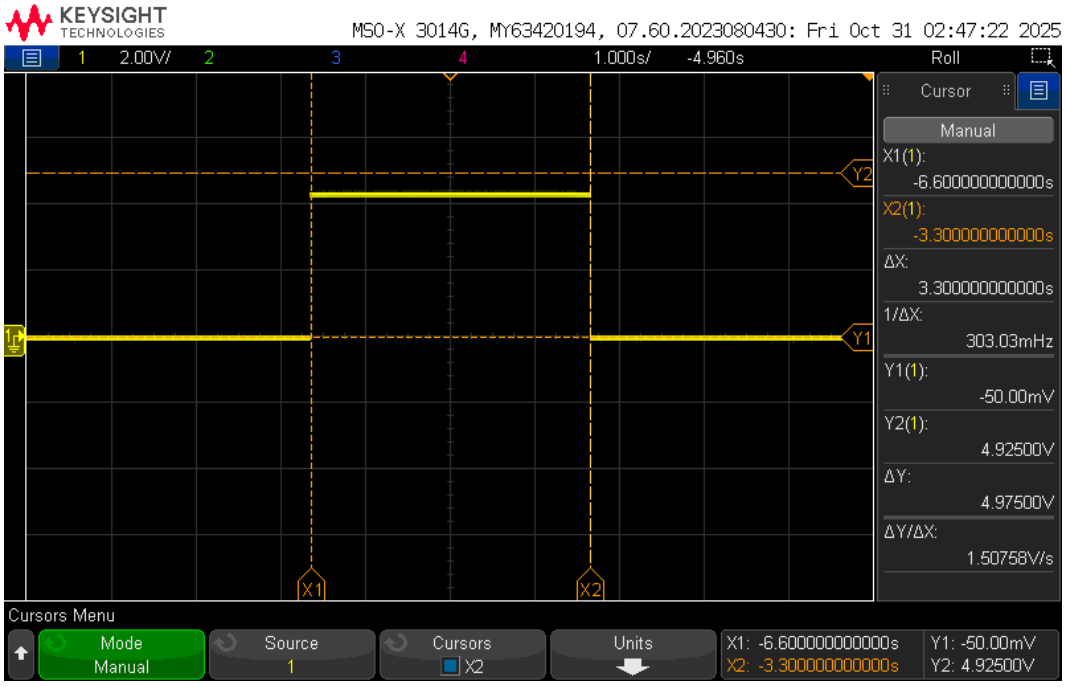
The LED dimmer circuit utilizes the 555 Timer in modified astable configuration where the major difference from the stable configuration before is the introduction of a variable resistor (potentiometer) in parallel with two 1N4148 diodes. One for charging via D_1 and a portion of the potentiometer and one for discharging via D_2 and the remaining portion of the potentiometer. When the output (Pin 3) is high, the timing capacitor C_1 charges through R_1, D_1, and the adjustable portion of the potentiometer. When the voltage across the capacitor reaches 2/3 V_{CC}, the internal threshold comparator resets the flip-flop, causing the output to switch low. The capacitor then discharges through D_2 and the other portion of the potentiometer until the voltage drops below 1/3 V_{CC}, at which point the output returns high again. By rotating the potentiometer, the resistance values in the charge and discharge paths change, effectively adjusting the ratio of T_{High} to T_{Low} (duty cycle). The frequency remains relatively constant, while the duty cycle can vary continuously from approximately 10% to 95%, depending on the potentiometer setting. Because the LED is connected to the output through a current-limiting resistor (330 Ω), its apparent brightness changes in proportion to the duty cycle of the PWM signal. At high duty cycles, the LED remains on longer per cycle, appearing bright. At low duty cycles, the LED is on for shorter durations, appearing dim.

Results

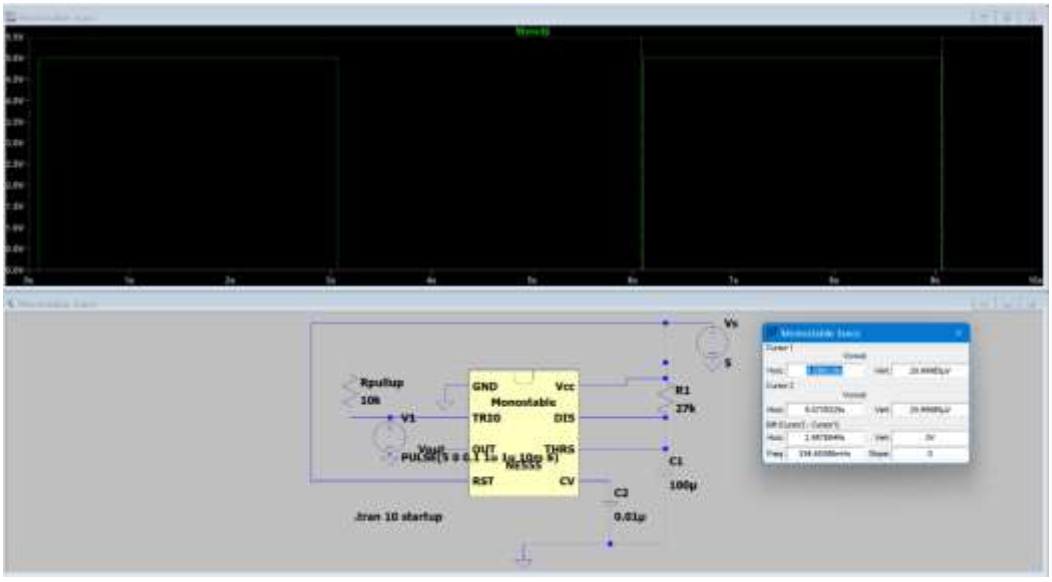
Monostable Mode

Calculated Period (s)	Simulated Period (s)	Experimental Period (s)	Percent Error (%)
2.97	2.99	3.30	11.1

3-second Monostable Circuit Measurements



Monostable 555 Timer Circuit (3s Period)



LTSpice Monostable 555 Timer Circuit (3s Period) Simulation

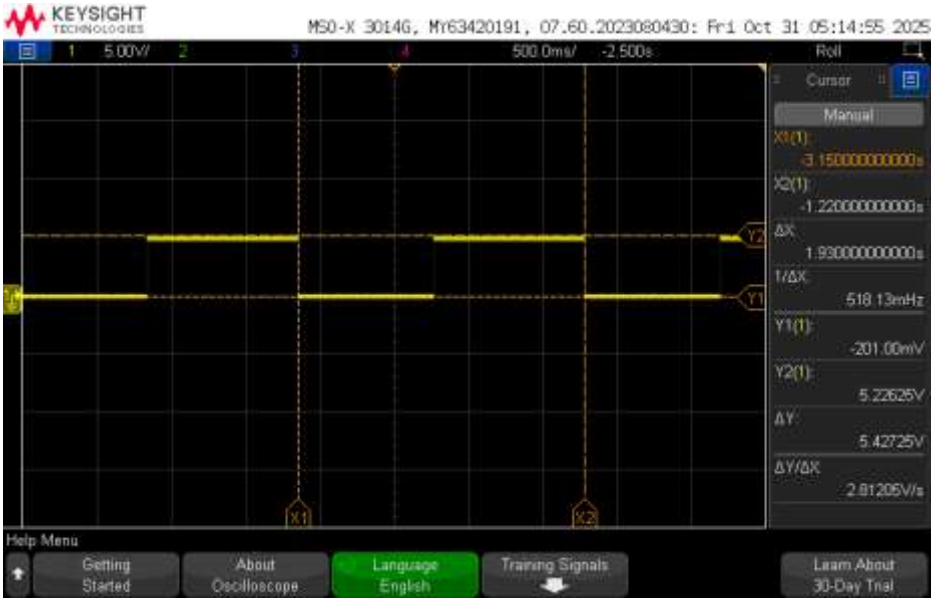
The 3-second monostable 555 Timer circuit demonstrated consistent behavior with theoretical calculations. Based on the design values of $R_1 = 27\ k\Omega$ and $C_1 = 100\mu F$, the theoretical pulse width was calculated at 2.97 seconds. The LTSpice simulation produced a pulse width of approximately 2.99 seconds, which aligns closely with the theoretical pulse width value. However, the experimental measurement using the oscilloscope resulted in a pulse width of 3.30 seconds, resulting in an 11.1% error.

This deviation is primarily attributed to component tolerances such as the ±20% variation in the electrolytic capacitor and potential resistance variation of up to ±2%. Additionally, manual triggering with a pushbutton introduces mechanical bounce, which may slightly alter the charge point. Despite these sources of error, the experimental waveform closely matched the simulated voltage curve, confirming proper one-shot behavior and demonstrating a successful 3 second monostable operation.

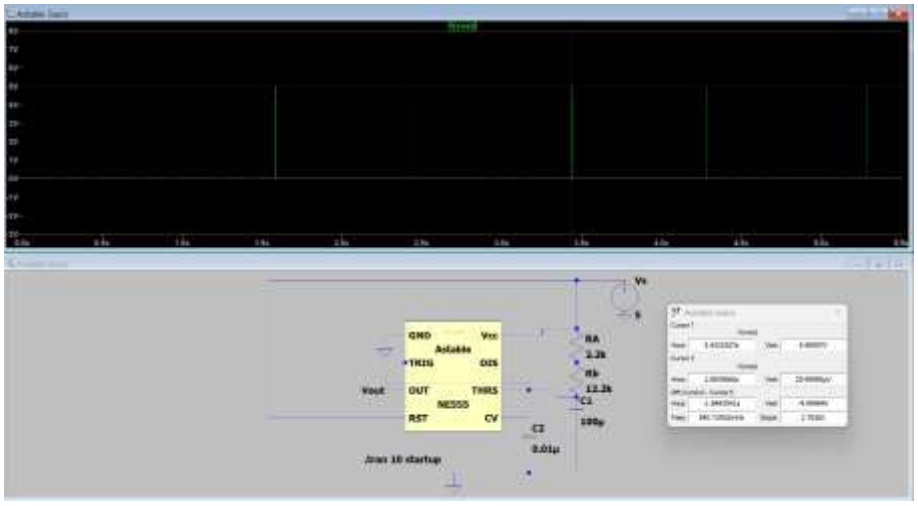
Astable Mode (2s Period)

Voltage	Calculated Period (s)	Simulated Period (s)	Experimental Period (s)	Percent Error (%)
High + Low	1.843	1.849	1.930	4.7
High	1.000	1.000	1.020	2.0
Low	0.843	0.849	0.910	7.9

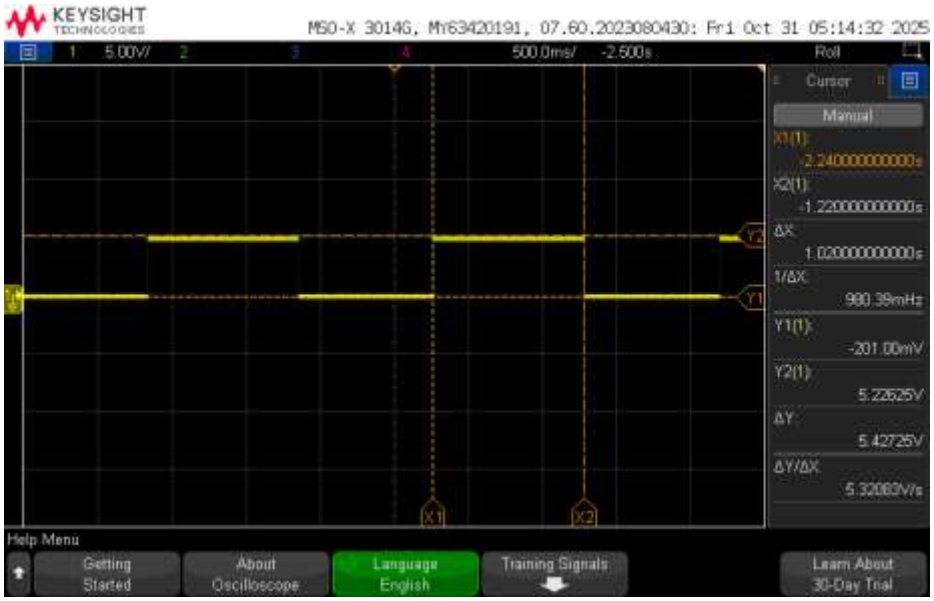
2-Second, 60% Duty Cycle Astable Circuit Measurements



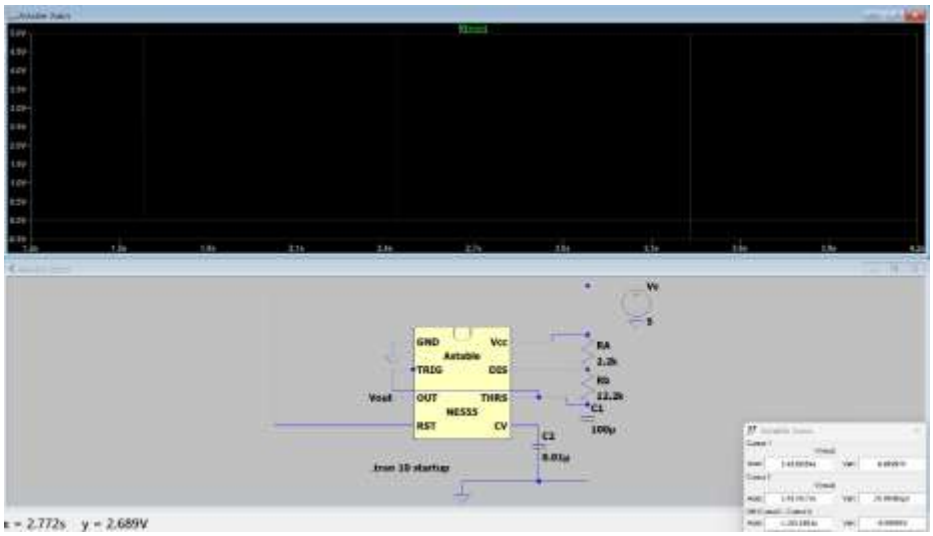
Astable 555 Timer Circuit (2 second period, 60% Duty Cycle) Full Period



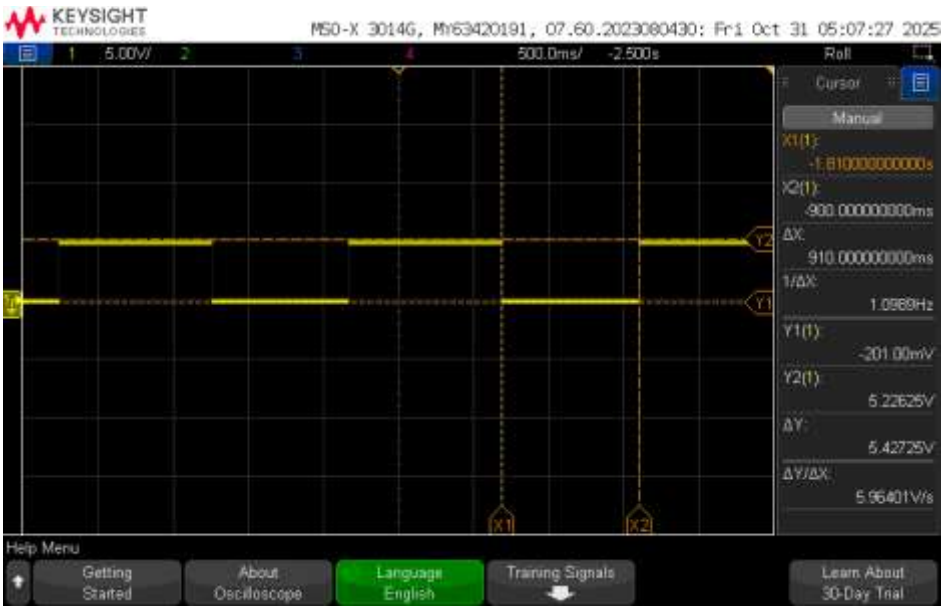
LTSpice Astable 555 Timer Circuit (2 second period, 60% Duty Cycle) Full Period Simulation



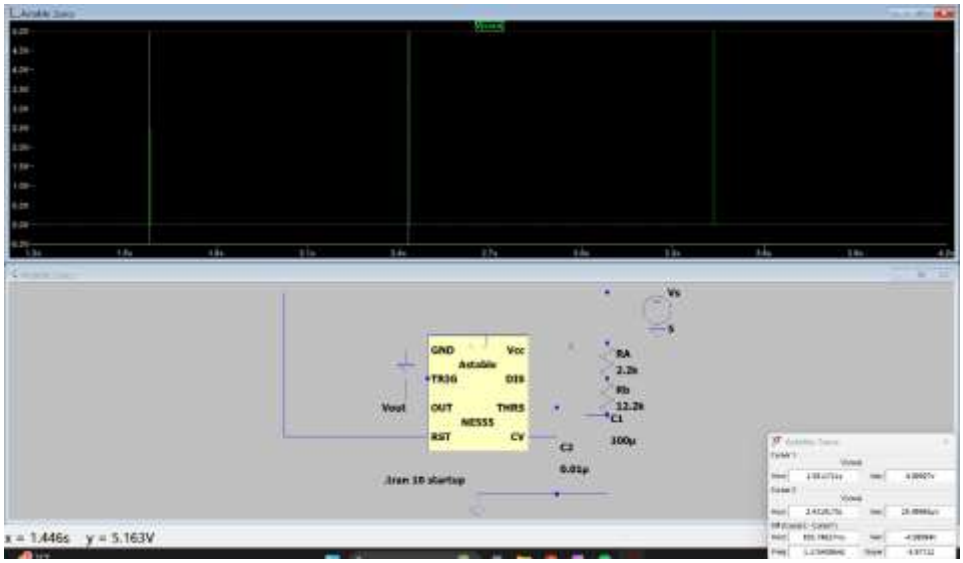
Astable 555 Timer Circuit (2 second period, 60% Duty Cycle) High Voltage Period



LTSpice Astable 555 Timer Circuit (2 second period, 60% Duty Cycle) High Voltage Period Simulation



Astable 555 Timer Circuit (2 second period, 60% Duty Cycle) Low Voltage Period

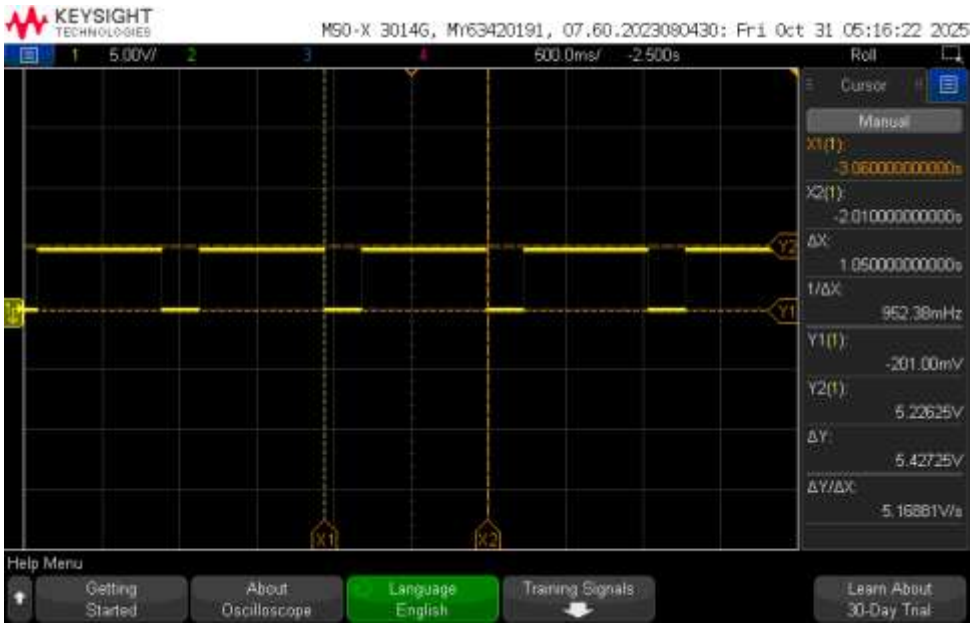


LTSpice Astable 555 Timer Circuit (2 second period, 60% Duty Cycle) Low Voltage Period Simulation

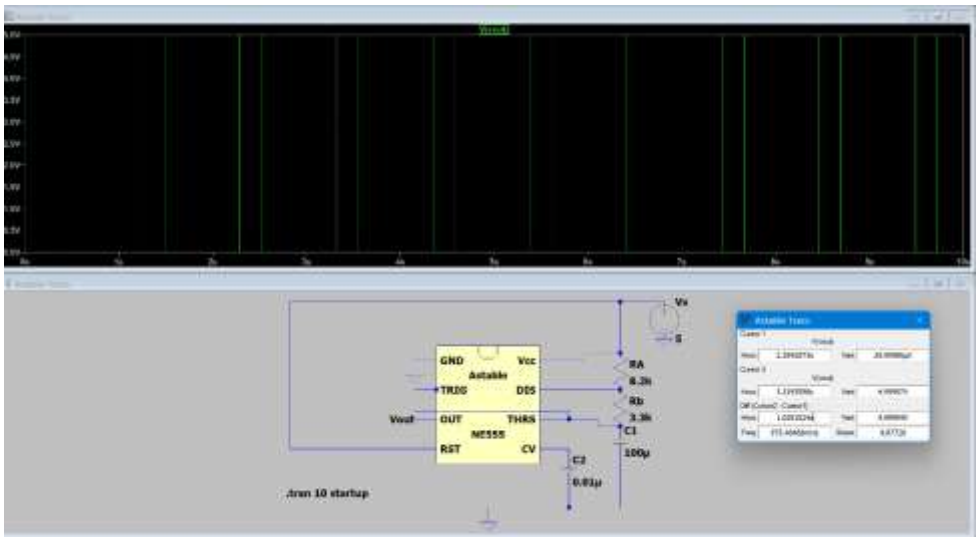
Astable Mode (1s Period)

Voltage	Calculated Period (s)	Simulated Period (s)	Experimental Period (s)	Percent Error (%)
High + Low	1.026	1.025	1.050	2.3
High	0.797	0.796	0.810	1.6
Low	0.229	0.229	0.240	4.8

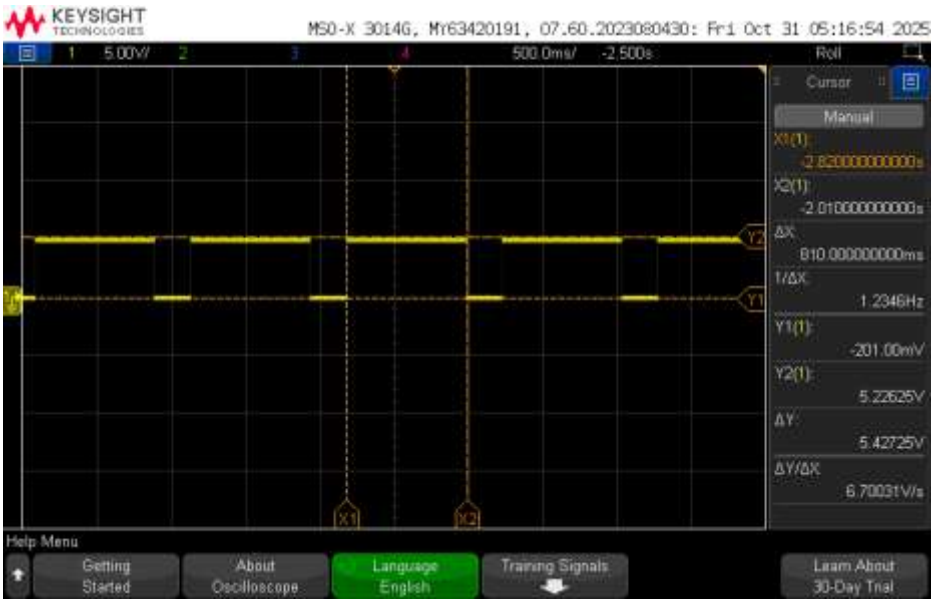
1-Second, 75% Duty Cycle Astable Circuit Measurements



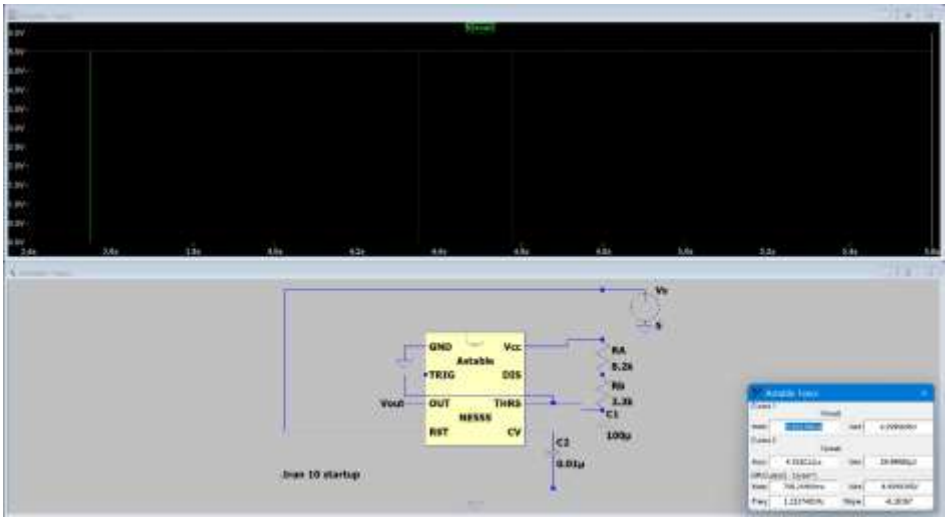
Astable 555 Timer Circuit (1 second period, 75% Duty Cycle) Full Period



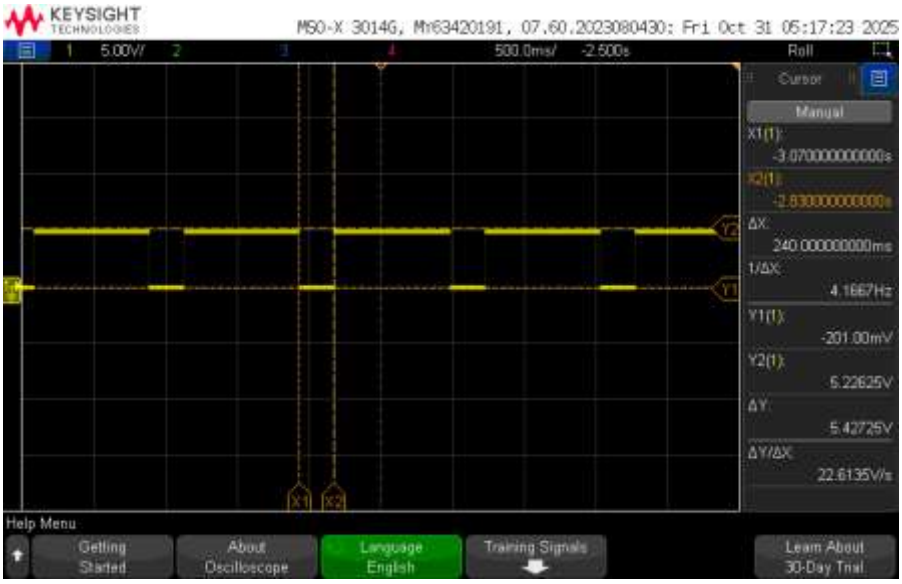
LTSpice Astable 555 Timer Circuit (1 second period, 75% Duty Cycle) Full Period Simulation



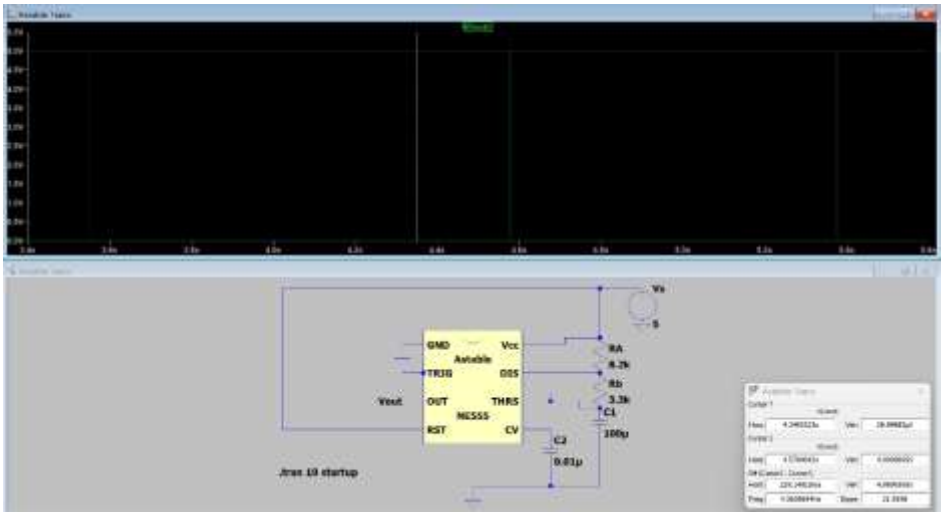
Astable 555 Timer Circuit (1 second period, 75% Duty Cycle) High Voltage Period



Astable 555 Timer Circuit (1 second period, 75% Duty Cycle) High Voltage Period Simulation



Astable 555 Timer Circuit (1 second period, 75% Duty Cycle) Low Voltage Period



LTSpice Astable 555 Timer Circuit (1 second period, 75% Duty Cycle) Low Voltage Period Simulation

For the 2-second, 60% duty cycle astable circuit, the theoretical period of 1.843 seconds was validated by simulation and measurement. The LTSpice simulation produced 1.849 s, and the oscilloscope showed 1.93 s, resulting in an experimental 4.7% error. The small variance is likely due to the electrolytic capacitor's tolerance and the finite switching time of the internal transistor network.

The measured duty cycle of approximately 53% is less than desired, however, it confirms that the circuit met the target design based on the available external electrical components and the very limited combination of said components. The oscilloscope waveforms clearly illustrate the alternating charge and discharge phases of the timing capacitor between one-third and two-

thirds of the supply voltage. The output waveform maintained a stable square shape, which indicates that the timer can continuously oscillate without external triggers.

Similarly, the 1-second astable circuit also produced reliable oscillations that indicated the circuit operated in the correct way. The calculated period of 1.026 seconds matched the simulation (1.025 s) and experimental measurement (1.05 s) within a 2.3% margin of error. The observed duty cycle averaged around 77%, very close to the intended 75%. Minor sources of error are from capacitor and resistor tolerances.

For both circuits, the results indicate that the 555 Timer's astable configuration performs predictably when designed with appropriate resistance and capacitance. The total period of both circuits had resulting percent errors within reason which provides evidence to the correct demonstration of the astable configuration of the 555 Timer.

Application of 555 Timer

Voltage	Calculated Period (ms)	Simulated Period (ms)	Experimental Period (ms)	Percent Error (%)
High + Low	0.808	1.070	1.500	85.6
High	0.785	1.040	1.490	89.9
Low	0.023	0.034	0.012	47.8

Full Brightness LED using Astable 555 Timer Circuit Measurements

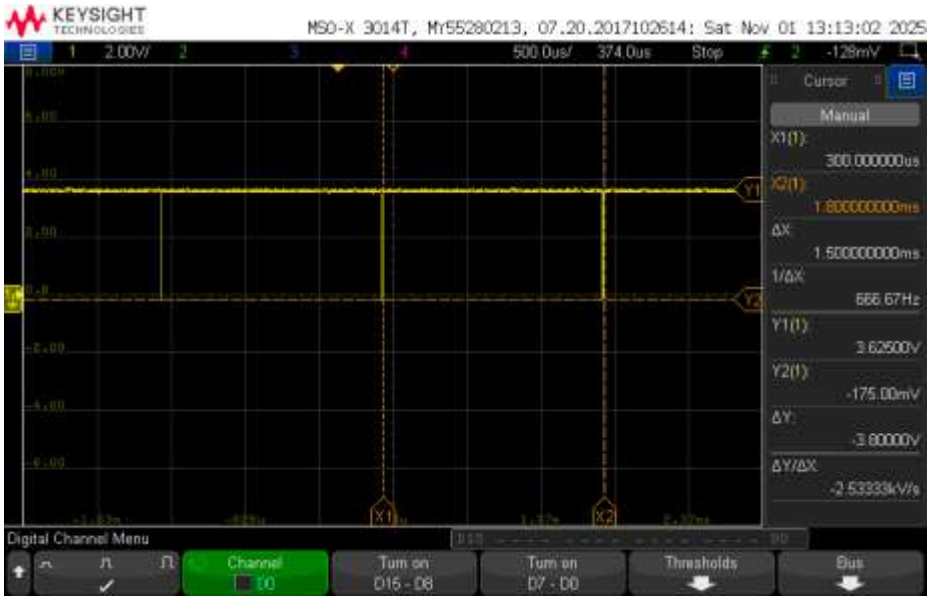
Voltage	Calculated Period (ms)	Simulated Period (ms)	Experimental Period (ms)	Percent Error (%)
High + Low	0.808	1.050	0.760	5.9
High	0.092	0.096	0.064	30.4
Low	0.716	0.964	0.696	2.8

Low Brightness LED using Astable 555 Timer Circuit Measurements

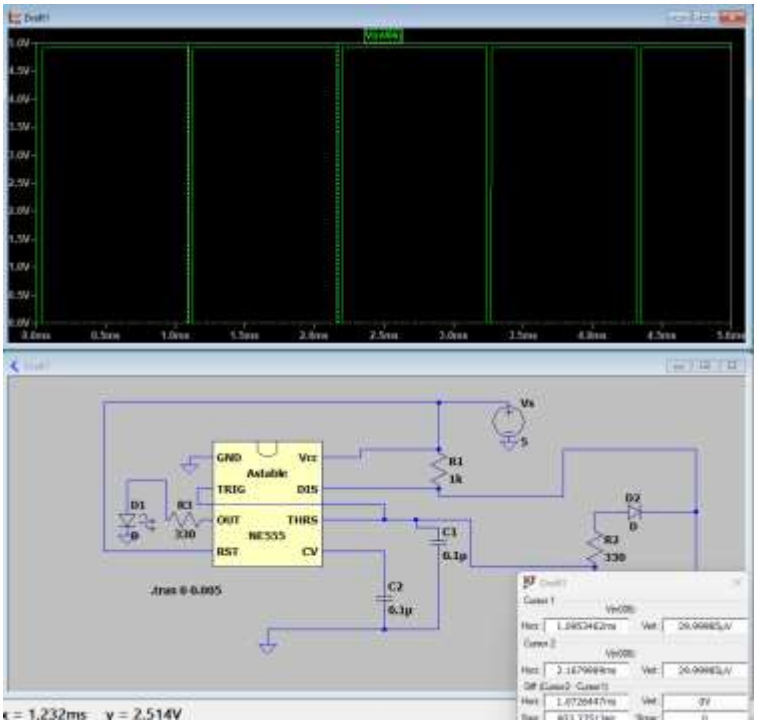
Voltage	Calculated Period (ms)	Simulated Period (ms)	Experimental Period (ms)	Percent Error (%)
High + Low	0.807	1.06	0.750	7.1
High	0.438	0.664	0.420	4.1

Low	0.369	0.391	0.310	16.0

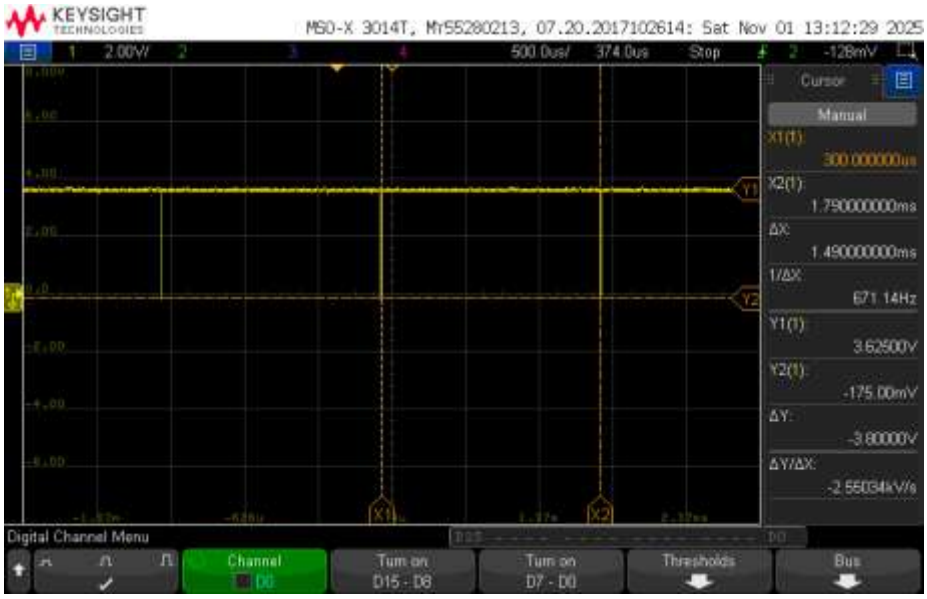
Medium Brightness LED using Astable 555 Timer Circuit Measurements



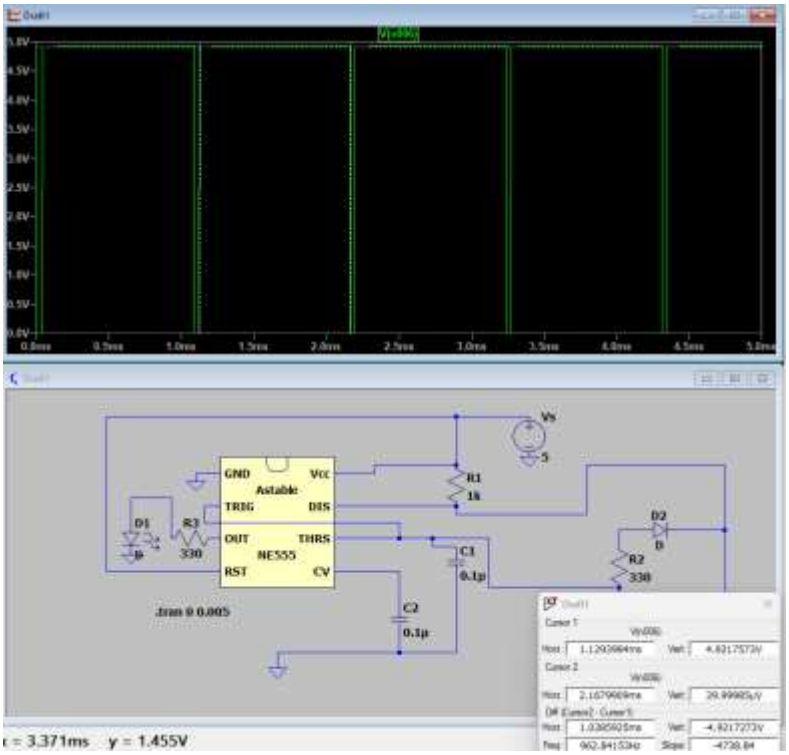
LED Dimmer Circuit using 555 Timer (Full Light, Full Period)



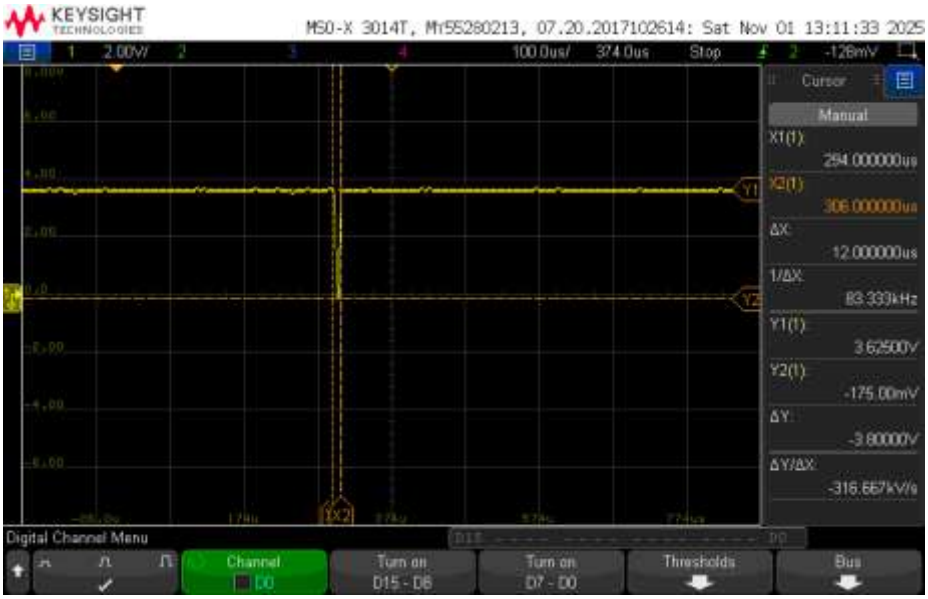
LTSpice LED Dimmer Circuit using 555 Timer (Full Light, Full Period) Simulation



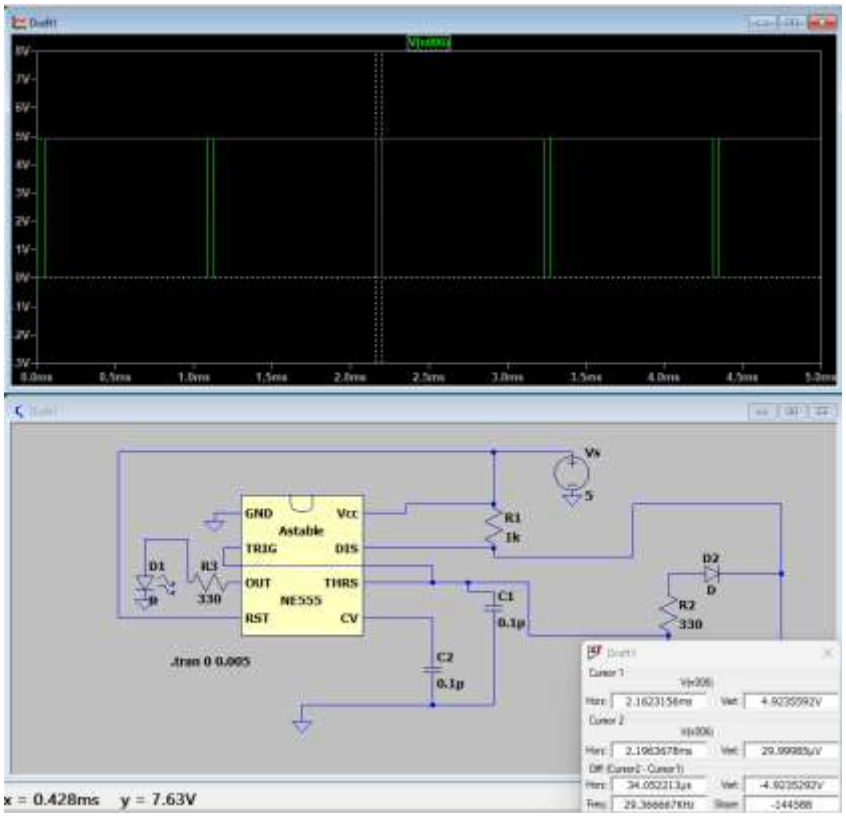
LED Dimmer Circuit using 555 Timer (Full Light, High Voltage Period)



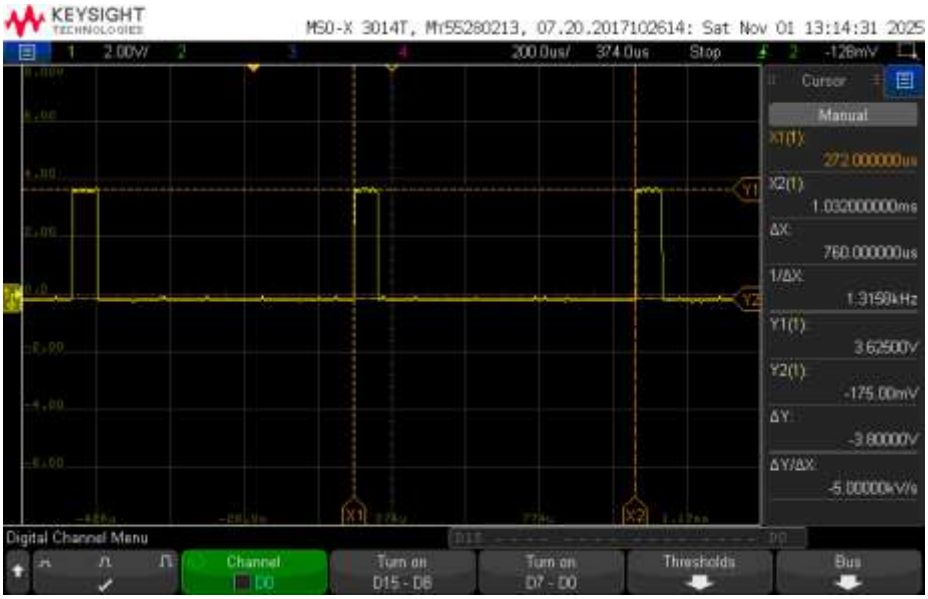
LTSpice LED Dimmer Circuit using 555 Timer (Full Light, High Voltage Period) Simulation



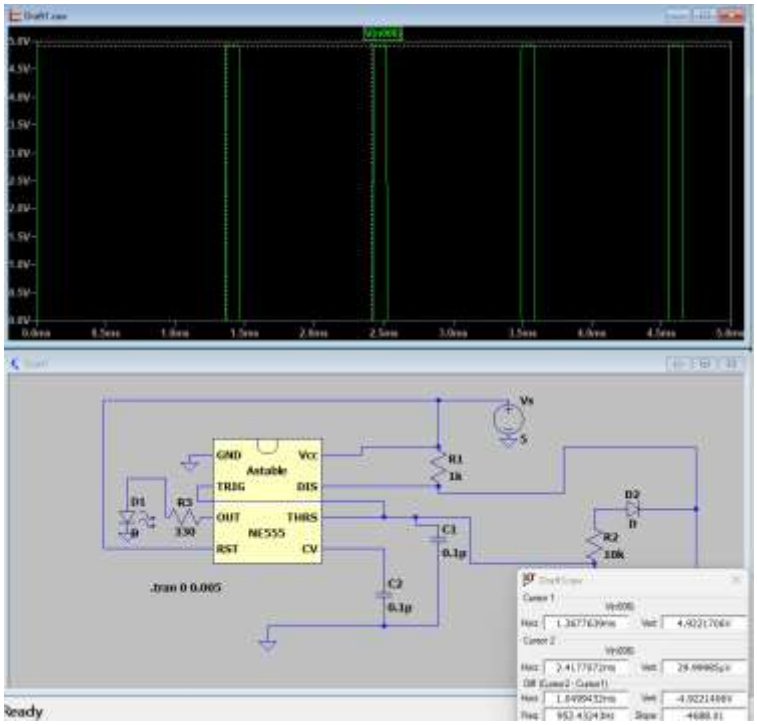
LED Dimmer Circuit using 555 Timer (Full Light, Low Voltage Period)



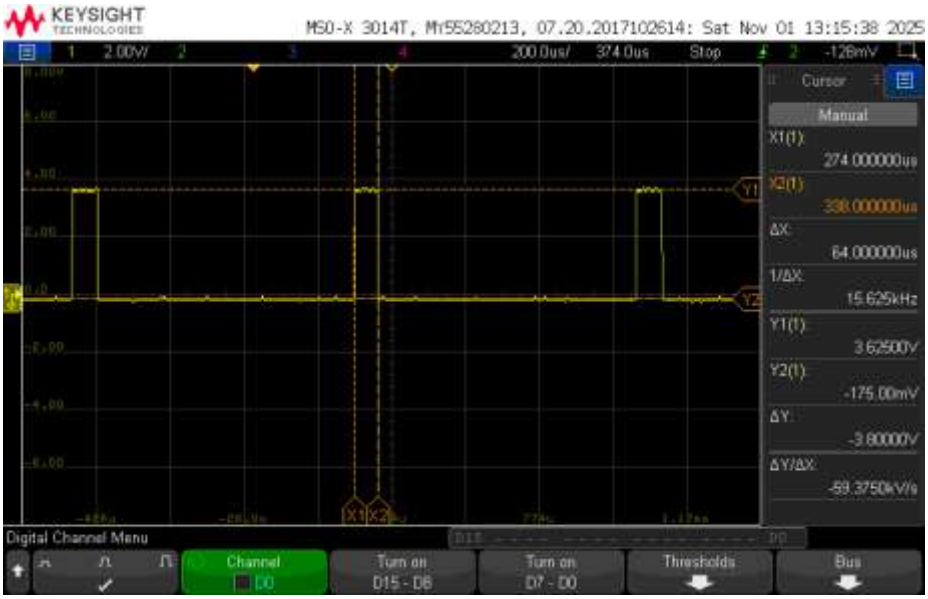
LTSpice LED Dimmer Circuit using 555 Timer (Full Light, Low Voltage Period) Simulation



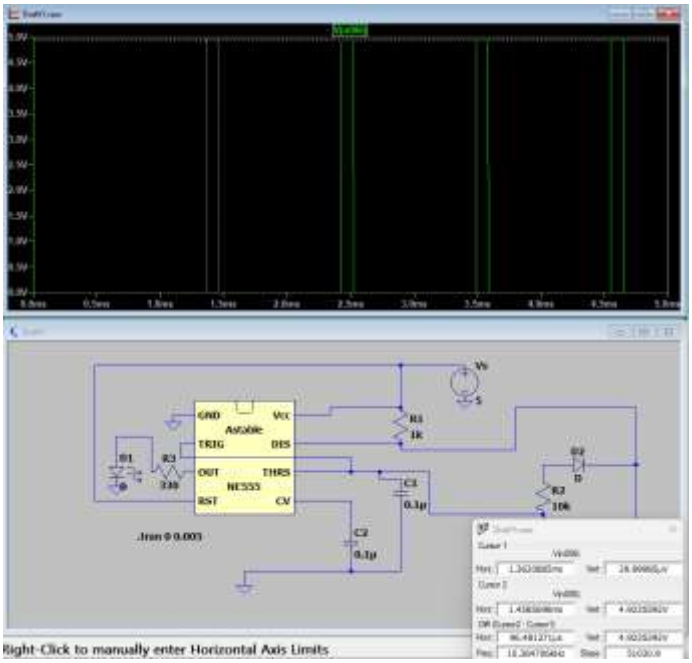
LED Dimmer Circuit using 555 Timer (Dim Light, Full Period)



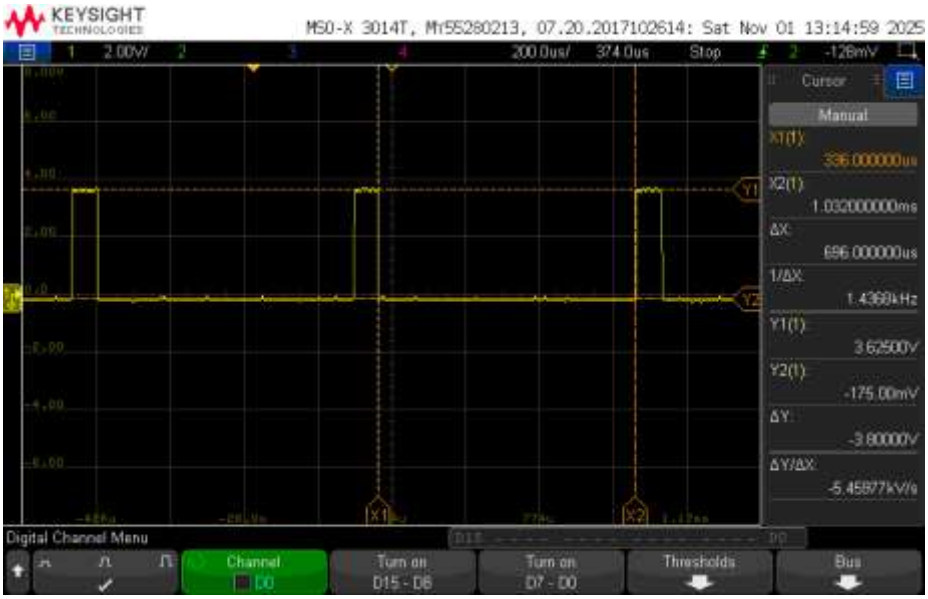
LTSpice LED Dimmer Circuit using 555 Timer (Dim Light, Full Period) Simulation



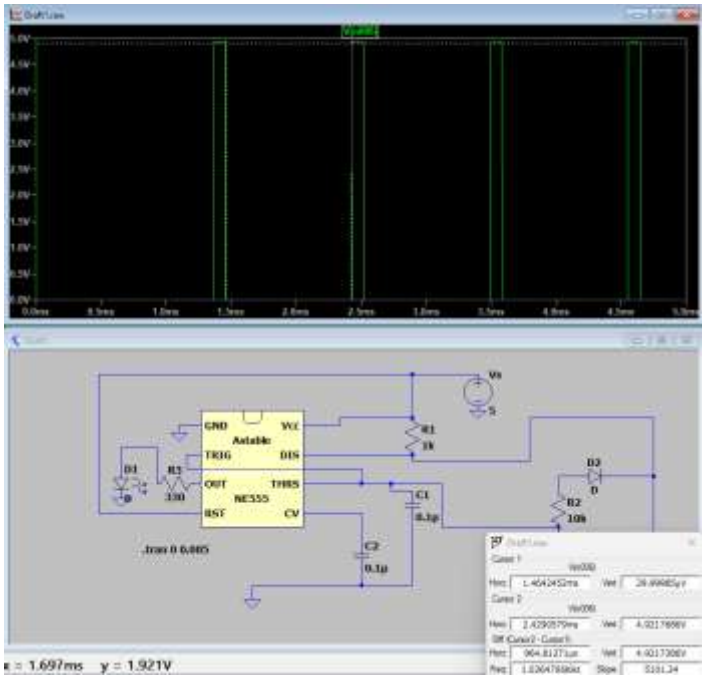
LED Dimmer Circuit using 555 Timer (Dim Light, High Voltage Period)



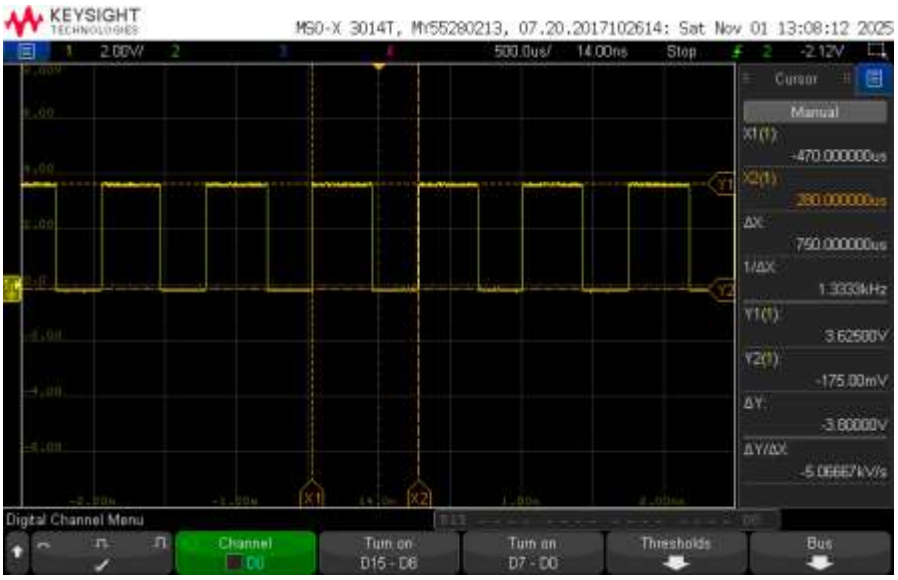
LTSpice LED Dimmer Circuit using 555 Timer (Dim Light, High Voltage Period) Simulation



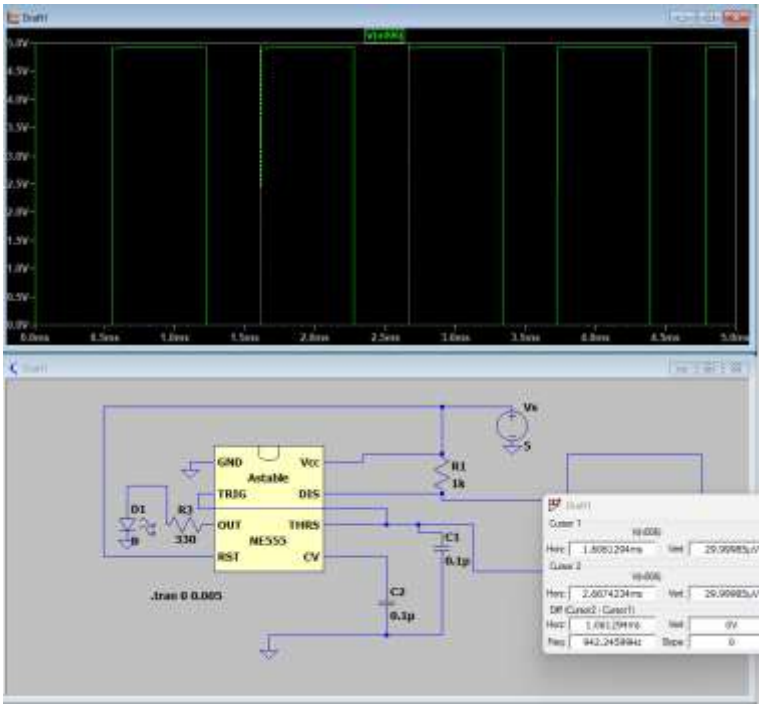
LED Dimmer Circuit using 555 Timer (Dim Light, Low Voltage Period)



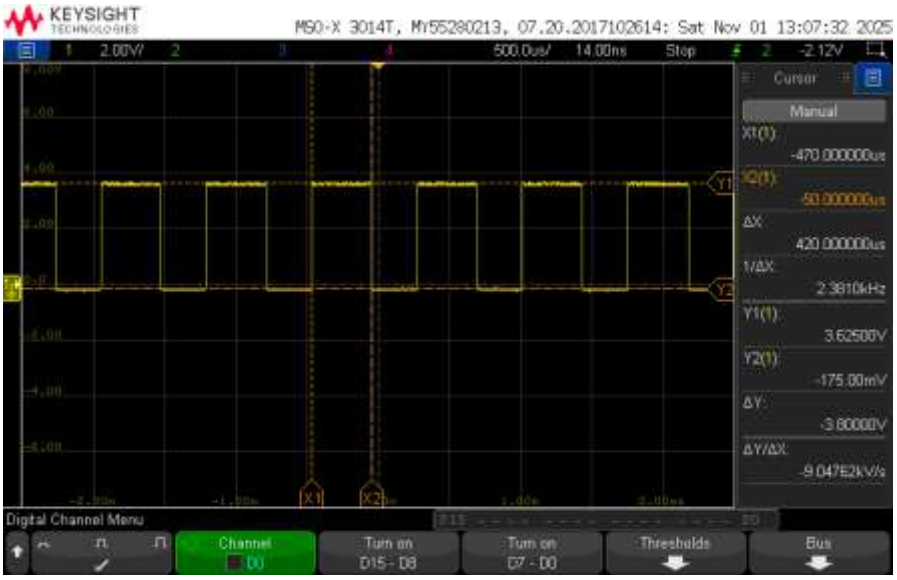
LTSpice LED Dimmer Circuit using 555 Timer (Dim Light, Low Voltage Period) Simulation



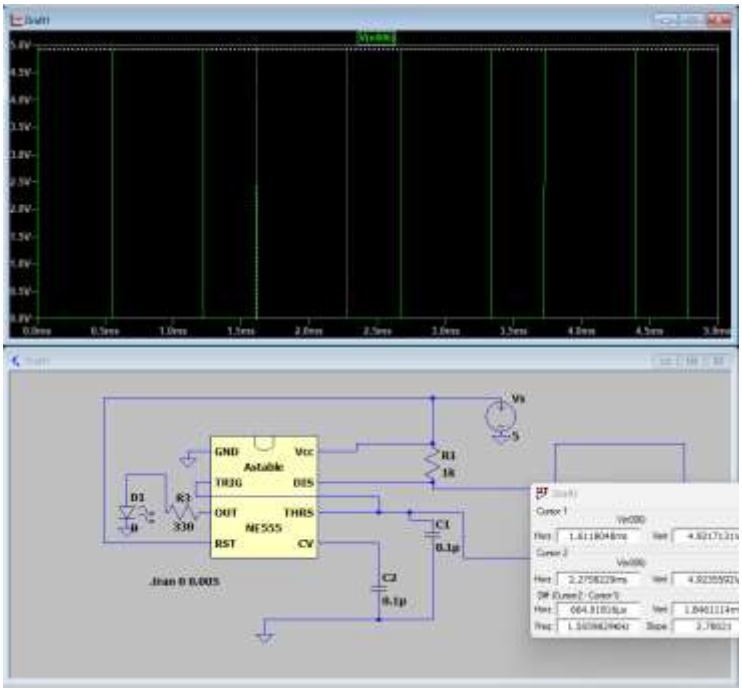
LED Dimmer Circuit using 555 Timer (Medium Light, Full Period)



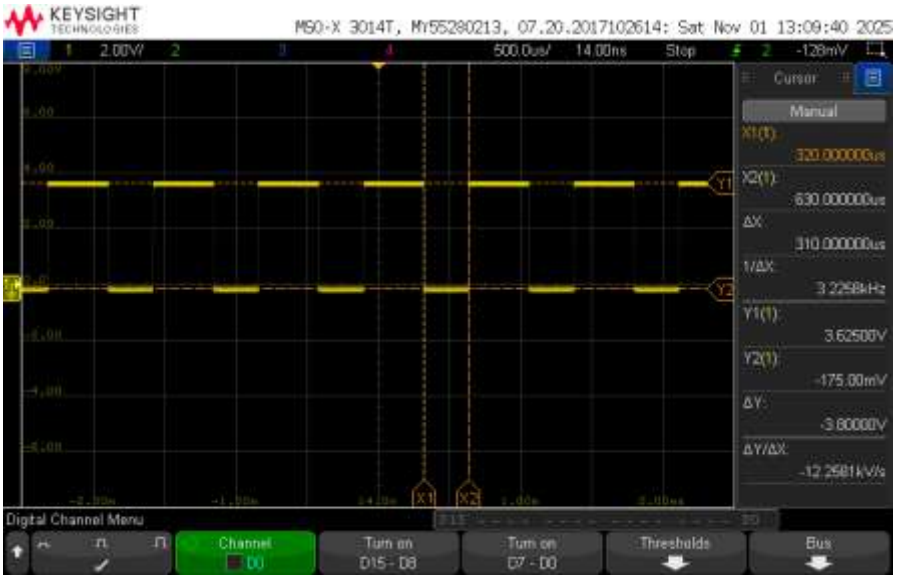
LTSpice LED Dimmer Circuit using 555 Timer (Medium Light, Full Period) Simulation



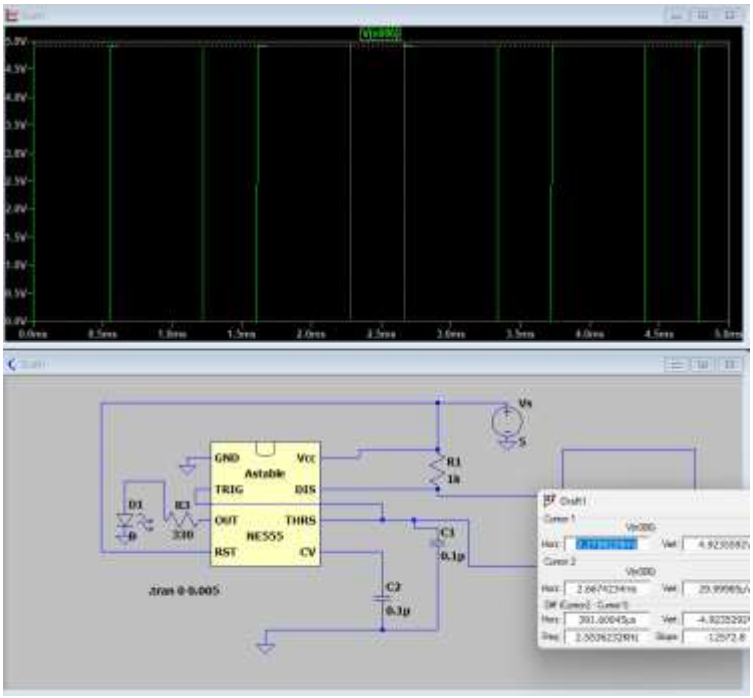
LED Dimmer Circuit using 555 Timer (Medium Light, High Voltage Period)



LTSpice LED Dimmer Circuit using 555 Timer (Medium Light, High Voltage Period) Simulation



LED Dimmer Circuit using 555 Timer (Medium Light, Low Voltage Period)



LTSpice LED Dimmer Circuit using 555 Timer (Medium Light, Low Voltage Period) Simulation

The LED dimmer circuit uses the 555 Timer in a modified astable configuration to generate a variable PWM signal. With a 10 kΩ potentiometer in combination with two 1N4148 diodes, the 555 Timer's output voltage can by independently controlled by changing the charge and discharge timings. This changes the duty cycle while maintaining nearly constant frequency allowing for the 555 Timer to control the voltage outputted.

Three potentiometer positions, minimum, medium, and maximum, were analyzed to observe the effect on LED brightness. Theoretical and simulated timing values for each configuration were compared with oscilloscope measurements. For example, at maximum brightness (97% duty cycle), the output waveform remained high for almost the entire period, resulting in a nearly continuous bright LED. Conversely, at minimum brightness (≈11% duty cycle), the LED emitted a faint light, as the high time was shorter. The mid-range setting yielded approximately 54% duty cycle, producing medium brightness as expected.

The simulation and experimental results closely aligned for the overall period, with average period error below 10%. However, the percentage errors in the high pulse width were larger due to component tolerances and the response of the potentiometer across its range. Additionally, oscilloscope resolution may contribute minor measurement errors as the pulse width at this frequency is only 1-2 milliseconds wide.

The design's main advantages include its efficiency, minimal component count, and versatility. However, the circuit also has several limitations. The adjustment range of brightness is not perfectly linear due to the non-linear resistance of the potentiometer, and slight flickering may occur. In addition, the 555's limited output current restricts the load size and prevents direct connection to high-power loads. To improve the design, a transistor or MOSFET could be added to handle higher current loads, and the operating frequency could be increased to eliminate any visible flicker. Using a linear potentiometer would also allow smoother brightness transitions.

Overall, the PWM dimmer effectively demonstrated how duty cycle variation directly influences LED brightness. The circuit performed as intended, verifying that the 555 Timer can efficiently modulate power to a load through duty cycle control while maintaining a constant switching frequency. This experiment highlighted the practical application of the timer's astable operation.

Conclusion and References

Conclusion

In monostable mode, the timer produced a single output pulse of around 3 seconds which matched the required circuit parameters and expectations. There were only minor deviations due to component tolerances and triggering inconsistencies. In astable mode, both the 2-second and 1-second circuits generated stable square waves with duty cycles and frequencies consistent with design calculations. The low percent errors demonstrated that the 555 Timer offers predictable and repeatable performance when used with accurately chosen resistors and capacitors.

The LED dimmer application successfully illustrated the capability of the 555 Timer in controlling voltage output through PWM. By adjusting the potentiometer, the brightness of the LED could be varied, proving the effectiveness of duty cycle modulation in managing output power without changing supply voltage.

Across all circuits, discrepancies between theoretical, simulated, and experimental results were primarily caused by capacitor tolerances, internal transistor voltage drops, and oscilloscope resolution limits. Improvements could include using precision resistors and film capacitors with smaller tolerances, adding supply decoupling capacitors, and using an electronic trigger circuit instead of a mechanical pushbutton to reduce noise and bounce that comes with physical components. Ultimately, this report provides insight into how the 555 Timer demonstrates simplicity and reliability in timing and control applications.

References

Atwell, Cabe. “The Origin, Explanation, and Applications of Triple-Five Timers.” Electronic Design, 20 Oct. 2022, www.electronicdesign.com/technologies/analog/article/21252714/electronic-design-the-origin-explanation-and-applications-of-triple-five-timers.

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