2025 Digital IC Design Homework 2

NAME	陳廷睿
Student ID	F74101034

Functional Simulation Result

Pattern1	Pattern2	Pattern3	Pattern4	Pattern5
Pass/Fail	Pass/Fail	Pass/Fail	Pass/Fail	Pass/Fail

Pattern 1

```
VSIM 25> run -all
# All data have been generated successfully!
#
#                    ////////////////////////////
#                    /                          /       |__||
#                    /  Congratulations !!      /      / 0.0  |
#                    /                          /    /_____   |
#                    /  Simulation PASS !!      /   /^ ^ ^ \  |
#                    /                          /  |^ ^ ^ ^ |w|
#                    ////////////////////////////   \m___m__|_|
#
#
# ** Note: $finish    : C:/Users/F74101034/Downloads/StudentID/file/testfixture.sv(162)
#    Time: 1325 ns  Iteration: 0  Instance: /testfixture
```

Pattern 2

```
VSIM 27> run -all
# All data have been generated successfully!
#
#                    ////////////////////////////
#                    /                          /       |__||
#                    /  Congratulations !!      /      / 0.0  |
#                    /                          /    /_____   |
#                    /  Simulation PASS !!      /   /^ ^ ^ \  |
#                    /                          /  |^ ^ ^ ^ |w|
#                    ////////////////////////////   \m___m__|_|
#
#
# ** Note: $finish    : C:/Users/F74101034/Downloads/StudentID/file/testfixture.sv(162)
#    Time: 1675 ns  Iteration: 0  Instance: /testfixture
```

Pattern 3

```
VSIM 29> run -all
# All data have been generated successfully!
#
#                    ////////////////////////////
#                    /                          /       |__||
#                    /  Congratulations !!      /      / 0.0  |
#                    /                          /    /_____   |
#                    /  Simulation PASS !!      /   /^ ^ ^ \  |
#                    /                          /  |^ ^ ^ ^ |w|
#                    ////////////////////////////   \m___m__|_|
#
#
# ** Note: $finish    : C:/Users/F74101034/Downloads/StudentID/file/testfixture.sv(162)
#    Time: 1715 ns  Iteration: 0  Instance: /testfixture
```

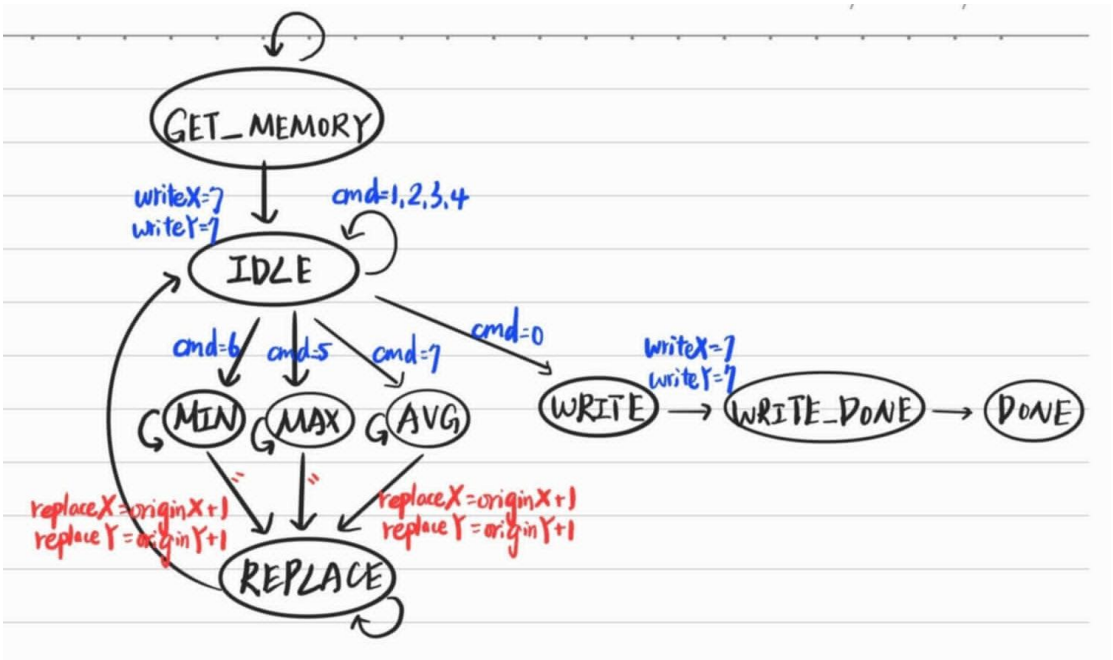
Pattern 4

```
VSIM 31> run -all
# All data have been generated successfully!
#
#                    ////////////////////////
#                    /                      /       |__||
#                    /  Congratulations !!  /      / 0.0  |
#                    /                      /    /_____   |
#                    /  Simulation PASS !!  /   /^ ^ ^ \  |
#                    /                      /  |^ ^ ^ ^ |w|
#                    ////////////////////////   \m___m__|_|
#
#
# ** Note: $finish    : C:/Users/F74101034/Downloads/StudentID/file/testfixture.sv(162)
#    Time: 1755 ns  Iteration: 0  Instance: /testfixture
```

Pattern 5

```
VSIM 33> run -all
# All data have been generated successfully!
#
#                    ////////////////////////
#                    /                      /       |__||
#                    /  Congratulations !!  /      / 0.0  |
#                    /                      /    /_____   |
#                    /  Simulation PASS !!  /   /^ ^ ^ \  |
#                    /                      /  |^ ^ ^ ^ |w|
#                    ////////////////////////   \m___m__|_|
#
#
# ** Note: $finish    : C:/Users/F74101034/Downloads/StudentID/file/testfixture.sv(162)
#    Time: 2735 ns  Iteration: 0  Instance: /testfixture
```

LCD_CTRL Finite-State Machine Design:



由 GET_MEMEORY 為起始狀態，先將 RAM 的資料複製到 temp_memory 後，狀態轉移至 IDLE，由接受到的 cmd 決定轉移狀態，cmd =1/2/3/4 為 shift，因此只需移動 origin_x/origin_y，狀態仍為 IDLE。若 cmd=5/6/7，則需查看原點附近 16 個值來決定替換值，並進行替換(state REPLACE)，替換後回到 IDLE。直到接收到到 cmd=0，將 temp_memory 寫回 RAM。