National Cheng Kung University

Department of Electrical Engineering

Introduction to VLSI CAD (Spring 2025)

Lab Session 5

FSM&Synthesis of Sequential Logic

Name	Student ID	
Practical Sections	**Points**	**Marks**
Lab in class	5	
Prob A	25	
Prob B	25	
Prob C	30	
Report	15	
File hierarchy, naming…etc.	5	
Notes:		

Due Date: 15:10, March 26th , 2025 @ moodle

Deliverables

1) All Verilog codes including testbenches for each problem should be uploaded.
   NOTE: Please **DO NOT** include source code in the paper report!
2) All homework requirements should follow the naming rule in this file hierarchy or you will not get the full credit.
   NOTE: Please **DO NOT** upload waveforms!
3) Important! TA will use the command in Appendix A to check your design under SoC Lab environment, if your code can not be recompiled by TA successfully using the commands, you will not get the full credit.
4) If you upload a dead body, which we cannot even compile, you will get **NO** credit!
5) All Verilog file before synthesizing should get at least 90% Superlint Coverage.
6) Lab5_Student_ID.tar (English alphabet of Student_ID should be **capital**.)

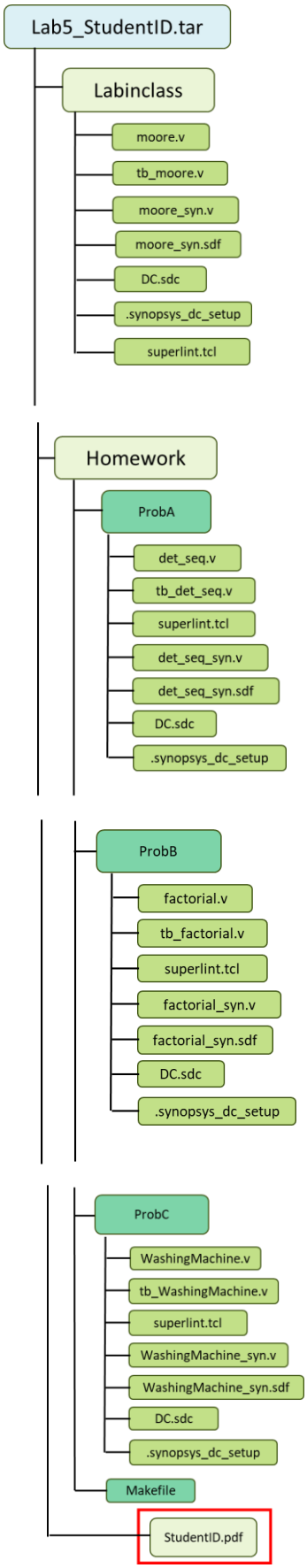
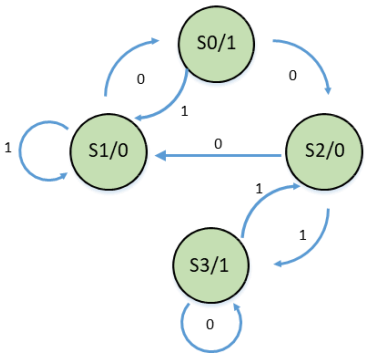


Fig.1 File hierarchy for Homework submission

1) Design a Moore machine circuit that can be synthesized. The following is Moore machine module's specification. (Do NOT add or delete I/O ports, but you can change their behavior.)



Current State	Next State		qout
	din=0	din=1	
S0=00	S2	S1	1
S1=01	S0	S1	0
S2=10	S1	S3	0
S3=11	S3	S2	1

Signal	Type	Bits	Description
clk	input	1	Clock pin.
rst	input	1	Reset pin. Reset all of the flip flops to zeros.
din	input	1	Control signal for fsm.
qout	output	1	1:when current state==S0 or current state==S3 0: when current state==S1 or current state==S2

2) Please describe your FSM in detail

Explanation about your FSM
分成 state transition(sequential)、nextstate logic(combinational)和 output logic(combinational)三個部分。 因為是 moore machine, 所以 output logic 只需要看在哪一個 state。 而 nextstate logic 則由當前 din 的值來判斷 next state 是誰，最後等 clk 的正緣賦值給 state。

3) After synthesizing your design, you may have some information about the circuit. Please fill in the following form.

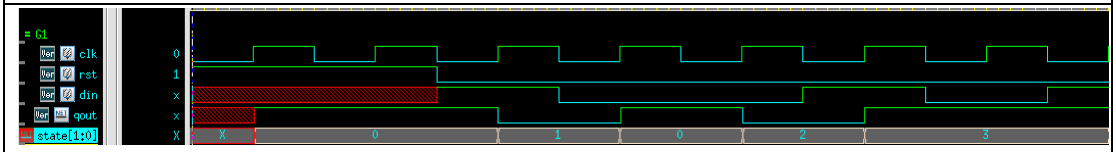
Timing (slack)	Area (total cell area)	Power (total)
9.91	**4.199**	**6.7289e-04 mW**

4) Please attach your design waveforms.

Your simulation result on the terminal :

```
**************************
**                      **       |\__||
**  Congratulations !!  **      / O.O  |
**                      **    /_____   |
**  Simulation PASS!!   **   /^ ^ ^ \  |
**                      **  |^ ^ ^ ^ |w|
**************************   \m___m__|_|


$finish called from file "tb_moore.v", line 87.
$finish at simulation time              140000
           V C S   S i m u l a t i o n   R e p o r t
Time: 140000 ps
CPU Time:      0.350 seconds;       Data structure size:   0.5Mb
Thu Mar 20 22:47:50 2025
CPU time: 5.749 seconds to compile + .283 seconds to elab + .424 seconds to link + .385 seconds in simulation
```

Your waveform :



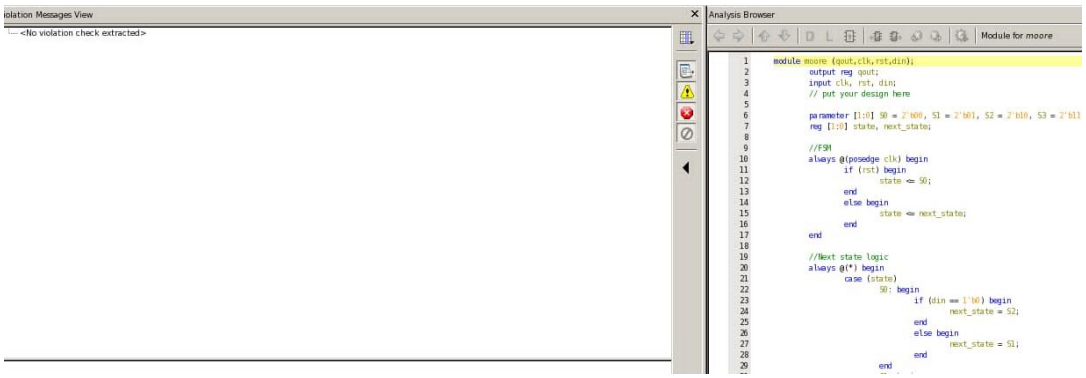
Explanation of your waveform :

state0 會輸出 1，din 為 1 會轉換至 state1，

state1 會輸出 0，din 為 0 會轉換至 state0，

state0 一樣輸出 1，但 din 為 0 因此轉換成 state2。

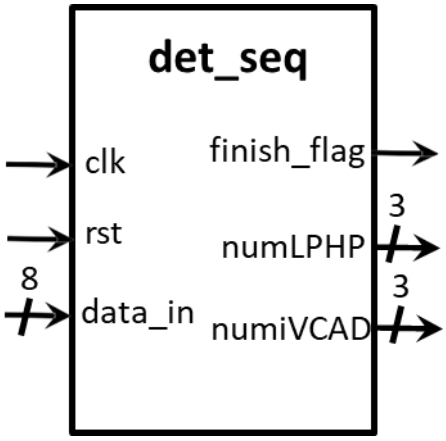
Superlint Coverage



Coverage=100%

ProbA: Design a circuit "detect sequence"

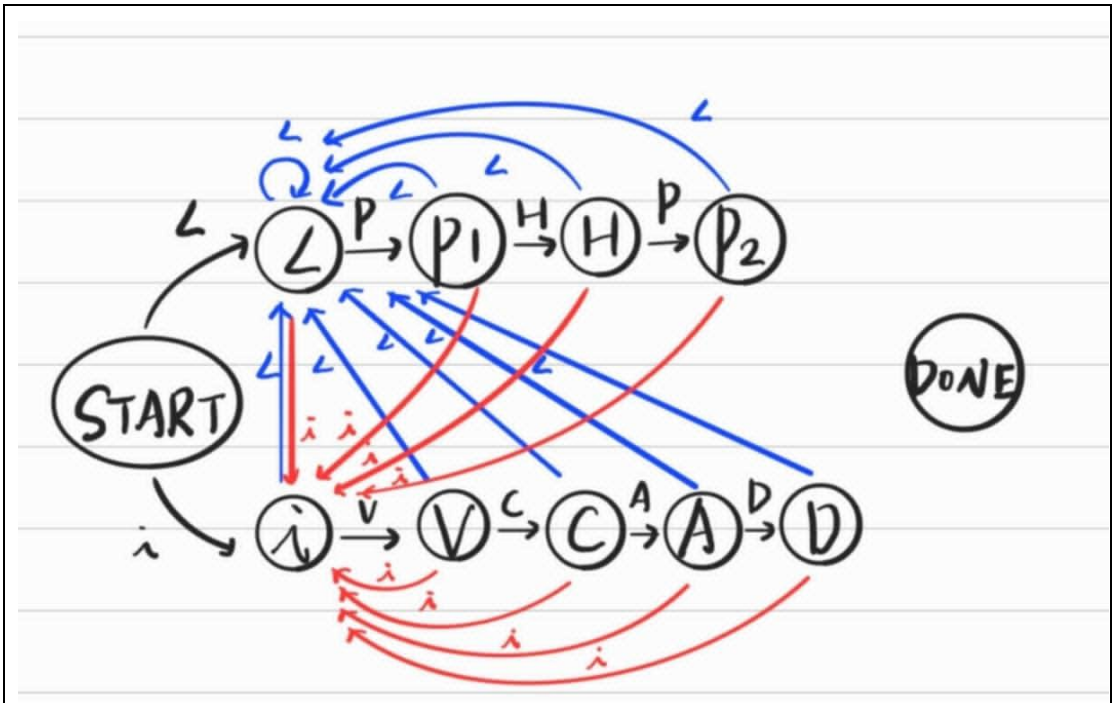
1) **Design a sequential circuit to detect pattern "LPHP" and "iVCAD" that can be synthesized with Moore machine. The following is det_seq module's specification. (Do NOT add or delete I/O ports, but you can change their behavior.)**



Signal	Type	Bits	Description
clk	input	1	clock
rst	input	1	reset, active high
data_in	input	8	data input
numLPHP	output	3	Count the number of pattern LPHP
numiVCAD	output	3	Count the number of pattern iVCAD
finish_flag	output	1	Finish flag

2) **Please describe your FSM in detail**

Explanation about your FSM



由 START 出發以 LPHP 為例，若吃到下一個字元符合，就往下一個 state 走，直到走到 state P2，numLPHP 會加一。在任何 state 吃到 L/i/.，就會分別跳到 stateL/statei/stateDONE, 若吃到非上述字元，則回 START。
跳到 stateDONE 後，拉高 finish 訊號。

3) After synthesizing your design, you may have some information about the circuit. Please fill in the following form.

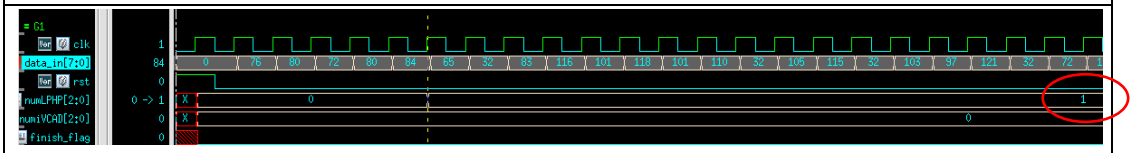
Timing (slack)	Area (total cell area)	Power (total)
9.78	29.49	2.3343e-03 mW

4) Please attach your design waveforms.

Your simulation result on the terminal :

```
---------------- Detect Sequence Test  -------------------

numLPHP 5 is correct

numiVCAD 6 is correct



        ***************************
        **                       **       |\__||
        **  Congratulations !!   **      / O.O  |
        **                       **    /_____   |
        **  Simulation PASS!!    **   /^ ^ ^ \  |
        **                       **  |^ ^ ^ ^ |w|
        ***************************   \m___m__|_|


$finish called from file "tb_det_seq.v", line 272.
$finish at simulation time                180600
           V C S   S i m u l a t i o n   R e p o r t
Time: 180600 ps
CPU Time:      0.340 seconds;       Data structure size:   0.5Mb
Thu Mar 20 23:00:19 2025
CPU time: 5.383 seconds to compile + .283 seconds to elab + .396 seconds to link + .375 seconds in simulation
```

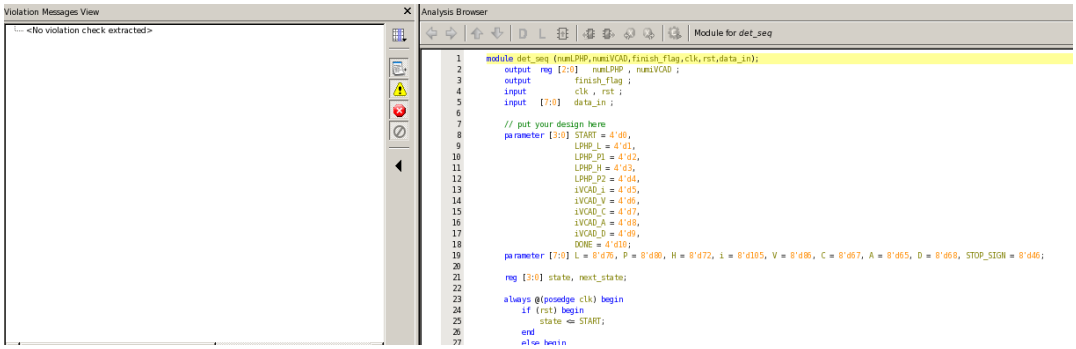
Your waveform :



Explanation of your waveform :

Data_in 依序為 8’d76(L)->8’d80(P)->8’d72(H)->8’d80(P)，因此 numLPHP 需加一，做至 Data_in 為 8’d46(.)升起 finish 訊號。

Superlint Coverage



Coverage=100%

ProbB: Design a Factorial Circuit

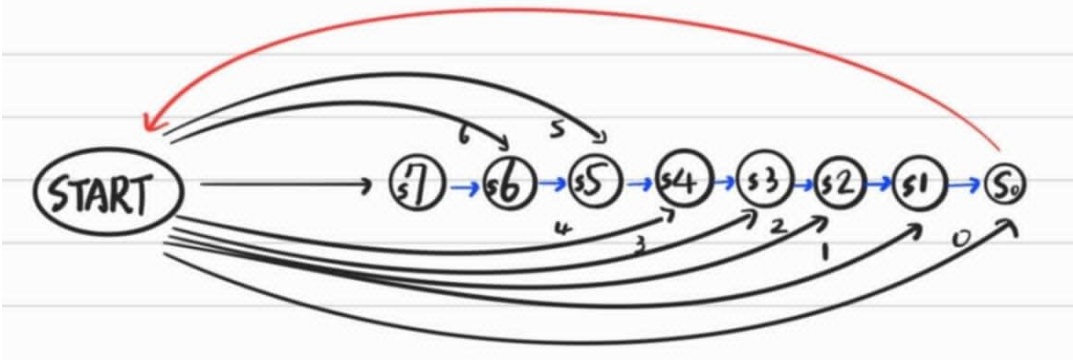
1) **Design a factorial circuit with Mealy machine. The following is factorial module's specification. (Do NOT add or delete any I/O ports, but you can change their behavior.)**

Signal	Bits	Type	Description
clk	1	input	clock
rst	1	input	reset(active high)
enable	1	input	When enable is high, the system will start to calculate the factorial result.
level	3	input	Different levels will calculate different factorial results.
result	14	output	Result of the factorial
valid	1	output	When valid is 1, result's value is valid.

2) **Please describe your FSM in detail.**

3)

Explanation about your FSM



State 從 start 出發，看 level 是多少就跳到該 state，並將 result 乘上該 state 的數字，在一路做至 state0。state0 會將 valid 拉至 1，並返回 START。

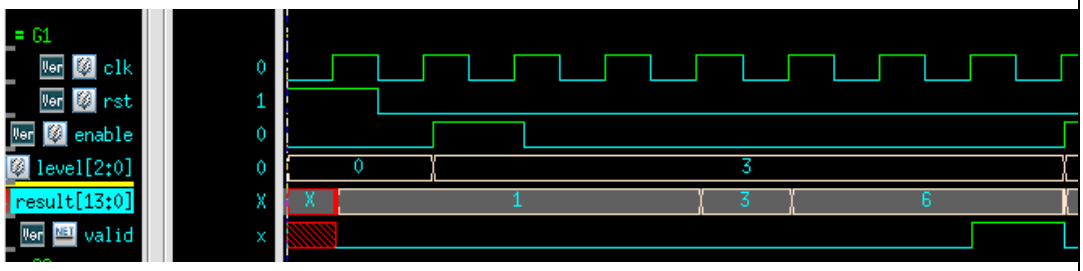
4) **After synthesizing your design, you may have some information about the circuit. Please fill in the following form.**

Timing (slack)	Area (total cell area)	Power (total)
9.55	**98.70**	**5.6534e-03 mW**

5) Please attach your design waveforms.

Your simulation result on the terminal.

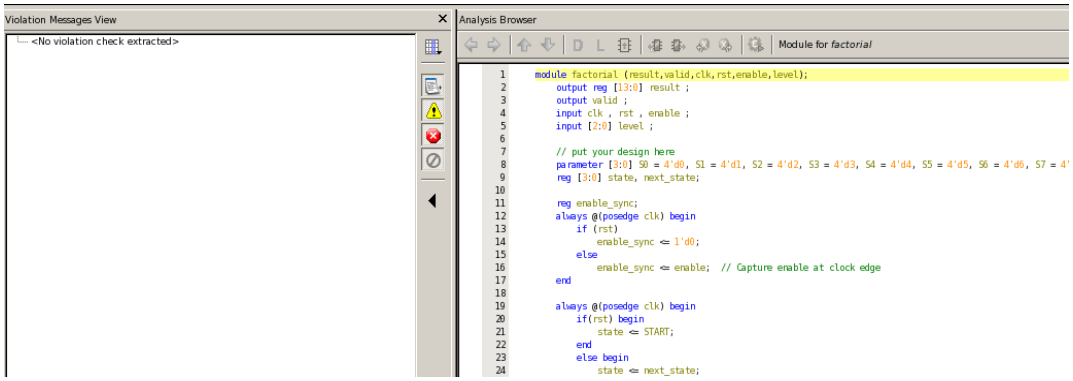
Your waveform :



Explanation of your waveform :

State 從 8(START state)開始，當 Level 為 3，會跳到 state = 3，並且將 result 值*3，再跳至 state=2 並將 result*2，依序做至 state=0，並將 valid 的值拉起。

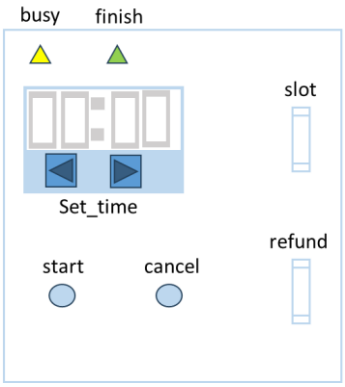
Superlint Coverage



Coverage = 100%

ProbC: Design a Washing Machine

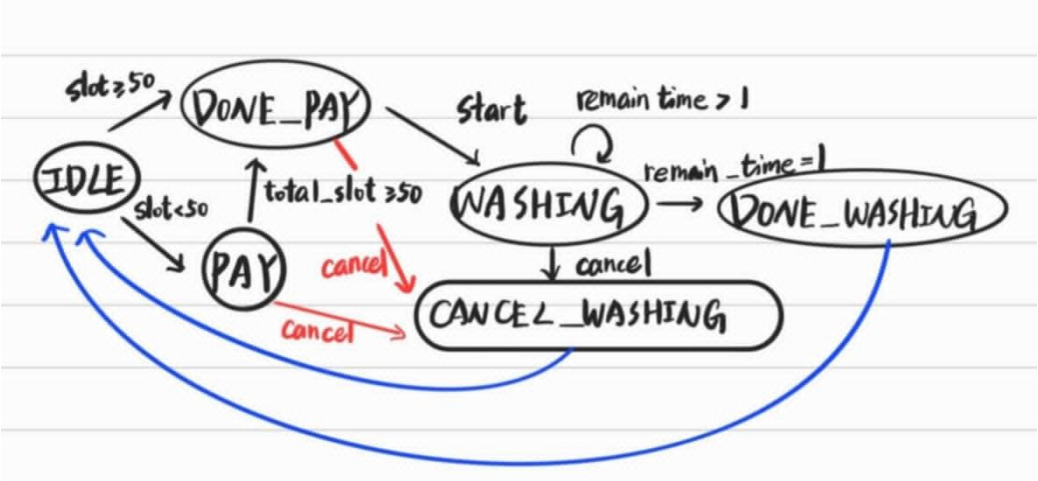
1) **Design a washing machine circuit that meets the functional requirements described in the Lab5 tutorial. The following are the specifications of the washing machine circuit.**



Signal	Type	Bits	Description
clk	input	1	clock
rst	input	1	reset(active high)
slot	input	6	insert money
refund	output	6	refund money
start	input	1	start button. Press the button to start machine.
cancel	input	1	Cancel button. Press the button to stop machine.
set_time	input	4	Setting the washing machine running time. The default washing time is **5 time units**.
busy	output	1	busy light. If machine is running, it should be set to 1.
finish	output	1	finish light. If machine is finish, it should be set to 1 for one cycle.

2) **Please describe your FSM in detail.**

Explanation about your FSM



從 IDLE 開始，如果 slot>=50 直接跳到 DONE_PAY, 若 slot<50 則等累積超過 50 後，再跳至 DONE_PAY。

若在 DONE_PAY, PAY, WASHING 的狀態收到 cancel 訊號，會轉移至 CANCEL_WASHING。

在 DONE_PAY 需收到 START 訊號後才能轉移至 WASHING。

在 WASHING 時須等到 remain_time=2 才轉移到 DONE_WASHING。

3) **After synthesizing your design, you may have some information about the circuit. Please fill in the following form.**

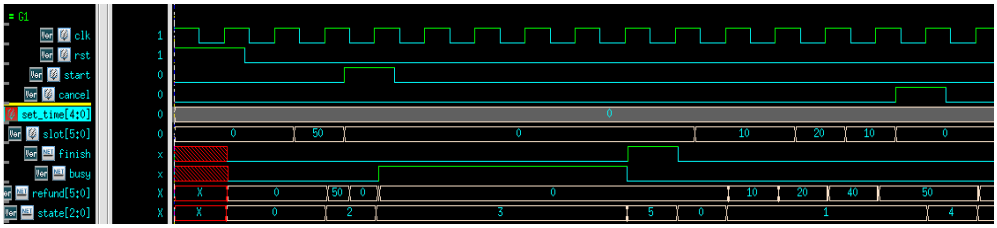
Timing (slack)	Area (total cell area)	Power (total)
9.77	**45.93**	**5.2813e-03 mW**

4) **Please attach your design waveforms.**

Your simulation result on the terminal.

```
**************************
*                        *       |__||
*  Congratulations !!    *      / O.O  |
*                        *    /_____   |
*  Simulation PASS!!     *   /^ ^ ^ \  |
*                        *  |^ ^ ^ ^ |w|
**************************   \m___m__|_|


$finish called from file "tb_WashingMachine.v", line 63.
$finish at simulation time              135400
         V C S   S i m u l a t i o n   R e p o r t
Time: 135400 ps
CPU Time:      0.340 seconds;       Data structure size:   0.5Mb
Fri Mar 21 12:23:43 2025
CPU time: 5.710 seconds to compile + .296 seconds to elab + .410 seconds to link + .376 seconds in
```

Your waveform :

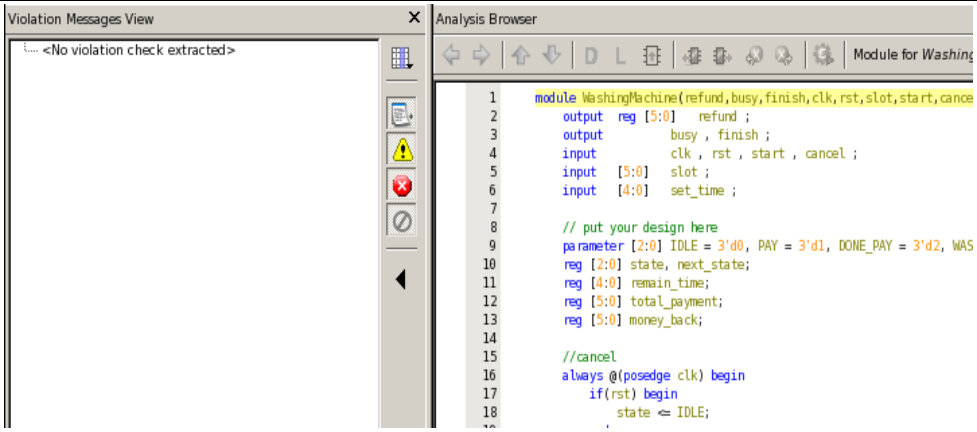


Explanation of your waveform :

Slot=50 後，因為已經足夠，跳至 state2(DONE_PAY)，並且接收到 start 訊號後開始洗衣服，因為沒有設定 set time，因此 state3(WASHING)持續 5 個 clock，完成後轉移至 state5(DONE_WASHING)並升起 finish 訊號。

當投入 slot=10 兩次和 20 一次時，因為皆未滿足 50 元，因此停留在 state1(IDLE)，後雖然因為再投入 10 元滿足 50 元，但因為接收到 cancel 訊號，因此需退費 50 元，state 也轉至 state4(CANCEL_WASHING)

Superlint Coverage



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Lesson Learned

At last, please write the lessons learned from this lab session.

這次的作業相較上周我覺得比較容易，困難的地方在於 tb 測試訊號的方式。以 probC 為例，我原本的寫法雖然 output 都正確，但是因為晚了一個 cycle(沒有在按下 cancel 或是 start 後馬上 output 正確 refund)，因此修改了很久，最後解決方式是放棄原本將 refund 定義為 reg 的方法，改用 wire 避免需要等 clk 的問題。

經過這周的訓練，我對於該變數要放在 sequential 還是 combinational block 越來越熟練，也可以透過波型快速 debug。之前因為都寫軟體的關係，debug 都可以透過 trace code 看變數的值，但是到硬體後需要看懂波型和 clk 之間的關係來除錯，這點會是很重要且基本的能力。

Appendix A : Commands we will use to check your homework

Problem		Command
Labinclass	Compile	% vcs -R moore.v -full64
	RTL-sim	% vcs -R tb_moore.v -debug_access+all -full64 +define+FSDB
	Gate-sim	% vcs -R tb_moore.v -debug_access+all -full64 +define+FSDB+syn

Situation	Command	Example
Simulation for ProbX	make probX	make probA
Dump waveform for ProbX	make nWaveX	make nWaveA
Open superlint for ProbX	make superlintX	make superlintA
Post-synthesis simulation for ProbX	make probX_syn	make probA_syn
Delete built files for simulation, synthesis or verification	make clean	