Department of Electrical and Electronic Engineering

Imperial College London

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Op-Amp Design

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1. Aim

This experiment has been generated to give you some insight and fundamental understanding of basic op-amp design principles, together with an appreciation of op-amp performance limitations.

The main objective of this experiment is to design and study the internal circuitry of a simple bipolar op-amp. The aim is to expose you to some of the basic amplifier building blocks, and also some of the techniques which have evolved over the years for combining these blocks to realise a complete op-amp.

Some of the more detailed circuit analysis has been put into an appendix, which you may want to look at in your own time.

The whole experiment will be conducted in LTSpice. Make sure to have a working laptop with the latest version of the program before starting this lab.

2. Introduction

The voltage-mode operational amplifier (op-amp) is the central key component of most analogue integrated circuits and systems. A typical op-amp architecture is shown in Figure 1, and generally has three gain stages.

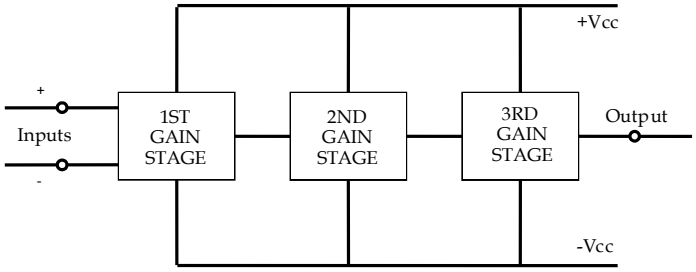


Figure 1 Typical op-amp architecture

The first gain stage is usually some form of directly coupled differential-input-to-single-ended-output converter. This is followed by a second high-gain stage, and a final power output stage which provides unity voltage gain but sufficient current drive into a load. With the advent of integrated circuit technology there has been a demand for more application-specific op-amps with several variations from the standard architecture, basically to suit the technology and performance required.

General purpose 'off the shelf' op-amps such as the 741-type have been around for many years. These op-amps are generally used in closed-loop applications, with external components providing negative feedback around the op-amp. The type of feedback component used will determine the closed-loop transfer function. In discrete analogue design (as covered in standard analogue text books), applications include inverting voltage amplifiers, integrators, differential amplifiers, rectifiers, active filters. Some of these circuits you have seen in the first part of the ADC course.

The BJTs we will use for this design are the 2N2907 (pnp) 2N2222 (npn). They are standard parts in LTSpice. If you cannot find these components after placing your bjt onto a schematic and using the "*Right Click | Pick New Transistor"* command, ask for help to a GTA. The datasheets are provided.

At each step, it may be wise to begin a new section of the simulations in a new schematic rather than deleting what you have already done. You may end up with schematics called "test1.asc", "test2.asc" etc.

3. A glance at the complete Op-Amp circuit

Figure 2 shows the complete op-amp you will "build" (in LTSpice) and test.

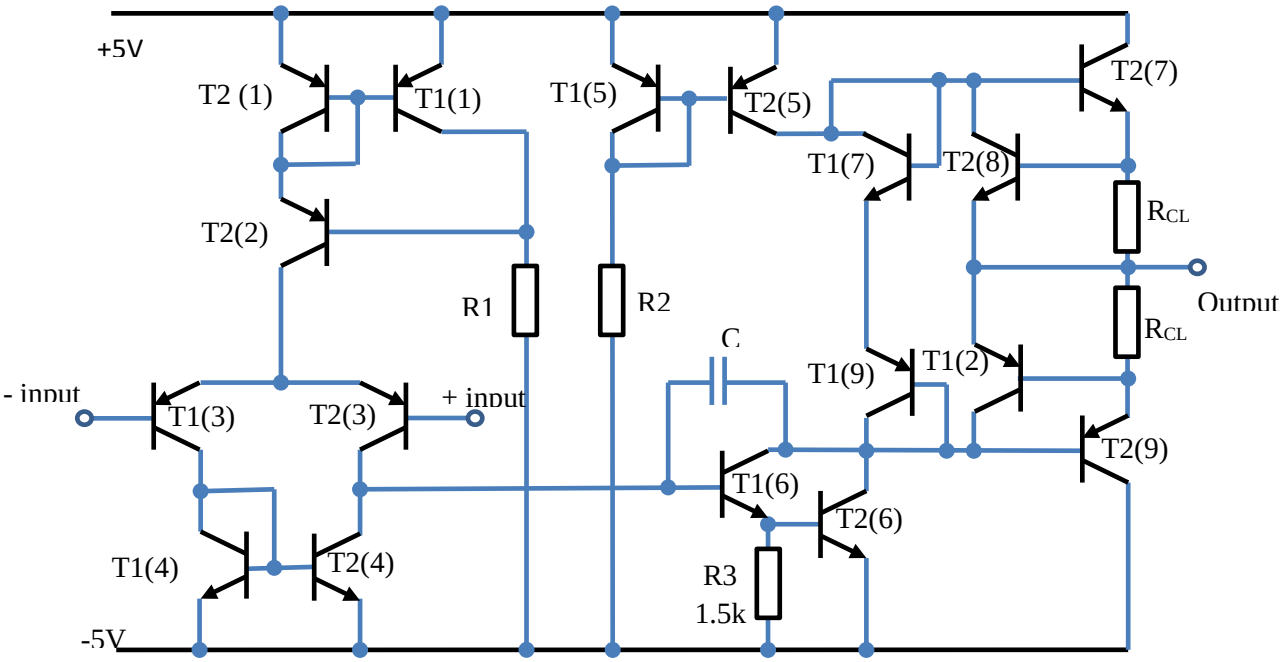


Figure 2 The complete op-amp circuit

The complete circuit looks quite complex. However the aim of the experiment is to break the op-amp down into constituent, recognisable parts, study each block, and view the complete op-amp from a more simplified perspective.

4. The Bipolar Transistor and Some Important Characteristics

The bipolar transistor (BJT) consists of two PN junctions placed back to back (Figure 3). Since the two junctions are placed so close together, significant interaction occurs between them.

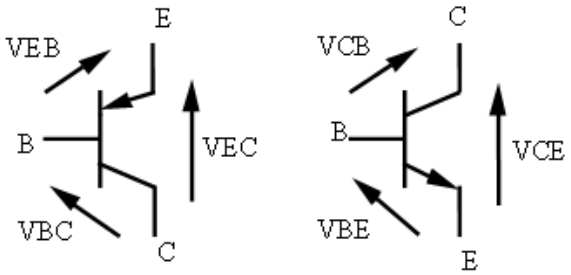


Figure 3 PNP and NPN junctions

Remember from the previous lab and lectures the following formulae. You can obtain the corresponding equations for PNP by replacing V_{BE} by V_{EB} and V_{CE} by V_{EC}.

$$I_C = I_S [\exp(V_{BE}/V_T)] [1+V_{CE}/E_A] \quad (1)$$

$$r_0 \approx E_A/I_C \quad (2)$$

Since $E_A >> V_{CE}$, equation (1) approximates to

$$I_C = I_S [\exp(V_{BE}/V_T)] \quad (3)$$

5. Current Mirrors and Current Sources/Sinks

The current-mirror is probably the most widely used building block in analogue circuit design. A current-mirror is essentially a current amplifier with unity current gain. The term current-mirror is coined since the output current is a duplication or mirror-image of the input current. A current mirror should have ideally zero input impedance and infinite output impedance, to allow maximum current from an input source to be driven directly into a load without loss. Figure 4 shows a simple PNP mirror.

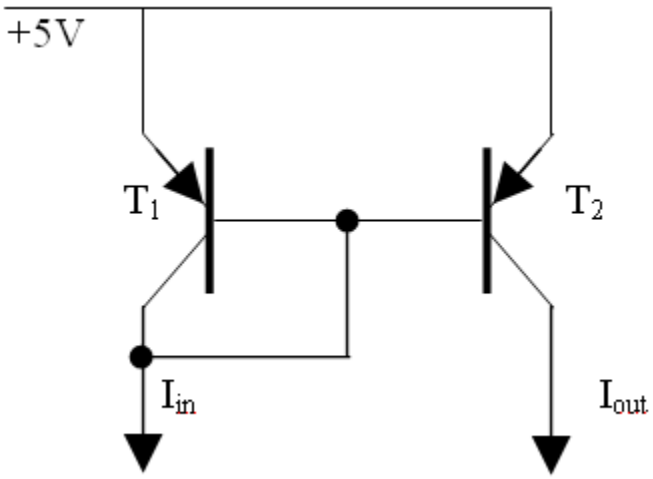


Figure 4 Simple current mirror

The basic circuit consists of two similar transistors with their bases and emitters connected. Since the base-emitter voltages of the two transistors are forced to be equal then from equation (1) their collector currents should also be equal. However, this assumes that both transistors are ideally matched (e.g. same emitter area, operating at same temperature etc.). In practice this is never the case, and a matched transistor pair will always have a small mismatch which results in a slight input – to – output current error. This error is typically quantified in terms of the notional difference in the base-emitter voltages that would be required to eliminate it, and accordingly the error is referred to as the "ΔV_{BE} error". See Appendix 2 for details.

The input transistor T_1 has its collector connected to its base. This is necessary so that both transistors obtain their

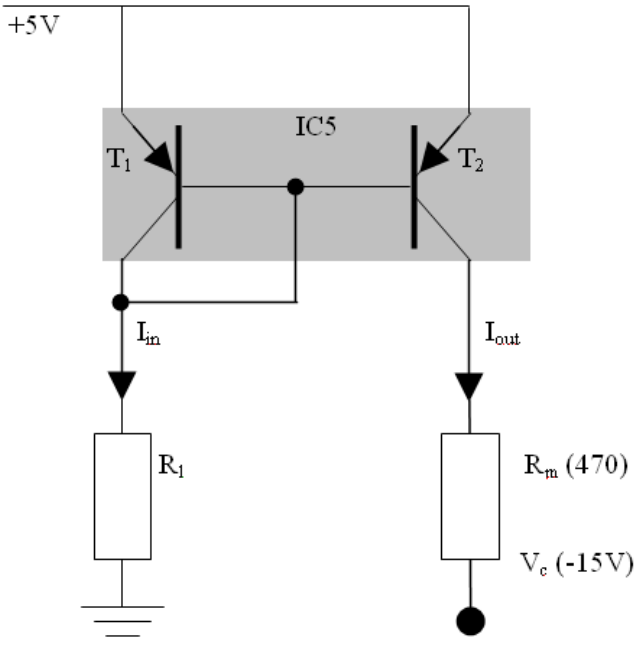


Figure 5 Implementation of simple current mirror

required base current from the input. Transistor T_1 is essentially now just a single PN junction and is referred to as a 'diode-connected' transistor for obvious reasons. Since the base current demand of the two transistors is effectively 'robbed' from the input, there will be a further contribution to error between input and output current (in addition to the error due to ΔV_{BE}). In fact in this simple current mirror, the error due to the base current (also referred to as finite β error) can be quite significant.

A final error contribution is the difference in output to input current due to differences in the collector-emitter voltage ($\Delta V_{CE} = V_{CE2} - V_{CE1}$) of the transistor pair. This error is related to the output characteristic of the BJT, and its deviation from the characteristic of an ideal constant current source. Again this error can be quite significant as you will see later, particularly in the above simple mirror where the two transistors may have to operate with a large V_{CE} differential. (Appendix 2 gives a more detailed description and analysis of various simple current-mirrors).

TEST 1: Simple Current Mirror Experimental Investigation

Diode-connected transistor $T_{1(5)}$ (see Figure 5) fixes the base-emitter voltage of $T_{2(5)}$. The collector-base connection of $T_{1(5)}$ is necessary to ensure that both $T_{1(5)}$ and $T_{2(5)}$ get their required base current, as mentioned earlier.

- Setup a new schematic in LTSpice and simulate the simple current mirror circuit shown above. Use two independent voltage sources for the + 5V power supply and the negative V_C supply.
- Assuming a base-emitter voltage drop of about 0.7V, choose resistor R_1 to give an input current of 1mA.
- Set voltage V_C initially to -10V and measure the input and output currents, and hence the input to output current transfer ratio of this current-mirror: Find the the voltage drop across R_1 (input current), and the voltage drop across R_m (output current).

Since there will be a large difference between the collector-emitter voltages of the two transistors (due to their operating conditions), it is likely that an error will exist between the output and input current of the mirror. This error is related to the transistors' output characteristic and is given approximately by $(V_{CE2} - V_{CE1})/E_A$ (see Appendix 2).

- Is this error close to your measured result?
- Increase V_C to -15V and measure the output current, then slowly reduce V_C to -5V (in steps of 2.5 V) and observe the change in output current. The ratio of incremental change in output voltage to output current is the current mirror's output resistance, $R_{out} = \Delta V_{out}/\Delta I_{out}$. Check that I_{in} remains constant during this exercise.

Note that the output voltage $V_{out} = V_{CE2}$. You may ignore the voltage drop across R_m since this will only be about 0.5V. You may find that the output current does not change very much. This means that your current-mirror is good, since ideally we would want I_o to remain constant and independent of the value of V_C, yielding very high output resistance. If you monitor the change in output current you can estimate the output resistance of the mirror.

The output resistance of this current mirror is simply the output resistance r_{CE2} of T_2. From equation (2), $r_{CE2} \cong E_A/I_C$. E_A for npn is 100 V and for the pnp is 120 V. Compare output resistance with your measured result. Do not worry if your values do not exactly agree, since these equations are only approximate.

TEST 2: Improved Current-Mirror Experimental Investigation

The performance of the simple current mirror is often inadequate in integrated circuit design. A much higher quality current-mirror can be obtained by the addition of just a single transistor, connected between the input and the output of the simple current-mirror. The modified circuit is shown in Figure 6 and is known as the Wilson current-mirror, named after its inventor.

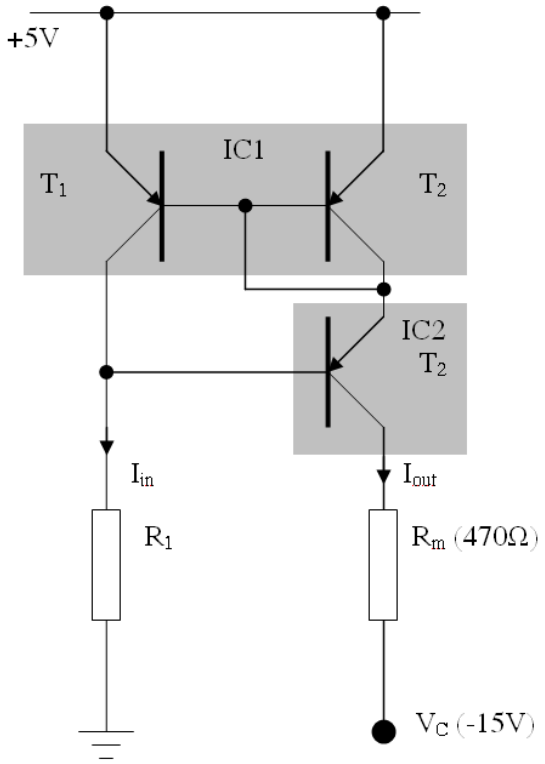


Figure 6 Implementation of the Wilson current mirror

Essentially, the additional transistor forms a 'negative feedback' loop from output to input, and results in a significant improvement in current-mirror output resistance and current transfer performance (see Appendix 2 for detailed operation). Furthermore, the V_{CE} difference between the two primary transistors ($T_{1(1)}$ and $T_{2(1)}$) is now only of the order of V_{BE}, and so the current transfer inaccuracy due to the output characteristic is reduced to approximately V_{BE}/E_A. In addition, the action of negative feedback significantly reduces the finite β error (assuming matched devices); the base current error is now β times smaller than that of the simple two transistor current-mirror (see Appendix 2).

- In a new schematic in LTSpice, simulate the above circuit setting the input current to about 1mA (choosing an appropriate value of $R_{1)}$. Start with V_C set to -15V. Measure the output current and note the improvement in current transfer accuracy compared to the simple current mirror.

- Reduce V_C to -5V in steps of 2.5 V and observe the changes in output current. Comment upon the output resistance of this current-mirror.

- Keep the basic circuit connected, but remove R_m.

6. Amplifier Stages

Single Stage Common Emitter Amplifier

In op-amp design, it is desirable to have a high voltage gain from a single amplifier stage. The most common configuration of a high gain voltage amplifier is the common emitter (CE) configuration (the emitter being the common point to input and output voltages). In fact, the CE stage is the only single transistor configuration that gives high voltage and high current gain simultaneously. Figure 7 shows a simple common emitter amplifier, together with associated biasing circuitry.

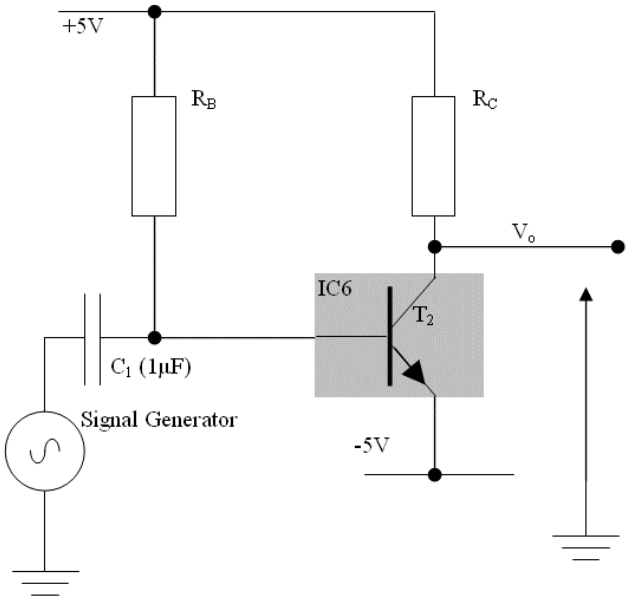


Figure 7 Common emitter circuit

Note that the emitter of $T_{2(6)}$ is at -5V, so the base voltage cannot exceed -4.3V. Make sure that any external connection to the base is AC coupled through C_1, otherwise you risk injecting a DC voltage higher than -4.3 into the base and letting the "virtual smoke" out of the virtual simulated component!

The biasing circuitry is designed as follows. For maximum AC output voltage swing, the DC output of the amplifier in the absence of a signal should sit half way between the power supplies. Using a symmetrical ±5V supply we can bias the output of the amplifier at a quiescent voltage of about 0V. Thus, 5V will be dropped across resistor R_C, so chose R_C to get 1mA of quiescent collector bias current. Choose an appropriate value of R_B (this should work out to be a very large resistor and depends on the actual β of your transistor).

Hint: Since capacitor C_1 is a DC blocking capacitor preventing input signals from affecting the bias levels, then the base current of $T_{2(6)}$ is simply set by R_B. As a starting point, find a typical value of β for Ic = 1mA, from the data sheet. You may then need to adjust R_B for your particular transistor, in order to get V_o to be 0V. From the final value of R_B, you can work out β for your particular transistor.

TEST 3: Voltage Gain and Input Resistance

- In a fresh schematic, simulate the CE amplifier (Figure 7). Make sure that you have set the -5V rail. Check that all DC levels of the amplifier are as you expect.

Figure 8 uses the simplified small signal hybrid-π model of the BJT to give the small-signal equivalent circuit of the common emitter amplifier:

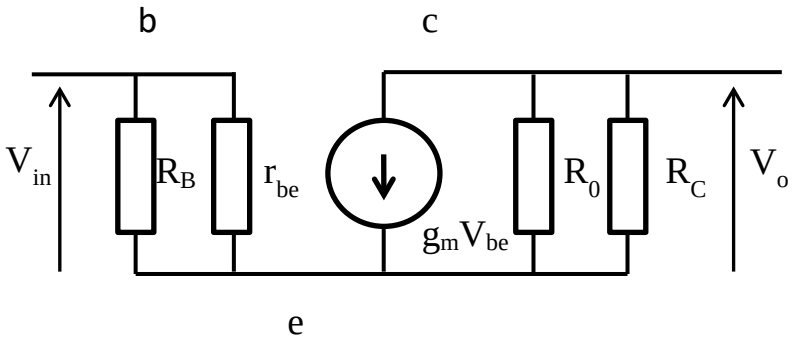


Figure 8 Small signal model of the BJT

where r_{be} is the input resistance of the common emitter amplifier, given by

$$r_{be} = \beta/g_m \quad (4)$$

and g_m is the small signal transconductance of the transistor which relates the change in collector output current to the change in base-emitter input voltage. From equation (3)

$$g_m = dI_C/dV_{BE} = I_C/V_T \quad (5)$$

Remember V_T is the device thermal voltage (about 25mV at room temperature).

From the above equivalent circuit, the voltage gain of the amplifier is

$$A_V = v_o/v_{in} = -g_m [R_C//r_0] \quad (6)$$

r_0 is the output resistance of the transistor (which as you have seen in the lectures, can be calculated as E_A/I_C).

- Derive equation (6) from the equivalent circuit.
- It is important to make sure that this circuit is correctly biased so that the output quiescent DC voltage level is around 0V. Measure the output voltage of the amplifier when its input is open-circuit and adjust R_B to get V_o less than ±0.2V.
- Measure the AC voltage gain of the amplifier by applying a sinewave of $20mV_{p-p}$ at a frequency of 1kHz to the input of the amplifier. Be sure to have the capacitor C_1 in place [1]. Compare the voltage gain with your prediction from equation (6).

Input resistance

Ideally, voltage amplifiers would have infinite input resistance, to ensure that all of the signal voltage from the source is transferred to the input of the amplifier. In other words, it is important to minimise the fraction of the input signal which is dropped across the finite source resistance. To measure the input resistance of the amplifier we will use the following spot frequency test.

- Apply a $20mV_{p-p}$ 1kHz sinewave input, and measure the output voltage of the amplifier, v_{out}.
- Connect 10kΩ in series with the amplifier input. Measure (v'_{out}) the output voltage again – it should have decreased. You can now compute the input resistance of your amplifier, since:

$$v_{out} = v'_{out} (1+10k/ R_{in})$$

Active Loads

The voltage gain of the original high gain amplifier can be increased to a maximum by making $R_C >> r_0$ so that

$A_V = -g_m r_0$ (from equation 7). However, this would be impractical because:

- ☹ It would require a much larger power supply to maintain the same collector current.
- ☹ A 1MΩ resistor could probably consume more chip area than the rest of the transistors in the op-amp (to give you some idea of resistor size in an integrated circuit).
- ☹ Stray capacitance associated with large resistors can be destructive for high frequency performance.

Wouldn't it be good if we could keep the 1mA collector current fixed, with the same 5V power supply, but have a very large collector resistor with almost the same chip area as a single transistor? We can achieve this by the use of an active current source known here as an active load. By the time you do this lab, you will either be doing in lectures, or about to study the use of what are called "active loads" that achieve exactly this.

The current-mirrors investigated earlier have the required properties. A current mirror has a high output resistance, and so the output of the current mirror can be used to replace the passive resistor. Furthermore, the output current of the current-mirror is independently set by its input.

TEST 4: CE Stage With Active Load

- Copy your previous circuit to a new schematic and replace R_C (Figure 7) in the single stage CE voltage amplifier, with the collector output of transistor $T_{2(5)}$ in the simple current mirror design (from section 5) as shown in Figure 9.
- Note that now R_1 (Figure 5), has been replaced by a resistor with a terminal connected to the -5V rail (R_B in Figure 9). Choose R_B to obtain an input current (into IC5) of 1 mA.

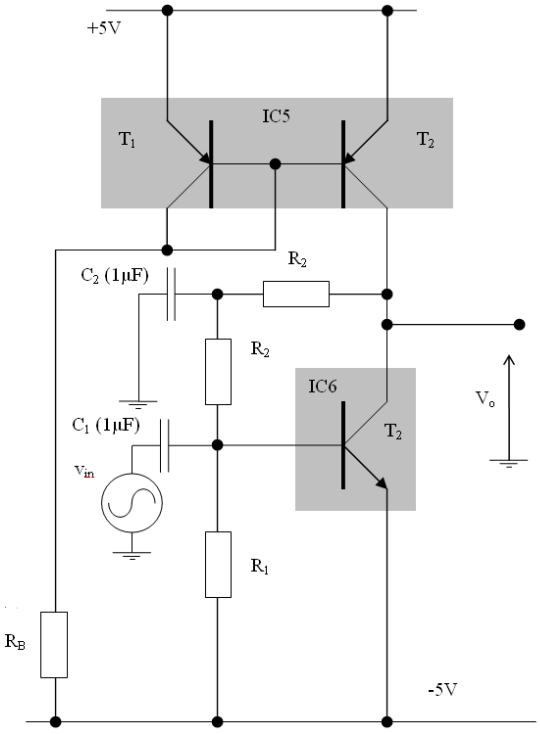


Figure 9 CE stage with active load

Resistors R_1 and R_2 are required to provide base current for transistor $T_{2(6)}$, as well as providing DC stabilisation for the amplifier since it is now a very high gain stage. Effectively we would like the output of the amplifier to sit around 0V DC. $T_{2(6)}$ has a V_{BE} drop of about 0.7V, and you know the (from test 3) value of β at 1mA, so you can compute R_1 and (2 R_2) (I_c is 1mA). Arrange for the current through R_1 to be about twice[1] the base current. The values of R_1 and R_2 should be large to ensure that they do not affect the AC voltage gain or input resistance of the amplifier. Again, you may need to adjust the actual value of (2 R_2) to get 0V output.

- Check initially that the DC output voltage is close to zero for zero input, adjusting (2 R_2) if necessary.

Since R_C is effectively replaced by the output resistance of $T_{2(5)}$ ($r_{ce2(5)}$), the voltage gain from equation (6) increases to:

$$A_V = v_o/v_{in} = -g_m [r_{ce2(5)}//r_{ce2(6)}//R_2] \qquad (7)$$

- Confirm this increase in voltage gain by applying an input signal to the amplifier and observing the output voltage.

Darlington pair

We frequently drive the input of a voltage gain stage from the output of the previous gain stage. It is therefore desirable to keep the input resistance of a voltage gain stage as high as possible, so that it does not load the previous stage. One solution used to increase the input resistance is emitter degeneration. Another useful solution in bipolar circuit design is the well - known Darlington pair configuration, used in place of a single common emitter transistor.

The Darlington connection is shown in Figure 10, replacing the single CE transistor $T_{2(6)}$ (hence we can keep the same old value of R_B).

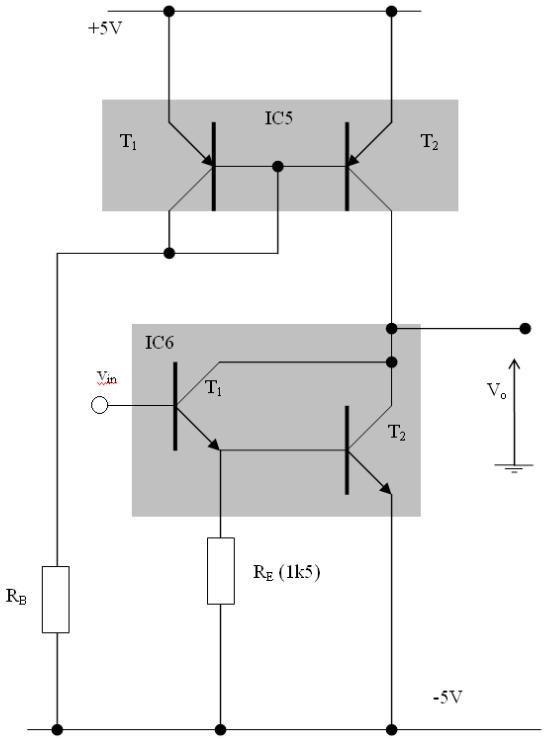


Figure 10 Darlington connection, with active load

[1] $I_B = I_C/\beta$. The voltage across R_1 is 0.7, and the voltage across $2R_2$ is (5-0.7). If the current through R_1 is $2I_B$, then the current through (2 R_2) must be $3I_B$

Assume initially R_E is disconnected. The effect of $T_{1(6)}$ is to increase the apparent input resistance of $T_{2(6)}$ by a factor of about β (resistance reflection rule!). This is essentially because the input base current of the transistor pair is the base current of $T_{2(6)}$ divided by $1+\beta_1$. The total input resistance of the pair is the sum of the input resistance of $T_{1(6)}$ and the modified input resistance of $T_{2(6)}$, and detailed analysis shows that this is given by:

$$r_{in} \approx 2\beta_1\beta_2/g_{m2} \qquad (8)$$

The 1k5 resistor connected across the base emitter junction of $T_{2(6)}$ in the actual circuit ensures that the collector bias currents through transistors $T_{1(6)}$ and $T_{2(6)}$ are almost equal. This is important for high frequency operation, since the bandwidth of a transistor varies with collector current (see the data sheet). With equal bias current, the two transistors should experience similar high frequency behaviour. However r_{be2} now appears in parallel with R_E, and so the input resistance of the amplifier becomes:

$$r_{in} \approx \beta_1(R_E//(\beta_2/g_{m2})).$$

Since the output impedance of the long tailed pair which supplies the input (we will consider this in the next section) is low (essentially 2k), the high input impedance is important. $T_{1(6)}$ is essentially an emitter follower with unity voltage gain, and the overall transconductance of the pair is essentially that of $T_{2(6)}$. Note that this transistor now carries only ~half of the total collector bias current.

Save the finished schematic from this section as "block2.asc"

7. The BJT Long Tailed Pair Differential Amplifier

Probably the most important input stage used in amplifier design is the emitter-coupled differential amplifier, better known as the Long Tailed Pair (LTP). It is a directly coupled amplifier with high differential-mode voltage gain, but has a low voltage gain to common-mode input signals (such as noise appearing on the two inputs). Figure 11 shows a typical LTP amplifier.

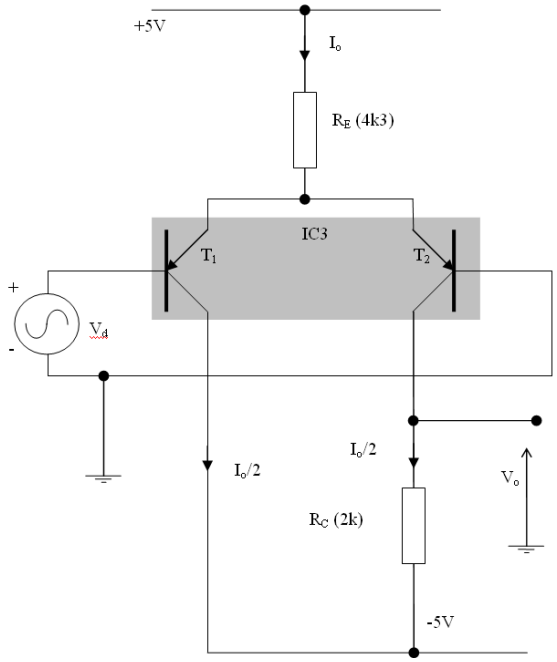


Figure 11 The long tailed pair

The objective of this section is to maximise the differential-mode voltage gain and minimise the common-mode voltage gain of the amplifier.

From a small signal analysis of the amplifier (refer to Appendix 2), the differential-input-to-single-ended-output voltage gain of the amplifier is:

$$A_d = v_o/v_d = (g_{m2}/2)\ (r_{ce2}//R_C) \qquad (9)$$

where v_d is the differential input voltage of the amplifier, $v_d = [V(+) - V(-)]$.

A_d is half the voltage gain of a single-stage common emitter amplifier (see equation (6)). Remember that g_m and r_0 are calculated from the large signal parameters V_T and E_A, where $r_{ce2} \cong E_A/I_{C2}$ and $g_{m2} \cong I_{C2}/V_T$.

TEST 5: Differential Voltage Gain and Input Resistance

Differential voltage gain

- In a new schematic, construct the LTP amplifier.
- A differential input is obtained by grounding the -ve input (base of $T_{2(3)}$) terminal and supplying an input signal v_d to the +ve input (base of $T_{1(3)}$) terminal.
- Decide why the input polarities are in this order. With $v_d = 0$, check the dc value of v_o (it should be around -4V – why?)
- Set v_d to 15 mV_{p-p} at 1kHz, and measure the voltage gain of the amplifier.
- How well does this value compare with the theoretical value (equation (9)?

Note that the dc offset of about -4V is desirable, because the dc input level of the Darlington pair is (-5V + $2V_{BE}$), and the LPT is being directly coupled.

You may find that the voltage gain is less than the above theory would predict. This could be due to the input loading effect of the series base spreading resistance (r_{bb}) of the lateral PNP devices. This resistance can be fairly large (several hundred ohms for lateral devices). If β is low for your device, the input base current would be fairly large causing a voltage drop across r_{bb}, thus reducing the gain. You may want to check this out, but only if you have plenty of time!

Differential input resistance

The small-signal differential input resistance of the amplifier is

$$r_{ind} \cong 2\ r_{be} = 2\beta/g_m \qquad (10) \text{ (see Appendix 2)}$$

assuming equal collector currents through both transistors, and matched β values. Calculate the theoretical value of r_{ind} and then experimentally measure r_{ind} using a spot frequency test at 1kHz (refer to section 6, TEST 3, for more detail on this measurement). Because of the imperfections described above, your measured values of gain and r_{ind} will probably be within a factor of 1.5 of theory.

TEST 6: Common-Mode Voltage Gain and Common-Mode Rejection Ratio (CMRR)

Common-mode voltage gain.

A figure of merit of the LTP is its ability to reject common-mode input signals (such as noise) appearing at both inputs of the amplifier. The common-mode gain of the amplifier is the ratio of amplifier output voltage to a common-mode input voltage.

The small signal common-mode gain of the amplifier (see Appendix 2) is given by

$$A_c = v_o/v_c = -R_C/2R_E \qquad (11)$$

Ideally we would want a common mode gain of zero, so let's now consider how good this simple LTP amplifier is at rejecting common-mode input signals.

Apply a common-mode input voltage v_c to the amplifier by simply applying the same input signal to both the +ve and -ve input terminals of the amplifier. Set the input voltage v_c initially to 15 mV_{p-p} at 1kHz and measure the output voltage, and hence calculate the common-mode gain of the amplifier. You may need to increase v_c in order to measure an output voltage. Compare your measured result with the theoretical prediction given by equation (11).

- ☹ We could reduce R_C to reduce the common mode gain, but this would be most undesirable (why?). Instead, we will increase R_E.

Common-mode rejection ratio (CMRR)

Manufacturers usually quote the CMRR of an op-amp as the ratio of differential gain to common-mode gain:

$$CMRR = A_d /A_c = g_m R_E = (I_o/2V_T)\, R_E \qquad (12)$$

or, in decibel (dB):

$$CMRR_{db} = 20 \log_{10} (R_E I_o/2V_T) \qquad (13)$$

CMRR is a better representation of common-mode capability, since it clearly illustrates the combined requirement of obtaining high differential voltage gain by increasing I_o and low common-mode gain by increasing R_E. Ideally the CMRR of an amplifier should be infinite.

- What is the CMRR of the amplifier you have built?

To increase the CMRR of the amplifier we have two options: either to increase the tail bias current I_o (which would be undesirable due to increase in power consumption), or to increase the tail resistance R_E.

Once again we have a situation whereby increasing a resistor value improves a particular circuit performance. However by physically increasing R_E the circuit will require a larger positive power supply voltage to maintain the same bias current I_o. Since we can obtain a large resistance with the same bias current and power supply voltage using an active current sink, we can simply replace R_E with a current mirror design. We can use the Wilson current-mirror constructed in section 5 to optimise the amplifier's CMRR, because it offers a very high output resistance.

- Connect the collector output of the Wilson current-mirror you constructed in section 5 in place of resistor R_E (Figure 12).

- **Set R1 to give a tail current of 1 mA.**

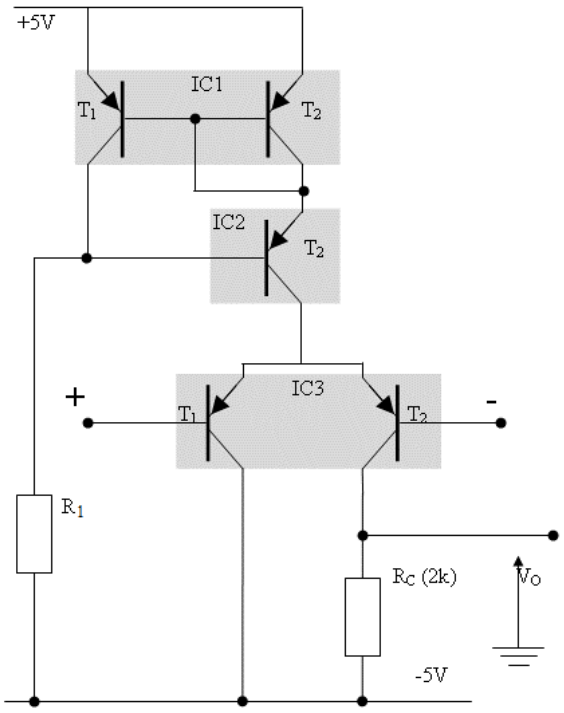


Figure 12 LTP with active load

- Repeat your measurement of small signal common-mode voltage gain and note the improvement over the previous circuit. Remember to first check your DC output voltage.

Increasing the Differential Voltage Gain

Now we have improved the CMRR of the LTP amplifier, the next step is to improve the differential voltage gain. To do this, the output collector resistor R_C can be replaced with yet another active current source. Before you do this let me emphasise a very important analogue design rule. Never waste signal current; if you have got it, use it! The circuit is inefficient if you generate signal current then waste it. Going back to the LTP, we are wasting the signal current in the collector lead of $T_{1(3)}$ which simply runs into the negative power supply. This current is the anti-phase version of the collector current of $T_{2(3)}$, which forms our output. Let's use it!

In the high voltage gain circuit (Figure 13), the simple current mirror (met earlier in section 5, but now in NPN format) performs two functions:

(i) $T_{2(4)}$ replaces R_C to create a high output resistance current-mirror active load, and hence improves the amplifier's differential voltage gain.

(ii) The signal current through $T_{1(3)}$ which was wasted to the supply is now 'current mirrored' to the output, and thus adds to the signal current of $T_{2(3)}$. This has the effect of further doubling the voltage gain. The 100k resistors and 1µF capacitors ensure that the circuit is stabilised for DC voltages but still give a very high voltage gain for AC signals.

- Make this modification to the circuit since this is required for the final op-amp.

The small signal voltage gain should now increase to

$$A_d = g_{m2(3)} [r_{02(3)} // r_{02(4)} // R] \qquad (15)$$

This value is of similar magnitude to that of the single-stage CE amplifier with active load investigated earlier and so you will again need to attenuate the input signal to be able to measure the gain.

It is interesting to note throughout these design exercises how we are constantly eliminating the use of resistors. A discrete to integrated circuit transformation!

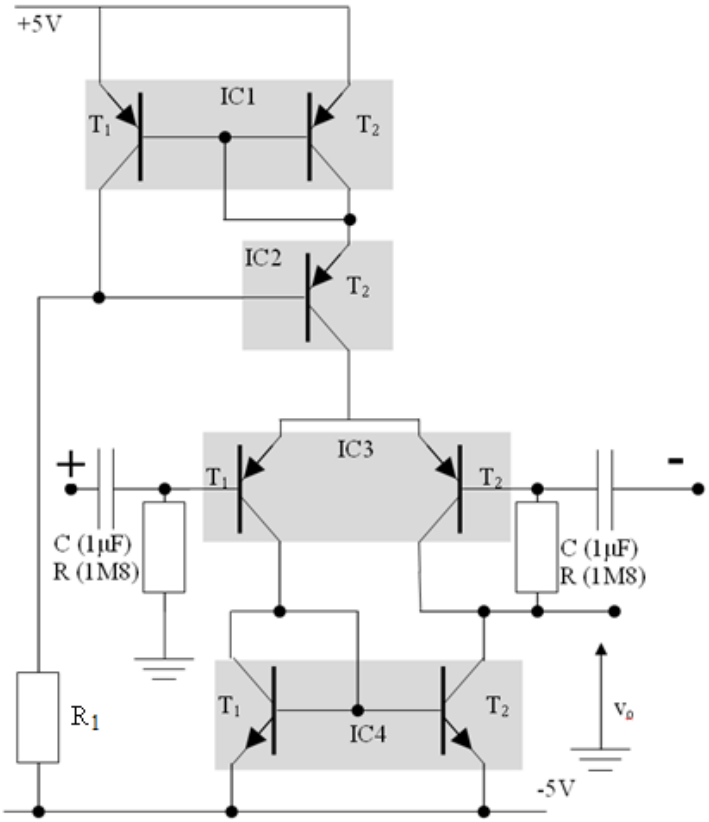


Figure 13 Complete input stage

Save the finished schematic from this section as "block1.asc"

8. Power Amplifier Output Stages

Power amplifiers are capable of providing high voltage swing and high current drives into a load, and this type of circuit is most desirable as the output stage of an op-amp. So far we have developed amplifiers which generally boost the input signal voltage up to a large signal level. The role of the power amplifier is to post-amplify the signal with high current gain, but unity voltage gain. The simplest circuit to achieve this is the class B complementary emitter follower, better known as the push-pull common-collector amplifier (Figure 14).

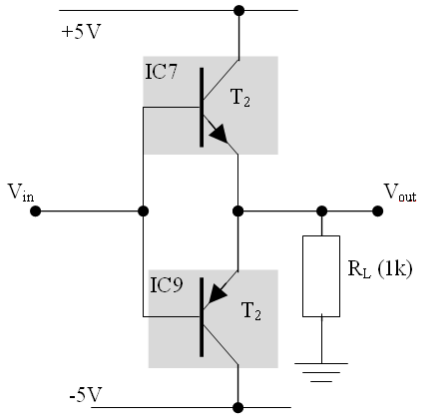


Figure 14 Simple class B push-pull amplifier

The circuit provides a well-defined unity voltage gain since the input signal voltage is fed into the base and out of the emitter of a transistor. It also has a high current gain of approximately β.

There is (intentionally) no bias current flowing through the transistors, and so with zero input signal voltage both transistors are cut off. This has the advantage that under quiescent conditions (no signal) the standby power dissipation is virtually zero, and so the amplifier is highly efficient. The disadvantage however is significant 'cross-over distortion', due to the fact that as the input signal changes polarity (crosses zero) neither transistor will conduct until a signal level of about 0.55V is reached.

TEST 7: Cross-Over Distortion

- Construct the power amplifier circuit using $T_{2(7,9)}$.
- Input a sinusoidal waveform of $2V_{p\text{-}p}$ at 1kHz and sketch the output waveform. Cross-over distortion should be clearly evident.
- What is the voltage gain of the amplifier, and why is it misleading to quote this value?
- Why do you think this amplifier is termed 'push-pull'?

There are various ways of reducing the low-level cross-over distortion to an acceptable level, the simplest being to supply some dc bias for the transistors to just keep them in their forward active region, (Figure 15). This circuit is generally referred to as a class AB push-pull power amplifier.

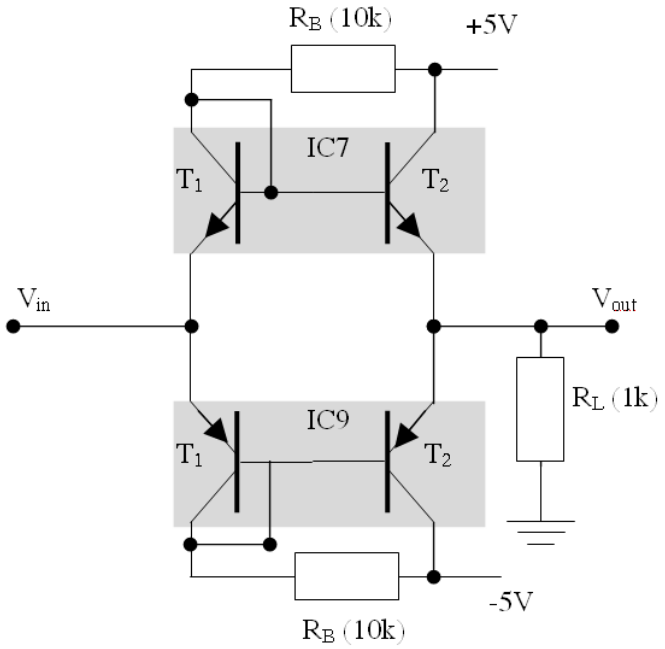


Figure 15 AB push - pull

The DC bias current of the amplifier is set by the two resistors R_B and the two diode-connected transistors $T_{1(7,9)}$.

If T_1 and T_2 are well matched, then the collector currents will be the same (note current-mirror similarity). The bias network therefore ensures that both $T_{2(7,9)}$ are biased 'just on' for zero input signal, and so reduces cross-over distortion.

- Construct this circuit using the two transistors $T_{1(7,9)}$.
- Input a sinusoidal waveform of $2V_{p-p}$ at 1 kHz and again observe the output. Sketch the new output waveform and compare the magnitude of cross-over distortion to the previous class B amplifier.

TEST 8: Current Limit and Short Circuit Output Protection

In the power amplifier you have built, accidental short circuit at the output will 'blow' the output transistors, since there is no current limiting at the output. Output current limiting is extremely important, to protect the output devices in the amplifier from over-loading.

This block will not affect the operation of your amplifier, but it provides you with some general knowledge on how to design a block to protect your circuit from potential mistakes (very important if you were actually building the circuit, rather than simulating it).

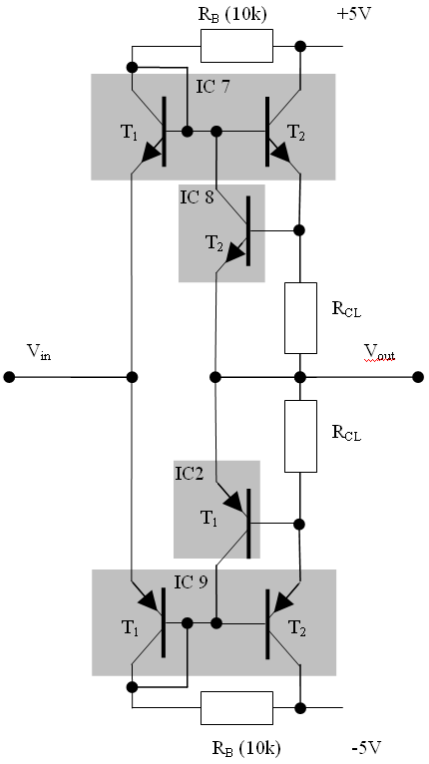


Figure 16 Current limiting circuit

Consider the top half of the power amplifier (Figure 16): when $T_{2(7)}$ is active and conducting current through the load, $T_{2(8)}$ will remain off. $T_{2(8)}$ will only come on when the current through resistor R_{CL} is sufficient to cause a voltage drop of greater than about 0.6V, and hence forward bias $T_{2(8)}$. $T_{2(8)}$ will conduct and 'rob' current from the base of $T_{2(7)}$. The load current will thus remain fixed at approximately $0.6/R_{CL}$. This is the output current limit of the amplifier and is set by resistor R_{CL}.

For example, using an output transistor which has a maximum current rating of say 12mA, you might wish to output current limit your amplifier to 6mA. A suitable value of R_{CL} would in this case be 100Ω.

- Find (data sheet) the maximum current rating for T_2 and work out a suitable resistance value (R_{CL}) to current limit to about half of this.

- Connect current limiting circuitry to both $T_{2(7,9)}$ in the previous class AB power amplifier, using transistors $T_{2(8)}$ and $T_{1(2)}$ and suitable resistors R_{CL}.

- Test the complete circuit by keeping V_{in} fixed at $2V_{p\text{-}p}$ and reduce the load resistance of the amplifier to say 10Ω. The current through the load should be the current limit value.

A drawback of this classical class AB power amplifier is the use of resistors R_B to set the bias current. A common collector (which is a unity gain voltage amplifier) should have very high input resistance, and this is seriously degraded by R_B. Furthermore, the larger the voltage drop across resistor R_B, the greater the limitation imposed on the maximum output voltage swing of the amplifier, since

$$V_o \max \approx V_{supply} - VR_B - V_{BE} \qquad (16)$$

To create the effect of a large value of R_B while reducing the value VR_B to an acceptably low level, we can replace the resistors with active current sources (current-mirrors). This will allow a much larger undistorted output voltage swing. We will implement this technique in the final op-amp design.

Save the finished schematic from this section as "block3.asc"

9. Putting the op-amp together

You have now made three circuit blocks. When you connect them together, you will finish up with the circuit in section 3 - follow the instructions to get there!

So far you have been exposed to some of the basic analogue building blocks. We shall now see how these blocks can be arranged and connected together to form a complete op-amp. Block (1) is the differential input amplifier (see Figure 13). Block (2) is the high gain single-stage amplifier (see Figure 10), and block (3) is the output stage power amplifier (Figure 16). Before we connect the blocks together there are certain biasing components to be removed, as these were only required for stand-alone testing.

Final connection

- To construct the complete op-amp shown in section 3 at the beginning of the experiment, make the following modifications to the circuit:

  i. In Block (1) (Figure 13) remove the two 100k resistors and the input capacitors (1μF).

  ii. In Block (3) (Figure 16) remove the two R_B's (10k).

  iii. Connect the output of Block (1) to the input of Block (2) (V_o1 to $V_{in}2$). This creates the very high differential gain stage of the op-amp.

  iv. In Block (2) (Figure 10) disconnect the collector of $T_{2(5)}$ from the collectors of $T_{1(6)}$ and $T_{2(6)}$.

  v. The joint collectors of $T_{1(6)}$ and $T_{2(6)}$ of Block (2) should now be connected to the base-collector connection of $T_{1(9)}$ in Block (3). This forms the driver source of Block (3).

  vi. The collector of $T_{2(5)}$ in block (2) should also be connected to the base-collector of $T_{1(7)}$ in block (3). Remember that the value of R2 should be chosen to supply a collector current of 1 mA to $T_{1(7)}$.

  vii. Note that in going from Figure 11 to Figure 2, the inverting and non-inverting inputs have become swapped round (why?).

TEST 9: Testing The Complete Op-Amp

At this stage you are strongly advised to label your nets, so you can "abstract" your analysis to the block shown in Figure 17. Set up labels for +/-VCC, +/-INPUT and OUTPUT.

Unity gain test and compensation

There are many tests we can make to establish the various performances of the op-amp. Probably the simplest test is to connect the op-amp in the unity voltage gain configuration known as a voltage follower, Figure 17. Because the high gain stage (block 2) is phase inverting, the polarity of the inputs in the differential input stage is reversed. So to apply negative feedback the output of the op-amp must be connected as shown below.

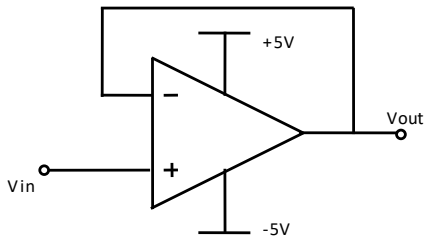


Figure 17 Unity gain voltage follower

- Apply an input signal of about 100 mV_{p-p} at 1 kHz to the input of the voltage follower and measure its voltage gain. You will probably find that the op-amp oscillates - if it doesn't, then the chances are that it will not work properly!

Frequency Compensation

At higher signal frequencies, the op-amp output signal begins to lag behind the input signal. Effectively, there is an open-loop negative phase shift from input to output. When we apply negative feedback around the op-amp this additional phase shift can cause problems, because it may turn the applied negative feedback into positive feedback which is likely to result in oscillation.

In order to enable an op-amp to be used with any amount of negative feedback, we must be sure that even as the open loop gain of the op-amp falls and the output starts to lag behind the input, positive feedback does not occur with significant magnitude to cause instability

A solution is to make the frequency response of the amplifier dominated by one very low frequency 'pole'. This is achieved by adding a compensation capacitor C from the output of the second gain stage to the output of the first gain stage; effectively we add a capacitor link across the collector-base junction of $T_{1(6)}$ in block (2). The value of compensation capacitor could be anywhere in the range 10pF - 1nF for your design.

- Choose a suitable value of C to 'tame' your amplifier. Use the minimum value that you can get away with!

TEST 10: Final Tests

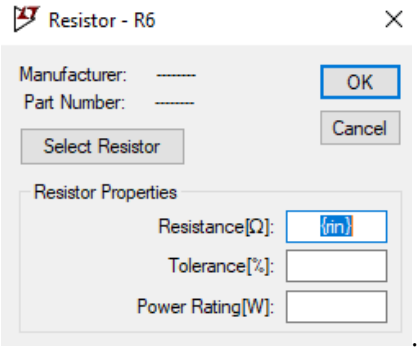
If time permits, measure the small-signal bandwidth of your op-amp by keeping v_{in} fixed at $10mV_{p-p}$ and increasing the frequency, until v_o drops to $(10/\sqrt{2})$ mV. This frequency is the -3dB bandwidth of your unity gain amplifier, better known as the unity gain bandwidth product (GB) of the op-amp. It is also worth

measuring your amplifier's gain at 1 kHz. (An accidental short circuit will also give a unity gain voltage follower!).

- Set up an AC analysis to obtain the bode plot of your amplifier and comment on the results.

Finally, choose suitable values of R_{in} and R_f to create a x-5 amplifier (Figure 18), and convince yourself that your op-amp really works!

- Set up an AC analysis to obtain the bode plot of your amplifier with DC gains of -5, -100 and -1000 and comment on the results.
- Hint: you can set up a parametric sweep of Rf as a function of Rin and gain. You do this by declaring a value of Rin with the directive *.param rin=TYPEVALUEHERE*. Now we set the Rin to *rin* by declaring the value in curly brackets:



Now we set a parametric sweep for the gain as the spice directive: *.step param gain list 5 100 1000*. We can now declare the value of Rf as {gain*rin} similarly to how we have set Rin, and just run the AC simulation.

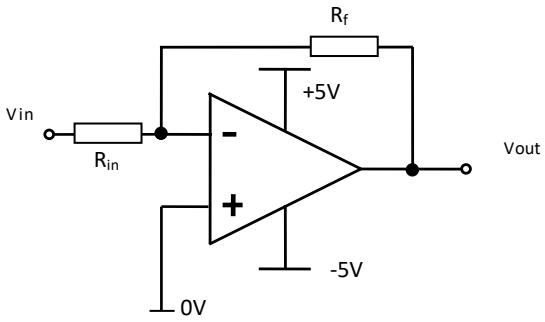
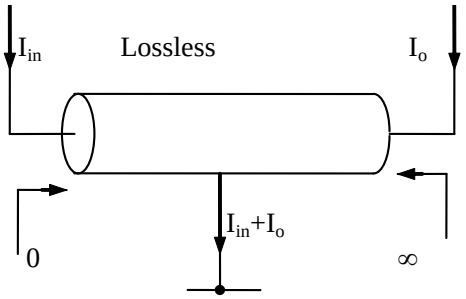


Figure 18 Inverting amplifier Vout /Vin = - Rf / Rin

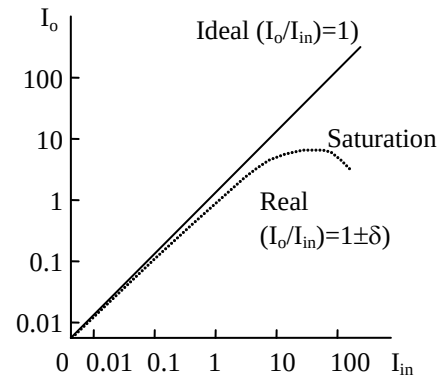
It is a stimulating reward when you see the non-linear 'wild' high gain op-amp you have constructed stabilise itself and behave very calmly as a closed-loop amplifier with well-defined gain. This is one of the most fascinating applications of negative feedback.

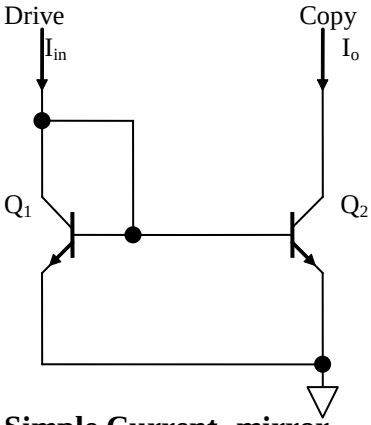
10. Appendix I Current Mirrors

Ideal Current Mirror



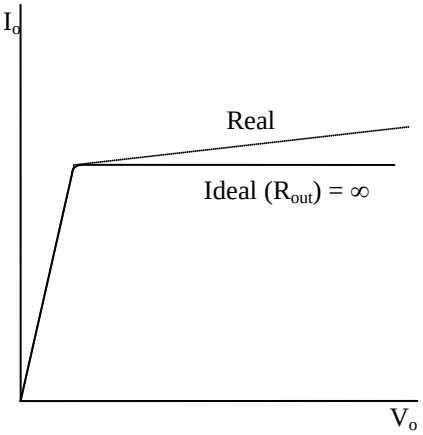
Ideal Current-mirror





Simple Current -mirror

(Widlar 1965)



Simple Current-mirror

Ideally, $I_o/I_{in} = 1$, $R_{out} = \infty$

In reality:

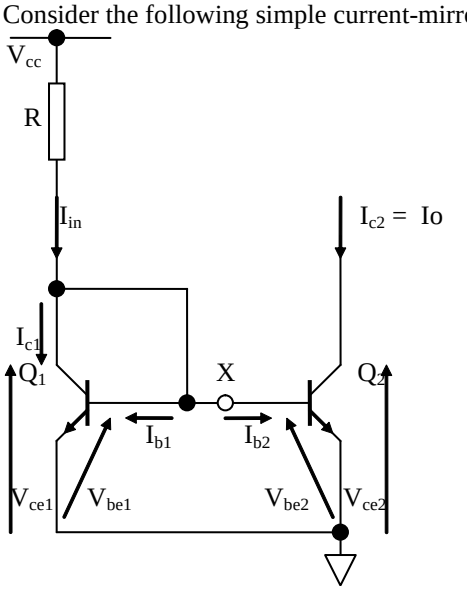
$I_o/I_{in} = 1 - \delta_1 + \delta_2 + \delta_3$

where δ_1 is the finite beta error due to supply of base currents to Q_1 and Q_2

δ_2 is the ΔV_{be} error, or V_{be} differential error due to emitter area mismatch between Q_1 and Q_2

δ_3 is the ΔV_{ce} error due to finite output resistance of Q_1 and Q_2

Consider the following simple current-mirror:



The input current for this circuit is

$I_{in} = (V_{cc} - V_{be1}) /R$

and we will show that:

$I_o/I_{in} \approx 1 - 2/\beta + \Delta V_{be}/V_T + \Delta V_{ce}/Ea$

i.e. $\delta_1 = 2/\beta$, $\delta_2 = \Delta V_{be} /V_T$, $\delta_3 = \Delta V_{ce} /Ea$

where ΔV_{be} is the V_{be} mismatch of the two transistors, and $\Delta V_{ce} = (V_{ce2} – V_{ce1})$ is the difference between the collector voltages.

1) Finite beta error

From the circuit, $I_{in} = I_{c1} + I_{c1}/\beta_1 + I_{c2}/\beta_2$

Assume that $\beta_1 = \beta_2 = \beta$ and $I_{c1} = I_{c2} = I_c$

For a matched transistor pair then,

$I_{in} = I_c[1+2\beta]$

$I_o/I_{in} = I_c/I_{in} = (1+2\beta)^{-1}$

$\approx 1-2/\beta$

Thus $\delta_1 = 2/\beta$

2) ΔV_{be} and ΔV_{ce} errors

The V_{be} mismatch represents any discrepancy between the saturation currents of the two transistors and is defined such that if Q_1 has a saturation current I_{s1}, then the saturation current of Q_2 will be giveb by $I_{s2} = I_{s1}\exp(\Delta V_{be}/V_T)$. The collector currents in the current mirror circuit can therefore be expressed as:

$I_{c1} = I_{s1}[\exp(V_{be}/V_T)]\ (1+V_{ce1}/Ea)$
$I_{c2} = I_{s1}[\exp\{(V_{be} + \Delta V_{be})/V_T\}]\ (1+V_{ce2}/Ea)$

where V_{be} is the actual base-emittter voltage (which is common to both transistors). The two transistors are assumed to have the same Early voltage, but may have different collector voltages. From these relations the ratio of the collector currents will be:

$I_{c2}/I_{c1} = [\exp(\Delta V_{be}/V_T)](1+V_{ce2}/Ea)/(1+V_{ce1}/Ea)$

Provided $\Delta V_{be} << V_T$ and $V_{ce} << Ea$, this can be approximated as:

$I_{c2}/I_{c1} \approx 1 + \Delta V_{be}/V_T + (V_{ce2} - V_{ce1})/Ea$

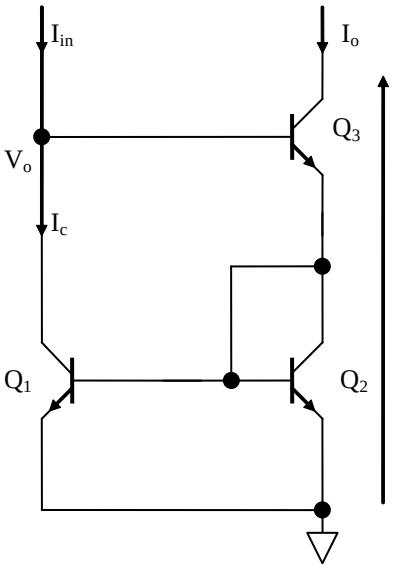
Comparing this with the original current ratio expression, and noting that $I_{c2}/I_{c1} = I_o/I_{in}$ in the absence of finite beta error, we see that:
$\delta_2 = \Delta V_{be}/V_T$ and $\delta_3 = \Delta V_{ce}/Ea$

Example

A simple (PNP) current-mirror is operating at room temperature, has an output current of 1mA and V_{ce2} = 10V.
Typical manufacturers' specifications for popular BJT types such as the SM2220 transistor arrays operating under these conditions are:
$\beta = 150$, $\Delta V_{be} = \pm 0.3$ mV, Ea = 100V and V_{be} = 0.58V. The figures indicate that
$\delta_1 = 2/\beta = 1.3\%$ error
$\delta_2 = \Delta V_{be}/V_T = 1.2\%$ error, V_T = 25 mV
$\delta_3 = (V_{ce2} - V_{ce1})/Ea = (10 - 0.6)/100 = 9.4\%$ error
So the <u>most serious error</u> is due to $\Delta V_{ce} \rightarrow \delta_3$ error
Note: Output resistance $\approx Ea/I_c$
$= 100/0.001 = 100k\Omega$
- which is quite low compared to higher performance mirrors which will be discussed later.

Wilson Current-Mirror

Probably the most popular current-mirror connection to date



Wilson Current -mirror

Function of Q_3

1) Buffers input (similar to buffered current-mirror) so that there is a reduction in δ_1.
i.e. $\delta_1 = 2/\beta^2$

2) Provides 'negative feedback loop' around Q_1, providing mirror with high output resistance similar to the cascode current -mirror
i.e. $R_{out} = [\beta_o/2]R_o$
We shall now consider this feedback operation in more detail:
Principle of operation
Let's 'use our thumbs'
1. Assume that I_{in} is constant
2. If V_o increases, so will I_o
3. The increase in I_o causes an increase in V_{be2}
4. V_{be2} increasing causes V_{be1} to increase
5. and this causes an increase in I_{c1}
6. If I_{in} is constant, then I_{b3} must reduce, and the base of Q_3 is pulled down through the finite output resistance of Q_1. V_{be3} must therefore also decrease.
7. Reducing V_{be3} causes a reduction in I_o opposing the assumed increase at step (2)
8. As I_o remains virtually constant with changes I V_o then R_{out} must be very large.

One can show that $R_{out} = [\beta_o/2]R_o$
Study the small signal analysis at your leisure. Good practice!

11. Appendix II - The Long-tailed pair and application review

Introduction

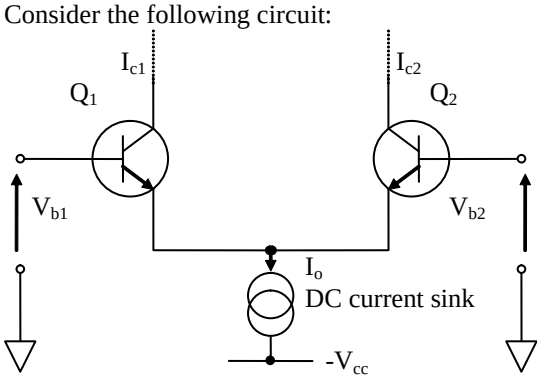
Probably the most important front-end amplifier in analogue circuit design is the long-tailed pair (LTP), also referred to as the emitter-coupled differential amplifier

The objectives of this session are to review the LTP and examine some of the many useful circuit applications that can be handled by the circuit.

In addition to basic differential amplifiers, the BJT LTP has wider applications, due to the well-defined exponential relationship between I_c and V_{be}, that can be extremely useful, for example in log, antilog, and multifunction generators

Analysis

Consider the following circuit:



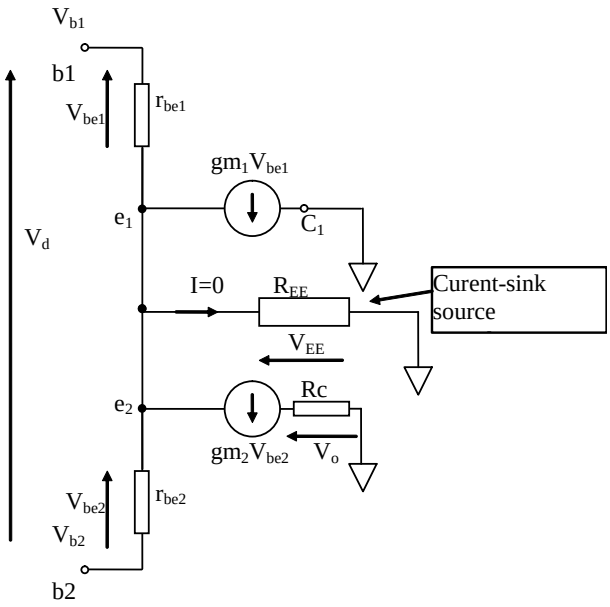
NB As usual, we will neglect base current for simplicity, since $I_b << I_c$

I_o is a constant current sink, such as one of the current-mirror circuit examined earlier.

Small-Signal Analysis

Rather than approaching the analysis from the large signal characteristics, it is sometimes more convenient to use the small-signal circuit:-

Let's use the simplified low frequency model, and, assume that the collector resistance is much lower than r_0, so that it is reasonable to omit r_0. The small-signal equivalent circuit is shown below.



If $V_{b1} = V_d/2$ and $V_{b2} = -V_d/2$ i.e. no common-mode signal, then $V_{ee} = 0$, since the emitters are at zero signal potential.

Differential Input gain, A_{vd}

Assuming that $Q_1 = Q_2$ then $g_{m1} = g_{m2} = g_m$

$r_{be1} = r_{be2} = r_{be} = \beta/g_m$

$V_{be1} = V_{be2} = V_d/2$

So $V_o = [g_m R_c]V_d/2$

$A_{vd} = V_o/V_d = [g_m/2]R_c$ (i.e. half the voltage gain of a CE amp)

where $g_m = [I_o/V_T]/2$

$A_{vd} = [I_o.R_c]/[4.V_T]$ This is the same as the result obtained earlier.

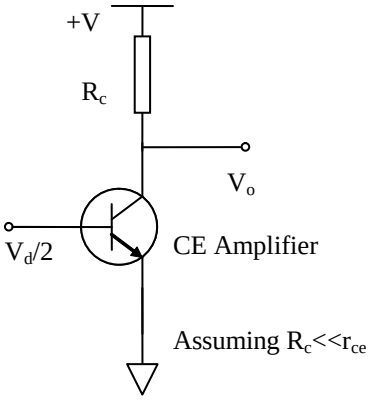
Alternatively, we can look at the amplifier as a series connected pair of common-emitter stages with one being fed with a signal of $+V_d/2$, and the other with $-V_d/2$. Since the voltage gain of a single CE stage is

$A_v = g_m R_c = I_c R_c/V_T = [V_o/(V_d/2)]$

Hence, the gain of this LTP is given by:

$V_o/(V_d) = I_c R_c/(2V_T)$

$A_{vd} = [I_o.R_c]/[4.V_T]$ - the same result again!

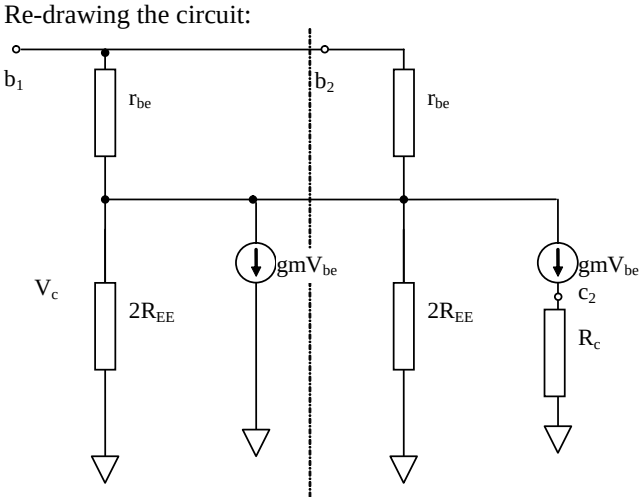


(What would the voltage gain be if R_c were an active load such as a current-mirror?)

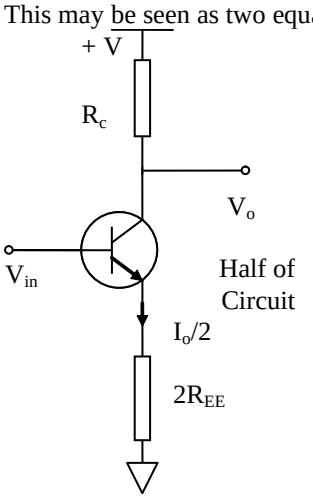
Common-mode gain, A_{VC}

Now suppose $V_{b1} = V_{b2} = V_c$, $V_d = 0$

But - V_{b1}, V_{b2}, and V_{ee} are not necessarily zero -
Re-drawing the circuit:



This may be seen as two equal paralleled halves!



$V_o = -g_m R_c V_{be}$

$V_{in} = [(g_m V_{be} + V_{be}/r_{be})2R_{EE} + V_{be}]$

Substituting $r_{be} = \beta/g_m$

$V_{in} = V_{be}[(g_m(1+\beta)/\beta)2R_{EE} + 1]$

Since $(1+\beta)/\beta \approx 1$

Then $V_o/V_{in} = A_{vc} \approx -(g_m R_c)/(g_m 2R_{EE}+1)$

This is the common-mode gain of the amplifier.

Since it is typically the case that $g_m R_{EE} >> 1$, this expression can be further simplied to

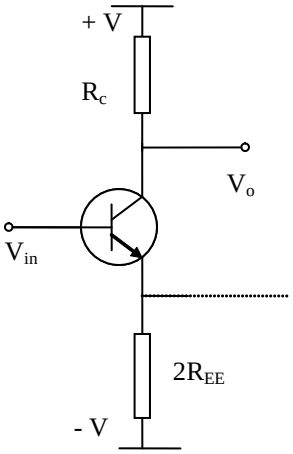
$A_{vc} \approx -[R_c/2R_{EE}]$

Clearly to obtain a high value of common-mode rejection ratio (ideally infinite) we should use a very good high impedance current-sink instead of a simple resistor R_{EE}.

Note

1. CMMR $\underline{\Delta}|A_{vd}/A_{vc}| = (I_o/2V_T).R_{EE}$ Ideally, CMMR = ∞
2. It is not feasible simply to increase the value of resistor R_{EE} to obtain a larger CMMR, since this would involve increasing the power supply to maintain the same value of I_o to maintain A_{vd}. Alternatively, we could replace R_{EE} with a ...?

An alternative is to view the amplifier wrt common-mode voltages as being two CE stages, each with emitter degeneration, in parallel. Since the gain is approximately $A_{vc} = -R_c/2R_{EE}$, no complex analysis is required.



CMMR - Common-mode rejection Ratio

Consider a simple BJT differential amplifier with a tail current of I_o = 2 mA, a collector resistance of 5kΩ and a tail current source with an impedance of 50kΩ. In this case

$Av_c = -5000/(2\times50{,}000) = -0.05$

This gives a CMMR of $A_{vd}/A_{vc} = 100/0.05 = 2000$,
Or, straight from the equation:
$CMMR = (50\times10^3)\times(2\times10^{-3})/(2\times25\times10^{-3}) = 2000$

The significance of CMMR can best be seen by example:

Example

Suppose the signal to be amplified is a voltage difference of 20mV, and the common-mode signal is 100 mV (say, noise).
Then signal/noise at input ≈ 0.2.
Since $Av_d = 100$ then $V_{od} = 2V$
$Av_c = -0.05$ then $V_{oc} = 0.005V$
So the output signal/noise is 2/0.005 = 400
Substantial improvement of S/N at output is due to high CMMR
i.e. $(S/N)_o = (S/N)_{in}$ x