國立清華大學

碩士論文

積體化電路設計之矽基體奈米線

An Integrated Circuit Design

for Silicon-Nanowire

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Abstract

Poly-silicon nanowire (SiNW) is a well-studied and interesting one-dimensional nanostructure. Since it was introduced to the biosensor field in 2001, it has become a promising candidate for ultra-sensitive, real-time and label-free sensor device. Nevertheless, many physical and chemical challenges constrain nanowire from being robust and practical. Nowadays, many studies adopt the integrated-circuit techniques to solve the problems. Circuits with different design concepts and purposes are proposed to meet practical needs.

In this thesis, based on the nanowire designed by Prof.Yang (National Chiao Tong University), we design our own read-out circuit. This research first analyzes biological experiments results (From Prof.Yang) and the electrical characteristics of the nanowires. The circuit specification and design is then based on these data analysis.

The circuit is capable of performing both DC-sweep (I_D-V_G sweep) and transient measurement. Moreover, we proposed a measurement method a combining of these two functions. We believe this method mitigates the device variability induced by the fabrication process. Currently, most operations in this method are manual. We hope to make them automatic in the future by inducing digital circuits and constructing a system-level structure.

致謝

感謝指導教授陳新老師提供一個新奇的題目，並在過程中給予許多有用的建議，在寫作與修改論文的過程中更感謝老師多番勞心勞力。感謝交大楊裕雄老師以及林志恆學長所提供的元件和數據，以及各種實驗上的幫助，使元件量測能夠順利進行。感謝所有 NEL，讓三年的研究所生活過的相當歡樂。感謝 LC，兩年多來陪我一同跨過各種困難和阻礙。最後感謝所有此論文的讀者，感謝你們的耐心與各種建議。

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Chapter 1

Circuit Results Discussion and Summary

This chapter presents the results of our read-out circuit and the summary of this thesis.

1.1 The Fronted Circuit and DC-sweep mode

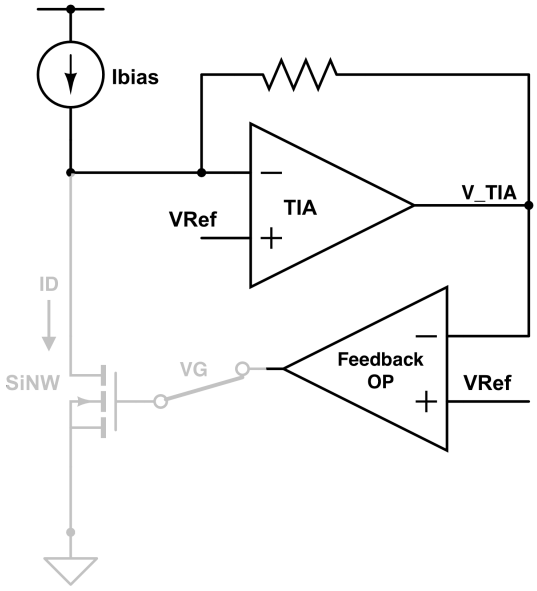


Figure 1.1: The fronted circuit

As in Fig.1.1(a), the fronted circuit includes a biasing current source (Ibias), tran-

simpedance amplifier (TIA) and an operational amplifier (OP). These three circuit blocks combined with the nanowire device (SiNW) form a feedback structure, which is DC-sweep mode of our circuit.

1.1.1 Ibias

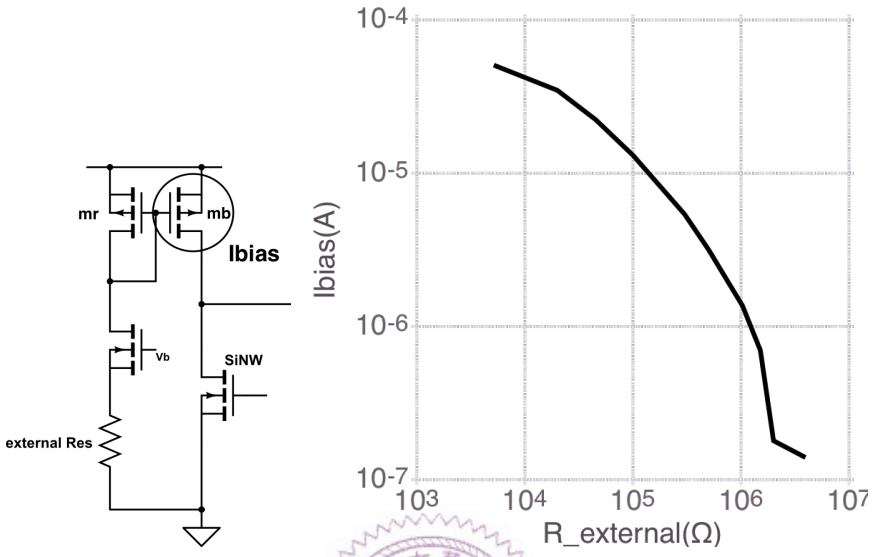


Figure 1.2: (a) The Ibias circuit. **(b)** The relation between biasing current (I_{bias}) and resistance of the external resistor.

The Fig.**??**(a) is the schematic of the Ibias circuit. The relation between the resistance of the external resistor and the biasing current is shown in Fig.1.2(b). The Ibias circuit is able to provide a biasing current from $100nA$ to $50\mu A$ stably. It should be noted that this biasing current range binds the operational range of DC-sweep mode circuit.

1.1.2 TIA

The Fig.1.3(a) and (c) show that the dynamic input current range of TIA is $+5.3\mu A \sim -15\mu A$. The Fig.1.3(b) and (d) are the respective derivative ($\frac{\partial V_{out}}{\partial I_{in}}$) As illustrated in these figures, the transimpedance of TIA is $103k$. It is notable that not all TIA on the chips have the same transimpedance. This is because the transimpedance value depends on the resistance of the resistor in TIA (Fig.1.1). This resistor is made of N-well, which should have the largest resistance-to-surface ratio among other kinds of

resistor. But since the doping concentration may vary with the fabrication process, such kind of resistor has a larger resistance variance (% 30). We have performed necessary simulations before tap out. It is assured that the variance does not disturb the important properties of whole read-out circuit such as stability and noise ratio.

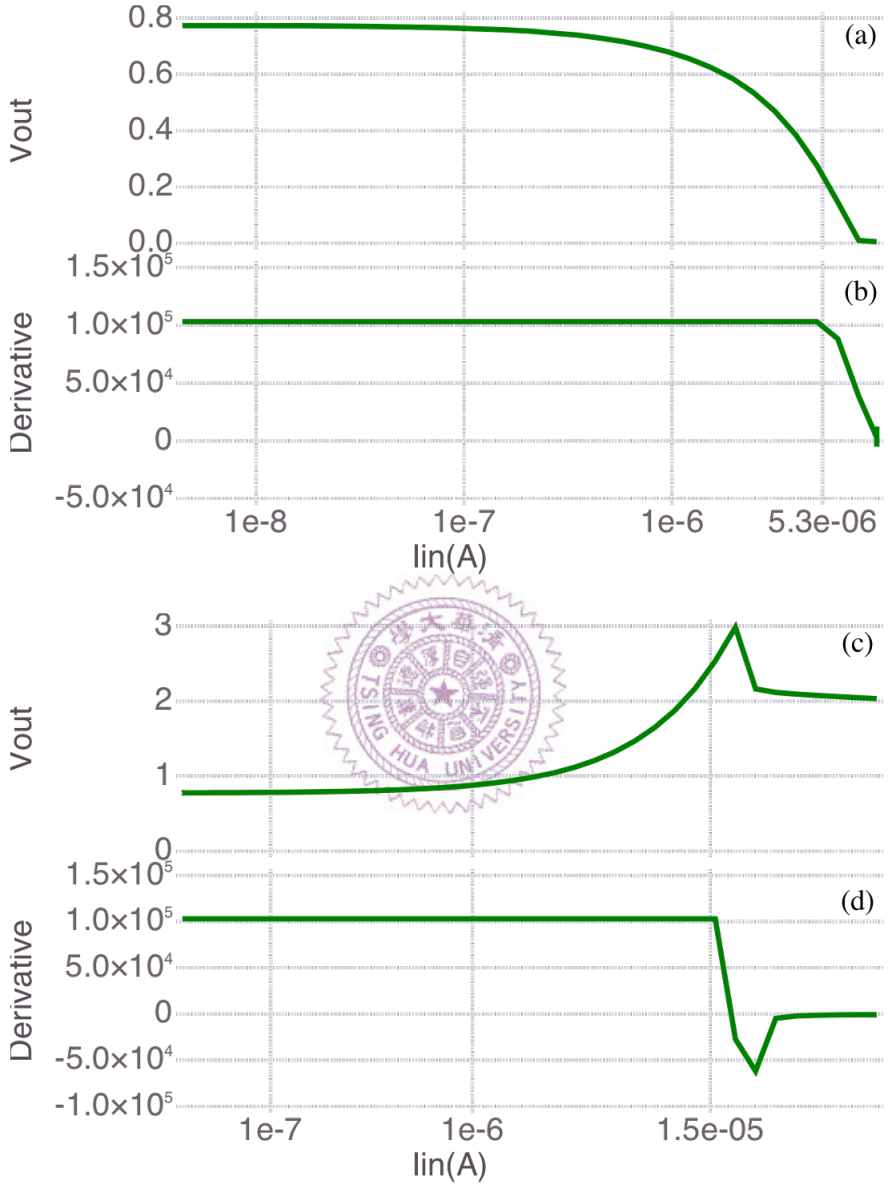


Figure 1.3: The dc simulation results of TIA. The x-axis represents positive/negative input current (log scale). **(a)** is the V_{out} responding to the positive input current while **(c)** is to the negative input current. **(b)** and **(d)** are the partial derivative of V_{out} with respect to input current ($\frac{\partial V_{out}}{\partial I_{in}}$) from (a) and (c) respectively.

1.1.3 OP

A sinusoidal signal is sent to the negative input of OP and the output signal is measured in Fig.1.4. It shows that the gain of the feedback OP is only about $1k$. However, the gain of OP was designed to be more than $5k$. We will discuss this problem in the following section.

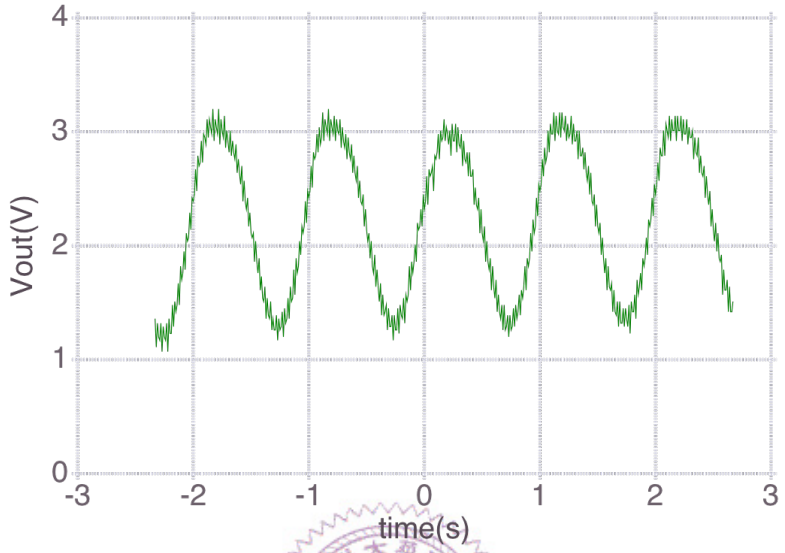


Figure 1.4: The output voltage of the feedback OP when the negative input is applied with a sinusoidal signal. This input sinusoidal signal has frequency of 1Hz and amplitude of $2mV$. The positive input of OP is biased with a constant voltage generated by the chip (VRef in Fig.1.5). The output signal has amplitude around $2V$, which means that the gain of OP is about $1k$.

1.1.4 Measurement with DC-sweep Mode Circuit and the Low-current Defect Problem

With DC-sweep mode (Fig.1.5), Ibias is swept and V_G and I_D are measured to obtain the I_D-V_G and I_{bias}-V_G curves (Fig.1.6). The chip works well when I_{bias} is larger than $1\mu A$. The overlap between two curves implies that I_D follows I_{bias} and V_G consequently alters owing to the feedback mechanism.

When current becomes low, the circuit fails to prompt nanowire to follow the biasing current. This phenomenon could be reasonable because lower I_D implies

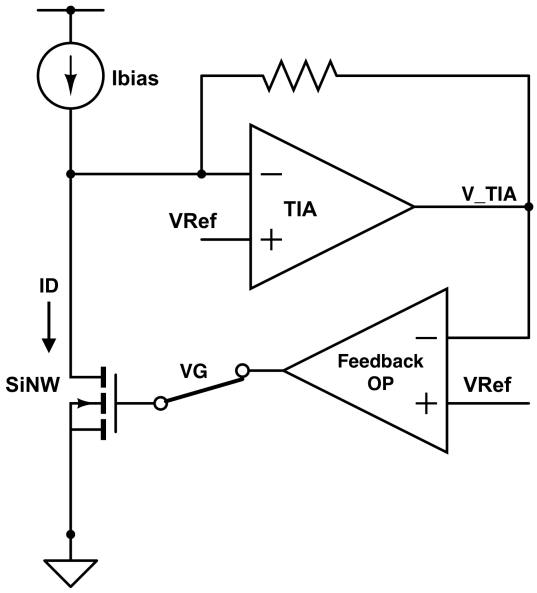


Figure 1.5: DC-sweep mode circuit

lower g_m and the feedback ability of the circuit may be not strong enough to push the gate of nanowire. However we expected this happens for g_m below $200n$. The Fig.1.7 indicates that the this happens when g_m is less than 5μ instead. We call this problem as low-current defect problem.

Insufficient Gain

We first suspected that it is caused by the insufficient gain of the feedback OP. According to the last section (Section.1.1.3), the gain is about $1k$. The discussion in Section.**??** suggests that the feedback mechanism depends on the loop gain. The loop gain should be larger than 100 for DC-sweep mode being functional. Based on Eq.(**??**) and Eq.(**??**), if A_{OP} is $1k$, the loop gain drops below 100 when g_m is less than 1μ. In other words, even though the gain of OP is 5 fold smaller than the gain we designed, the circuit should work well when g_m is larger than 1μ. But in fact, the circuit fails for gm below 5μ.

Input Offset Voltage

Another reason may be responsible for the low-current defect is the offset voltage at the input of the feedback OP.

The output voltage of TIA (V_{TIA}) of the DC-sweep experiment in Fig.1.6 is ex-

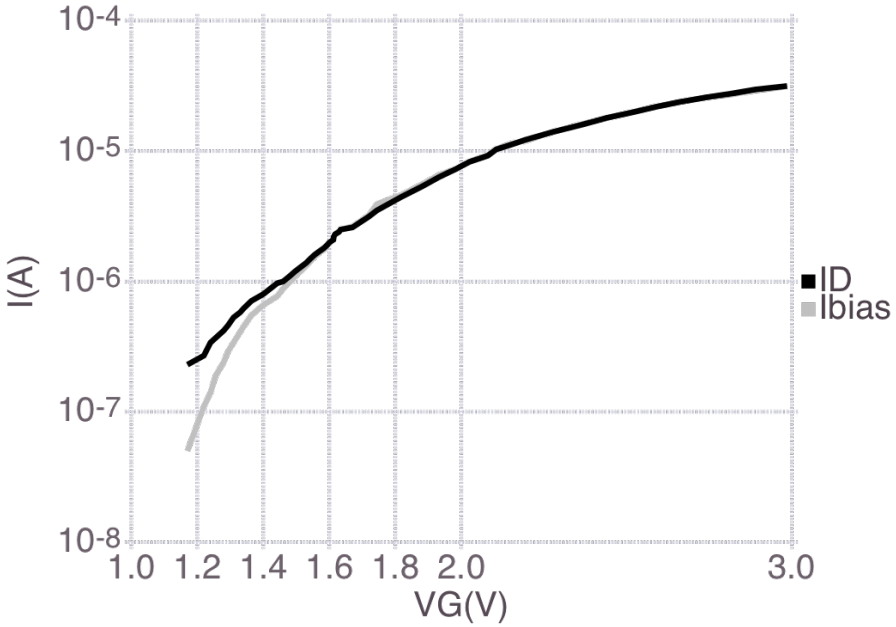


Figure 1.6: The measurement result of DC-sweep mode circuit. I_{bias} is the biasing current. I_D is the current flowing through the nanowire device. One can observe a separation between two curves in low current section ($< 1\mu A$).

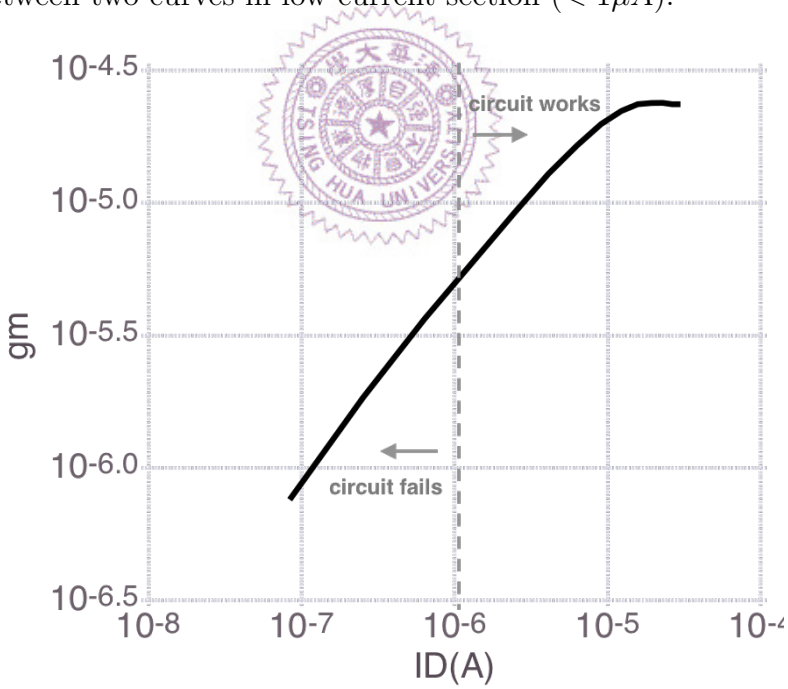


Figure 1.7: The g_m-I_D curve. It is obtained from the I_D-V_G curve in Fig.1.6. "Circuit fails" means the two curves in Fig.1.6 are separated where "circuit works" means they are overlapped.

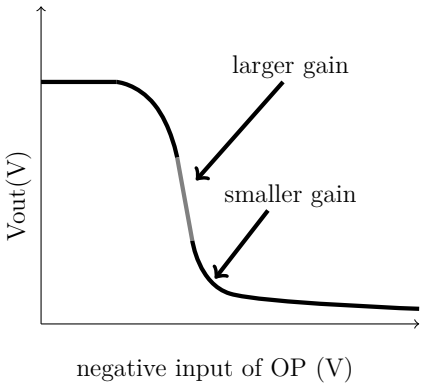


Figure 1.8: The illustration of the input-output response of the feedback OP.

amined and shown in Fig.1.9. Ideally, when feedback mechanism works well, V_{TIA} should be equal to V_{Ref}(Fig.1.5). However, the value of V_{Ref} is $0.802V$, which is smaller than V_{TIA}. (This V_{Ref} is connected to a constant voltage point inside the chip. its value is known indirectly by measuring the drain voltage of nanowire since the drain of nanowire is kept to be same as V_{Ref} by TIA.) When the circuit works well, V_{TIA} and V_{Ref} is still different by $15mV$. This voltage difference can result in a $150nA$ offset current flowing through TIA and into the nanowire device. This offset current becomes remarkable when the I_{bias} becomes small.

We suggest the reason that V_{TIA} is large than V_{Ref} is due to the offset voltage appearing at the input of the feedback OP. This speculation is reasonable with respect to the layout, which will be discussed in the next section.

Overall, the insufficient gain and the input offset may be the main reasons of the low-current defect. Both of them relate to the feedback OP. We then discuss these two reasons from the perspective of layout in the following section.

1.1.5 The Layout Problems of OP

The last section mentioned that the gain of OP is lower than we expected and there may exist an input offset voltage. In this section, we will deduce that several layout flaws may be responsible for these two problems.

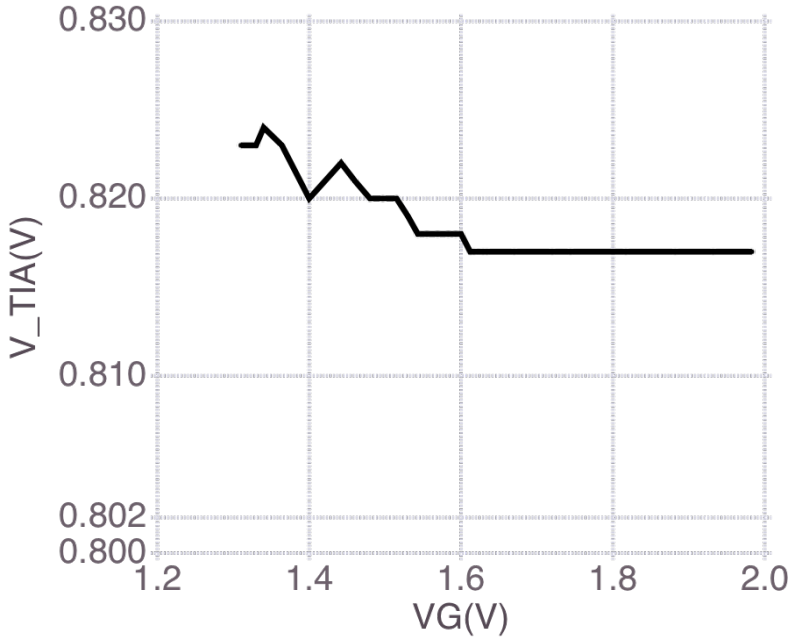


Figure 1.9: The V_{TIA}. The x-axis is the corresponding gate voltage. With the information from Fig.1.6, we found that the V_{TIA} is not equal to V_{Ref} no matter feedback mechanism works well or not.

1.1.5.1 The Possible Reasons for Insufficient Gain

The schematic presented in Fig.1.10 contains two sections. The left section is the body of the feedback OP and the local biasing circuit while the right one is a global biasing circuit. The global biasing circuit generated V_{bi} and V_{Ref}, which bias two pmos (M3, M4) and two nmos (M5, M6) respectively.

One layout flaw is that the M3 $\sim$ M6 are all single transistor. They are placed alone on the chip (Fig.1.11) without any protection. In consequence their size and doping concentration are more vulnerable to the process variation than other transistors. Another layout flaw is that the global biasing circuit is placed far from the OP circuit. The extent of the process variation from which the OP circuit and global biasing circuit suffer may be different.

Take an example, when process variation happens in global biasing circuit, V_{bi} and V_{Ref} change respectively. Ideally, the effect of these two changes on the gain of OP are countervailing. But this may not be true if M4 and M6 suffer another process variation. The changes on V_{bi} and V_{Ref} may affect M4 and M6 in different extent.

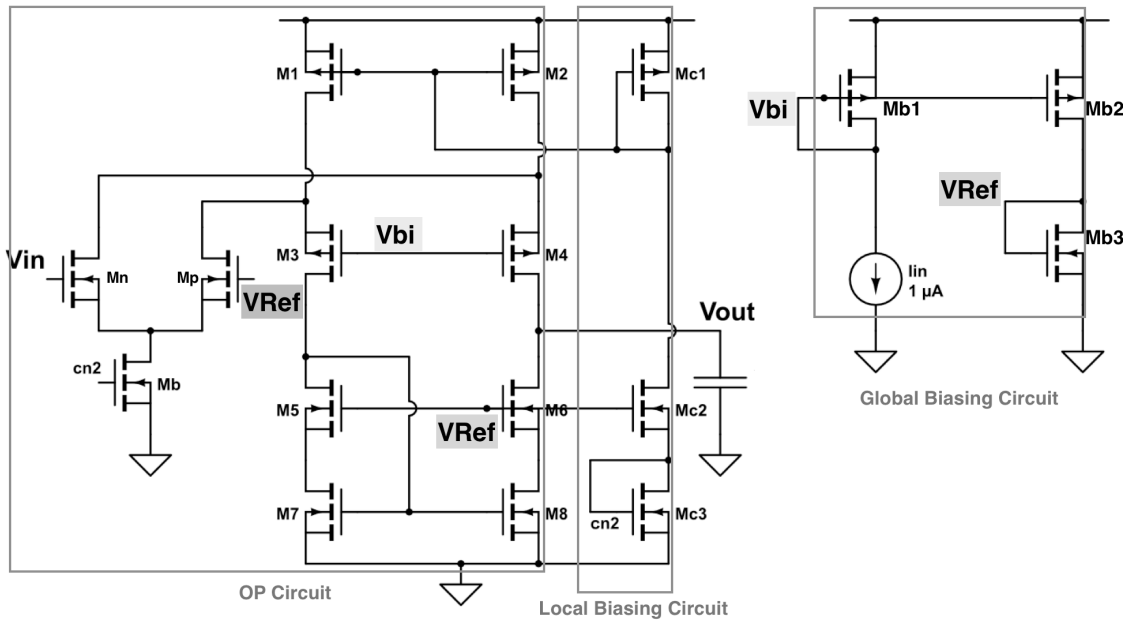


Figure 1.10: The left section is the schematic of the feedback OP including the local biasing circuit and OP circuit. The right section is the global biasing circuit for generating two global biasing voltages: V_{bi}, V_{Ref}. The Iin is an external current source.

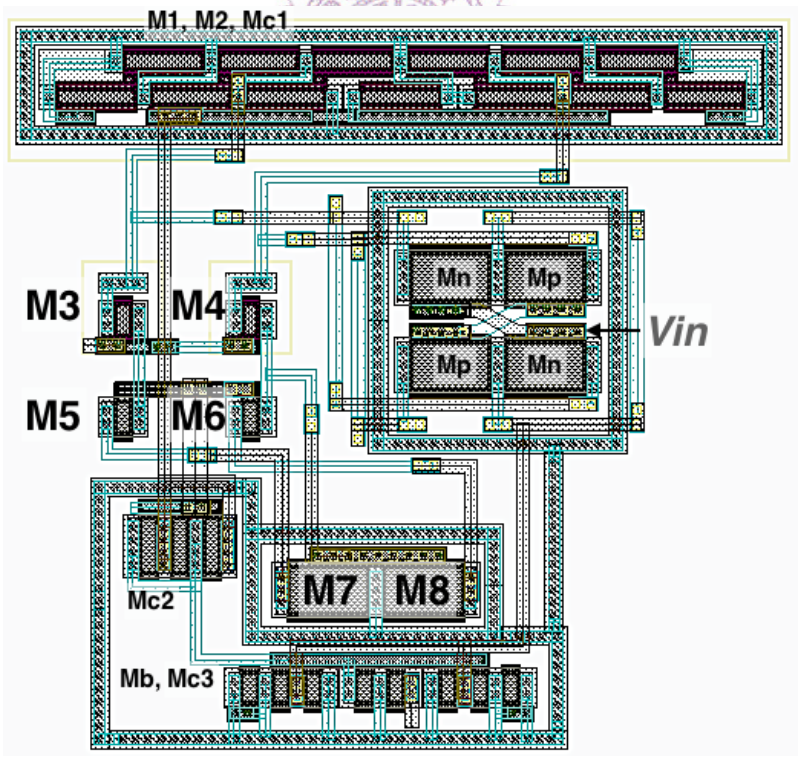


Figure 1.11: The layout of the feedback OP including the local biasing circuit.

Moreover, the high output impedance of OP amplifies this difference and as a result of the gain distortion.

1.1.5.2 The Possible Reasons for Input Offset

The input offset can be related to the size mismatch between M7 and M8 (Fig.1.11). The transistors were designed to be same. But there is no dummy gate or matching technique applied to the transistors. Therefore, the size mismatch may prone to happen on M7 and M8. In our case, the offset voltage is negative ($V_{\text{negative input}} > V_{\text{positive input}}$). If the size mismatch is responsible for it, the size of M8 should be relatively smaller than M7.

1.1.5.3 Improvement Methodology

Although all problems mentioned above relate to the layout, we do not think that simply revising the layout is a reliable solution. The feedback OP is an open-loop circuit with high output impedance. Its characteristics (such as gain and bandwidth) are hard to be control accurately considering the process variations. A better solution is to replace it with other amplifier. Since this OP serves as a high-gain and low bandwidth block, it can be substitued with a close-loop amplifier and low pass filter.

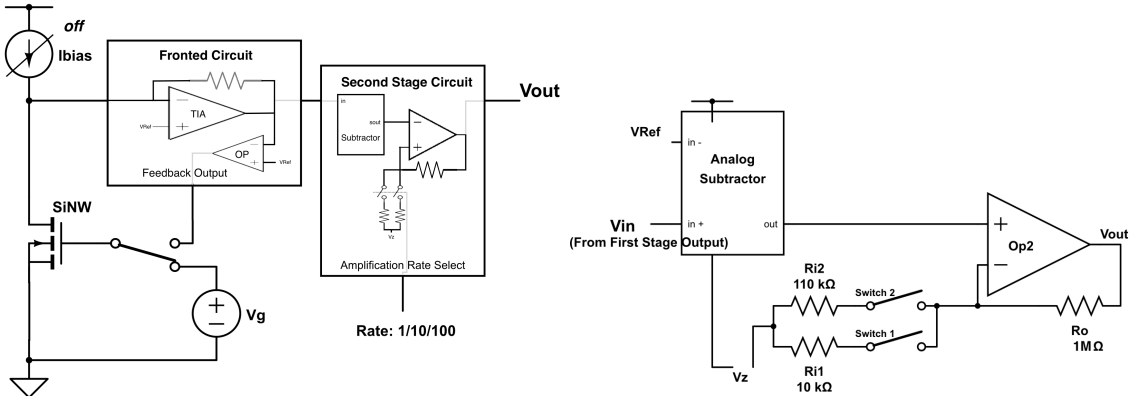
1.1.5.4 Summary of DC-sweep mode

The table that compares the chip properties and the specification for DC-sweep mode is given below (Table.1.1). The chip does not meet the specification due to the low-current defect problem.

	Design Spec.	Chip Properties
I_D	$100nA$ - $30\mu A$	$1\mu A$ - $50\mu A$
g_m	$200nA$ - $20\mu A$	3μ - $20\mu A$
V_G	$0.5V$ - $3V$	$0.45V$ - $3V$

Table 1.1: The comparison between the chip properties and the specification for DC-sweep mode from chapter 3.

1.2 The Second Stage Circuit and Transient Measurement Mode



(a) (b)

Figure 1.12: **(a)** The block diagram of Transient Measurement circuit. **(b)** The schematic of the second stage circuit.

As in Fig.1.12, Transient Measurement mode includes the second stage circuit and the Ibias and TIA from the fronted circuit. An analog subtractor and a resistor-based amplifier are included in the second stage circuit. The input signal can be sent from the gate or the source of nanowire (SiNW).

1.2.1 The Second Stage Circuit

This section presents the important properties of the second stage circuit. To be notable that the performance of the subtractor and amplifier cannot be measured independently because there is no external pad connected to the output of the subtractor. Besides, second stage input is always connected with the output of TIA. Due to the low output impedance of the TIA, it is hard to send input signal into the second stage circuit directly. Fig.1.13 is the alternative approach. The resistor Rs and the TIA compose a voltage amplifier. The input signal, which is usually triangular or sinusoidal, is injected through the Rs. It is then modulated in proportional to the ratio of Rs and TIA before being sent into the second stage

circuit.

$$\text{Input of the } 2^{nd} \text{ stage circuit} = V_s \times \frac{\text{transimpedance of TIA}}{R_s} \tag{1.1}$$

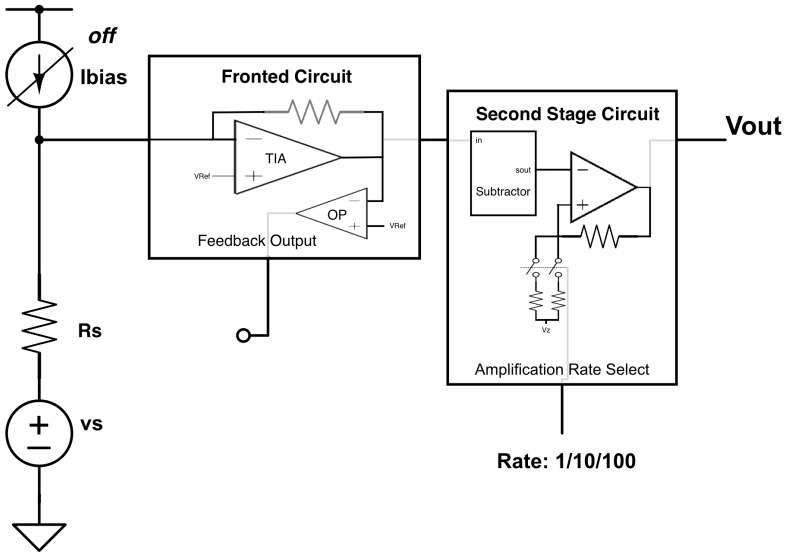


Figure 1.13: The second stage circuit measurement approach.

1.2.1.1 The Noise Oscillation Problem in Amplifier with Amplification Rate of 1

The amplifier in the second stage circuit has three amplification rate (A_{amp}): 1, 10 and 100. The amplifier works well as the A_{amp} is 10 and 100. However, when A_{amp} is 1, the output signal is flooded with noise. In Fig.1.14, the input is a 1Hz triangle signal. Ideally, the second stage output should be a similar triangle signal. But in fact the signal is flooded with noise.

We suggest that the oscillation of noise signal should be the main cause of the problem. When designing the amplifier, we did not consider the parasitic capacitance brought by the switches and the pad (with ESD circuit) at the output. The simulation below proves our suggestion. The parasitic capacitance is modeled by a $5pF$ capacitor. Fig.1.15(a) and (b) are the phase margin test of the amplifier before and after the capacitor is loaded on the output. The figures indicate that the second dominant pole locates at the output and the parasitic capacitors push it to the left. The phase margin is decreased subsequently.

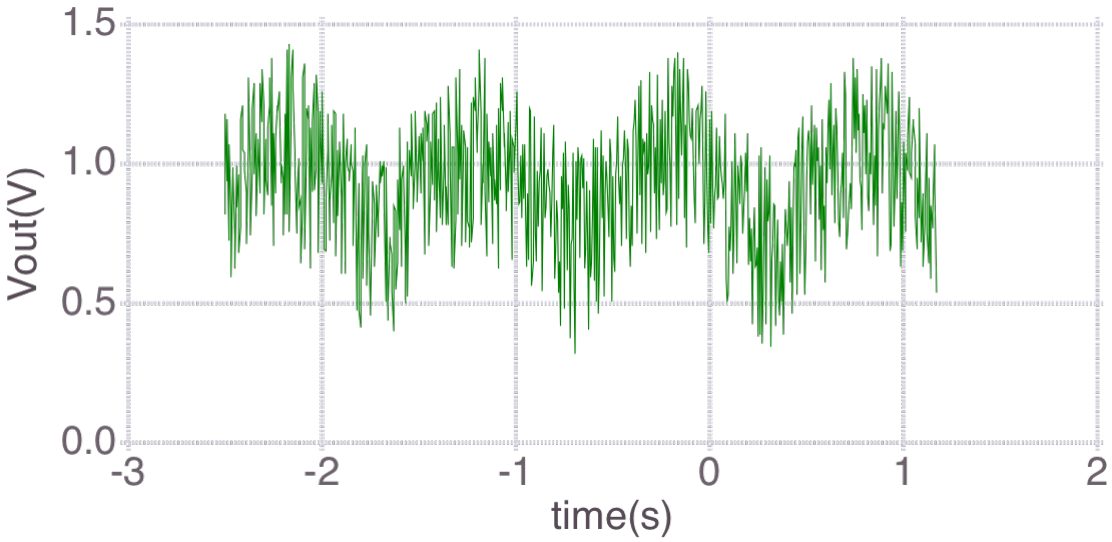


Figure 1.14: The noise ocsillation problem

The reason that the noise oscillation problem only happens when A_{amp} is 1 is because of the feedback mechanism. When A_{amp} is 1, the structure is similar to an unit-gain buffer (Fig.1.12(b)). In Fig.1.16, (a) is the feedback network of this structure while (c) is of the amplifier with A_{amp} is 10 and 100. To compute the loop gain, the structure is broken at the negative input and a tested signal is injected (Vt) as illustrated in Fig.1.16 (b), (d). The loop gain ($\frac{V_f}{Vt}$) of the two structure is derived as:

$$\text{when } A_{amp} = 1: \qquad \frac{V_f}{Vt} = A_{op} \tag{1.2}$$

$$\text{when } A_{amp} = 10 \text{ or } 100: \qquad \frac{V_f}{Vt} = A_{op} \times \frac{R_i}{R_i + R_o} \tag{1.3}$$

A_{op} is the gain of the OP in the amplifier. (A_{op} is similar in two cases even if the loading effect is taken into consideration becasue $R_O >> R_i$.) Since the R_O is at least larger than R_i by 10-fold, two loop gains are different by 10-fold as well. The smaller loop gain increases the phase margin of amplifier by about 45 degree and diminish the oscillation (Fig.1.17).

We tried to dealt with the noise oscillation problem by the signal average technique. The output signal is averaged out to remove the noise component. However, the average of the signal may lie on the wrong offset. Therefore, the amplifier with $A_{amp} = 1$ is used only when the signal trend is of interest (such as the dynamic input

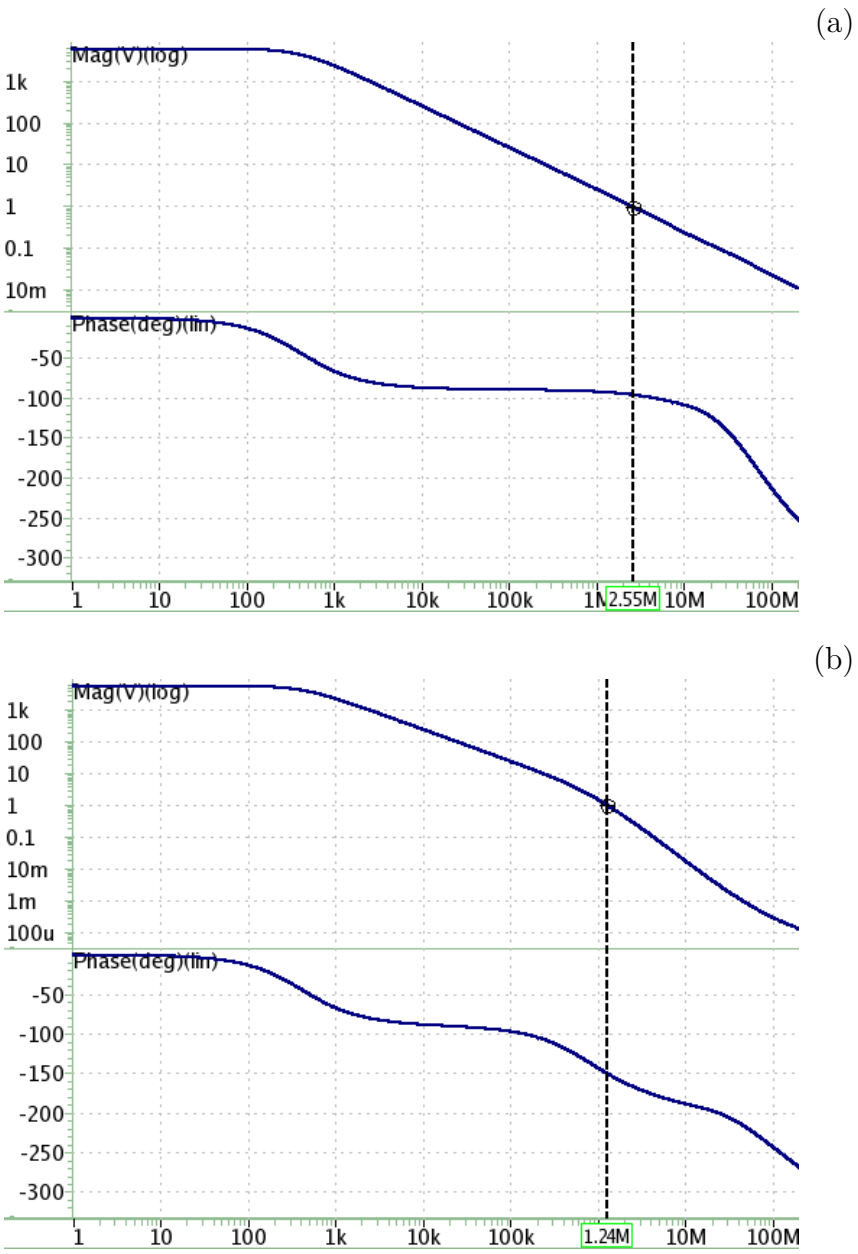


Figure 1.15: The post-simulation of the phase margin test of the amplifier when amplification rate is 1. **(a)** Without the parasitic capacitor, the phase margin is 108 degree. **(b)** With the parasitic capacitor (modeled by a $5pF$ capacitor), the phase margin becomes 30 degree.

range in Section.1.2.1.2). When the output signal is large and the amplification is not necessary, we simply measure the output of TIA.

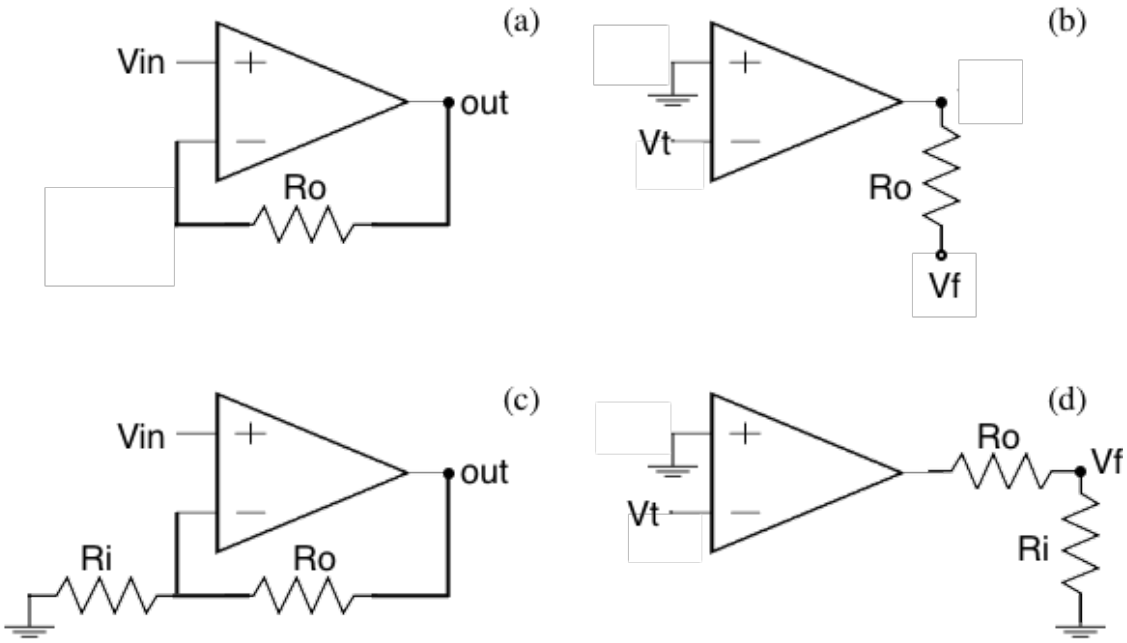


Figure 1.16: The feedback network and loop gain computation structure of the amplifier with **(a)**, **(b)** $A_{amp} = 1$ and **(c)**, **(d)** $A_{amp} = 10$ or 100.

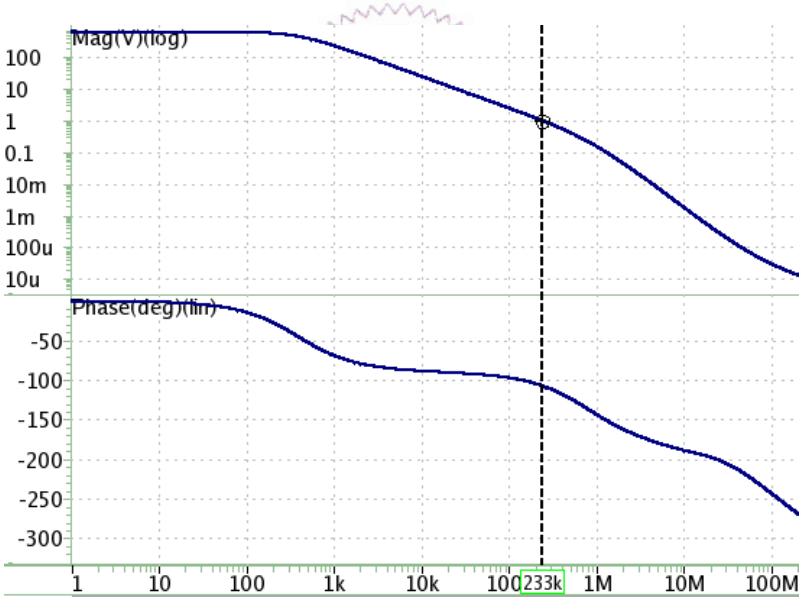


Figure 1.17: The post-simulation of the phase margin test of the amplifier when amplification rate is 10. With the parasitic capacitor loaded on the output(modeled by a $5pF$ capacitor), the phase margin is 73 degree

1.2.1.2 Dynamic Input Range

Fig.1.18 is the input-output response of the second stage circuit ($A_{amp} = 1$). It is used for finding the dynamic input range of the circuit. The linear region locates

at $Vin = 0.43V \sim 1.32V$. According to chapter 5, this range is determined by the subtractor block.

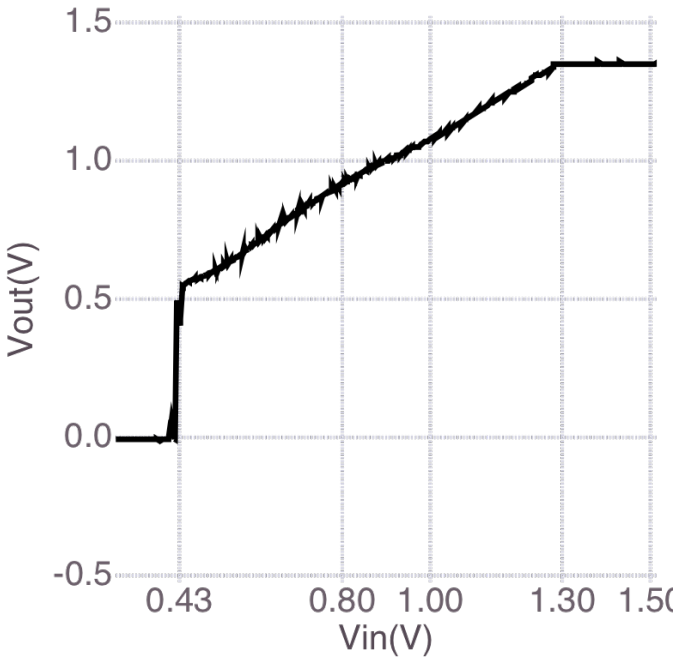


Figure 1.18: The input-output response of the second stage circuit ($A_{amp} = 1$).

Another input of the circuit is the Vz (Fig.1.12(b)). This voltage is for shifting the offset voltage. Its dynamic input range is measured and presented in Fig.1.19, which ranges from $0.62V$ to $1.47V$. To be notable that ideally the input Vz should be equal to the output. But in fact an offset voltage of $0.15V$ occurs in Fig.1.12 due to the noise oscillation problem mentioned in the last section. This offset does not exist when the A_{amp} is 10 and 100.

1.2.1.3 The Circuit Gain

A triangle wave is sent to the end of Rs (Fig.1.13) and the input and output of the second stage circuit are recorded by an oscillation scope. Fig.1.20) (a), (b) and (c) are the time domain results when the A_{amp} is 1, 10 and 100 respectively. The exact gain values are summarized in the Table.1.2.

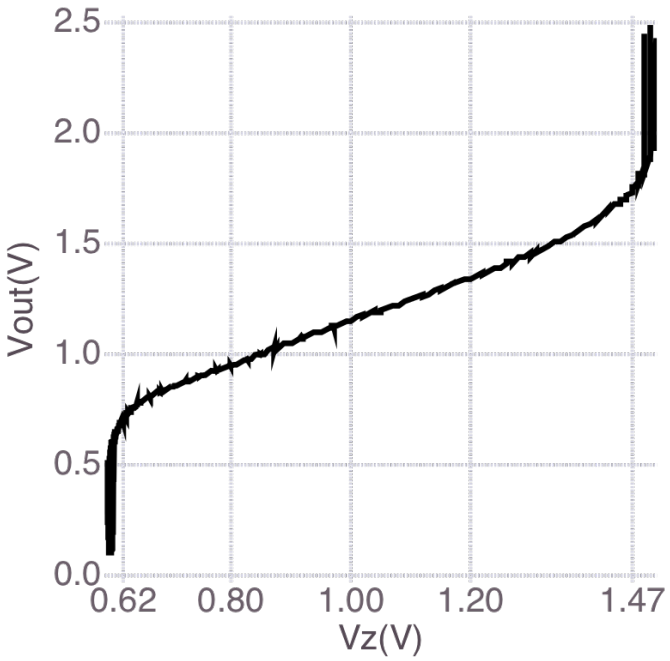


Figure 1.19: The input-output response of the second stage circuit. The input is Vz, which decides the output offset of the circuit.

Designed Amplification Rate	100	10	1
Measured Amplification Rate	93.3	9.2	1
Error Rate	7.7 %	8 %	0

Table 1.2: Comparison between the desgined and measured gain of the second srage circuit.

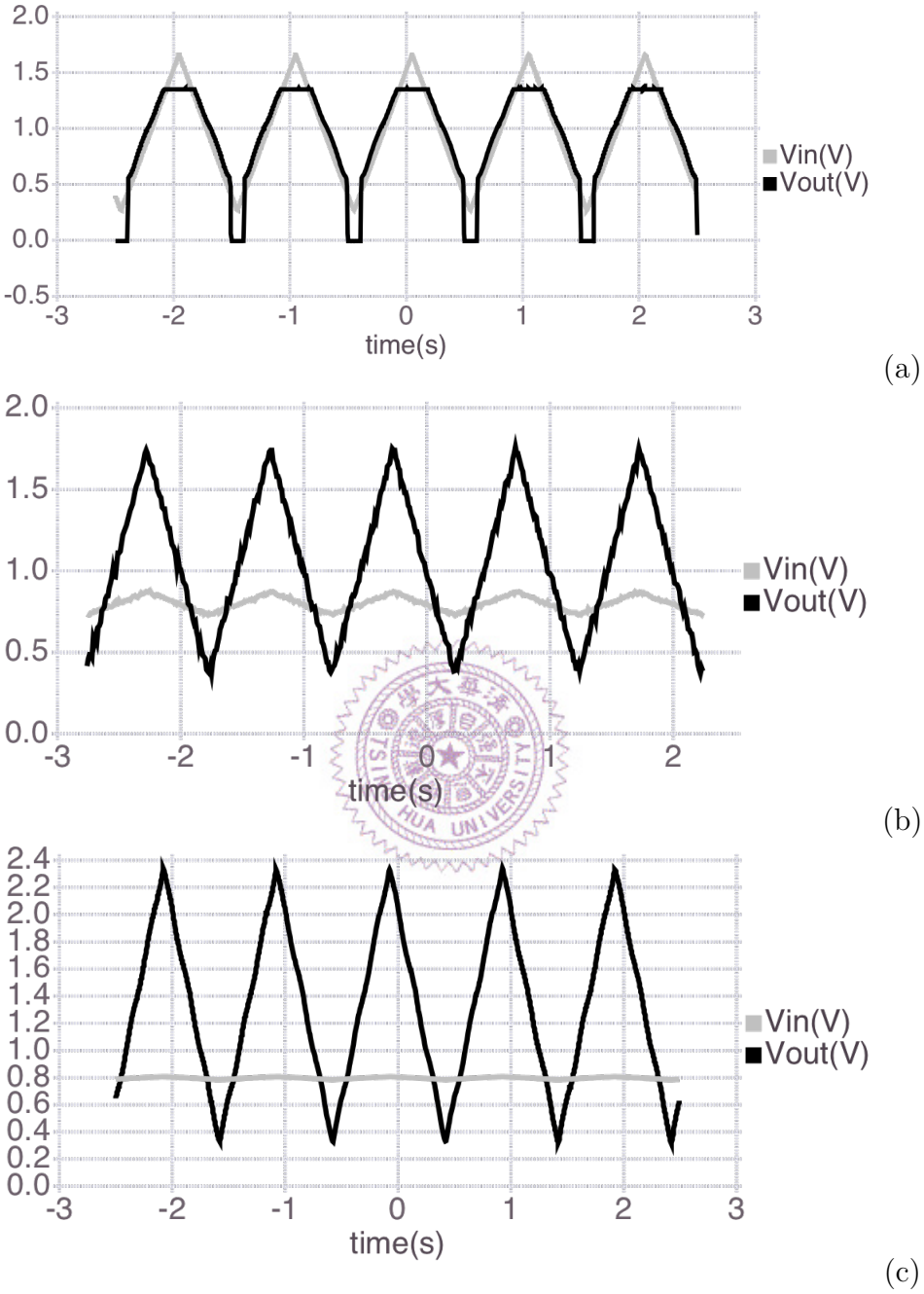


Figure 1.20: The input output signal of the second stage circuit in time domain when A_{amp} is **(a)** 1, **(b)** 10 and **(c)** 100.

1.2.2 Transient Measurement Mode

The second stage circuit and the TIA from the fronted circuit compose the circuit of Transient Measurement Mode. This section presents some of its important properties (gain, noise and bandwidth).

1.2.2.1 Bandwidth and Gain

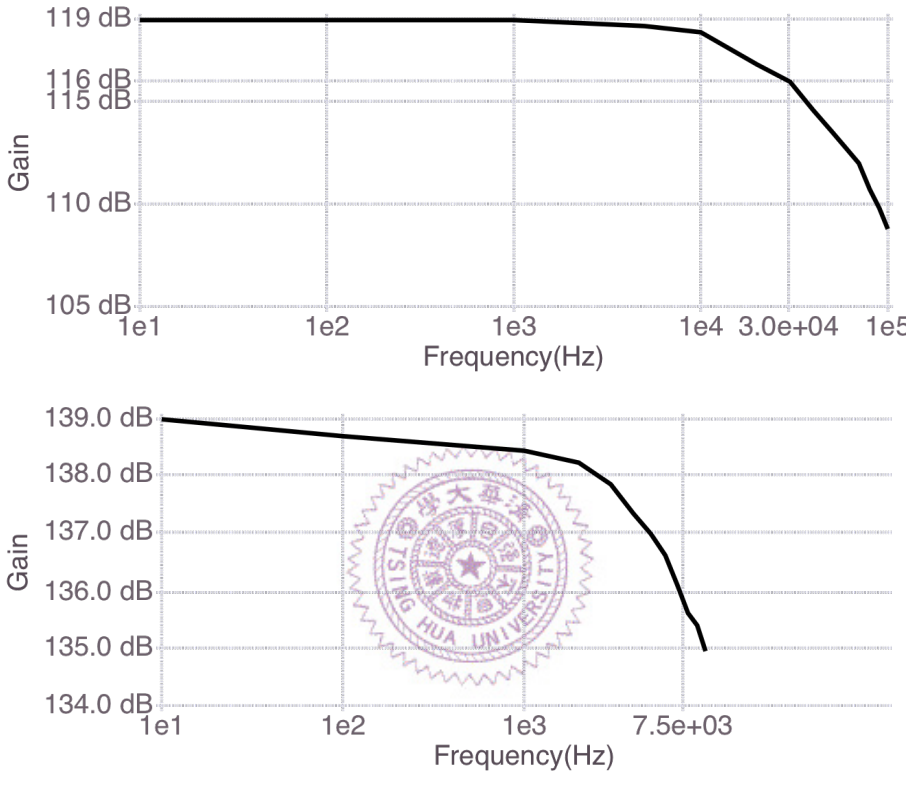


Figure 1.21: The gain and bandwidth of Transient Measurement circuit. The A_{amp} is 10 in **(a)** and 100 in **(b)**.

The gain is the input current to output voltage ratio. Because the noise oscillation problem may disturb the bandwidth measurement, we did not measure the circuit with A_{amp} of 1. The circuit with A_{amp} of 10 has gain of $891k$ and -3dB bandwidth of $30k$Hz. The circuit with A_{amp} of 100 has gain of $8.9M$ and -3dB bandwidth of $7.5k$Hz.

1.2.2.2 Input Referred Noise

The spectrum analyzer are used to measure the noise. The power spectral density (PSD) of noise at the output of the circuit is measured and is referred to the input to show the equivalent input current noise (Fig.1.22). Due to the equipment setting, the noise measring between 10Hz and While measurement is performing, Ibias provides $10\mu A$, which is same to the condition of the post-simulation measurement (Fig.**??**). The primary type of noise are the low frequency noise (flicker noise). Other types of noise such as 60Hz come from the environment and working machines. They may be lowered by adopting better method of experiment or equipments. Overall, the amount of noise is tolerable. The input current noise is $0.3nA$ at 1 Hz. The spec. from chapter 3 allows for a maximal input current noise of $2nA$.

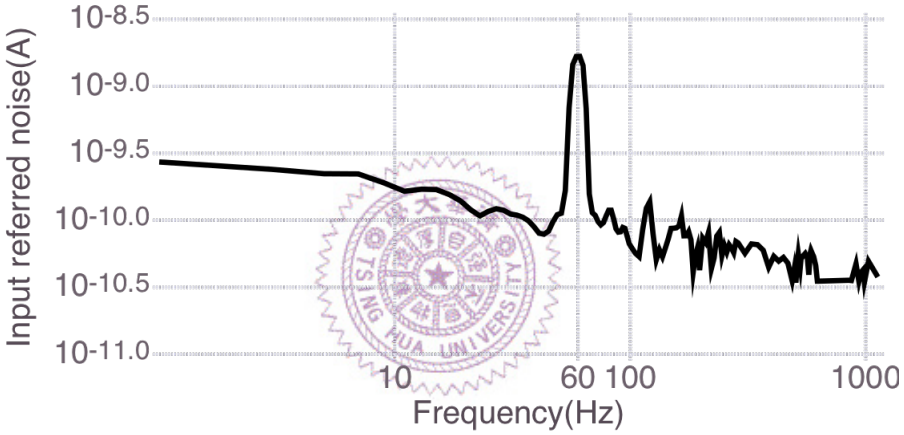


Figure 1.22: Input referred noise of Transient Measurement circuit.

1.2.2.3 Modulating biomolecule signals from the source terminal

The second usage of Transient Measurement mode is to apply a sinusoidal signal at the source of nanowire. In Fig.1.23, is obtained by this measurement method. The input is a sinusoidal signal with frequency of 500Hz and the amplitude of $0.5V$. The nanowire was put under two solutions with different pH values in (a) and (b). After dividing the amplitude of the output signal by the transimpedance gain of the circuit (891k), we learned that the g_m of nanowire under these two pH solutions are 1μ and 1.8μ.

This method aims to modulate the biomolecule signal into higher frequency to avoid the flicker noise and other kinds of low frequency noise. However, from the result below, it can be observed that the output contains large amount of high frequency noise. We believe the noise comes from the testing solution and through the gate of nanowire. In the future, a bandpass filter with adjustable center frequency should be added to the circuit to filter the signal of the unwanted frequency.

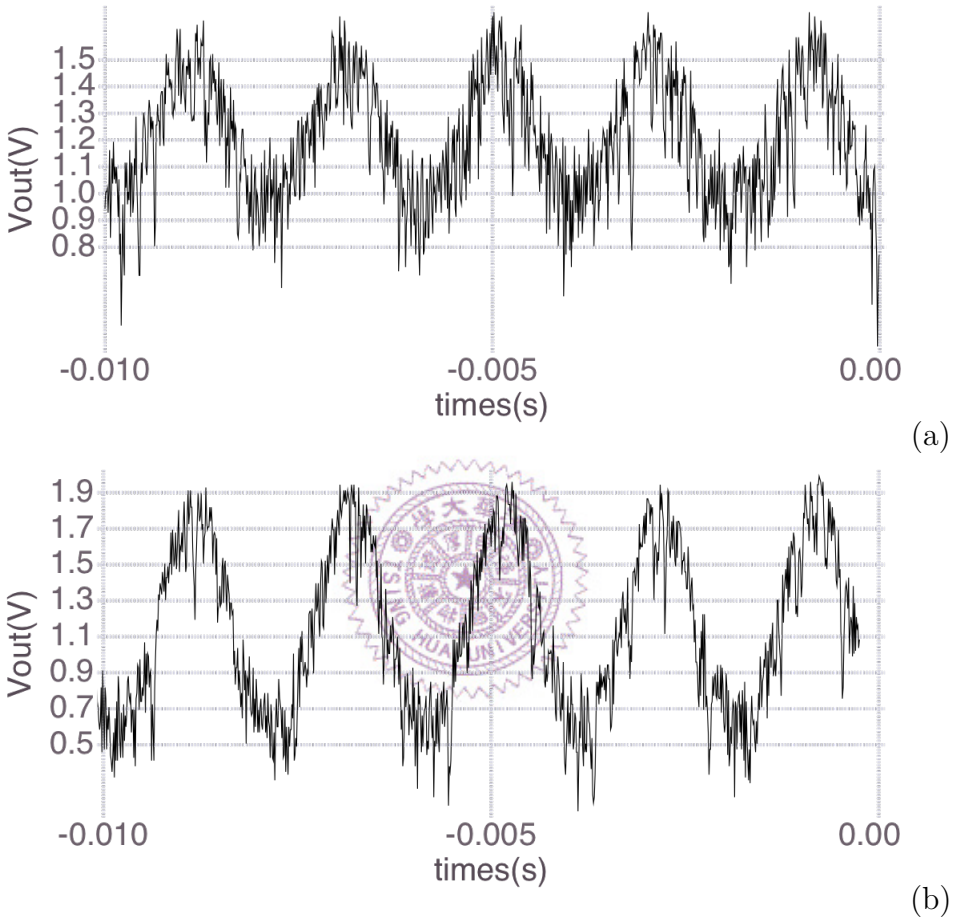


Figure 1.23: The output signal of the measurement using source of nanowire as input. The *gm* of nanowire in two figures are different by using testing solution with different pH values. The *gm* of nanowire is 1μ in **(a)** and 1.8μ in **(b)**.

1.2.2.4 Summary of Transient Measurement mode

The Table.1.3 compares the chip properties and the specification for transient measurement mode. Although there is the noise oscillation problem, the performance of the circuit is fine.

	Design Spec.	Chip Properties
IBias Current (I_D)	$600nA$ - $5\mu A$	$100nA$ - $50\mu A$
Dynamic Input Current Range(ΔI_D)	$\pm 20nA$ - $\pm 2.8\mu A$	$3nA \sim 5.3\mu A$ $-15\mu A \sim -3nA$
Input Referred Noise (A)	$< 2nA$	$< 0.3nA$ @ 1Hz
Transimpedance Gain (max)	$5M(\frac{V}{A})$	$8.9M(\frac{V}{A})$
Bandwidth	$> 1k$ (Hz)	$7.5kHz$

Table 1.3: The comparison between the chip properties and the specification for Transient Measurement mode from chapter 3.

1.3 Dealing with the Device Variability Problem

This section presents the measurement with the proposed variability-resisting method.

Two nanowire devices (nw1-2, nw2-1) lying on the same substrate are under test. The I_D-V_G curves of two devices are obtained and substantiate that they have device variability problem (Fig.1.24(a)). These curves are then transformed into gm-Id curves (Fig.1.24(b)). Based on the conclusion of appropriate operation region (Section.**??**), the gm of 2μ is selected. The certain I_D under which devices are biased are therefore determined. As illustrated in Fig.1.24(b), nw1-2 is biased under $340nA$ and nw2-1 is biased under $900nA$. The devices are connected with the circuit in Transient Measurement mode, where the bias current and gate voltage are set. Finally, the output response of two devices are presented in Fig.1.24(c) and (d). Two solutions with different pH values is used in substitution for the DNA solution. The pH value of solution A is lower than solution B. The lower pH value means the solution is more positive. Thus, solution B increase I_D and increases output voltage.

Two devices have similar output response, which suggest our method is functional. But still the responses are not exactly same. The voltage difference appears in the are different by 8% ($\frac{(|\Delta V_1 - \Delta V_2|)}{\Delta V_1}$). We can blame the inaccurate biasing current because DC-sweep mode circuit fails in low current and the V_G is manually adjusted to make the I_D follows the biasing current. Still there may be other reasons.

Although we keep the devices under a same gm, the output signals can diverge if

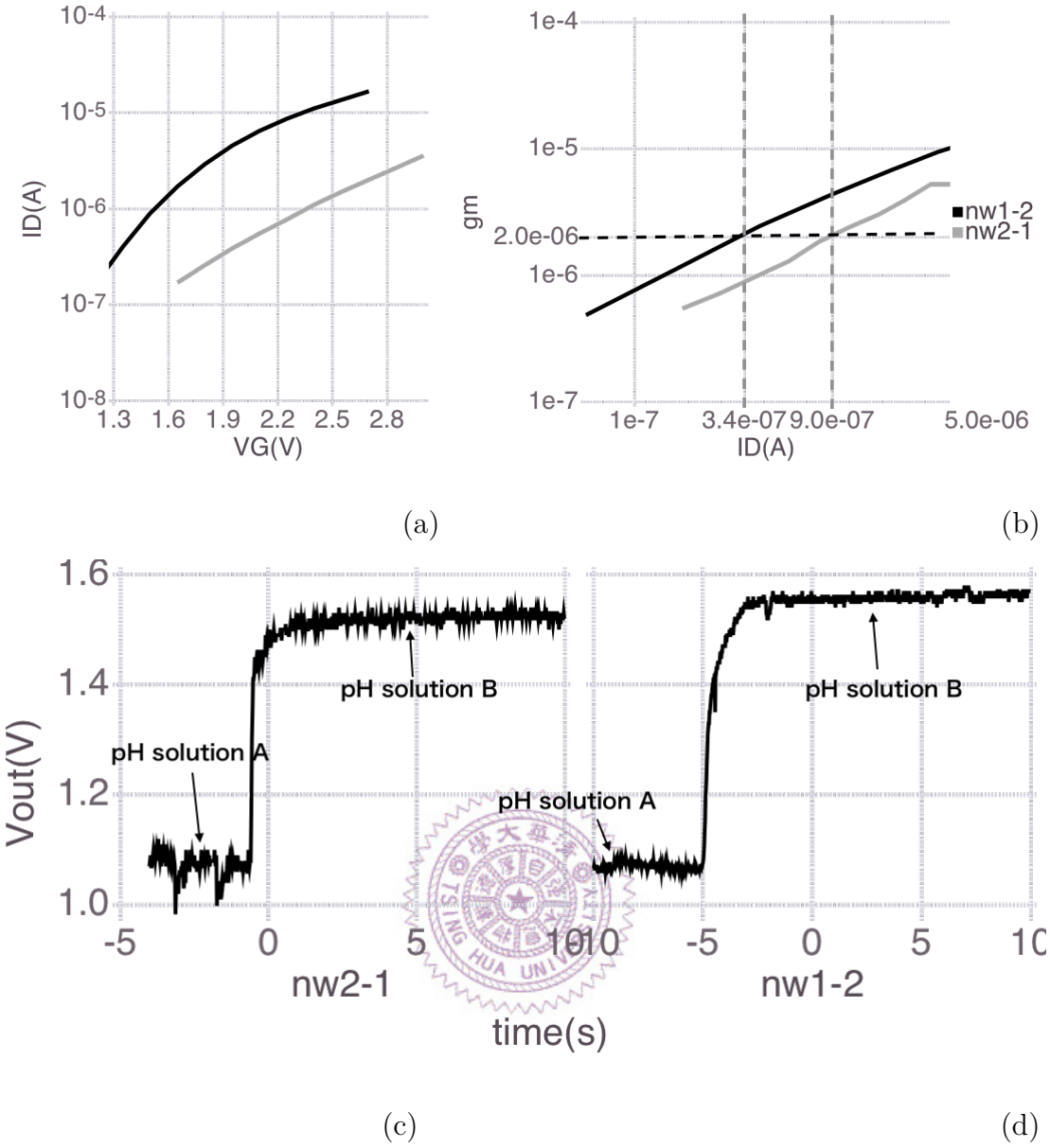


Figure 1.24: The variability-resisting method.

they receive incomparable input. The input of the experiment above is the equivalent voltage change induced by the concentration (pH value) difference (ΔV). Its value may be different because of two reasons. One is that the thickness of the each nanowire may not be same. There may be corrosion of the nanowire surface since the devices we use have been produced for more than 2 years and have bedd used repeatedly. The other is the gate coupling effect. The effect caused by the double layer capacitance varies with the gate voltage, which we have mentioned in Section.**??**.

The first reason can be solved by producing a new device. The second reason need the improvement on circuit structure. This reminds us one of the advantages of source follower structure (Section.**??**). The structure keeps V_G constant and adjusts the source voltage of nanowire instead. But changing source voltage will as well change the drain-to-source voltage (V_{DS}) of nanowire, which brings about the short channel effect. Therefore, in the future, if our circuit adopts the concept of source follower, the additional feedback network that keeps V_{DS} constant is required.

Overall, although our method does not entirely remove the device variability problem, it mitigates the problem. Furthermore, the improvement method is proposed and the progress can be looked forward.

1.4 Conclusion and Future Work

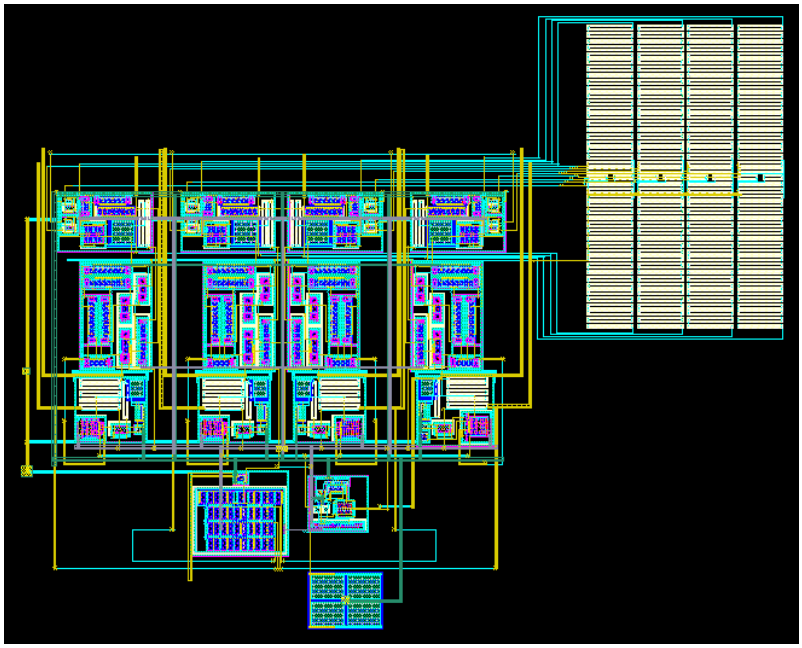


Figure 1.25: The layout of the Readout circuit

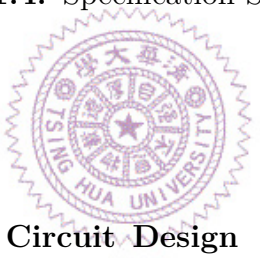
Fig.1.25 is the chip layout of the circuit. It contains four unit of the read-out circuits and is able to measure four nanowire devices at the same time.

In this project, a circuit with two mode: DC-sweep mode and Transient Measurement mode is designed. The first mode is to perform I_D-V_G sweep while the second mode is to perform transient measurement. By combining two mode, the cir-

cuit perform measurement by the variability-resisting method we proposed in this project. This method mitigate the device variability problem and can be further improve in the future. In Table.1.4, our circuit is compared with the methods that were reviewed in chapter 2 [1], [2]. Our circuit has wider ΔI detection range and lower power consumption when comparing with the similar work [2]. The work in [1] has better performance over all. Still our circuit deals with the device variability problem, which does not be mentioned in both works.

	[1]	[2]	This work
ΔI	$120\mu A \sim 0.12nA$	$3\mu A \sim 60nA$	$3nA \sim 5.3\mu A$ $-15\mu A \sim -3nA$
Power consumption	14.82uW	2mW	1.48mW
CMOS Technology	0.13um	0.18um	0.35um
Device Variability	No Discussion	No Discussion	Variability-resisting method

Table 1.4: Specification Summary



1.4.1 Future Work

1.4.1.0.1 Problems in the Circuit Design The low current defect in DC-sweep mode is the most important problem that must be solved. The solution for it is to replace the feedback OP with other closed-loop amplifier. Another problem is the noise oscillation problem that happens when the A_{amp} of the amplifier in the second-stage circuit is 1. This problem can be solved simply by fixing the insufficient phase margin.

1.4.1.0.2 Introduce Filter and Better Experimental Process The noise included in Transient Measurement mode could be removed by simply introduce a bandpass filter. The problem of this is that the signal speed is still hard to be defined. Besides, currently we use pipetman to change the concentration of solution. This process can evoke undesired noise and sometimes may not be carried on smoothly. Both of these factors destroy or affect the speed of the signal. If the process is

improved and the signal speed is decided, a filter can be introduced and the noise can be reduced.

Furthermore, for the measurement dealing with the device variability problem, a method to decide when to switch between DC-sweep and Transient Measurement mode is needed. This may be achieved by introducing digital circuit or by adding a feedback circuit for detecting whether the concentration changing reach a balance.

1.4.1.0.3 The ΔV Problem In Section.1.3, the method is functional but not perfect. We have discussed the improvement methods. They should help the further development of design and finally remove the device variability problem.

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[2] Jiawei Xu, Peter Offermans, Guy Meynants, Hien Duy Tong, Cees J. M. van Rijn, and Patrick Merken. A low-power readout circuit for nanowire based hydrogen sensor. *MICROELECTRONICS JOURNAL*, 41(11, SI):733–739, NOV 2010.