??

I_D

g_m

??

??

??

I_D

??

I_D

V_G

I_D

V_G

I_D

I_D

V_G

??

V_{out}

?

g_m

??

v_s

V_{out}

$v_s g_m \times$

R_{TIA}

$I_D V_G$

g_m

$g_m = $

$\frac{\partial I_D}{\partial V_G}$

g_m

V_{out}

g_m

V_G

I_D

I_D

g_m

??

R_{NW}

I_{NW}

(a)

?

R_{NW}

??

(b)

$I_{NW} = $

$(V_{Ref} - $

$V_{in})/R_{NW}$

$\Delta i = $

$\Delta vi/R_{NW}$

??

$$V_{TIA} = V_{Ref} + I_{NW} R_{TIA} + \Delta i R_{TIA}$$

(1)

I_{NW}

R_{TIA}

$Ref -$

$VSS \underset{R_{TIA} < I_{NW} < \frac{VDD - V_{Ref}}{R_{TIA}}}{}$

R_{TIA}

I_{NW}

??

$$V_{TIA} = V_{Ref} + (I_{NW} - I_{bias}) R_{TIA} + \Delta i R_{TIA}$$

(2)

I_{NW}

Δi

??

R_{TIA}

However, the chip area con- strains the size of re- sis- tors. In our cir- cuit de- sign, it is hard to make a wide lin- ear range re- sis- tor with re-

shows the Transimpedance Amplifier circuit. We implement the operational amplifier in TIA with the two-stage, differential-pair structure. This simple structure has merits such as large output current and wide output voltage range.

$_dc.jpg$ The dc simulation results of TIA. The $x-axis$ represents positive/negative input current (log scale). **(a)** is the $_{out}$

(c)

(b)

(d)

V_{out}

$\frac{\partial V_{out}}{\partial I_{in}}$

(a)

(c)

$_ac.jpg$ The ac simulation results of TIA. The $x-axis$ is the input signal frequency. **(a)** is the $_{out}$

(b)

Fig. **??** and Fig. **??** are the dc and ac post-simulation of the TIA. Fig. **??** shows that the TIA has a constant transimpedance of $100k\Omega$ when the input current range is $6\mu A \sim -10\mu A$. Fig. **??**(a) indicates that the band-width