國立清華大學

碩士論文

積體化電路設計之矽基體奈米線

An Integrated Circuit Design for Silicon-Nanowire

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中華民國 106 年 3 月

Abstract

Poly-silicon nanowire (SiNW) is a well-studied and interesting one-dimensional nanostructure. Since it was introduced to the biosensor field in 2001, it has become a promising candidate for ultra-sensitive, real-time and label-free sensor device. Nevertheless, many physical and chemical challenges constrain nanowire from being robust and practical. Nowadays, many studies adopt the integrated-circuit techniques to solve the problems. Circuits with different design concepts and purposes are proposed to meet practical needs.

In this thesis, based on the nanowire designed by Prof.Yang (National Chiao Tong University), we design our own read-out circuit. This research first analyzes biological experiments results (From Prof.Yang) and the electrical characteristics of the nanowires. The circuit specification and design is then based on these data analysis.

The circuit is capable of performing both DC-sweep (I_D-V_G sweep) and transient measurement. Moreover, we proposed a measurement method a combining of these two functions. We believe this method mitigates the device variability induced by the fabrication process. Currently, most operations in this method are manual. We hope to make them automatic in the future by inducing digital circuits and constructing a system-level structure.

中　文　摘　要

矽基體奈米線（以下簡稱奈米線）乃一有趣並經過充分研究的一維奈米結構物。自從於 2001 年該元件被引入生物量測領域，奈米線就被賦予高度期望，能成為具有高靈敏度、即時性和不需生物標記等優勢的生物分子感測元件。雖然如此，目前仍有有物性和化性上的因素，限制了奈米線的良率和實用性。如今，許多研究採用了積體電路的技術，設計出在概念上和目的上不同的電路，來解決奈米線所遇到的問題和應付特定的需求。

我們使用由交大楊裕雄老師的奈米線元件和一部分量測資料，設計出一套元件訊號讀取電路。本篇研究首先進行生物實驗和電性量測的數據分析，接著根據分析結果來訂出電路的規格和進行電路設計。

我們的電路可以進行直流掃描量測（DC-sweep）和暫態量測（Transient measurement）。並且，藉由結合此二量測，我們提出一套元件量測方式。這個量測方式被認為具有減輕因製程變異性而導致的元件差異問題（Device Variability）的能力。目前，該量測方式多採用手動操作，我們希望日後能引入數位電路於系統性架構，使量測能夠自動化。

致謝

感謝指導教授陳新老師提供一個新奇的題目，並在過程中給予許多有用的建議，在寫作與修改論文的過程中更感謝老師多番勞心勞力。感謝交大楊裕雄老師以及林志恆學長所提供的元件和數據，以及各種實驗上的幫助，使元件量測能夠順利進行。感謝所有 NEL，讓三年的研究所生活過的相當歡樂。感謝 LC，兩年多來陪我一同跨過各種困難和阻礙。最後感謝所有此論文的讀者，感謝你們的耐心與各種建議。

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Chapter 1

Introduction

1.1 Motivation

Poly-silicon nanowire(SiNW) is a well-studied and promising one-dimensional nanostructure. It was first introduced to the biosensor field in 2001[1] and has become a potential candidate for various features such as high surface-to-volume ratio, ultra sensitivity, label-free electrical detection and real-time measurement.

Although there have been substantial advances on nanowire structure design [2], the work on the system-level engineering is still insufficient. Systems designed for a specific purpose can help the device to meet practical needs such as noise reduction, real-time measurement, and analog-to-digital conversion. Moreover, there are still several challenges that may be overcome through a better signal acquisition system [2].

One of the challenges is that the mass production of robust nanowire device is still improbable. Device variability may be the main reason among others. This problem also happens to the measurement of our nanowire. The nanowire we use is made by Professor Yang's team (National Chiao Tong University). According to them, the nanowire uses thick gate dielectric and has non-regular cross-sectional shape, which result in the problem of fabrication uncertainty [3].

1.2 Design Overview

In this project, we design a nanowire read-out circuit with two modes: DC-sweep mode and Transient Measurement mode. In DC-sweep mode, one can use the circuit to perform a DC sweep of drain-to-source current (I_D) to show how the gate voltage (V_G) changes, or gives nanowire a constant I_D and measures the V_G response to different solution concentration. In Transient Measurement mode, the circuit detects and amplifies the variance of I_D with constant bias voltages applied (V_D, V_G, V_S). We also combine two modes to implement our proposal: the variability-resisting method. This method of measurement may mitigate the device variability problem.

Dealing with the Device Variability Problem: the Variability-resisting Method

The variability-resisting method is based on two assumptions:

1. The transconductance ($g_m = \frac{\partial I_D}{\partial V_{GS}}$) of nanowire in weak inversion is linearly dependent on I_D and independent of V_{GS}.
2. The change of biomolecule concentrations can induce potential change on the surface of the gate of a nanowire.

(Since the source of nanowire is always grounded in this method, from now on V_{GS} is simplified as V_G.) The first assumption implies one can control the nanowire transconductance by its I_D. The second assumption means that as long as different nanowire elements have the same transconductance, the I_D variance induced by a concentration difference should be same.

The method works as follows:

Initial stage At the beginning of each measurement event, we perform a DC sweep with DC-sweep mode. By analyzing the sweep results with numerical method, we keep all nanowire devices under a selected transconductance by controlling their I_D and corresponding V_G.

Measurement stage We bias the circuit in Transient Measurement mode at this stage. Since the transconductance of all devices are same, they should behave uniformly based on assumption 2. At the end of the stage, we return to DC-sweep mode to reset I_D of the elements. The circuit adjusts their V_G to do so.

At the beginning of each measurement stage, a device always has the same I_D but different V_G. Based on assumption 1, its transconductance is kept constant.

Other details are reviewed in chapter 5. Currently, most operations are manual. We hope to make them automatic in the future, which may require digital circuits.

1.3 Design Flow and Chapter Layout

In this thesis, there are six chapters sorted according to the design flow.

Chapter 2 reviews the basic theories and the literature that are related to our work.

Chapter 3 gives a brief description of nanowire structure. It is then followed by two sections about some measurement and data analysis. The data of the first one is from the biological experiments while the second one is from the electrical measurement. We use the analysis results to design the read-out circuit.

Chapter 4 is an "accessory". This chapter contains the discrete circuit which was designed for ion-sensitive field-effect transistor (ISFET) [4]. It is constructed and some electrical measurements are performed The purpose of this process is to practice the constant-current constant-voltage method. The outcomes of this chapter underpin our integrated circuit design.

Chapter 5 talks about the schematic, design process and the simulation results of the read-out circuit.

Chapter 6 presents the measurement results of our integrated circuit and the conclusion of this project.

Chapter 2

Literature Review & Theory Description

As previously mentioned in the introduction section, the read-out circuit has two operation modes. DC-sweep mode controls the drain current (I_D) of nanowire while Transient Measurement mode is for current variance measurement. Each of them refers to different sources. Section 2.1 talks about the reason why we perform I_D-V_G sweep. It is then followed by the literature review related to the circuit design of DC-sweep mode. The literature related to Transient Measurement mode circuit design is in section 2.2. The last section discusses the two assumptions mentioned in section 1.2.

2.1 DC Sweep: I_D-V_G Curves

This section reviews the knowledge and an article that is related to DC-sweep mode.

2.1.1 I_D-V_G and Transconductance

A common method for examining nanowire electrical properties is to perform DC sweep. Among all kinds of sweep method, we choose the I_D-V_G in respect of the physical characteristic. In the n-type transistor, the binding of negatively charged biomolecules induces surface-near silicon ions discharged and thus increases the threshold voltage. It is straightforward to think of these binding molecules as a

voltage signal input to the gate with its value depends on the concentration. And this voltage signal effects nanowire in the same way V_G does. So by plotting I_D-V_G curves, we can have a thumbnail of how concentration affects the I_D.

2.1.2 The Source Follower Structure

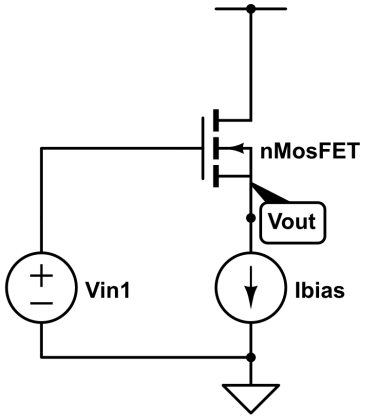

Figure 2.1: Sorce Follower

As one of the basic single stage amplifier, source follower (common drain) are employed to transfer voltage signal from gate to source while keeping I_D constant. The transfer function can be derived as:

$$\frac{V_{out}}{V_{in}} = \frac{r_{ds}g_m}{1 + r_{ds}g_m} \tag{2.1}$$

$$\approx 1 \qquad \text{for} \quad r_{ds}g_m >> 1 \tag{2.2}$$

g_m is the transconductance ($\frac{\partial I_D}{\partial V_{GS}}$) and r_{ds} is the drain-to-source resistance. Although we have not seen the structure being applied to the nanowire, there have been several applications in the read-out circuits of ISFET (Ion-sensitive Field-effect Transistor)[4, 5] for a while.

The read-out circuit in [4] employs ISFET as a biological transducer that converts detected bio-signals into electrical signals, which resembles our nanowire biosensor. It adopts the source follower structure as its analog front-end. The potential change induced by the biomolecules at the gate of ISFET is converted to the source. This structure requires a biasing current which needs to be stable, noiseless or wide-range on demand. Since the biasing current is usually under micro-scale or even nano-scale,

it is impractical to use an external current source. The article [4] uses two resistors and an op-amp to design a current scale down circuit. As in Fig.2.2, bias current decreases in proportional to the resistance ratio (N) as the current source circuit IB.

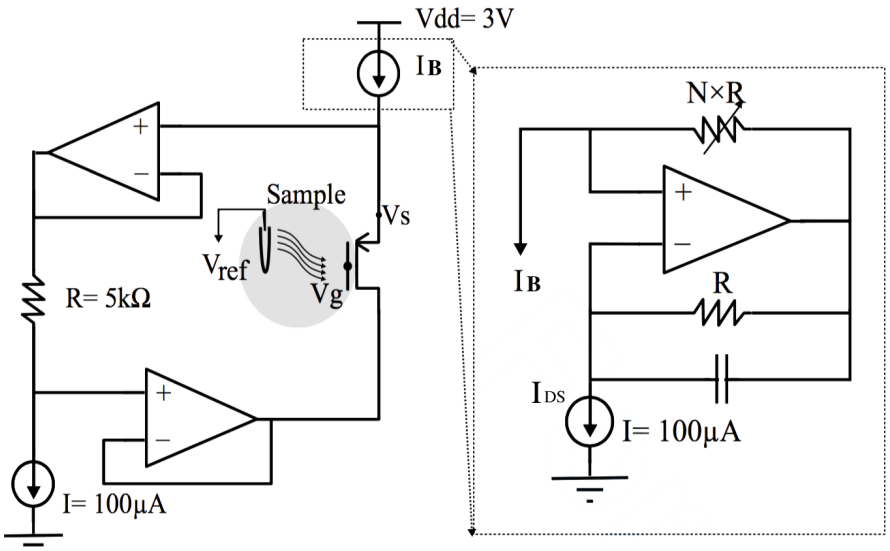

Figure 2.2: ISFET readout circuit in [4]

The circuit in Fig.2.2 also removes the short channel effect by keeping V_{DS} at a constant value (0.5v). It adopts two op-amp based unit gain buffer to force the voltage at drain follows the source.

Attention should be paid to the impedance matching between the device-under-test (DUT) and the current source circuit. The output impedance of current source should be much larger than the input impedance of the DUT. By using nanowire as the DUT, the input impedance of it is:

$$\frac{r_{ds}}{1 + g_m r_{ds}} \tag{2.3}$$

This equation can be simplified as:

$$\frac{1}{g_m} \qquad \text{for} \quad g_m r_{ds} >> 1 \tag{2.4}$$

The output impedance of the current source I_B is:

$$N \times Z_{DS} \tag{2.5}$$

Z_{DS} is the impedance of the current source Ids in Fig.2.2. In the integrated circuit, Z_{DS} is non-ideal but usually close to the r_{ds} of a single MOSFET.

As mentioned, Eq.(2.5) should be far larger than Eq.(2.4). However, g_m is proportional to I_B, which means Eq.(2.4) is inversely proportional to N. When the biasing current decreases, the output impedance of Ib decreases while the input impedance at the source of ISFET increases. This relationship determines the limit for I_B. We observed this boundary when we constructed this circuit with discrete elements. These will be presented and discussed in chapter 4.

The source follower structure provides a direct signal transition method. It is a good candidate for the read-out circuit with the aim of detecting transconductance or threshold voltage variance. Nevertheless, post-processing such as amplification and filtering is necessary. The experiment results in [4] are untreated. Significant signal attenuation exists, which is mainly caused by low-frequency noise and ISFET drift [6]. The drift problem is dealt with by signal processing techniques while noise problem is left untreated.

2.2 Small Signal (AC) Measurement Method Review

The previous section mentioned that he source follower exhibits compelling advantages as a signal processing structure of nano-device. However, the structure faces obstacles when being applied to the small signal detection. Parasitic capacitors and resistors can influence the results.

As the parasitic elements are included in Fig.2.3, the transfer function Eq.(2.2) is modified as:

$$\frac{V_{out}}{V_{in}} = \frac{r_{ds}(sC_{gs} + gm)}{1 + r_{ds}(gm + s(C_{gs} + C_s))} \tag{2.6}$$

The equation can be similar to Eq.(2.2) which roughly equals to 1 as long as C_s is far smaller than C_{gs}. Unfortunately, C_s can be close to or greater than C_{gs} since the output of the source follower is connected to a next stage input or a pad. In that case, the signal may be attenuated.

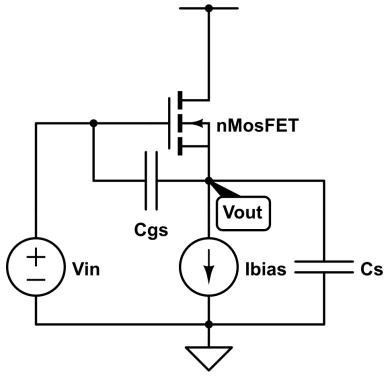

Figure 2.3: Sorce Follower with parasitic capacitance

We want to build another circuit structure that can not only perform AC signal measurement but also disregard parasitic capacitance. We started by reviewing the works trying to measure the parasitic capacitance. Below, the works from two teams aim to measure the drain-to-source resistance (R_{NW}) and the drain-to-source capacitance (C_{NW}). The review focuses on the function and design theory of their read-out circuits.

2.2.1 RC Time Delay Measuring

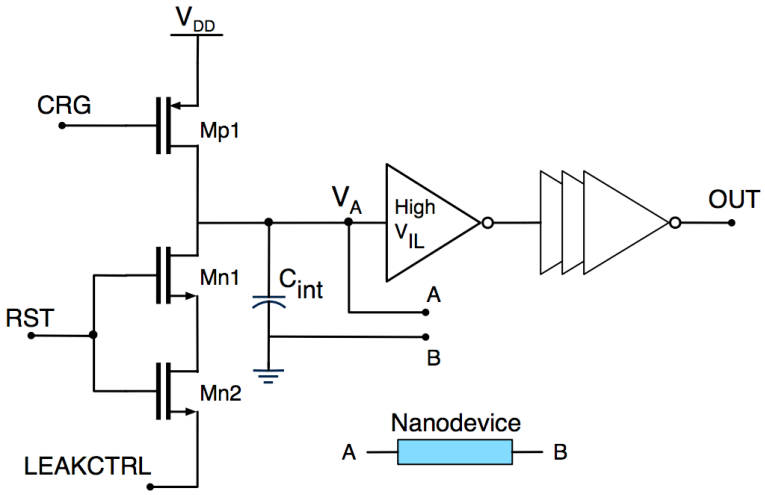

Figure 2.4: (a) Schematic of [7].

The measurement system for ZnO-nanowire based sensor array from [7] applies the Time-over-Threshold technique to its read-out circuit (Fig.2.4). The circuit alternatively charges an on-chip capacitor (C_{int}) with a constant current and discharges

it through the nano-material resistance (nanowire). An inverter with its output switches from on to off when the capacitor is charged to its input threshold voltage, and vice versa. This behavior converts information of nanowire such as capacitance and resistance into time information.

The work presented in [7] does not have enough explanation of how they interpret the capacitance and resistance information. It merely mentioned that a microcontroller is responsible for the calculation. Besides, the work lacks simulation and experiment of measuring complex devices. Most of the results are the measurement of a concrete resistor as the substitute for nanowire, and C_{NW} is regarded as $0pF$. The only nanowire experiment does not have good performance. It seems that the design may only be applied to a device with pure resistance or pure capacitance.

The recent publican [8] by the team is more elaborate and contains the measurement of complex devices (A device composed of a discrete resistor and a discrete capacitor).

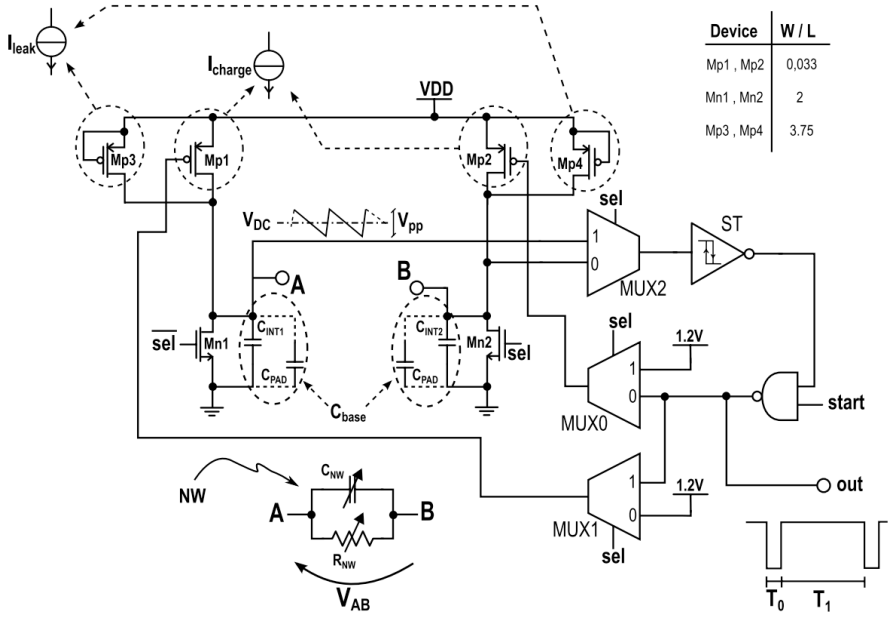

Figure 2.5: Schematic of [8].

In Fig.2.5, nanowire appends between point A and B. The charging current can be applied from Mp1 or Mp2, which is determined by the "sel" signal with the aid from MUXs. Below, it is assumed that sel = 1 and point B is virtual ground. (When the sel = 0, the circuit measures the device with a reversed biasing current.) The circuit

design concept is the same as [7]. The current charge both C_{int} and C_{NW}. When the voltage at A exceed the threshold voltage, the output switches off and causes Mp1 to turn off. (It is notable that the inverter at the output stage in [7] is replaces by a Schmitt trigger in [8]) Then the capacitor discharges through nanowire (r_{ds}).

The bottom-right plot in Fig.2.5 defines T_0 as the charging time and T_1 as the discharging time. The calculation of the R_{NW} and C_{NW} can be simplified as:

$$C_{NW} = T_0 - C_{base} \tag{2.7}$$

$$R_{NW} = \frac{T_1 R_{par}}{(C_{NW} + C_{base})R_{par} - T_1} \tag{2.8}$$

$$\text{where} \qquad R_{NW}||R_{par} = \frac{T_1}{C_{NW} + C_{base}} \tag{2.9}$$

C_{base} are the C_{int} plus parasitic capacitance and R_{par} the parasitic resistance. These parasitic elements come from the transistor in the integrated circuit block such as MUX and Mp. It is notable that we do not consider the hysteresis of the Schmitt trigger here owing to simplicity.

2.2.2 Complex Impedance Solving

The nanowire-based hydrogen sensor measurement system in [9] adopts another method. It uses a lock-in amplifier to realize both resistive and capacitive impedance measurement.

As the previous method, it treats nanowire as a device with complex impedance. The nanowire is modeled as a resistor and a capacitor in parallel connection. The system applies a sinusoidal voltage signal to one end of the device. Another end of the device is virtually grounded by a transimpedance amplifier (TIA). The TIA then converts the current variance into a voltage output which depends on the complex impedance of the nanowire. The resistance is in the real part while the capacitance is in the virtual part.

$$V_{out} = I_{NW} R_{TIA} \tag{2.10}$$

$$I_{NW} = V_{in}(\frac{1}{R_{NW}} + j2\pi f C_{NW}) \tag{2.11}$$

f is the frequency of input signal.

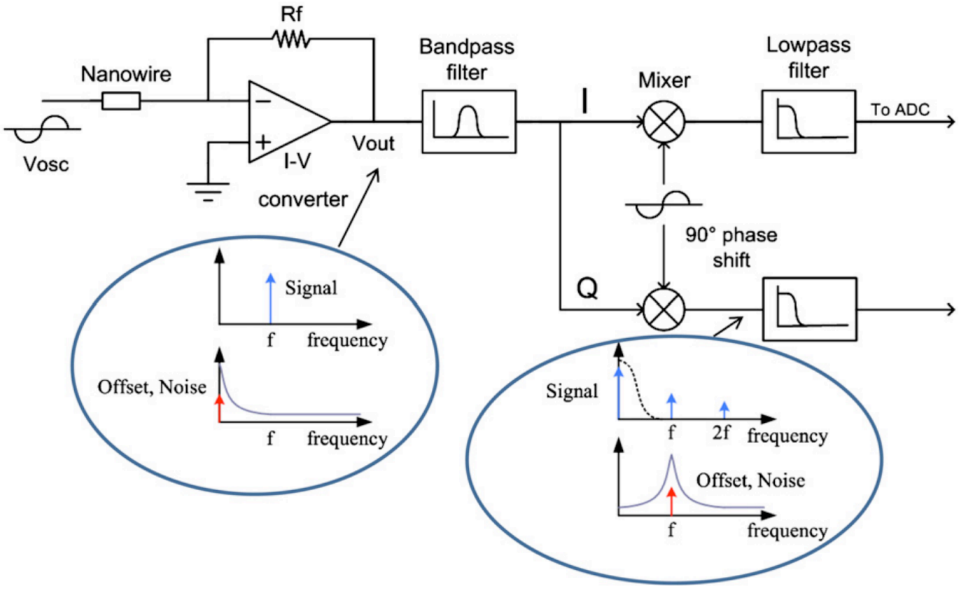

Figure 2.6: Block diagram of the lock-in amplifier in [9]

The output of TIA is followed by a controllable bandpass filter (BP). The BP removes high-order harmonic interferences. Then the signal is demodulated. The resistive and capacitive impedance values are resolved through two channels: I and Q with their phase different by 90 degrees. A mixer which is a linear multiplier performs the demodulation. With a radio frequency (RF) input and a local oscillator (LO) input, it produces an output signal that consists of signals with frequencies $f_{RF} + f_{LO}$ and $f_{RF} - f_{LO}$.

2.2.3 Comparison and Conclusion

We compare the Method 1 (Sec.2.2.1) and Method 2 (Sec.2.2.2) here. Both of them focus on detecting the R_{NW} difference. According to the comparison table below (2.1), we can see the resistor measurement range of Method 1 is different from Method 2 by a large extent. It is not appropriate to make a comparison directly. These ranges are conformed to a detecting range for the current variance, which is also more helpful for our circuit design.

The resistance measuring range of Method 1 is $1M\Omega \sim 1G\Omega$. Since the circuit applies an input ac signal with amplitude of $120mV$ to the nanowire device, the equivalent current variance is $120\mu A \sim 0.12nA$.

	[8]	[9]
R meas range	1M - 1G	10 - 40k
R meas error	$< 2.5\%$	$< 2\%$
C meas range	100fF - 1uF	0.5 - 1.8nF
C meas error	$< 3\%$	$< 3\%$
Detection of Input Current Varinace	$120\mu A$ - $0.12nA$	$3\mu A$ - $60nA$
SNR	$>$ 45dB	-
Input referred noise	-	190 nV/sqrt(Hz) @ 5 kHz
CMOS Technology	0.13um	0.18um
Power consumption	14.82uW	2mW

Table 2.1: Specification Summary

As for Method 2, the measuring range relates to the noise. A $3mV$ output referred noise limits the detecting range. According th the article, this noise value is equivalent to a 2% resistance resolution. Therefore, the output voltage range should be $3mV \sim 0.15V$. Moreover, the gain of the post-stage (BP and last-stage low pass filter) is 5 and the Rf in the TIA is 10k Hence the current variance that circuit can detect should be $60nA \sim 3\mu A$.

The relatively narrow current detection range of Method 2 should be because of the TIA block it adopts. Our method adopts this TIA block and will discuss this problem in Section.**??**.

Method 2 performs well when it comes to noise suppression. In fact, the circuit in Method 1 does not provide noise reduction ability. The particular structure it uses (The article [7] mentioned it as Micro-for-Nano (M4N) approach [10].) is the one responsible for that.

Method 1 has lower power consumption. However, it does not include the power of microcontroller and may be underestimated.

Overall, Method 1 has the advantage in detecting range and accuracy while Method 2 has better noise suppression.

In our project, capacitance measurement is not our object. But we still need to consider the parasitic capacitor effect in our circuit design. Method 1 converts the

resistance information into time (frequency) information. If one wants to avoid the effect of the parasitic capacitor, he should apply a C_{int} that is much larger than C_{NW}. However, it is not practical in integrated design because the chip size is limited.

Method 2 uses a TIA to measure resistance and capacitance together first and then resolves the complex value. We can write the complex impedance value as:

$$\frac{R_{NW}}{1 + i2\pi f R_{NW} C_{NW}} \tag{2.12}$$

In Eq.(2.12), i is the imaginary unit and f is the signal frequency. The equation can be simplified as R_{NW} when $i2\pi f R_{NW} C_{NW} < 0.1$. The simplification can be applied when the signal frequency or $C_{NW} R_{NW}$ is small enough.

Since our goal is to ignore the capacitance and merely detect the resistance (or transconductance), Method 2 is more suitable for us. Because it is easier to separate capacitive and resistive measurement by Method 2 than by Method 1.

2.3 Two assumption for Dealing with Device Variability Problem

In chapter 1, to deal with device variability problem, we assume that:

1. The transconductance ($g_m = \frac{\partial I_D}{\partial V_G}$) of nanowire in weak inversion is linearly dependent on I_D and independent of V_G.

2. The change of the biomolecule concentration can induce potential change on the surface of the gate of a nanowire..

We discuss them in this section.

2.3.1 Transconductance and I_D

With the MOSFET model of weak and strong inversion, we have the I_D equations of MOSFET :

$$\text{weak inversion:} \quad I_D = I_0 e^{\kappa V_{GS}/\phi_t}(1 - e^{-V_{DS}/\phi_t}) \tag{2.13}$$

$$= I_0 e^{\kappa V_{GS}/\phi_t} \quad \text{where } V_{DS} > 4\phi_t \tag{2.14}$$

$$\text{strong inversion:} \quad I_D = \mu C_{ox}\frac{W}{L}((V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}) \tag{2.15}$$

$$= \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2 \quad \text{where } V_{DS} > V_{GS} - V_{th} \tag{2.16}$$

V_{GS} is the gate-to-source voltage ($V_{GS} = V_G - V_S$). It will be written as V_G in the following paragraphs since source is considered to be grounded. C_{ox} is the oxide capacitance and μ is the electron mobility. Both of them depends on doping concentration. W and L are the width and length of the transistor. ϕ_t is the thermal voltage depending on temperature. The κ is the gate coupling coefficient. To be noted that we ignore the short channel effect, which does not effect our discussion since V_{DS} is always kept constant.

We then derive g_m:

$$\text{weak inversion:} \quad g_m = \frac{\kappa I_D}{\phi_t} \tag{2.17}$$

$$\text{strong inversion:} \quad g_m = \sqrt{2\mu C_{ox}(\frac{W}{L})I_D} \tag{2.18}$$

The Eq.(2.17) shows that the g_m in weak inversion is affected by the gate coupling effect. This effect is illustrated in Fig.2.7. The κ is actually the ratio of voltage divider:

$$\kappa = \frac{C_{ox}}{C_{ox} + C_{dep}} \tag{2.19}$$

The fact that C_{dep} varies with V_G makes κ a non-linear parameter. Its value ranges from 0.4 to 0.9. The structure of nanowire is different from MOSFET and is illustrated in Fig.2.8 The SiO2 insulator in MOSFET is replaced by the solvent

and the C_{ox} becomes C_{sol}. According to the famous Gouy-Chapman model, the potential difference in the solution affect the double layer capacitance in solution [11]. Thus, it is still true that V_G affect gm. Nevertheless, it is convinced that the κ value is very close to 1 because C_{sol} is much greater that C_{dep}. This will be discussed later.

As for the strong inversion, g_m linearly depends on $\sqrt{I_D}$ and independent of V_G. However, in nanowire, the C_{ox} is replaced by C_{sol} and is affected by V_G and the solvent concentration. Therefore, the assumption 1 cannot be applied to nanowire in strong inversion region.

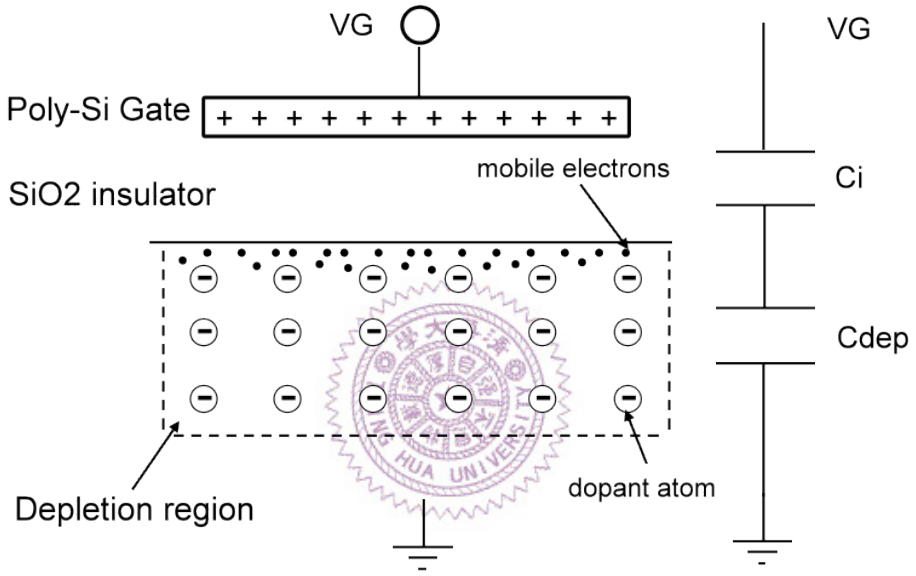

Figure 2.7: The gate coupling effect in MOSFET [12].

Estimation of C_{sol}

C_{sol} can be estimated by applying the famous Gouy–Chapman–Stern model [13]. The model explains the double-layer capacitance (C_{DL}), which is the structure appears on the contact surface between liquid and metal or solid particle. The capacitance is considered to be two capacitors in series:

$$\frac{1}{C_{DL}} = \frac{1}{C_{stern}} + \frac{1}{C_D} \tag{2.20}$$

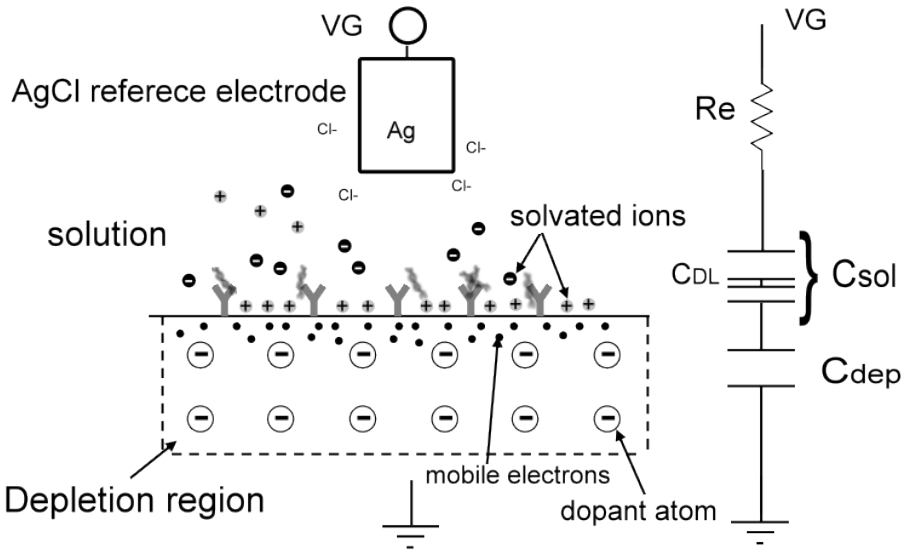

Figure 2.8: The gate coupling effect in nanowire.

C_{stern} represents the capacitor in the stern layer and C_D represents the capacitor in diffusion layer. For DNA solution and PBS as buffer, the relative permittivity is 8 [14] and debye length is about 0.7nm. C_{stern} is therefore roughly $97\mu/cm^2$. As for C_D, the value is hard to know since it relates to ion concentration and fluid potential. However, the model implies that C_{DL} is mostly dominated by C_{stern}. Only if the solution contains scarce solvent, C_D should be taken into consideration. It is clearly not our case because the PBS buffer we use has high ion concentration.

2.3.2 A Simple Model for Concentration Effect

In [15], the team plots the I_D-V_G curves and study how the curves change with the concentration of biomolecules. We observed that in the plot (Fig.2.9) with a log scale for the y-axis, curves with different concentrations exhibit the same rising trend when I_D is low ($<$ 100nA). Each curve seems to be different from each other by a constant shift. We found that this concentration effect can be explained by applying the weak inversion current equation of MOSFET.

$$I_{D1} = I_0 e^{\kappa(V_G)/\phi_t} \tag{2.21}$$

$$I_{D2} = I_0 e^{\kappa(V_G+\Delta v)/\phi_t} \tag{2.22}$$

$$\rightarrow I_{D2} = f(\Delta v) \times I_{D1} \quad \text{where} \quad f(\Delta v) = e^{\Delta v/\phi_t} \tag{2.23}$$

The I_{D1} and I_{D2} are the current of two nanowire devices immersed in solutions with different concentrations. The (Δv) is a concentration related variable we create. The Eq.(2.23) implies that when nanowire is in weak inversion region, its $\log I_D$ difference is independent of V_G.

$$\log I_{D2} - \log I_{D1} = \log \frac{I_{D2}}{I_{D1}} = \log f(\Delta v) = \Delta v/\phi_t \tag{2.24}$$

As for the strong inversion region corresponding to the large current segments in Fig.2.9, the difference among the curves diminish as V_G increases. This is reasonable when V_G is far larger than Δv and the concentration effect becomes ignorable.

We will further prove the two assumptions by the data of biology experiment in section.**??**.

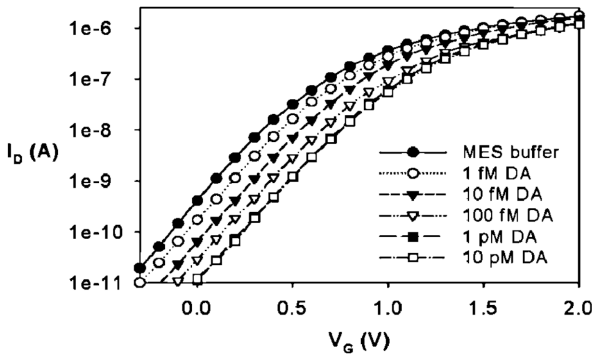

Figure 2.9: Concentration-dependent electric response($I_D - V_G$) of biotin-modified poly-Si NWFET following biotin–streptavidin interaction.[15]

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