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碩士論文

Your Thesis Tile in English

論文中文標題

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An Integrated Circuit Design for Silicon-Nanowire

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Abstract

中　文　摘　要

關鍵詞：

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Chapter 1

Introduction

1.1 Motivation

Poly-silicon nanowire(SiNW) is an interesting and promising one-dimensional nano-structures. Many research of fabrication and electrical properties have been conducted [?]. It was first introduced to the biosensor field in 2001[?] and has become a promising candidate for various features such as high surface-to-volume ratio, ultra sensitivity, label-free electrical detection and real-time measurement.

Although there has been some great advances on nanowire structure design [?], the work of systems-level engineering is still insufficient. Systems designed for specific purpose can help the device to meet pratical needs.

Such as low noise

Problem Define

With our experience from some application of nanowire, there are three problems which needs integrated circuit solution:

1. Disparity

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2. The second item

3. The third etc …

By the nanowire measurement (These are presented in the section 3),

1.2 Design Description

In our biosensing system, nanowire is treated as a MOSFET. Its gate bias under a specific voltage source And the bio-siganl is viewed as small voltage signal input to the gate.

with its drain-source current (I_{ds}) biased by a pmos current source. When a measurement event happens (such as a DNA concentration variation), the transconductance of nanowire changes and induces a current variance. This variance is converted into an amplified voltage signal. After the measurement, a feedback circuit pulls up/down the nanowire gate-source volatge (V_{gs}) to set I_{ds} to the initail value.

1.3 Contribution to Knowledge

Chapter 2

Literature Review

Chapter 3

Nanowire Structure and Measurement

3.1 Brief Description of Nanowire Structure

The nanowire we use is made by Prof.Yang's team (National Chiao Tong University)[?]. A sectional view of the nanowire structure is given below. The fabrication process is based on the poly-silicon sidewall spacer technique. The n-Type doped poly-SiNW FET has 2 to 10 poly-silicon channels. Each channel is 80nm in width and 2µm in length. Large portion of the channel surface is exposed to environment. The exposed region, through several post-process, capture the DNA probe and serve as the sensing site for DNA molecules.[1, 2]

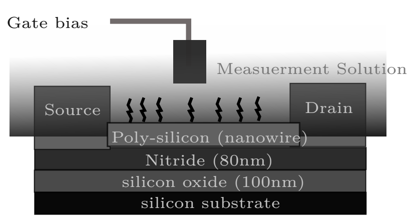


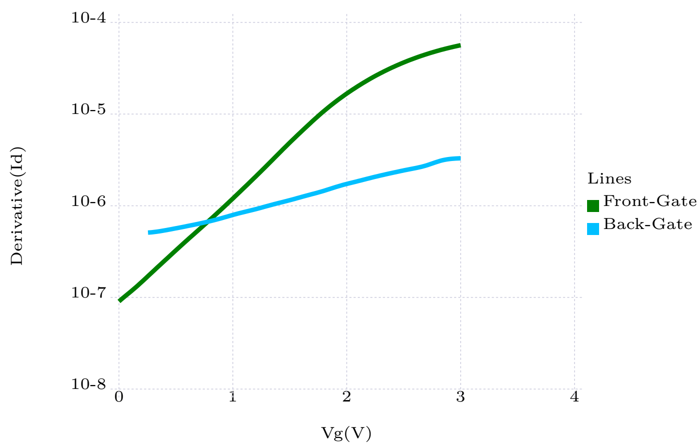
Figure 3.1: Nanowire Structure

3.2 Measurement

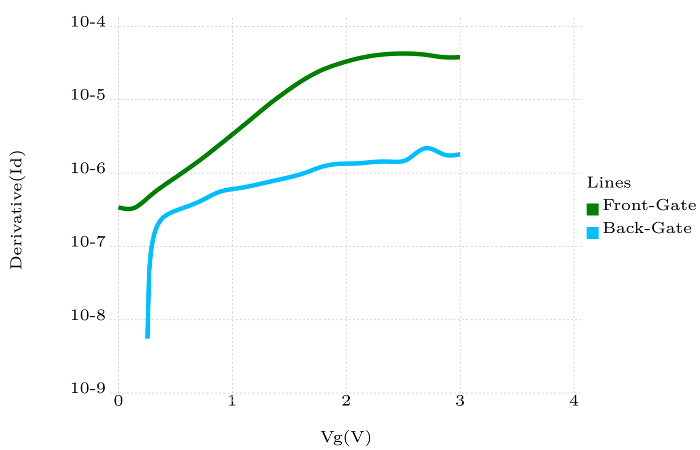
This section presents the results.

Front Gate and Back Gate

Two gates are available: front-gate (liquid gate) and back-gate. We choose front-gate as the operation gate in spite of some advantages that back-gate has. One of them is the ablility to lower the 1/f noise [4, 3]. However, this only happens in a very high gate voltage, which is not practical in the integrated circuit design. Moreover, the front-gate induces larger drain-current. In other words, it has higher transconductance. And a high transconductance leads to a stronger feedback ability in our design.



(a)

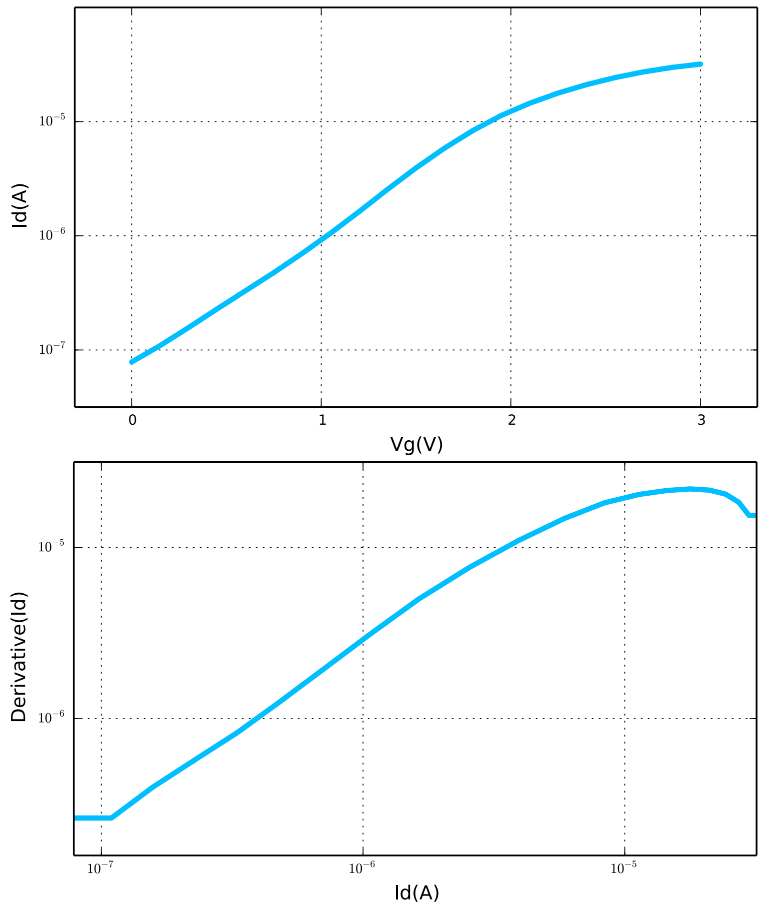


(b)

Figure 3.2:

3.2.1 Parameters

The most crucial parameter for our circuit design is the transconductance (gm). The gm is acquired by finding the relation between drain-to-source current (I_d) and gate-source voltage (V_g), and perform differentiation: $\frac{\partial I_d}{\partial V_g}$. use standard PBS as



(a)

(b)

Figure 3.3:

The Id-Derivative figures indicates there is a “linear region” where gm is proportional to Id. This property implies the transconductance can be controlled in simple way. As mentioned in introduction, we may find specific bias Id for distinct elements and adjust their transconductance to a same value.

We also prove that the transconductance under this region is unaffected by the drain-source voltage variance.

None

Figure 3.4: Distinct element with a line idicate they have same transconductance

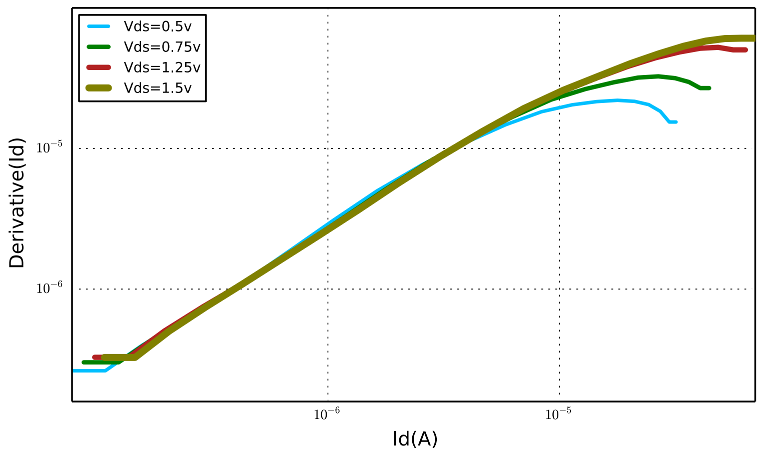


Figure 3.5: Id-transcinductance with Vds variance

3.2.2 External Factor and Experimental Protocol

Several conditions effect nanowire performance. According to Yang's team, the nanowire using thick gate dielectric and having non-regular cross-sectional shape result in uncertainties of fabrication [2]. Figure below shows that two elements lying on the same wafer can exhibit different electrical characteristics.

None

Figure 3.6: Nanowire Structure

Chapter 4

Integrated Circuitry Design

Chapter 5

More Experiment Result

Chapter 6

Discussion and Conclusions

Bibliography

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Acknowledgement