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碩士論文

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研究生：< 中文名 >(<English Name>)

指導教授：< 中文名 > 教授 (Prof. <English Name>)

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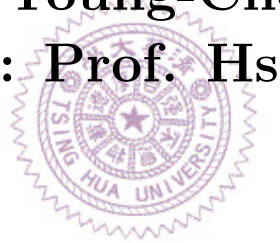
An Integrated Circuit Design for Silicon-Nanowire

Student: Young-Chen Chang
Advisor: Prof. Hsin Chen



Department of Electrical Engineering
National Tsing Hua University
Hsinchu, Taiwan, 30013, R.O.C.

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Abstract

中　　文　　摘　　要

關鍵詞：

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Chapter 1

Introduction

1.1 Motivation

Poly-silicon nanowire(SiNW) is an interesting and promising one-dimensional nanostructures. Many research of fabrication and electrical properties have been conducted [**?**]. It was first introduced to the biosensor field in 2001[**?**] and has become a promising candidate for various features such as high surface-to-volume ratio, ultra sensitivity, label-free electrical detection and real-time measurement.

Although there has been some great advances on nanowire structure design [**?**], the work of systems-level engineering is still insufficient. Systems designed for specific purpose can help the device to meet practical needs. Such as low noise Moreover, there are still several challenges that may be overcome through a better signal acquisition system [1].

One of the challenges is that the mass production of robust nanowire is still improbable. Element disparity may be a main reason among others. This problem also happens to the measurement of our own nanowire (Fig. 3.5). The nanowire we use is made by Professor Yang's team (National Chiao Tong University). And according to them, the nanowire use thick gate dielectric and have non-regular cross-sectional shape, which result in uncertainties of fabrication [3].

1.2 Introduction

In this project, we design a nanowire readout circuit that is capable of performing both large signal and small signal measurement. Specifically, it can be used for finding the Id-Vgs relation, and for reading current variance of nanowire. We also combines these two function to try a method for solving the disparity problem.

Method for solving the disparity problem

It base on two assumptions.

1. The nanowire transconductance is proportional to the drain-to-source current (Id).

2. The changing of the concentration of targeted biomolecule can be viewed as the small signal voltage input to the gate end of a transistor.

The first assumption implies one can control the nanowire transconductance by the biasing Id. The second assumption means that as long as different nanowire elements have a same transconductance, they produce same output current (small signal). We testify these assumption in chapter 3.

We implement the method through through our read-out circuit with large signal mode (LS) and small signal mode (SS). The LS mode biases nanowire under a selected current by altering the gate voltage The SS mode measures the drain current variance, which is a response to the concentration change of the targeted biomolecule. In the beginning of each measurement event, we applied the LS mode to initialized the drain current and gate voltage of nanowire. This is to standardize every nanowire under a same transconductance. Under these current and voltage, we turn to the SS.

Some minutiae is reviewed in chapter 5. Currently the operation in the first mode is fully manual. In the future work this needs to be modified and may requires digital circuit assistance.

1.3 Design Flow and Chapter Layout

There are six chapters in this thesis, which are sorted according to the design flow.

Chapter 2 are divided into two part. The first part is the literature review. ... The other is the analysis of measurement data from Yang's team. Most of those are the drain current of nanowire sweeping along the gate voltage (Id-Vg curves). We present some of the raw data and the analysis results in this part.

Chapter 3 gives a brief description of nanowire structure. It is then followed by our own nanowire measurement based on the information in the previous chapter. The measurement includes:

1. Comparison between front gate and back gate
2. Nanowire transconductance
3. Nanowire drain-to-source resistance

Chapter 4 is an "accessory". We construct an discrete circuit which was designed for ion-sensitive field-effect transistor (ISFET) [4]. The purpose of this process is to practice the constant current method. The outcomes are deficient and it is its reference value which we spotlight.

Chapter 5

None

Figure 1.1: Design Flow

1.4 Contribution to Knowledge

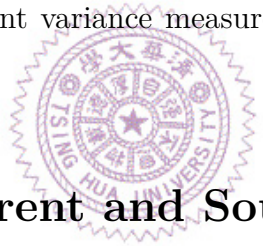
Our

Chapter 2

Literature Review &

2.1 Literature Review

As previously mentioned in the introduction section, the read-out circuit we proposed has two operation mode (LS and SS). The LS mode is for drain current biasing while the SS mode is for current variance measurement. Each of them references different sources.



2.2 Constant Current and Source Follower

2.2.1 Source Follower

As one of the basic single stage amplifier, source follower (common drain) are employed to transfer voltage signal from gate to source while keeping drain current constant. Although we haven't seen it is applied to nanowire, there have been several applications in the read-out circuits of ISFET (Ion-sensitive Field-effect Transistor)[5, 7] for a long time.

In "Rapid Detection of E.coli Bacteria using Potassium-Sensitive FETs in CMOS", ISFET is applied as a biological transducer that convert detected bio-signal into it's input signal on the gate-end, which is resemble to our biosensor of nanowire. An read-out circuit of source follower is served as the analog front-end. The bio-signal induced voltage difference at the ISFET gate-end are converted to the source-end. There is no need for an extra current-to-voltage converter which may import more

signal fluctuation such as shot noise or flicker noise. But on the other hand, the circuit requires a biasing current source. This current source may have to be stable, noiseless or wide-range on demand. And since the current value are usually under micro-scale even nano-scale, it is impractical to merely use external current source. The article use two resistors and an op-amp to design a current scale down circuit. Bias current decreases in proportional to the resistance ratio (N) of one resistor to another. Moreover, by keeping Vds at a constant value (0.5v), the circuit also removes the channel affect which is a factor that may effect linearity of the results. It is showed in the schematic below that two op-amp based unit gain buffer are added to force the voltage at drain-end follows the source-end.

Schematic

An issue need to be noticed is the impedance matching between the element and the current source circuit. It is known that the output impedance of current source should be much larger than the input impedance of the biased element. The equation for the output impedance of source follower is:

$$\frac{r_{ds}}{1 + g_m r_{ds}} \tag{2.1}$$

The g_m is the transconductance ($\frac{\partial I_d}{\partial V_{gs}}$) and the r_{ds} is the drain-to-source impedance. This equation can be simplified as:

$$\frac{1}{g_m} \qquad \text{for} \quad g_m r_{ds} >> 1 \tag{2.2}$$

We also compute the output impedance of the current source circuit:

$$N \times R_i \tag{2.3}$$

R_i is the impedance of the current source I1 in Fig. In the integrated circuit, R_i is not ideal but usually close to the r_{ds} of a single MOSFET.

As mentioned, Eq.2.3 should be far larger than Eq.2.2. However, g_m is proportional to the I_d, which means Eq.2.2 is inversely proportional to N. When the bias current decreases, the output impedance decreases while the input impedance at the ISFET source-end increases. This creates a lower boundary of the bias current.

The source follower structure provides a direct signal transition method. It is a good candidate for the read-out circuit with the aim of detecting transconductance

or threshold voltage variance. Nevertheless, post-processing such as amplification and filtering are necessary. The experiment results in the article are untreated. Some strong signal attenuation exist, which are mainly caused by noise.

We constructed this circuit with discrete elements and applied it to our nanowire. The results are presented in chapter 4.

2.3 Data Analysis

Chapter 3

Nanowire Structure and Measurement

3.1 Brief Description of Nanowire Structure

The nanowire we use is made by Prof.Yang's team (National Chiao Tong University)[**?**]. A sectional view of the nanowire structure is given below. The fabrication process is based on the poly-silicon sidewall spacer technique. The n-Type doped poly-SiNW FET has 2 to 10 poly-silicon channels. Each channel is 80nm in width and 2μm in length. Large portion of the channel surface is exposed to environment. The exposed region, through several post-process, capture the DNA probe and serve as the sensing site for DNA molecules.[2, 3]

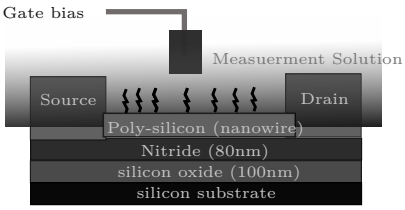


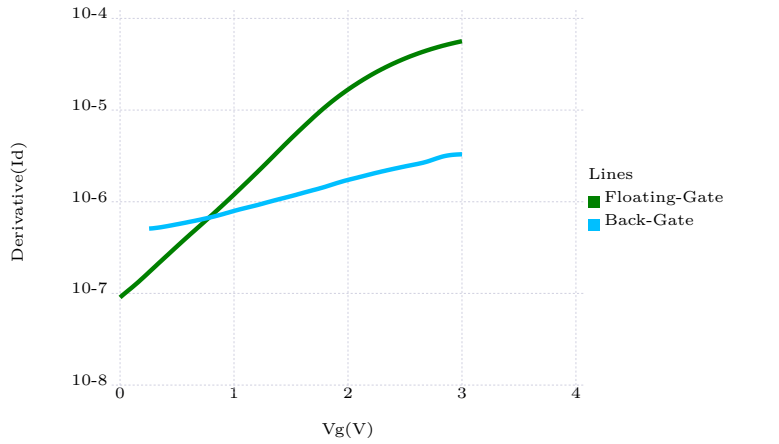
Figure 3.1: Nanowire Structure

3.2 Measurement

This section presents the results.

Front Gate and Back Gate

Two gates are available: floating gate (liquid gate) and back-gate. We choose floating gate as the operation gate in spite of some advantages that back-gate has. One of them is the ability to lower the 1/f noise [8, 6]. However, this only happens in a very high gate voltage, which is not practical in the integrated circuit design. Moreover, the floating gate induces larger drain-current. In other words, it has higher transconductance. And a high transconductance leads to a stronger feedback ability in our design.



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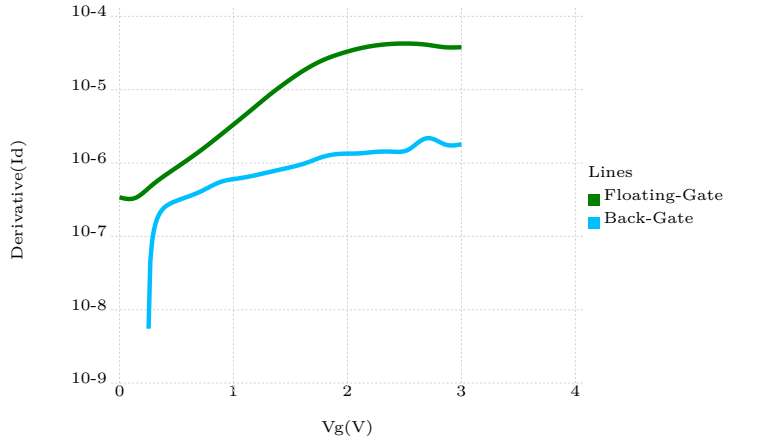
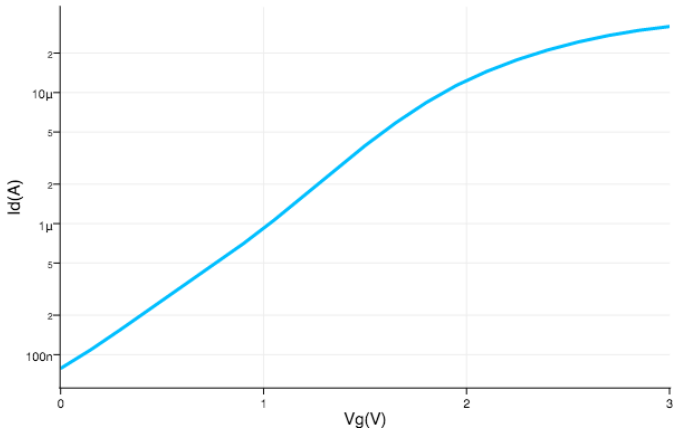


(b)

Figure 3.2:

3.2.1 Parameters

The most crucial parameter for our circuit design is the transconductance (gm). The gm is acquired by finding the relation between drain-to-source current (I_d) and gate-source voltage (V_g), and perform differentiation: $\frac{\partial I_d}{\partial V_g}$. use standard PBS as



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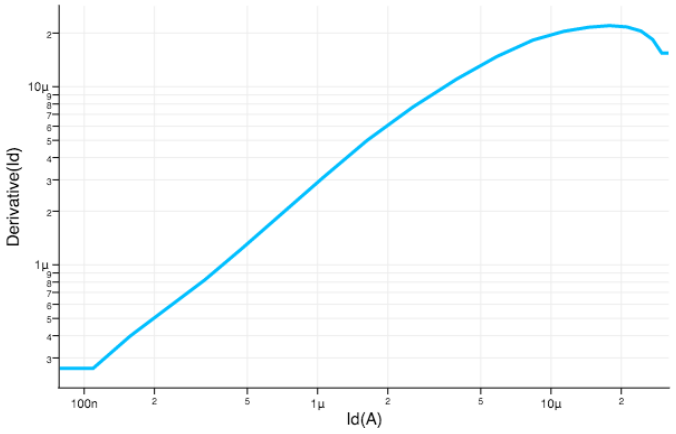

(b)

Figure 3.3:

The Id-Derivative figures indicates there is a "linear region" where gm is proportional to Id. This property implies the transconductance can be controlled in simple way. As mentioned in introduction, we may find specific bias Id for distinct elements and adjust their transconductance to a same value.

We also prove that the transconductance under this region is unaffected by the drain-source voltage variance.

By measuring two nanowire element which lie on the same wafer and are immersed

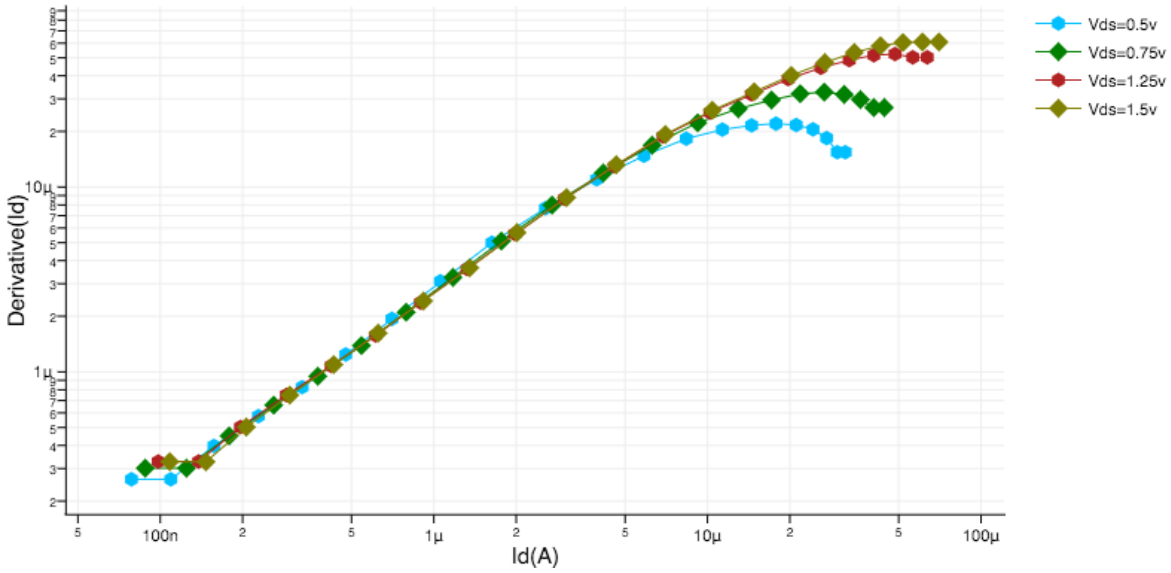

Figure 3.4: Id-transconductance with Vds variance

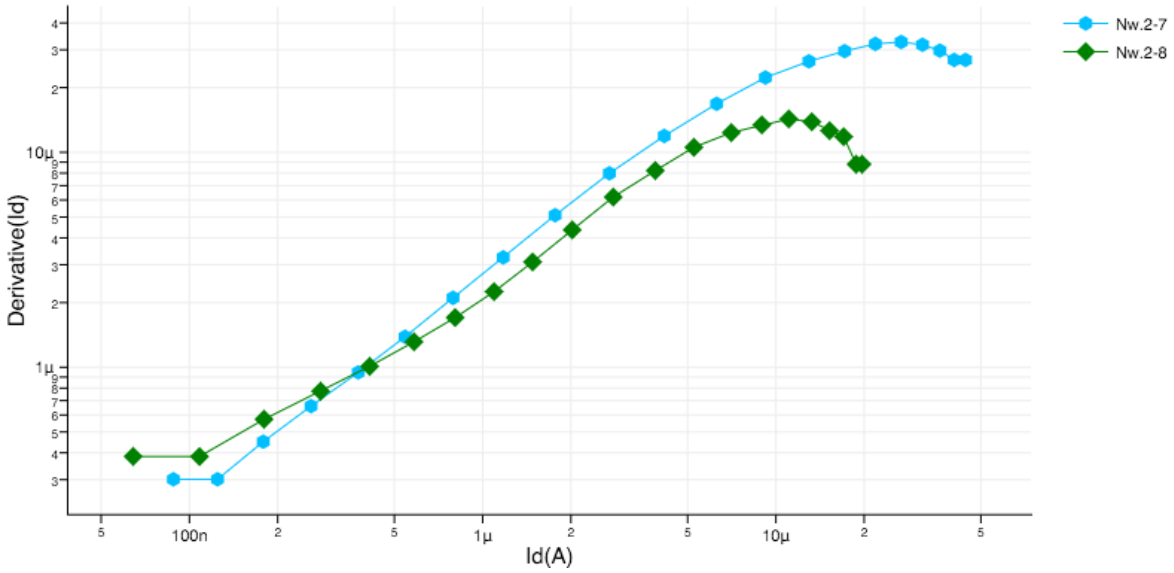

Figure 3.5: Distinct element with a line idicate they have same transconductance

with the same testing PBS solution

Chapter 4

Discrete Circuitry Design

Chapter 5

Integrated Circuitry Design

5.1 Signal Acquisition Method

Chapter 6

Discussion and Conclusions

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Acknowledgement