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碩士論文

積體化電路設計之矽基體奈米線

An Integrated Circuit Design  
for Silicon-Nanowire



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# Abstract

Poly-silicon nanowire (SiNW) is a well-studied and interesting one-dimensional nanostructure. Since it was introduced to the biosensor field in 2001, it has become a promising candidate for ultra-sensitive, real-time and label-free sensor device. Nevertheless, many physical and chemical challenges constrain nanowire from being robust and practical. Nowadays, many studies adopt the integrated-circuit techniques to solve the problems. Circuits with different design concepts and purposes are proposed to meet practical needs.

In this thesis, based on the nanowire designed by Prof.Yang (National Chiao Tong University), we design our own read-out circuit. This research first analyzes biological experiments results (From Prof.Yang) and the electrical characteristics of the nanowires. The circuit specification and design is then based on these data analysis.

The circuit is capable of performing both DC-sweep ( $I_D$ - $V_G$  sweep) and transient measurement. Moreover, we proposed a measurement method combining of these two functions. We believe this method mitigates the device variability induced by the fabrication process. Currently, most operations in this method are manual. We hope to make them automatic in the future by inducing digital circuits and constructing a system-level structure.

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# Chapter 1

## Literature Review & Theory Description

As previously mentioned in the introduction section, the read-out circuit we proposed has two operation mode (DC and AC). The DC-sweep mode control the drain current ( $I_D$ ) of nanowire while the Transient Sweep mode is for current variance measurement. Each of them refers to different sources. In section 2.1, we first talk about the reason why we perform  $I_D$ - $V_G$  sweep. Then we review the literature related to our DC-sweep mode circuit design. The literature related to the Transient Sweep mode circuit design is in section 2.2. In the last section, we discuss the two assumptions mentioned in section 1.2.

### 1.1 DC Sweep: $I_D$ - $V_G$ Curves

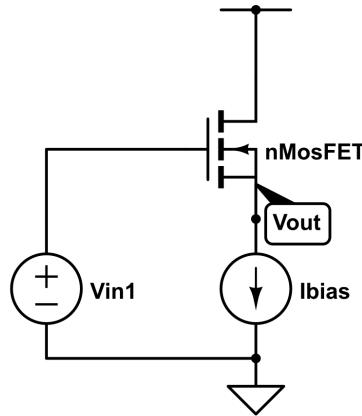
In this section, we review the knowledge and an article that is related to our design of large signal mode (DC).

#### 1.1.1 $I_D$ - $V_G$ and Transconductance

A common method for examining nanowire electrical properties is to perform DC sweep. Among all kinds of sweep method, we choose the  $I_D$ - $V_G$  in respect of the physical characteristic. In the n-type transistor, the binding of negatively charged biomolecules induces surface-near silicon ions discharged and thus increase

the threshold voltage. It is straightforward to think of these binding molecules as a voltage signal input to the gate with its value depends on the concentration. And this voltage signal effect nanowire in the same way  $V_G$  does. So by plotting  $I_D$ - $V_G$  curves, we can have a thumbnail of how concentration affects the  $I_D$ .

### 1.1.2 Source Follower



**Figure 1.1:** Sorce Follower

As one of the basic single stage amplifier, source follower (common drain) are employed to transfer voltage signal from gate to source while keeping drain current constant. The transfer function can be derived as:

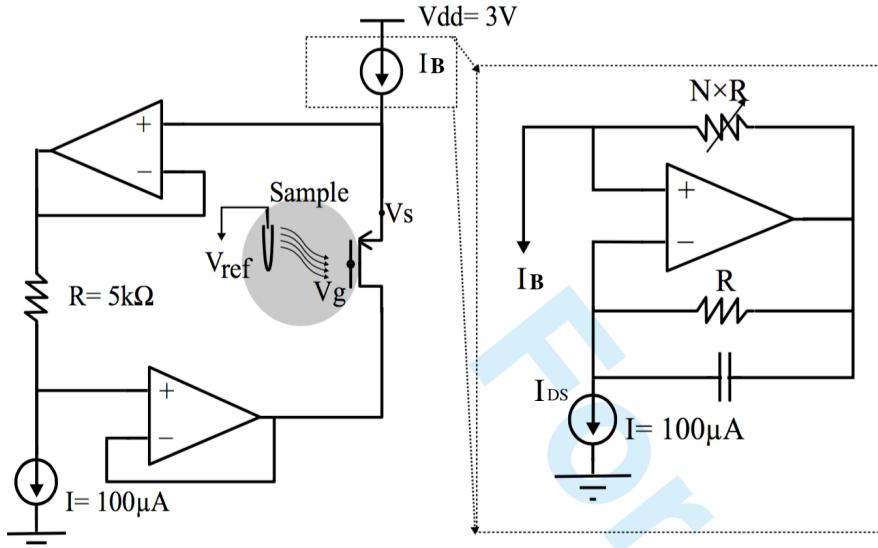
$$\frac{V_{out}}{V_{in}} = \frac{r_{ds}g_m}{1 + r_{ds}g_m} \quad (1.1)$$

$$\approx 1 \quad \text{for} \quad r_{ds}g_m \gg 1 \quad (1.2)$$

$g_m$  is the transconductance ( $\frac{\partial I_d}{\partial V_{gs}}$ ) and  $r_{ds}$  is the drain-to-source resistance. Although we have not seen the structure being applied to the nanowire, there have been several applications in the read-out circuits of ISFET (Ion-sensitive Field-effect Transistor)[9, 12] for a long time.

The read-out circuit in [9] employed ISFET as a biological transducer that converts detected bio-signals into electrical signals, which resembles our nanowire biosensor. It adopts the source follower structure as its analog front-end. The potential change induced by the biomolecules at the gate of ISFET is converted to the source. This structure requires a biasing current which needs to be stable, noiseless or wide-range

on demand. Since the biasing current is usually under micro-scale or even nano-scale, it is impractical to use an external current source. The article [9] used two resistors and an op-amp to design a current scale down circuit. As in Fig.1.2, bias current decreases in proportional to the resistance ratio ( $N$ ) as the current source circuit  $I_B$ .



**Figure 1.2:** ISFET readout circuit in [9]

The circuit in Fig.1.2 also removes the short channel effect by keeping  $V_{DS}$  at a constant value (0.5v). It adopts two op-amp based unit gain buffer to force the voltage at drain follows the source.

Attention should be paid to the impedance matching between the device-under-test (DUT) and the current source circuit. The output impedance of current source should be much larger than the input impedance of the DUT. By using nanowire as the DUT, the input impedance of it is:

$$\frac{r_{ds}}{1 + g_m r_{ds}} \quad (1.3)$$

This equation can be simplified as:

$$\frac{1}{g_m} \quad \text{for } g_m r_{ds} \gg 1 \quad (1.4)$$

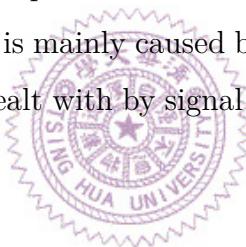
The output impedance of the current source  $I_B$  is:

$$N \times Z_{DS} \quad (1.5)$$

$Z_{DS}$  is the impedance of the current source  $I_{DS}$  in Fig.1.2. In the integrated circuit,  $Z_{DS}$  is non-ideal but usually close to the  $r_{ds}$  of a single MOSFET.

As mentioned, Eq.(1.5) should be far larger than Eq.(1.4). However,  $g_m$  is proportional to  $I_B$ , which means Eq.(1.4) is inversely proportional to N. When the biasing current decreases, the output impedance of  $I_B$  decreases while the input impedance at the source of ISFET increases. This relationship determines the current. We observed this boundary when we construct this circuit with discrete elements. These will be presented and discussed in chapter 4.

The source follower structure provides a direct signal transition method. It is a good candidate for the read-out circuit with the aim of detecting transconductance or threshold voltage variance. Nevertheless, post-processing such as amplification and filtering is necessary. The experiment results in [9] are untreated. Significant signal attenuation exists, which is mainly caused by low-frequency noise and ISFET drift [8]. The drift problem is dealt with by signal processing techniques while noise problems are left untreated.



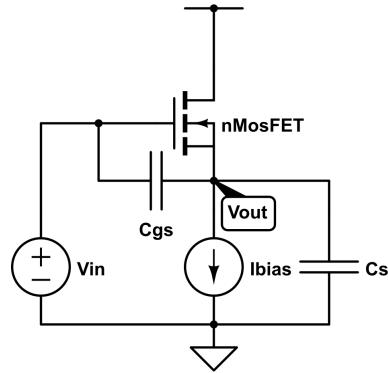
## 1.2 Small Signal (AC) Measurement Method Review

In the previous section, the source follower we mentioned exhibited compelling advantages as a signal processing structure of nano-device. However, the structure faces obstacles when being applied to the small signal detection. Parasitic capacitors and resistors can severely influence the results.

As the parasitic elements are included in figure 1.3, we modify the transfer function Eq.(1.2) as:

$$\frac{V_{out}}{V_{in}} = \frac{r_{ds}(sC_{gs} + gm)}{1 + r_{ds}(gm + s(C_{gs} + C_s))} \quad (1.6)$$

The equation can be similar to Eq.(1.2) which roughly equals to 1 as long as  $C_s$  is far smaller than  $C_{gs}$ . Unfortunately,  $C_s$  can be as large as the output of the source



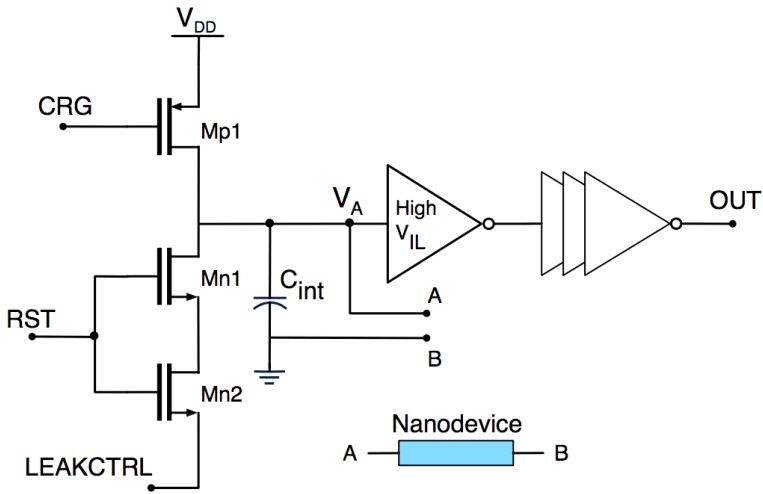
**Figure 1.3:** Sorce Follower with parasitic capacitance

follower is connected to a next stage input or a pad. In that case, the parasitic capacitors may attenuate the signal.

We want to build another circuit structure that can not only perform AC signal measurement but also disregard parasitic capacitance. We started by reviewing the works trying to measure the parasitic capacitance. Below, the works from two teams aim to measure the drain-to-source resistance ( $R_{NW}$ ) and the drain-to-source capacitance ( $C_{NW}$ ). The review focuses on the function and design theory of their read-out circuits.



### 1.2.1 RC Time Delay Measuring



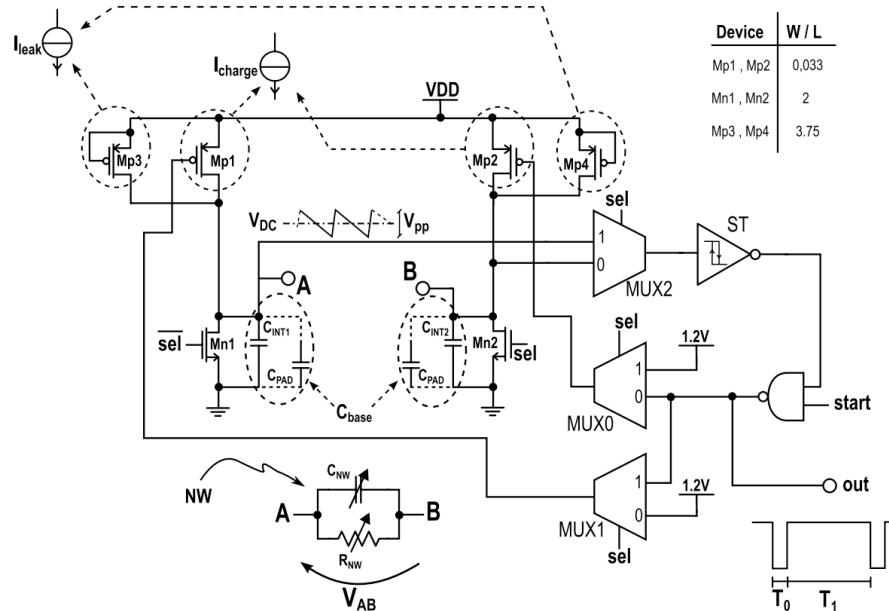
**Figure 1.4:** (a) Schematic of [2].

The measurement system for ZnO-nanowire based sensor array from [2] applies the

Time-over-Threshold technique to its read-out circuit (Fig.1.4). The circuit alternatively charges an on-chip capacitor ( $C_{int}$ ) with a constant current and discharges it through the nano-material resistance (nanowire). An inverter with its output switches from on to off when the capacitor is charged to its input threshold voltage, and vice versa. This behavior converts information of nanowire such as capacitance and resistance into time information. Both  $C_{int}$  and  $C_{NW}$  affect charging time, while the  $R_{NW}$  affect the discharging time.

The work presented in [2] does not have enough explanation of how they interpret the capacitance and resistance information. It merely mentioned that a microcontroller is responsible for the calculation. Besides, the work lacks simulation and experiment of measuring complex devices. Most of the results are the measurement a concrete resistor as the substitute for nanowire, and  $C_{NW}$  is regarded as  $0pF$ . The only nanowire experiment does not have good performance. It seems that the design may only be applied to a device with pure resistance or pure capacitance.

The recent publication [4] by the team is more elaborate and contains the measurement of complex devices (A device composed of a discrete resistor and a discrete capacitor).



**Figure 1.5:** Schematic of [4].

In Fig.1.5, nanowire appends between point A and B. The charging current can

be applied from Mp1 or Mp2, which is determined by the “sel” signal with the aid from MUXs. We simply assume sel = 1 and point B is virtually ground. (When the sel = 0, the circuit measures the device with a reversed biasing current.) Now, we can see that the circuit design concept is the same as [2]. The current charge both  $C_{int}$  and  $C_{NW}$ . When the voltage at A exceed the threshold voltage, the output switches off and causes Mp1 to turn off. (It is notable that the inverter at the output stage in [2] is replaced by a Schmitt trigger in [4]) Then the capacitor discharges through nanowire ( $r_{ds}$ ).

The bottom-right plot in Fig.1.5 defines  $T_0$  as the charging time and  $T_1$  as the discharging time. The calculation of the  $R_{NW}$  and  $C_{NW}$  can be simplified as:

$$C_{NW} = T_0 - C_{base} \quad (1.7)$$

$$R_{NW} = \frac{T_1 R_{par}}{(C_{NW} + C_{base}) R_{par} - T_1} \quad (1.8)$$

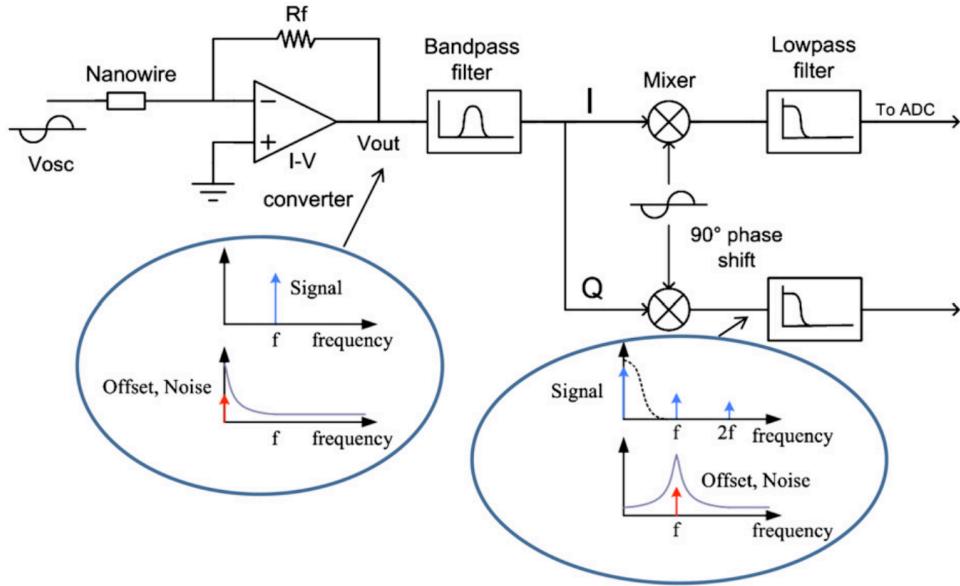
$$\text{where } R_{NW} || R_{par} = \frac{T_1}{C_{NW} + C_{base}} \quad (1.9)$$

$C_{base}$  are the  $C_{int}$  plus parasitic capacitance and  $R_{par}$  the parasitic resistance. These parasitic elements come from the transistor in the integrated circuit block such as MUX and Mp. It is notable that we do not consider the hysteresis of the Schmitt trigger here owing to simplicity.

### 1.2.2 Complex Impedance Solving

The nanowire-based hydrogen sensor measurement system in [13] adopts another method. It uses a lock-in amplifier to realize both resistive and capacitive impedance measurement.

As the previous method, it treats nanowire as a device with complex impedance. The nanowire is modeled as a resistor and a capacitor in parallel connection. The system applies a sinusoidal voltage signal to one end of the device. Another end of the device is virtually grounded by a transimpedance amplifier (TIA). The TIA then converts the current variance into a voltage output which depends on the complex impedance of the nanowire. The resistance is in the real part while the capacitance



**Figure 1.6:** Block diagram of the lock-in amplifier in [13]

is in the virtual part.

$$V_{out} = I_{NW} R_{TIA} \quad (1.10)$$

$$I_{NW} = V_{in} \left( \frac{1}{R_{NW}} + j2\pi f C_{NW} \right) \quad (1.11)$$

$f$  is the frequency of input signal.

The output of TIA is followed by a controllable bandpass filter (BP). The BP removes high-order harmonic interferences. Then the signal is demodulated. The resistive and capacitive impedance values are resolved through two channels: I and Q with their phase different by 90 degrees. A mixer which is a linear multiplier performs the demodulation. With a radio frequency (RF) input and a local oscillator (LO) input, it produce an output signal that consists of signals with frequencies  $f_{RF} + f_{LO}$  and  $f_{RF} - f_{LO}$ . Incidentally, the signal is immune to the perturbation of low-frequency noise which is a common problem for the biosensor.

### 1.2.3 Comparison and Conclusion

We compare the Method 1 (Sec.2.2.1) and Method 2 (Sec.2.2.2) here. Both of them focus on detecting the  $R_{NW}$  difference. According to the comparison table below (1.1), we can see the resistor measurement range of Method 1 is different from

Method 2 by a large extent. This is because the biasing current of nanowires that the circuits provide are limited differently. The current in Method 1 is limited by the pmos(I charge) and the leakage current. In Method 2, it is limited by the TIA. Our method adopts this TIA block and will discuss this problem in section.3.1.4.1.

Method 2 performs well when it comes to noise suppression. In fact, the circuit in Method 1 does not provide noise reduction ability. The particular structure it uses (The article [2] mentioned it as Micro-for-Nano (M4N) approach [3].) is the one responsible for that.

Method 1 has lower power consumption. However, it does not include the power of microcontroller and may be underestimated.

	[4]	[13]
R meas range	1M - 1G	10 - 40k
R meas error	< 2.5%	< 2%
C meas range	100fF - 1uF	0.5 - 1.8nF
C meas error	< 3%	< 3%
SNR	> 45dB	-
Input referred noise	-	190 nV/sqrt(Hz) @ 5 kHz
CMOS Technology	0.13um	0.18um
Power consumption	14.82uW	2mW

**Table 1.1:** Specification Summary

In our project, capacitance measurement is not our object. But we still need to consider the parasitic capacitor effect in our circuit design. Method 1 converts the resistance information into time (frequency) information. If one wants to avoid the effect of the parasitic capacitor, he should apply a  $C_{int}$  that is much larger than  $C_{NW}$ . However, it is not practical in integrated design because the chip size is limited.

Method 2 uses a TIA to measure resistance and capacitance together first and then resolves the complex value. *We can write the complex impedance value*

as:

$$\frac{R_{NW}}{1 + i2\pi f R_{NW} C_{NW}} \quad (1.12)$$

In Eq.(1.12),  $i$  is the imaginary unit and  $f$  is the signal frequency. The equation can be simplified as  $R_{NW}$  when  $i2\pi f R_{NW} C_{NW} < 0.1$ . The simplification can be applied when the signal frequency or  $C_{NW} R_{NW}$  is small enough. Thus, one needs to select the appropriate signal frequency or to determine the  $R_{NW}$  detecting range.

Another reason that makes Method 2 more attractive is that it is more flexible. One can add other analog blocks such as a noise filter or an amplifier to it.

Overall, Method 1 has the advantage in detecting range and accuracy while Method 2 has better noise suppression and flexibility.

### 1.3 Two assumption for Dealing with Disparity Problem

In chapter 1, to deal with disparity problem, we assume that:

1. The nanowire transconductance ( $g_m = \frac{\partial I_D}{\partial V_{GS}}$ ) depends on  $I_D$  and is independent of  $V_{GS}$ .
2. The changing of the biomolecule concentration can be viewed as a voltage signal input to the gate end of a transistor.

We discuss them in this section.

### 1.3.1 Transconductance and $I_D$

With the MOSFET model of weak and strong inversion, we have the  $I_D$  equations of MOSFET:

$$\text{weak inversion: } I_D = I_0 e^{\kappa V_{GS}/\phi_t} (1 - e^{-V_{DS}/\phi_t}) \quad (1.13)$$

$$= I_0 e^{\kappa V_{GS}/\phi_t} \quad \text{where } V_{DS} > 4\phi_t \quad (1.14)$$

$$\text{strong inversion: } I_D = \mu C_{ox} \frac{W}{L} ((V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2}) \quad (1.15)$$

$$= \mu C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2 \quad \text{where } V_{DS} > V_{GS} - V_{th} \quad (1.16)$$

$C_{ox}$  is the oxide capacitance and  $\mu$  is the electron mobility. Both of them depends on doping concentration.  $W$  and  $L$  are the width and length of the transistor.  $\phi_t$  is the thermal voltage depending on temperature. The  $\kappa$  is the gate coupling coefficient. To be noted that we ignore the short channel effect, which does not effect our discussion since we always keep  $V_{DS}$  constant.

We then derive  $g_m$ :

$$\text{weak inversion: } g_m = \frac{\kappa I_D}{\phi_t} \quad (1.17)$$

$$\text{strong inversion: } g_m = \sqrt{2\mu C_{ox} (\frac{W}{L}) I_D} \quad (1.18)$$

For the strong inversion, the Eq.(1.18) shows that the assumption 1 is correct.

However, the assumption is not completely right for transistor in weak inversion.

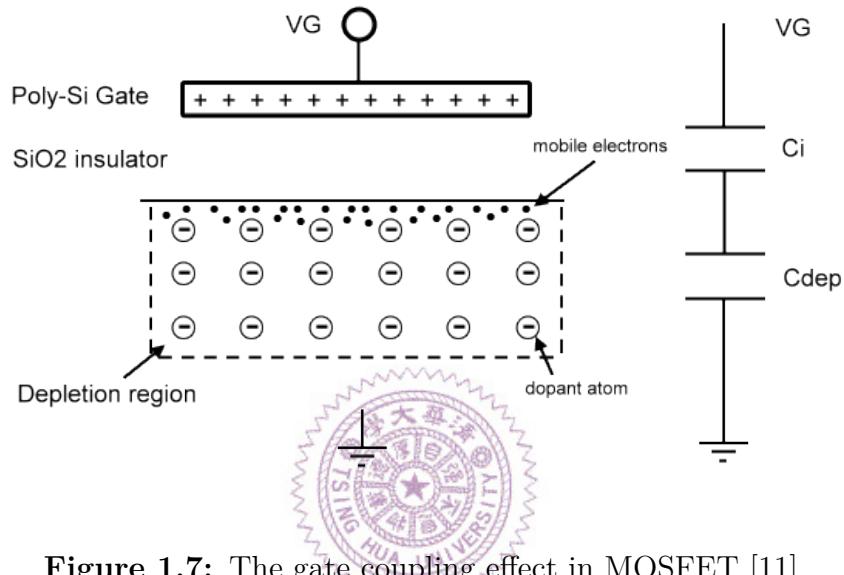
According to the Eq.(1.17), the  $g_m$  is affected not only by  $I_D$  but also by the gate coupling coefficient  $\kappa$ . *The gate coupling effect is illustrated in Fig.1.7. The  $\kappa$  is the ratio of voltage divider:*

$$\kappa = \frac{C_i}{C_i + C_{dep}} \quad (1.19)$$

*The fact that  $C_{dep}$  varies with  $V_G$  make  $\kappa$  be a non-linear parameter. Its value ranges from 0.4 to 0.9. For our nanowire, the structure is*

different from MOSFET. The  $\text{SiO}_2$  insulator in MOSFET is replaced by the solvent. According to the famous Gouy-Chapman model, the potential difference in the solution affect the double layer capacitance in solution [1]. Thus, it is still true that  $V_G$  affect  $gm$ .

Based on the experience in MOSFET, the gate coupling effect is not destructive.  $gm$  can still be approximated to. Therefore, in our circuit design, this problem is left unsolved and left for the future work.



**Figure 1.7:** The gate coupling effect in MOSFET [11]

### 1.3.2 A Simple Model for Concentration Effect

In [5], the team plot the  $I_D-V_G$  curves and study how the curve changes with the concentration of biomolecules. We observe that in the plot (Fig.1.8) with a log scale for the y-axis, curves with different concentrations exhibit the same rising trend when  $I_D$  is low ( $< 100\text{nA}$ ). Each curve seems to be different from each other by a constant shift. By applying the weak inversion current equation of MOSFET, we found that the assumption can explain this concentration effect.

$$I_{D1} = I_0 e^{\kappa(V_{GS} - V_{th})/\phi_t} \quad (1.20)$$

$$I_{D2} = I_0 e^{\kappa(V_{GS} - (V_{th} - \Delta v))/\phi_t} \quad (1.21)$$

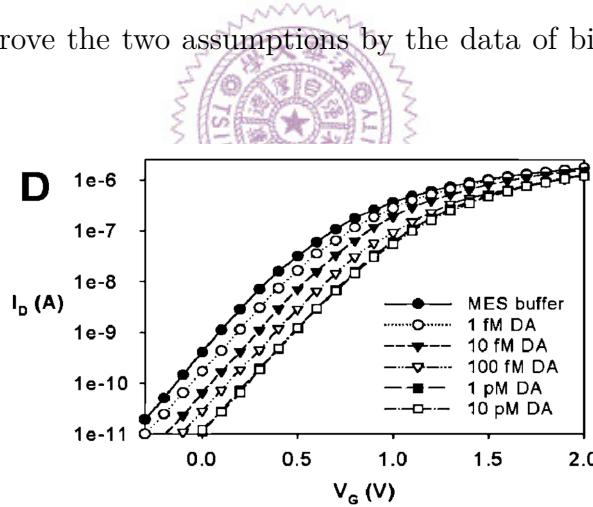
$$\rightarrow I_{D2} = f(\Delta v) \times I_{D1} \quad \text{where } f(\Delta v_g) = e^{\Delta v/\phi_t} \quad (1.22)$$

The  $I_{D1}$  and  $I_{D2}$  are the current of two nanowire devices immersed in solutions with different concentrations. The  $(\Delta v)$  is a concentration related variable we create. The Eq.(1.22) implies that when nanowire is in weak inversion region, its  $\log I_D$  difference is independent of  $V_g$ .

$$\log I_{D2} - \log I_{D1} = \log \frac{I_{D2}}{I_{D1}} = \log f(\Delta v) = \Delta v/\phi_t \quad (1.23)$$

As for the strong inversion region corresponding to the large current segments in Fig.1.8, the difference among the curves diminish as  $V_G$  increases. This is reasonable when  $V_{GS}$  is far larger than  $\Delta v$  and the concentration effect becomes ignorable.

We will further prove the two assumptions by the data of biology experiment in section.2.2.2.

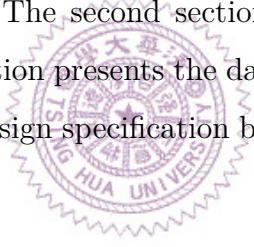


**Figure 1.8:** Concentration-dependent electric response( $I_D - V_G$ ) of biotin-modified poly-Si NWFET following biotin–streptavidin interaction.[5]

# Chapter 2

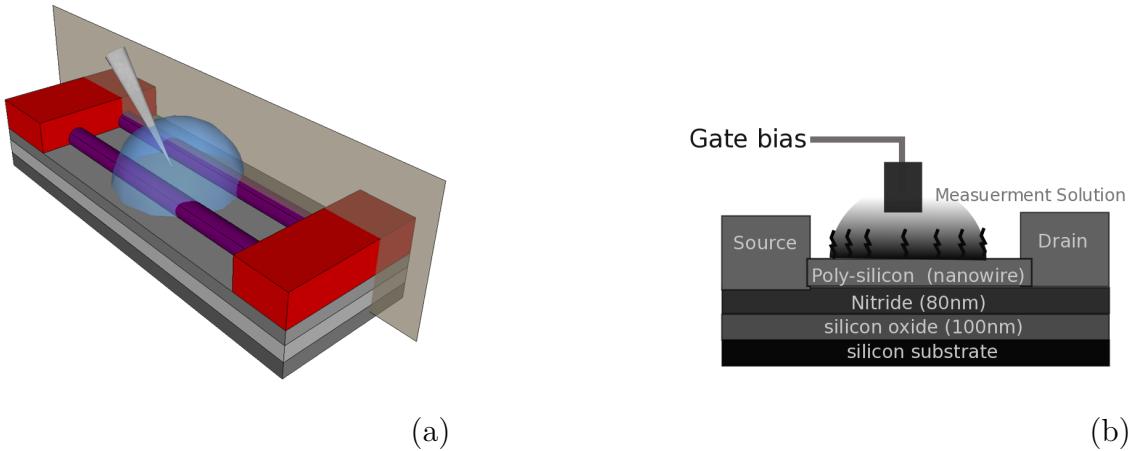
## Nanowire Structure and Measurement

In this chapter, we present the experiment data and some analysis which are the foundation of our circuit design. The first section describes briefly the silicon nanowire in our experiments. The second section analyzes the data of the biology experiments. The third section presents the data of the electrical measurement. The last section provides the design specification based on the information given by the previous sections.



### 2.1 Brief Description of Nanowire Structure

The nanowire we use is made by Prof.Yang's team (National Chiao Tong University)[6]. Fig.2.1 is the cross-sectional view of the nanowire structure. The fabrication process is based on the poly-silicon sidewall spacer technique. The n-Type doped poly-SiNW FET has two to ten poly-silicon channels. Each channel is 80nm in width and 2 $\mu$ m in length. A Large portion of the channel surface is exposed to the environment. The exposed region, through several post-process steps, captures the DNA probe and serves as the sensing site for DNA molecules.[6, 7]



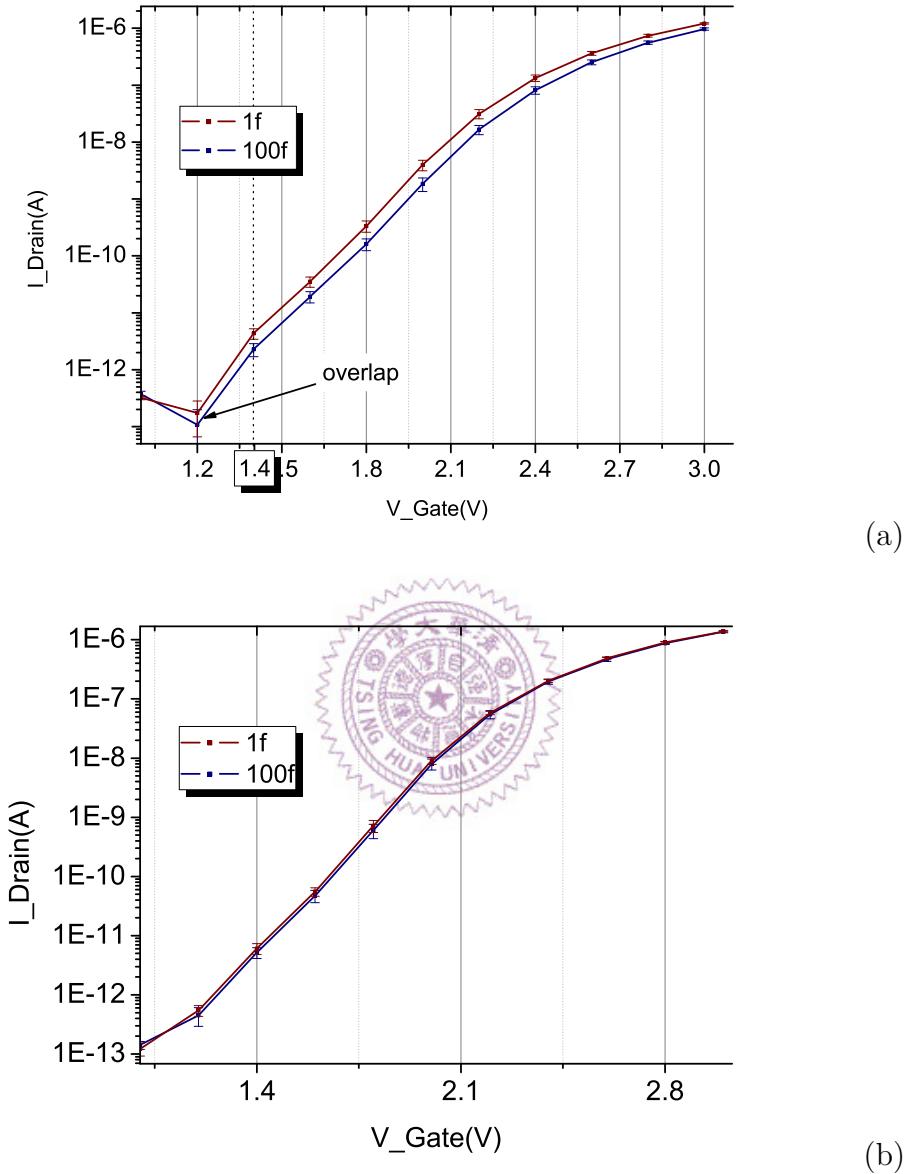
**Figure 2.1:** Nanowire Structure. (a) A nanowire device with two poly-silicon channels. (b) is the sectional view of the cutting plane in (a).

## 2.2 Biology Experiment

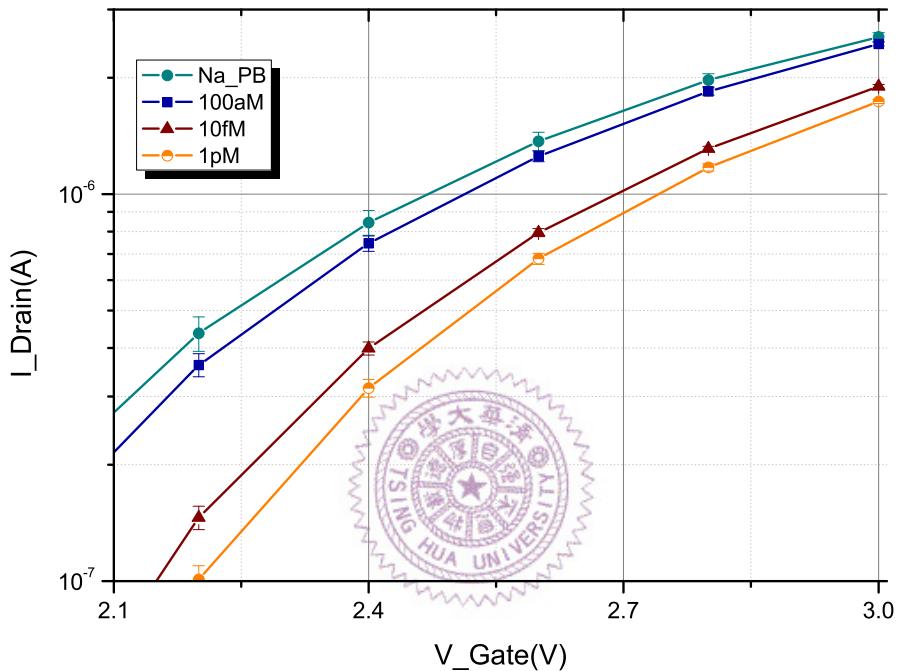
The biology experiment data are provided by Prof.Yang's team. These data are the Id-Vg measurement of the same biomolecule placed under different circumstances or with different nanowire devices. With each measurement repeated for three times, we find the mean and standard deviation (SD) of them and consider the SD value as the intrinsic noise of nanowire. We want to ensure that such noise should not be greater than the signal. To be more specific, we examine whether the Id-Vg curves of different concentrations overlap with each other or not. We present an example below:

Fig.2.2 are concentration-dependent measurements (1 femto mole(fM) and 100fM biomolecule solution) obtained with two devices ((a) and (b)). The two curves in (a) are distinguishable from each other after gate voltage is above 1.4v. They are not distinguishable in (b) since they overlap with each other. We thus assert that the device of (b) can not detect the concentration difference between 1fM and 100fM. The noise is stronger than the signal (The signal means difference in  $I_D$  caused by the concentration difference). The device of (a) can do so if it is biased at a gate voltage larger than 1.4v or a drain current larger than 1E-11.

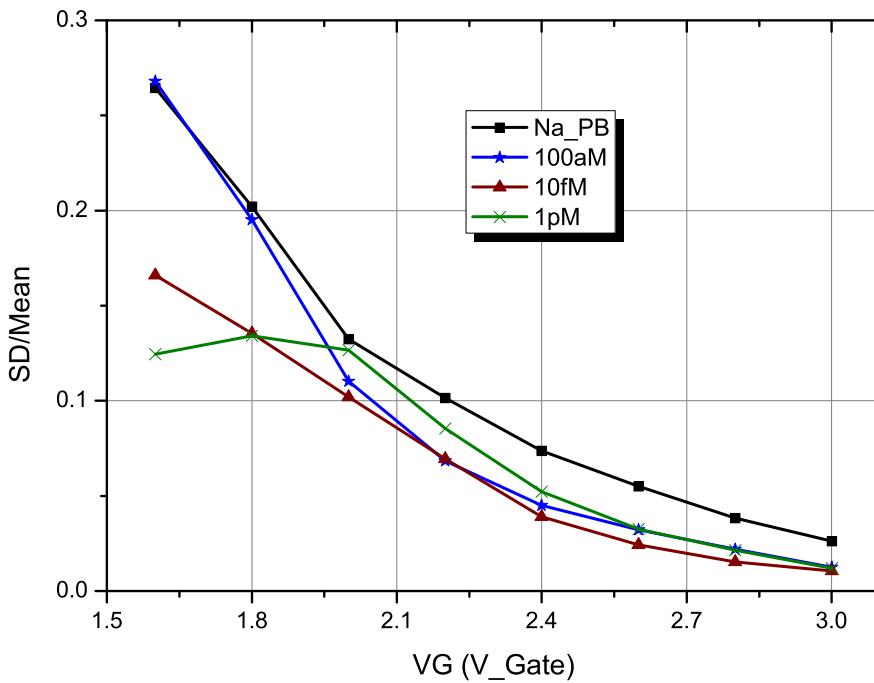
In Fig.2.3,  $I_D$  increases with the biomolecule concentration. One can find that there is only a small separation between the curve for PBS buffer and the solution containing 100aM of biomolecules. Hence 100aM should be the limit of detection.



**Figure 2.2:** Concentration-dependent  $I_D$ - $V_G$  curves of two equivalent nanowire devices. In (a), the measurement result of  $1\text{fM}$  and  $100\text{fM}$  biomolecule solution is distinguishable. There is no overlap between two curves. This is not true in (b).



**Figure 2.3:** Concentration-dependent  $I_D$ - $V_G$  curves with concentration of Na\_PB(Buffer solution only), 100aM, 10pM, 1pM. Since the biomolecule is negative-charged, the lower the concentration is, the higher the curve is. To be noticed, the 10fM curve is closer to the curve of 1pM than 100aM.



**Figure 2.4:** The normalized variation of Fig.2.3. The normalized variation is obtained by dividing SD by Mean.

It is worth noting that there is more significant difference between the curve for 100aM and 10fM than that between 10fM and 1pM. Besides, Fig.2.4 shows that the normalized variation:  $SD/Mean$  is independent of concentration. Hence, the analysis indicates that the “resolution” for detecting concentration ranging from 100aM to 10fM may be better than the that ranging from 10fM to 1pM.

### 2.2.1 Appropriate operation region

In [7], the team found that the current change ( $I_D$ ) induced by biomolecules was dependent on the applied gate voltage (VG). A device with a larger  $I_D$  change means that the device is more sensitive to the concentration difference. Thus, the team tried to find a biasing gate voltage which concentration difference can induce more  $I_D$  change.

We also want to operate the nanowire under the condition that the device has higher sensitivity. Differently, we suppose that one should find the appropriate

operation region instead of a bias range for  $V_G$ . And we take noise into consideration. The comprehensive method we proposed below proves that the nanowire should be operated in the weak inversion region adjacent to the transition region.

Our method is that we choose the operation region with more “noise tolerance”. The noise tolerance is defined as below:

$$\text{For } I_{D1} > I_{D2} \quad (2.1)$$

$$\text{Noise Tolerance} = \frac{\text{Noise Margin}}{I_{D2}} \quad (2.2)$$

$$\text{Noise Margin} = (I_{D1} - S_{D1}) - (I_{D2} + S_{D2}) \quad (2.3)$$

$I_D$  and  $SD$  are the mean and standard deviation of several  $I_D-V_G$  curves obtained in a same experimental condition. The larger the noise tolerance implies there is more space between two curves. And more space implies the less chance of overlapping that may happen between two concentration curves.

We present analysis results from three nanowire devices in Fig.2.5. Figure (a), (c), (e) are the  $I_D-V_G$  curves of three devices and Fig.2.5(b), (d), (f) are the noise tolerance respectively. One can observe in (b) and (d) that there is first a rising trend then followed by a drop as gate voltage decreases. The drop does not exist in (f) may because the measurement failed before the drop appears (The failure is because the  $I_D$  is too small to be detected.). But one can still observe the rising trend. The highest points of (b) and (d) locates in the weak inversion region and is adjacent to the transition region (The region between strong inversion and weak inversion region). We therefore suggest that in this section nanowire should have better sensitivity than other sections.

### 2.2.2 $g_m$ - $I_D$ Plot

We plot the  $g_m$ - $I_D$  curve for the data in Fig.2.3. The result in Fig.2.6 clearly proves our two assumptions for dealing with the device variability problem, which we have discussed in section 1.3.

In Fig.2.6, the  $g_m$  of nanowire is almost independent of concentration and merely depends on  $I_D$  when  $I_D$  ranges from 0.1nA to 1 $\mu$ A. In fact, the curves start splitting

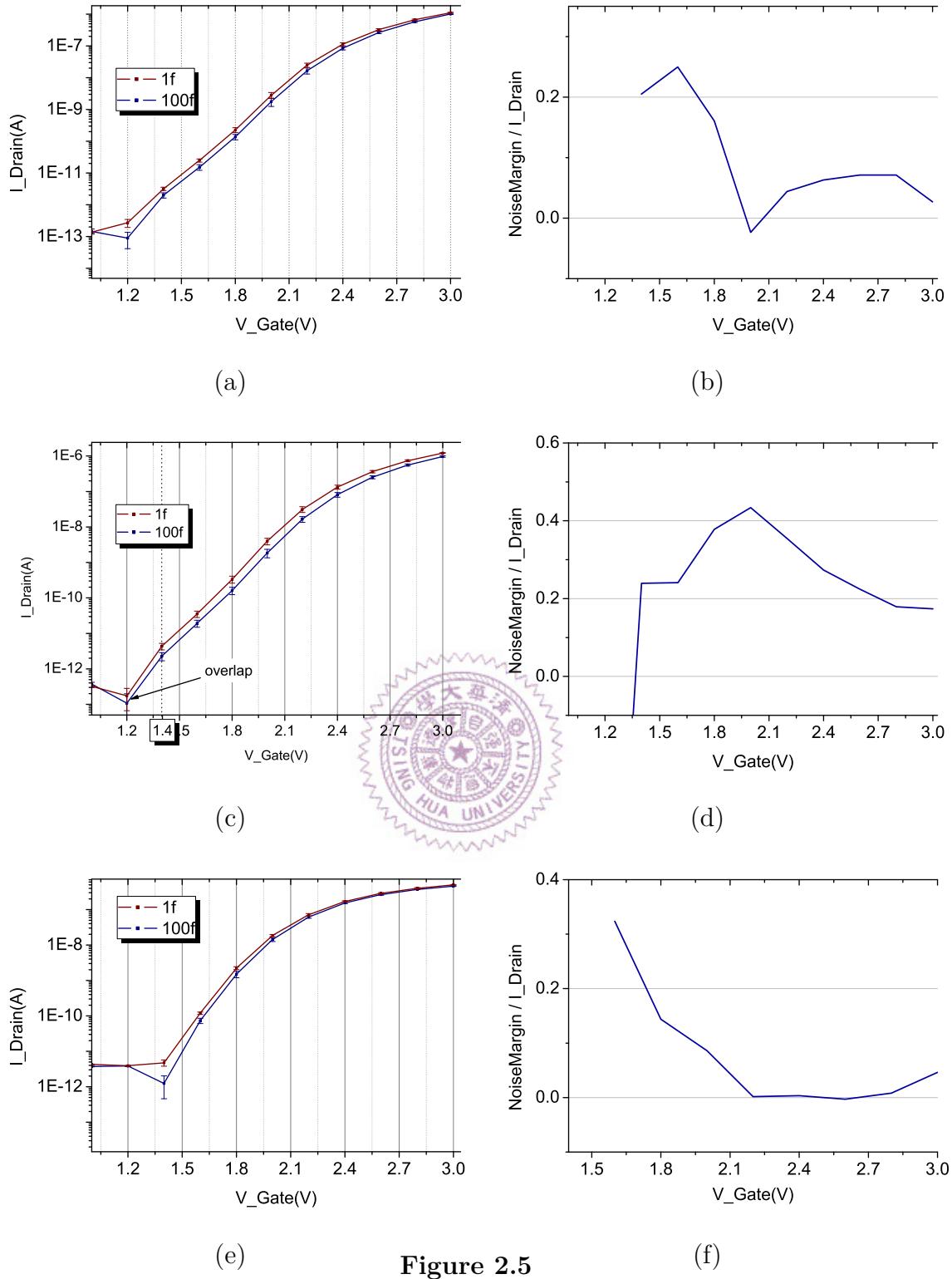
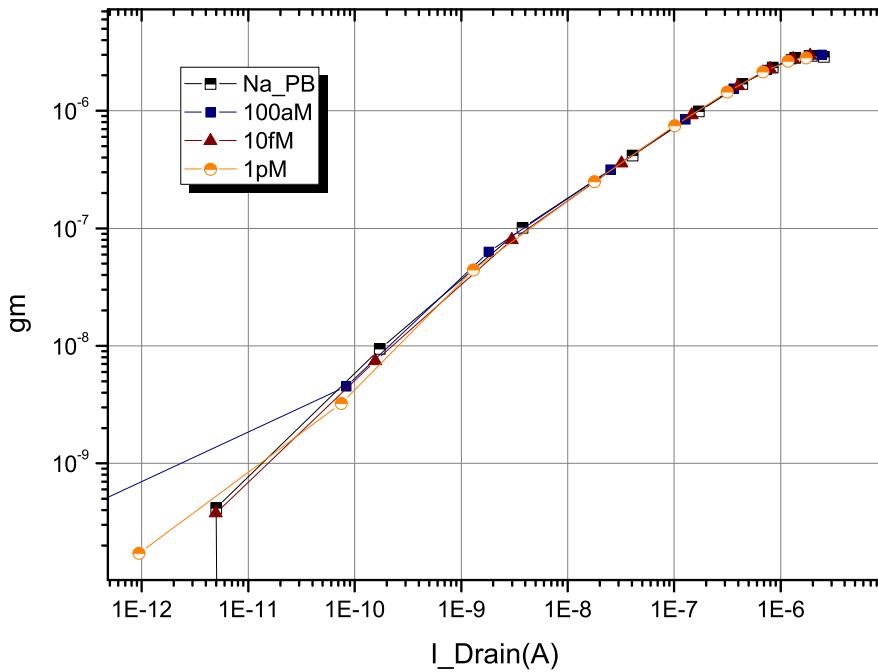


Figure 2.5

after  $I_D > 1\mu\text{A}$ . It means the device is no longer in weak inversion region but enters strong inversion region.

With the data from Fig.2.3, we may find the equivalent voltage change induced



**Figure 2.6:** The  $g_m$ - $I_D$  curve obtained by the  $I_D$ - $V_G$  curve in Fig.2.3. The curves start splitting after  $I_D > 1\mu\text{A}$  where the device may enter into strong inversion region.

by the concentration difference based on the assumption 2 (section.1.3). The values is changeable, which may depend on the gate-coupling coefficient (Eq.1.13).

Concentration Difference	Na_PB - 100aM	100aM - 10fM	10fM - 1pM
Equivalent voltage value	$30mV - 40mV$	$200mV - 280mV$	$38mV - 60mV$

**Table 2.1:** The equivalent voltage value generated by the concentration difference. We obtained the data by the data from Fig.2.6. We divided the  $I_D$  difference of different concentration by their  $g_m$  ( $\Delta I_D = g_m \Delta V_G$ ).

## 2.3 Electrical Measurements

This section presents the data analysis results. The data are obtained from our measurements with the source meter (Keithley 2602). To exclude the effect of ions,

we placed nanowire devices in the distilled deionized water instead of biomolecule solution. And there is no DNA probe on the surfaces of poly-silicon channel.

### 2.3.1 Front Gate and Back Gate

Our nanowire has two gates available: floating gate (liquid gate) and back-gate. We choose floating gate as the operation gate mainly because the floating gate can induce a larger drain current. In other words, it has higher transconductance (Fig.2.7). In our circuit design, nanowire is placed in a feedback loop where its transconductance is proportional to the loop gain (chapter 5).

There are some advantages of back-gate. One of them is the ability to lower the  $1/f$  noise [14, 10]. But this only holds for a very high gate voltage, which is not practical in the integrated circuit design.

### 2.3.2 Transconductance

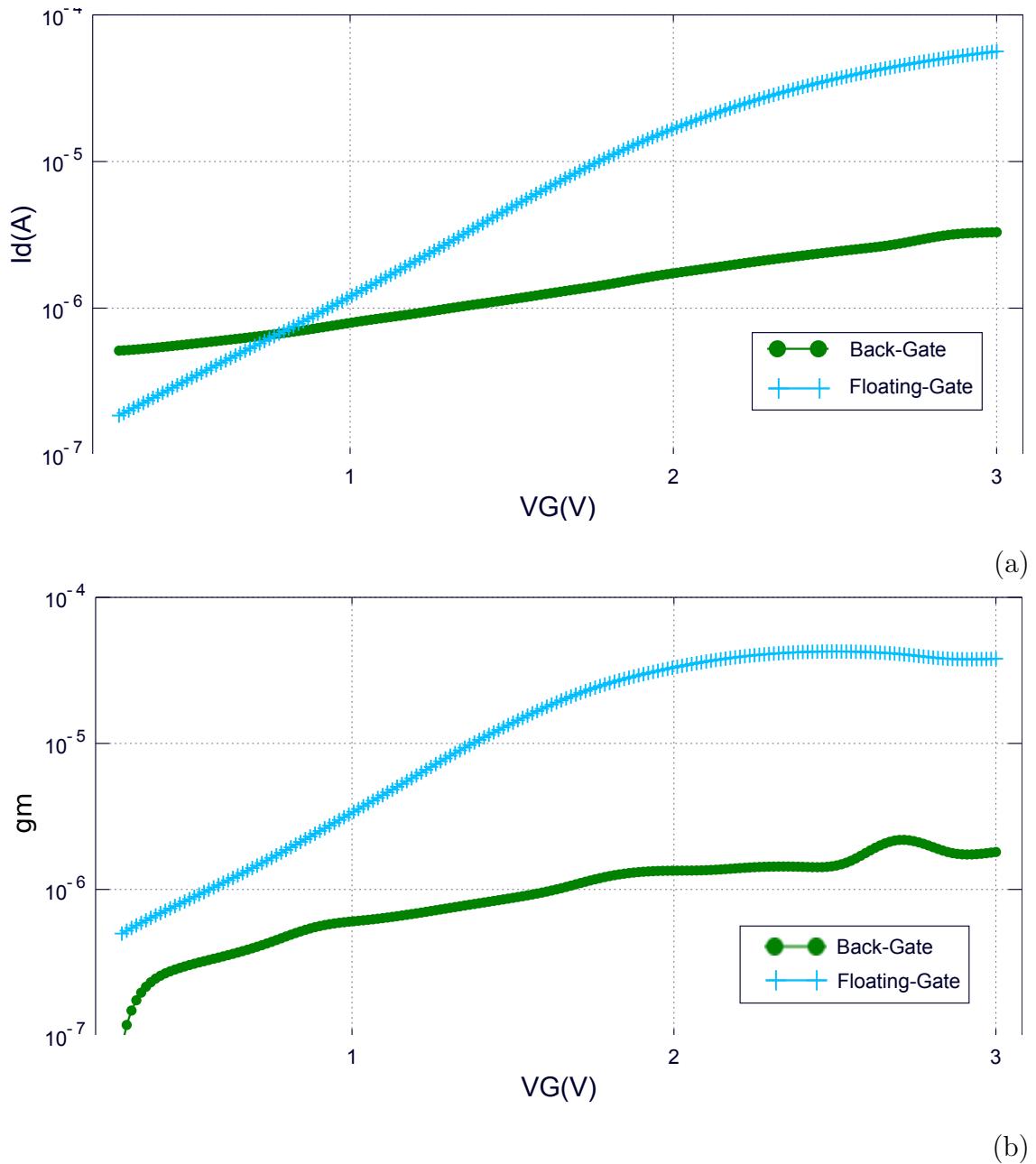
The most crucial parameter for our circuit design is the transconductance ( $g_m$ ). We acquire it by calculating the partial derivative of  $I_D$  with respect to  $V_G$ . Since in section.1.3.1 we proved that  $g_m$  is dependent on  $I_D$ , we plot the  $g_m$ - $I_D$  curve to reveal their relation (Fig.2.8(b)).

The  $g_m$ - $I_D$  plot indicates that there is a “linear region” where  $g_m$  is proportional to  $I_D$ . This corresponds to our derivation in Eq.(1.17). We can recognize that our nanowire device is operated in weak inversion region when  $I_D$  is less than  $10\mu\text{A}$ . Therefore, by the section.2.2.1, we decide the  $I_D$  of our nanowire should be operated below  $10\mu\text{A}$ .

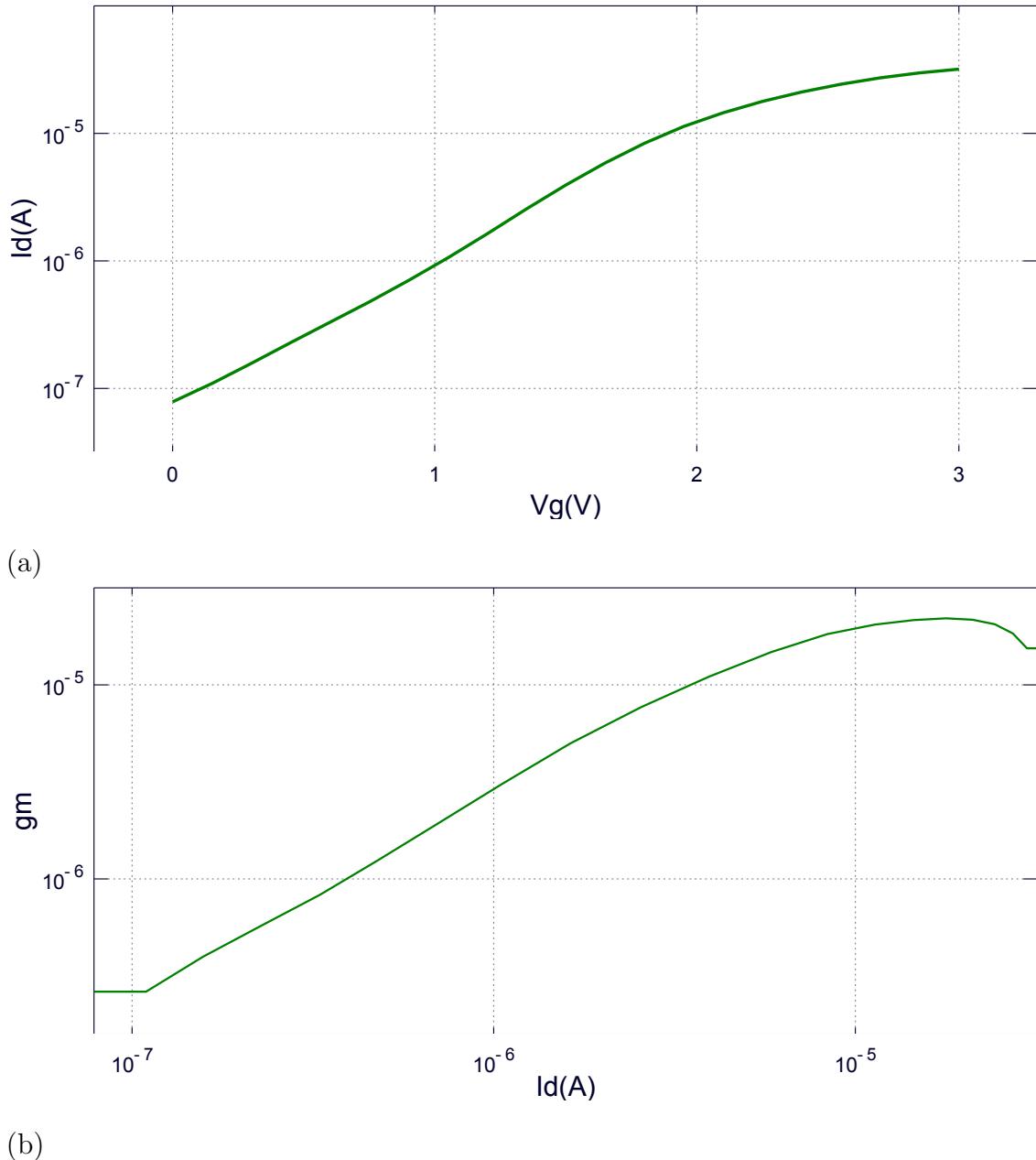
We also proved that the transconductance under this region is unaffected by  $V_{DS}$ .

### 2.3.3 Drain-to-source impedance ( $r_{ds}$ )

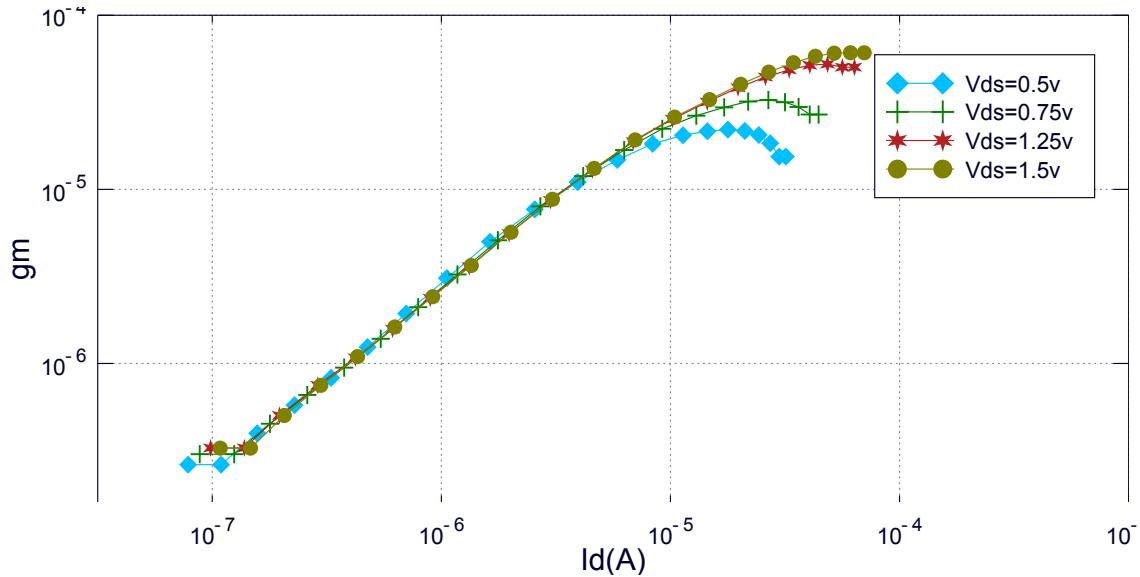
In our circuit design, we keep  $V_{DS}$  constant. According to the measurement data from Fig.2.9,  $V_{DS}$  of 0.7V is enough to keep nanowire in saturation region for  $V_G$  ranging from 0v to 3v. However, due to the fabrication variance, the value varies from 0.75v to 1v.



**Figure 2.7:** Comparison between the DC sweep of voltage on the floating gate and back gate. (a)  $I_D$  (b) Transconductance ( $g_m$ ): the derivative of  $I_D$ . The transconductance of the floating gate is larger than the back gate.



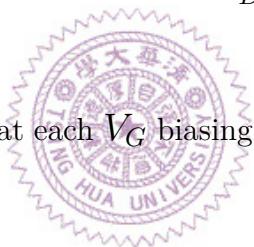
**Figure 2.8:** Electrical response of a nanowire device. (a) Sweep  $V_G$  and measure the  $I_D$  changes. And by finding the transconductance ( $g_m$ ): the derivative of  $I_D$  with respect to  $V_G$ , we plot (b) the  $g_m$ - $I_D$  curve



**Figure 2.9:**  $I_D$ -transconductance with  $V_{DS}$  variance

We concern about how  $I_D$  effect  $r_{ds}$ . The way we obtained  $r_{ds}$  is as follows:

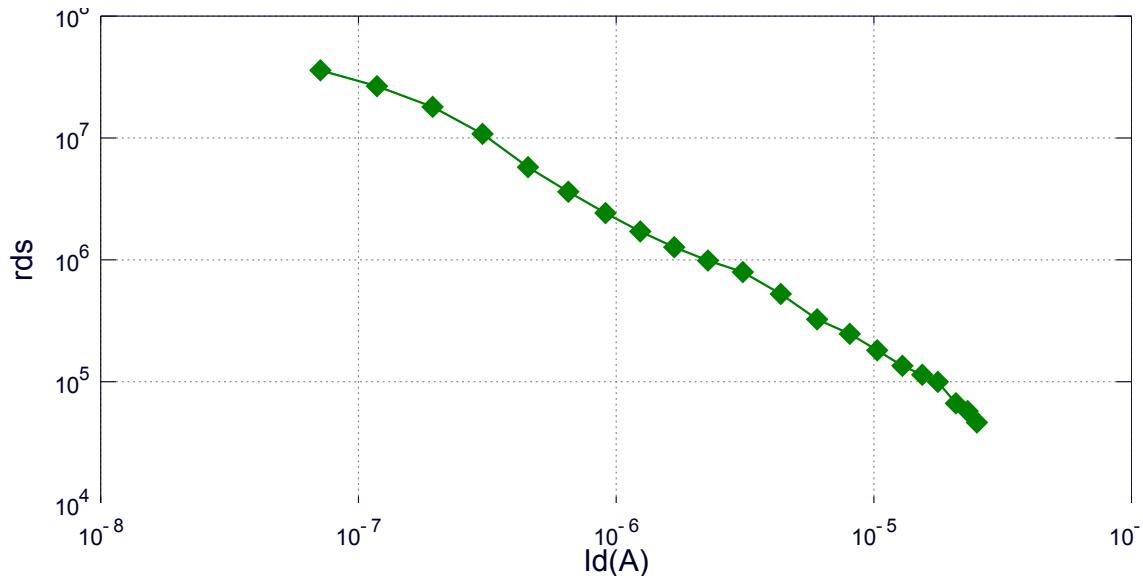
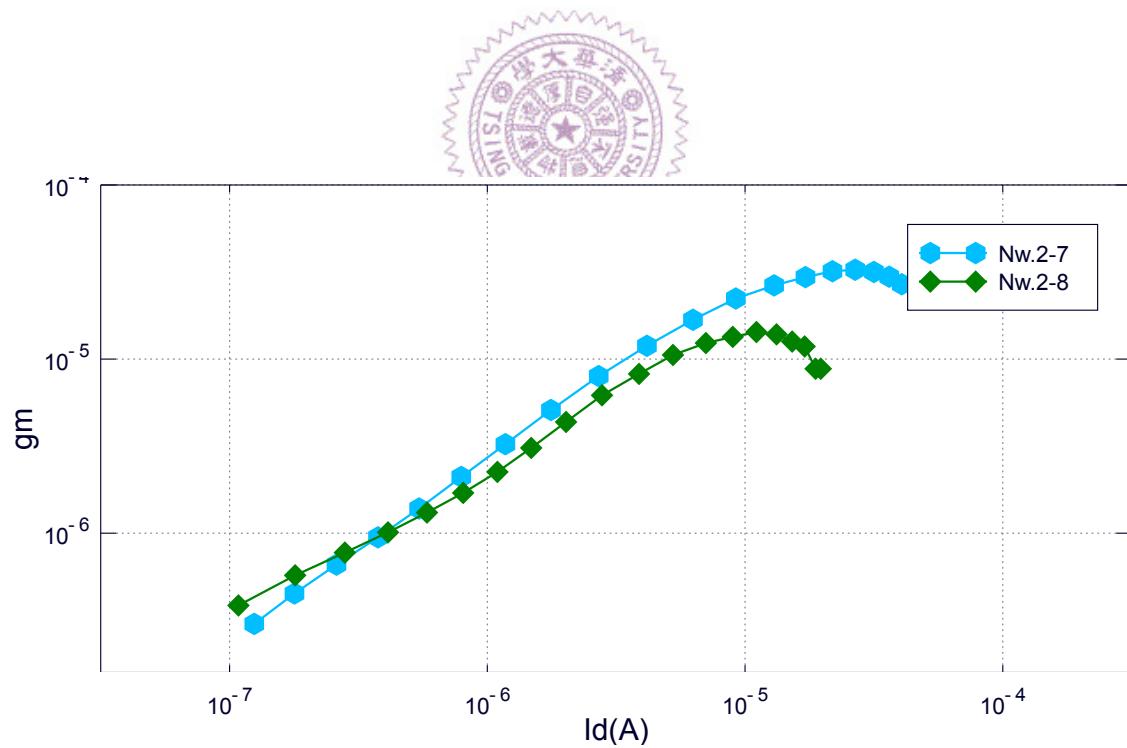
1. Perform  $I_D$ - $V_G$  sweep with two different  $V_D$ . We picked  $V_D$  values of 0.75V and 1V.
2. Find the difference of  $I_D$  at each  $V_G$  biasing point and divide it by the difference of  $V_D$ .



The result is presented in Fig.2.10. It shows that the  $r_{ds}$  is inversely proportional to  $I_D$ . Its value ranges from  $40k\Omega$  to  $30M\Omega$ . This result becomes useful when we perform the analysis of impedance matching in chapter 5.

### 2.3.4 Device variability Problem exists

We measured two nanowire devices which lie on the same wafer and are immersed with the same testing PBS solution. Below, the  $g_m$ - $I_D$  plot (Fig.2.11) shows that even the environment is same, two devices exhibit different electrical responses. *This problem causes issues such as non-uniform specification for measurement or bad quality assurance in a mass production. We try to diminish it by performing the variability-resisting measurement, which have been mentioned in chapter 1.*

**Figure 2.10:**  $I_D$ - $r_{ds}$  plot**Figure 2.11:** Device variability problem cause nanowire devices with same environment can exhibit different electrical responses.

## 2.4 Conclusion and Design Specification

Table.2.2 summarizes the electrical characteristics of our nanowire.

Operation Region	$I_D$	$V_G$	$g_m$	$r_{ds}$
Cut off	$< 100nA$	$< 0V$	-	-
weak inversion	$100nA - 10\mu A$	$0V - 2.5V$	$200n - 20\mu$	$50M\Omega - 200k\Omega$
strong inversion	$> 1\mu A$	$> 2.2V$	$20\mu - 30\mu$	$< 200k\Omega$

**Table 2.2:** Electrical characteristics. There are overlaps due to the device variability

We hence decide the design specification for the DC-sweep mode as Table.2.3.

$I_D$	$g_m$	$V_G$
$100nA - 30\mu A$	$200n - 20\mu$	$0.5V - 3V$

**Table 2.3:** Detecting specification for the DC-sweep mode

*As for the Transient Measurement mode, section.2.2.1 suggests that the device should be operated in the weak inversion region adjacent to the strong inversion region. And Table.2.1 indicates that the voltage change ( $\Delta V_G$ ) induced by concentration difference ranges from 20mV to 280mV. These factors give result to the table of device characteristics for the transient measurement (Table.2.4).*

*The design specification for the Transient Measurement mode is presented in Table.2.5.  $\Delta I_D$  is the multiplication of  $\Delta V_G$  and  $g_m$  from Table.2.4. The limitation of input referred noise (referred to the gate) is 10% of the minimal  $\Delta V_G$  ( $< 2mV$ ) or 10% of the minimal  $\Delta I_D$  ( $1\mu \times 20mV \times 10\% = 2nA$ ). The transimpedance (input current to an output voltage) is  $5M\Omega$ . This is because the minimal  $\Delta I_D$  is  $20nA$  and a transimpedance of  $5M\Omega$  allows the output voltage to be larger than 0.1V. The bandwidth is 1k Hz. The input signal  $\Delta I_D$  is a very slow signal with the speed less than 10 Hz. However, we implement a modulation method in chapter 5, which resembles the method adopted by*

[?]. The input signal is modulated to a higher frequency to avoid the low frequency noise. Thus, we determined that the bandwidth of the circuit should be at least 1k Hz.

$I_D$	$g_m$	$\Delta V_G$
600nA - 10 $\mu$ A	1 $\mu$ - 20 $\mu$	20mV - 280mV

**Table 2.4:** The summation of the nanowire characteristics when applied with the Transient Measurement mode circuit

$\Delta I_D$	Input Referred Noise (referred to $V_G$ )	Input Referred Noise (referred to $I_D$ )	Transimpedance Gain (max)	Bandwidth
20nA - 2.8 $\mu$ A	< 2mV	< 2nA	5E6( $\frac{V}{A}$ )	> 1k (Hz)

**Table 2.5:** Specification for the Transient Measurement mode circuit



# Chapter 3

## Integrated Circuitry Design

This chapter presents the design of the read-out circuit and the post-simulation results.

### 3.1 Fronted Circuit Design

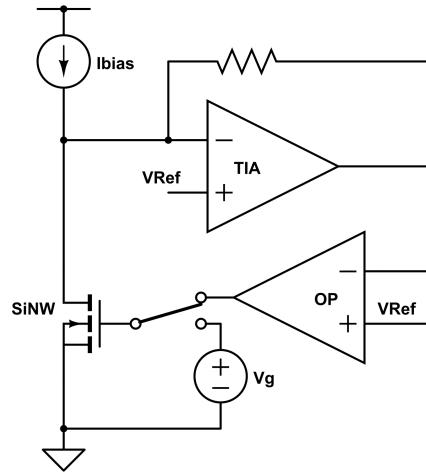
The review of the source follower in section.1.1.2 suggests the constant current method for the circuit of DC-sweep mode. The data analysis from chapter 3 supports it by the linear relation between  $I_D$  and  $g_m$ . However, section.1.2 shows that source follower is not suitable for transient measurement. It alternatively recommends the circuit in Fig.1.6 which measures the transient current signal and converts it into a voltage output.

The fronted circuit combined these two methods into one circuit structure with two modes available: the DC-sweep mode and the Transient Measurement mode.

#### 3.1.1 The DC-sweep mode

Fig.3.1 is the fronted circuit operated in the DC-sweep mode. The switch turns the circuit into the DC-sweep mode by connecting the output of OP with the gate of nanowire.

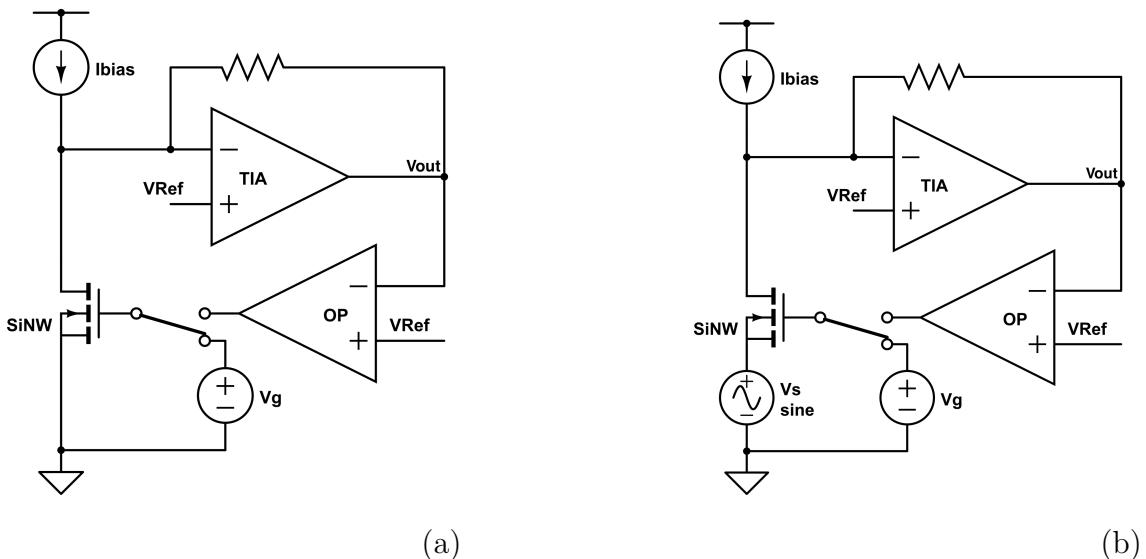
As in the source follower, our circuit contains a biasing current source (Ibias) for controlling the  $I_D$ . The difference is that the Ibias inputs the current into drain instead of source. In addition, we employs the transimpedance amplifier (TIA) from



**Figure 3.1:** The fronted circuit operated in DC-sweep mode.

section.1.2 ([13]). Its output is connected to an OP amplifier to form a negative feedback loop. When  $I_D$  is less than Ibias, the output voltage of TIA falls and the gate voltage  $V_G$  rises to increase  $I_D$ . On the contrary, output voltage of TIA rises and the gate voltage ( $V_G$ ) drops if Ibias is smaller than  $I_D$ . Finally, the feedback mechanism forces  $I_D$  to be the same as Ibias by adjusting  $V_G$  automatically.

### 3.1.2 Transient Measurement mode



**Figure 3.2:** Two usage ((a), (b)) of the fronted circuit operated in Transient Measurement mode.

In Fig.3.2(a), the switch turns to a simple voltage source ( $V_g$ ) that provides a constant gate voltage. The feedback OP is nonfunctional in this mode. When performing measurement, we directly find how the output voltage ( $V_{out}$ ) changes with the biomolecule concentration. This output voltage will be sent into a second stage circuit for further amplification.

**Another Usage of Transient Measurement mode** There is another method to perform measurement with the Transient Measurement mode, which resembles the measurement in [13]. This method measures the  $g_m$  of the nanowire. As shown in Fig.3.2(b), a sinusoidal signal with an amplitude of  $v_s$  is sent to the source of the nanowire. The output response ( $V_{out}$ ) is a sinusoidal signal at the same frequency with an amplitude equaling to  $v_s g_m \times R_{TIA}$ . The values of Ibias and  $V_g$  can be arbitrary. But one need to be aware that their values should not cause the output of TIA or the second-stage circuit to saturate.

### 3.1.3 Dealing with the device variability Problem

As mentioned in chapter 1, we combine the DC-sweep mode and Transient Measurement mode to perform a variability-resisting measurement.

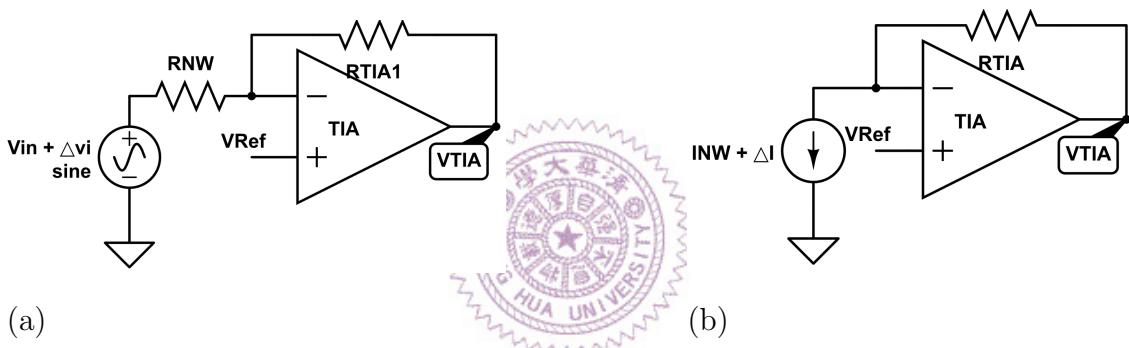
**Method Procedure** Assuming there are two nanowire devices and the device variability problem exists between them. Initially, we use these element to perform the  $I_D-V_G$  sweep in the DC-sweep mode. We use the DC-sweep results to find the  $g_m$  of each device. ( $g_m = \frac{\partial I_D}{\partial V_G}$ ) When we turns to the Transient Measurement mode, we bias these two devices under the same  $g_m$  by setting Ibias and  $V_g$  correspondingly. After the buffer solutions, the same voltage difference at the output ( $V_{out}$ ) should be detected because the two devices have the same  $g_m$ . Before a new solution is added, we return to the DC-sweep mode again. This is for finding the new biasing  $V_G$  to reset their  $I_D$  to be the same as Ibias. This implies that every time when we enter the Transient Measurement mode, the devices always have the same  $I_D$  and  $g_m$  as those in the beginning of experiments.

### 3.1.4 Design Description

In this section, we first talk about the TIA block and focus on how we improve the detecting limits of this block. It is followed by the design of the TIA circuit. Then we analyze the feedback mechanism of the DC-sweep mode and the input impedance of the circuit. After that, we discuss the stability issue. Finally, we show the design of the feedback OP block.

#### 3.1.4.1 Strategies for lowering current detecting limits

The TIA subcircuit in section 1.2.3 is shown as Fig.3.3(a), we mentioned that the detecting range of  $R_{NW}$  is limited by  $I_{NW}$  provided by the TIA. We now discuss the causes of the upper and lower limits, and show the strategies we use to improve them.



**Figure 3.3:** (a) The transimpedance block (TIA) of the read-out circuit from [13]. The circuit input a voltage signal into resistive nanowire element  $R_{NW}$ . To compare it with our circuit (Fig.3.4), we transform the voltage input into an equivalent current input in (b). The  $I_{NW} = (V_{Ref} - V_{in})/R_{NW}$  and  $\Delta i = \Delta vi/R_{NW}$

**Lower Limit:** In Fig.3.3(b), the TIA output voltage is:

$$V_{TIA} = V_{Ref} + I_{NW}R_{TIA} + \Delta iR_{TIA} \quad (3.1)$$

Two reasons relate to a large offset current  $I_{NW}$ . One is that the output current provided by the TIA is restricted by design. The other is that the restriction of the current flowing through the resistor  $R_{TIA}$ :

$$\frac{V_{Ref} - V_{SS}}{R_{TIA}} < I_{NW} < \frac{VDD - V_{Ref}}{R_{TIA}} \quad (3.2)$$

Both reasons lead to the output saturation of TIA.

A naive way to handle the first one is to increase the maximum output current the TIA can provide. The disadvantage of this method is the increase in power consumption and chip area. As for the second one, using smaller  $R_{TIA}$  can release the restriction on  $I_{NW}$ . Unfortunately, this is unpreferable because it reduces the current-to-voltage gain of the TIA.

Our strategy for decreasing the lower limit is to utilize the biasing current source ( $I_{bias}$ ) of nanowire. As shown in Fig.3.4, Eq.(3.1) is transformed into:

$$V_{TIA} = V_{Ref} + (I_{NW} - I_{bias})R_{TIA} + \Delta i R_{TIA} \quad (3.3)$$

Now we can diminish the large  $I_{NW}$  by  $I_{bias}$ .

In conclusion, the large offset current causes the saturation of the output of TIA. We use the biasing current source to diminish that offset current, so as to increase the detection range.

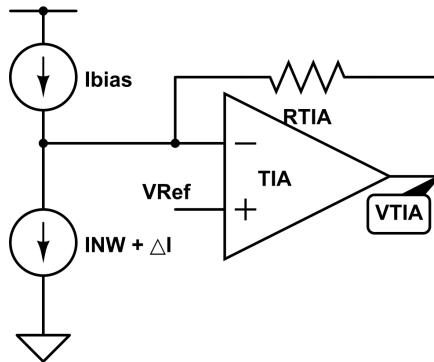
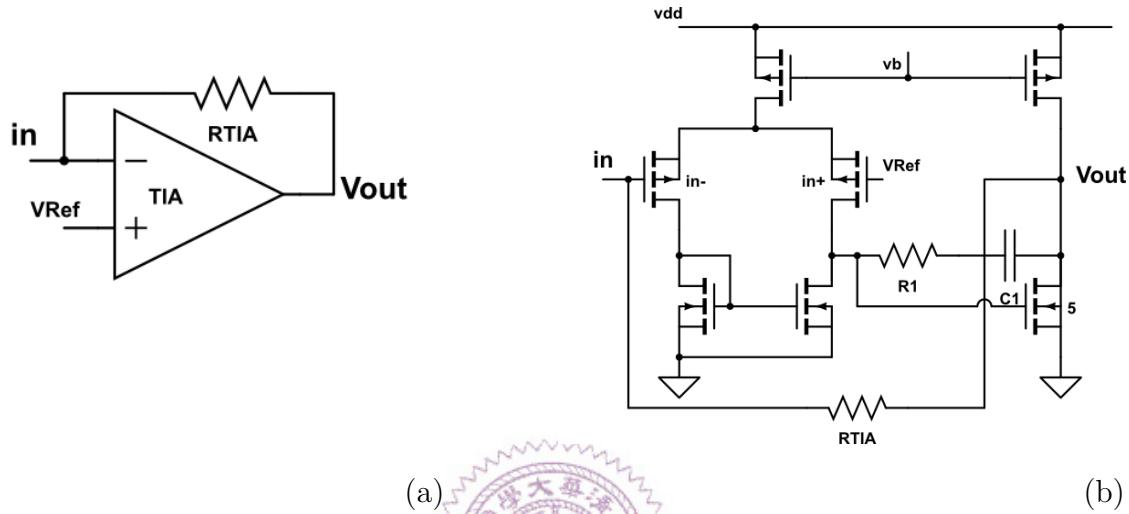


Figure 3.4

**Upper Limit:** The upper limit depends on the output resolution. When the input current signal  $\Delta i$  in Fig.3.4 is too small, the output response may be defeated by the noise. This may be solved by increasing the SNR through a larger  $R_{TIA}$ . However, the chip area constrains the size of resistors. In our circuit design, it is hard to make a wide linear range resistor with resistance value out of  $100k\Omega$ . Furthermore, even if the resistor can be greater, one need to concern for the noise brought by the large resistance.

Our strategy is to boost the SNR of TIA by designing its input MOSFETs with a large area. We also amplify the output signal through the second-stage circuit.

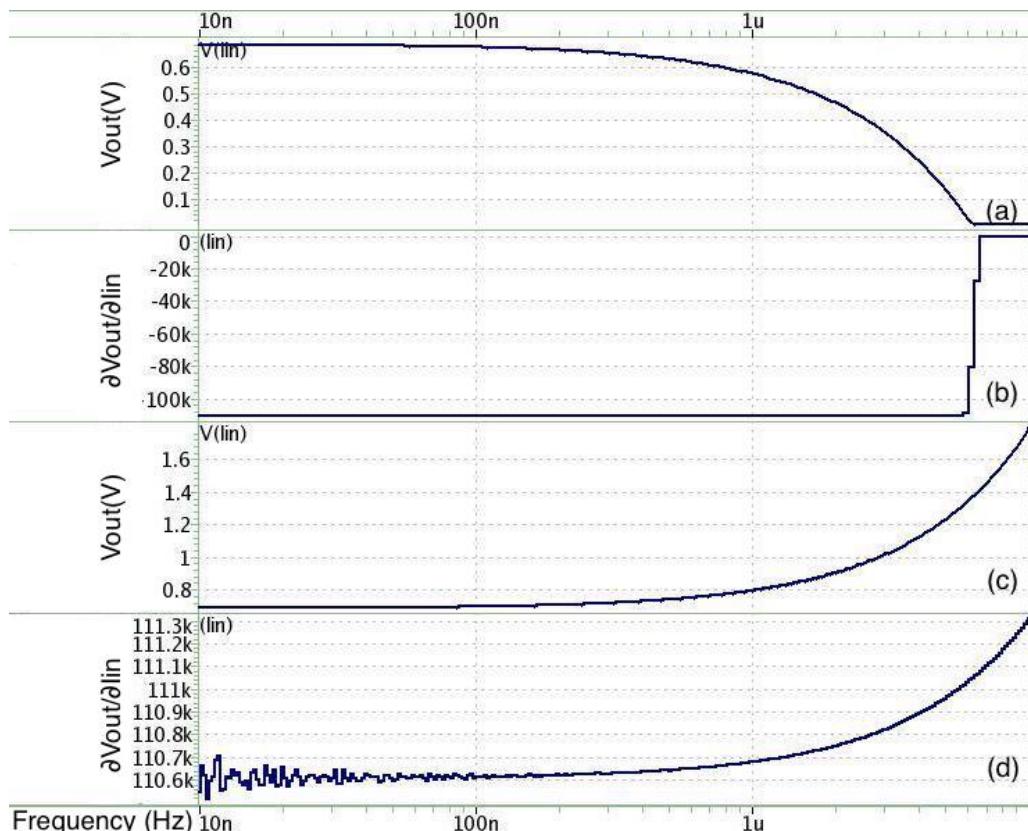
### 3.1.4.2 TIA (Transimpedance Amplifier) Design



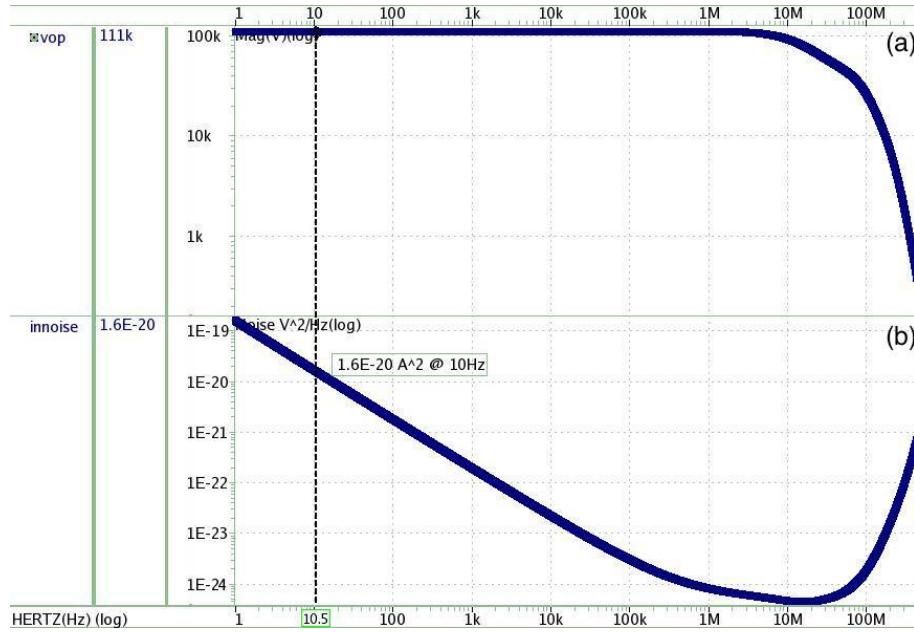
**Figure 3.5:** (a)The transimpedance block and the (b) schematic

*Fig.3.5 shows the Transimpedance Amplifier circuit. We implement the operational amplifier in TIA with the two-stage, differential-pair structure. This simple structure has merits such as large output current and wide output voltage range.*

*Fig.3.6 and Fig.3.7 are the dc and ac post-simulation of the TIA. Fig.3.6 shows that the TIA has a constant transimpedance of  $100k\Omega$  when the input current range is  $6\mu A \sim -10\mu A$ . Fig.3.7(a) indicates that the bandwidth is  $7MHz$ . Fig.3.7(b) is the input referred noise (referred to the gate of nanowire). In Table.3.1, these three parameters are compared with the specification given by Table.2.5. Other results such as biasing current, spec. of  $OP$  ... etc. are also provided in it.*



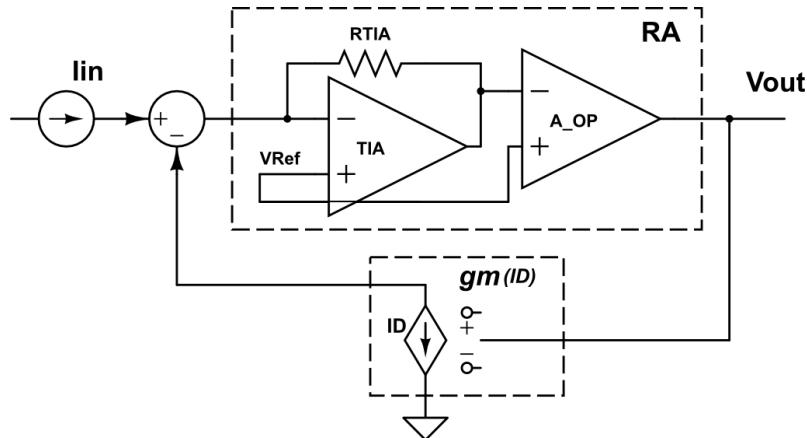
**Figure 3.6:** The dc simulation results of TIA. The x-axis represents positive/negative input current (log scale). (a) is the  $V_{out}$  responding to the positive input current while (c) is to the negative input current. (b) and (d) are the derivative of  $V_{out}$  of input current ( $\frac{\partial V_{out}}{\partial I_{in}}$ ) from (a) and (c) respectively.



**Figure 3.7:** The ac simulation results of TIA. The x-axis is the input signal frequency. (a) is the  $V_{out}$  and (b) is the input-referred noise.

VDD	3.3V	
Biasing Current	$35\mu\text{A}$	
Transimpedance	$100k(V/I)$	
<b>Closed loop</b>		
	Post-simulation	Spec. from Table.2.5
Input Current range	from $6\mu\text{A}$ to $-10\mu\text{A}$	$\pm 20n\text{A}$ - $2.8\mu\text{A}$
Output Voltage range	$0.1V$ - $2.8V$	-
Bandwidth	7M Hz	1k Hz
Input referred noise (@10Hz)	$0.13n\text{A}$	$< 2n\text{A}$
<b>Open loop</b>		
Output dynamic range	$0.1V$ - $3.1V$	
Phase Margin	103 (degree)	
PSRR	$60dB$	
CMRR	$123dB$	
ICMR	$0.1V$ - $2.6V$	

**Table 3.1:** Post-simulation result of TIA



**Figure 3.8:** Block diagram of the DC-sweep mode. The  $I_{in}$  refers to the Ibias and  $V_{out}$  refers to the output voltage of OP, which is also the gate voltage of nanowire (Fig.3.1). The  $gm(I_D)$  is the transconductance of nanowire whose values depends on  $I_D$ .

### 3.1.4.3 Feedback Mechanism

The DC-sweep mode circuit forms a negative feedback loop. Fig.3.8 is the block diagram of the circuit.

From the block diagram, we can compute the loop gain ( $LG$ ) and the transfer function ( $TF$ ):

$$R_A = R_{TIA} \times A_{OP} \quad (3.4)$$

$$LG = R_A \times g_m \quad (3.5)$$

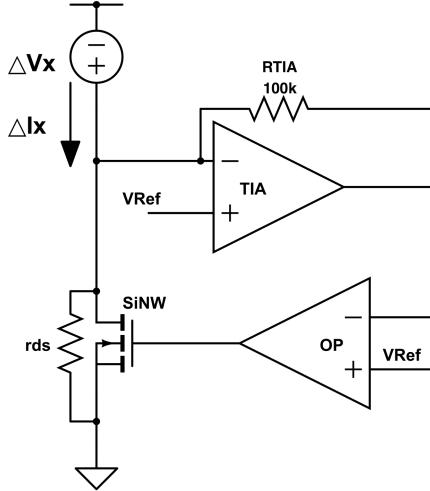
$$TF = \frac{V_{out}}{I_{in}} = \frac{R_A}{1 + LG} \quad (3.6)$$

$$\approx \frac{1}{g_m} \quad \text{If } LG \geq 100 \quad (3.7)$$

The transfer function suggests that if we want to obtain an  $I_D-V_G$  sweeping curve with an error less than %1, our loop gain should be greater than 100. According to chapter 3, the specification for  $g_m$  detection ranges from  $200n$  to  $20u$ . This implies that  $A_{OP}$  should be at least greater than 5k. We will show in the next section that the  $A_{OP}$  in the post-simulation is 10k.

### 3.1.4.4 Input Impedance (DC-sweep mode)

In chapter 4, we have discussed the impedance matching between the current source and the nanowire device. Here we compute the input impedance of the circuit.



**Figure 3.9**

In Fig.3.9, we apply an input voltage  $\Delta v_x$  and find the  $\Delta i_x$ . The input impedance of the circuit is  $\Delta v_x / \Delta i_x$ .

$$\Delta I_x = \frac{\Delta V_x}{r_{ds}} + I_{SiNW} \quad (3.8)$$

$$I_{SiNW} = \frac{\Delta V_x}{r_{ds}} LG \quad (3.9)$$

$$\rightarrow \Delta I_x = \frac{\Delta V_x}{r_{ds}} + \frac{\Delta V_x}{r_{ds}} LG \quad (3.10)$$

$$\rightarrow \frac{\Delta V_x}{\Delta I_x} = \frac{r_{ds}}{1 + LG} \quad (3.11)$$

$$\text{where } LG = R_{TIA}A_{OP}g_m \quad (3.12)$$

The  $A_{OP}$  is the gain of the feedback OP. The  $r_{ds}$  is the drain-to-source resistance of nanowire, which is larger than  $100k\Omega$ .

*The OpAmp of TIA holds the gain of 1000 (60dB), which makes the  $Z_{in}$  of 100. The LG is greater than 5k from the last section. By the section.2.3.3, the  $r_{ds}$  ranges from  $40k\Omega$  to  $30M\Omega$ . Thus, the maximal input impedance of the feedback circuit is  $6k\Omega$  ( $\frac{30M\Omega}{5k\Omega}$ ). In our design, the Ibias is a simple pmos. Its output impedance ranges from  $1M\Omega$  to*

$1G\Omega$ , which is much larger than the input impedance of the feedback circuit. Therefore, the impedance matching is fine.

### 3.1.4.5 Stability and Feedback OP Design

To decide the structure of the feedback OP, we must discuss the stability of the feedback loop in the DC-sweep mode. The OP plays a crucial role in the stability issue because it not only decides the loop gain but also contains the dominant pole at its output.

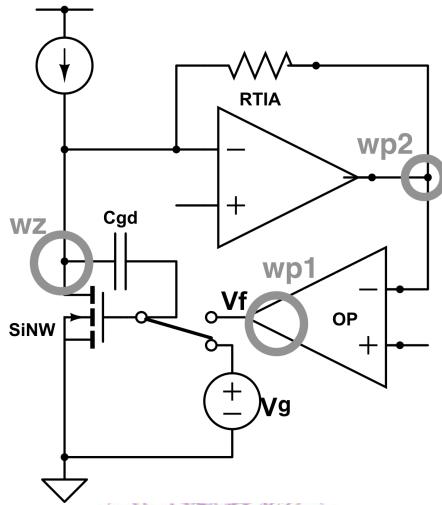


Figure 3.10

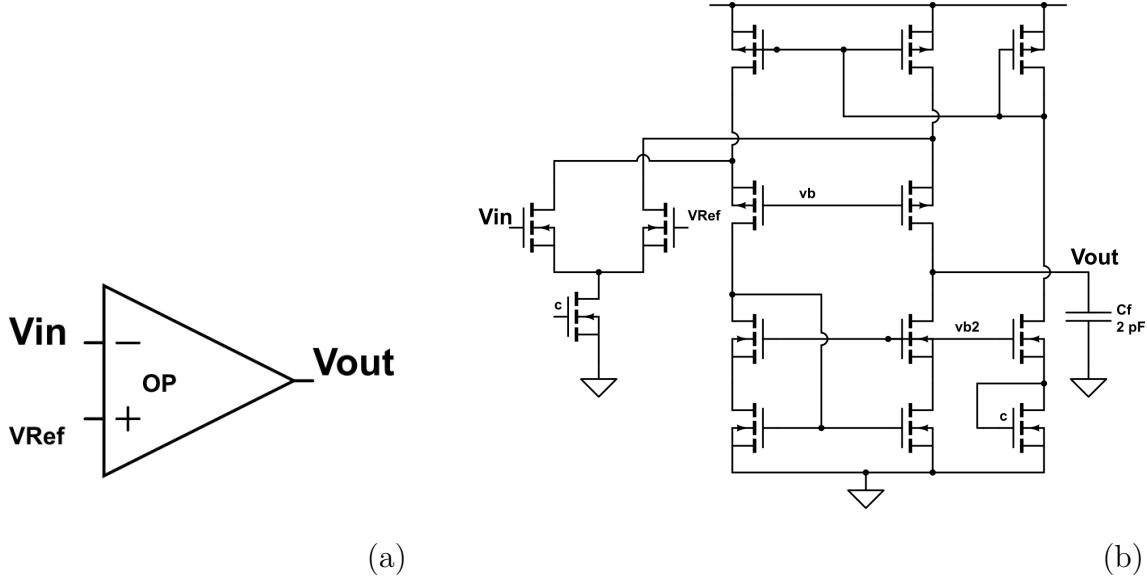
In Fig.3.10, we mark the dominant pole ( $w_{p1}$ ), second order dominant pole  $w_{p2}$ ) and the zero ( $w_z$ ). We can write the loop gain as:

$$\frac{v_f}{v_g} = R_{TIA} \times A_{OP} \times g_m \frac{1 - s/w_z}{(1 + s/w_{p1})(1 + s/w_{p2})} \quad (3.13)$$

$$w_z = \frac{g_m}{C_{gd}} \quad (3.14)$$

The parasitic capacitance  $C_{gd}$ , at the conservative estimate, has a maximum value of  $1pF$  (The estimation is based on the fabrication information in [5] and [7]). And because the lower bound of  $g_m$  in our design specification (Table.2.3) is  $200n$ , the  $w_z$  can be as small as  $20k(rad/s)$ . To force the total loop gain to drop to 1 before  $s > 2k(rad/s)$ , we have to reduce the first dominant pole frequency.

We choose  $w_{p1}$  as the first dominant pole. From section 3.1.4.3, we learned that the  $A_{OP}$  should be larger than  $5k$ . Thus, we choose a folded cascode structure which provides high output impedance and gain.



**Figure 3.11:** (a)The feedback OP block and its (b) schematic

We designed a folded cascode OP with a gain of 10k (80dB) and bandwidth less than 3Hz (Fig.3.11, Table.3.2). A higher gain reduces the effect of fabrication variation (30% deviation of the impedance of the  $R_{TIA}$  in TIA block). The low bandwidth is owing to the large capacitance ( $C_f$ ) appended to the output. This capacitance results in a lower slew rate, which is fine because the circuit is for DC signal and there is no need for high speed operation.

VDD	3.3V
Ibias	$35\mu A$
BandWidth	2 Hz
Max Gain	81dB
Output Dynamic Range	0.45V - 3V
PSRR	$41(dB)$
CMRR	$126(dB)$
ICMR	0.32V - 3.1V

**Table 3.2:** Post-simulation result of feedback OP

### 3.1.5 The Post-simulation Result of the DC-sweep mode circuit

#### 3.1.5.1 DC Current (Ibias) Sweep

We swept Ibias and measured the output voltage of the feedback OP which is also the gate voltage of SiNW in Fig.3.1. We also measured the  $I_D$  of the transistor. (Because we don't have nanowire model, we performed the simulation by using an alternative mosfet.) In Fig.3.12(a), the curve of  $I_{bias}$ - $V_G$  is compared with the curve of  $I_D$ - $V_G$ . Based on Eq.(3.7),  $\frac{\partial I_{bias}}{\partial V_G}$  is approximately equal to  $g_m$ . This is verified in Fig.3.12(b) where two  $g_m$ : the measured  $g_m$  ( $\frac{\partial I_{bias}}{\partial V_G}$ ) and the intrinsic  $g_m$  ( $\frac{\partial I_D}{\partial V_G}$ ) are plotted together.

We defined the difference between two  $g_m$  as error rate. That is:

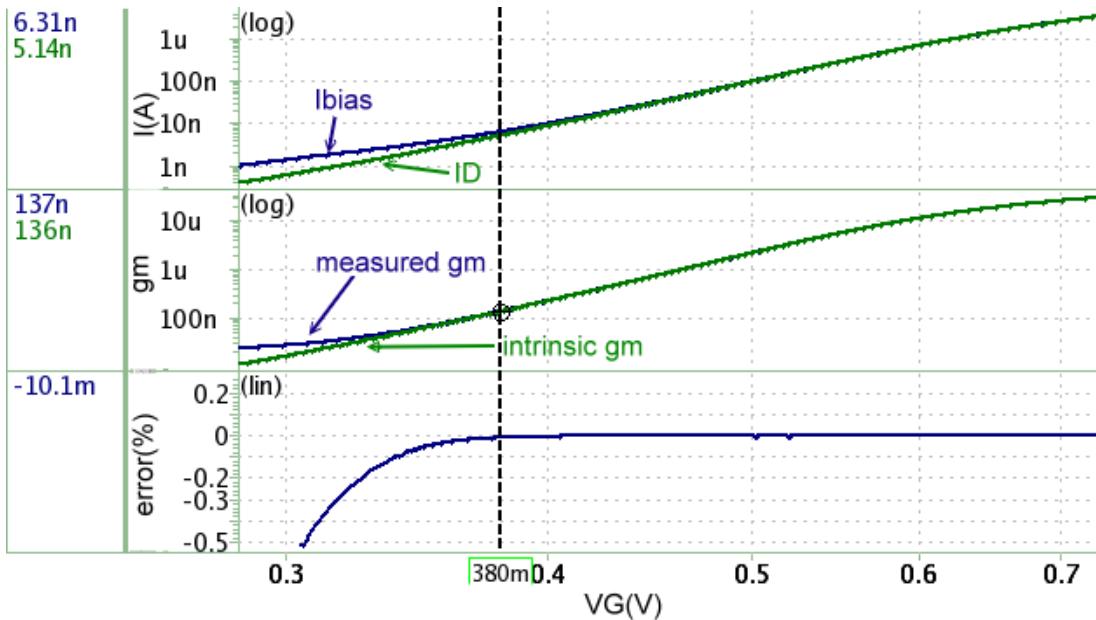
$$\text{error} = \left| 1 - \frac{\text{measured } g_m}{\text{intrinsic } g_m} \right| (\%) \quad (3.15)$$

The error rate is showed in Fig.3.12(c) It is pointed out by the cursor that after the intrinsic  $g_m$  is less than 130n, the error is over 1%.

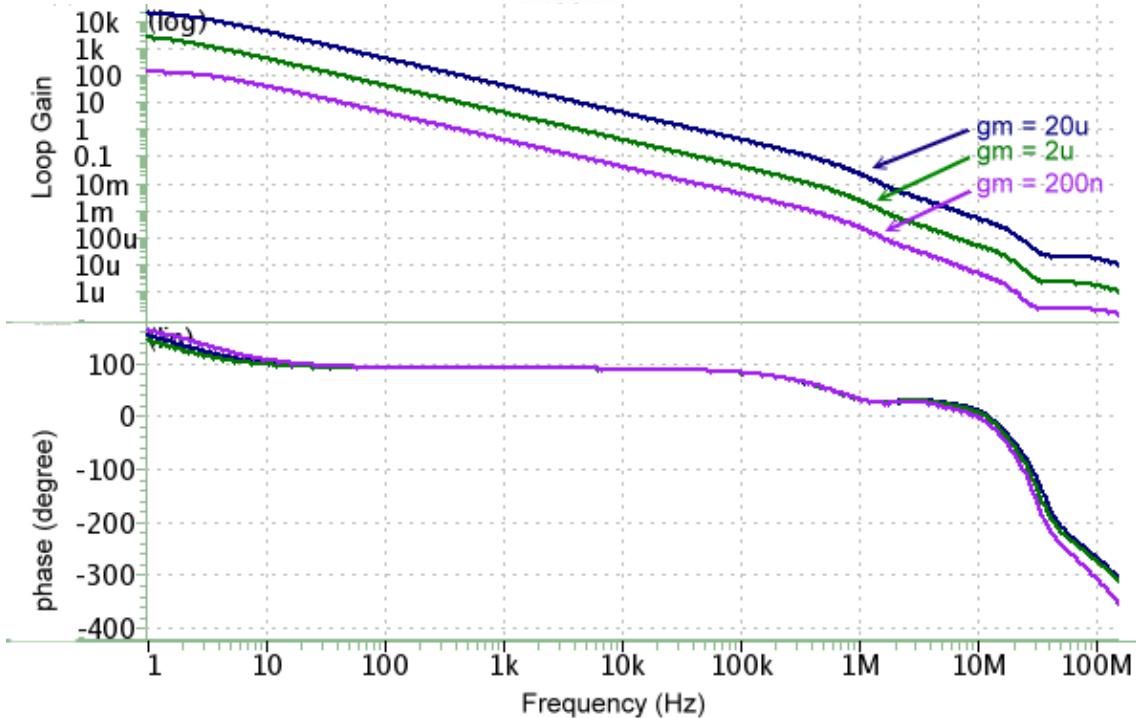
#### 3.1.5.2 Bode Plot of Loop Gain and Phase

The simulation here is according to the stability section (section.3.1.4.5). We present the Bode plot of the loop gain and the phase (Fig.3.13). The summarization table is also given (Table.3.3). We adjusted the transistor to the specific  $g_m$  values by selecting Ibias and corresponding  $V_G$ . We also appended a  $1pF$  capacitor to model the  $C_{gd}$ .

Table.3.4 compares the design specification and the simulation result. It is notable that in fact the upper limits of  $g_m$  is depends on two factors. One is the gate voltage. Table.3.2 shows that the maximal gate voltage that the Feedback OP can provides is 3V. The other is the current



**Figure 3.12:** Post-simulation result of the dc sweep of Ibias in Fig.3.1. (a) is the  $I_D$ - $V_G$  curves of  $I_D$  and  $I_{bias}$ . (b) is the  $g_m$ - $V_G$  curves of intrinsic  $g_m$  and measured  $g_m$ . (c) is the ratio of the difference between two  $g_m$  (error).

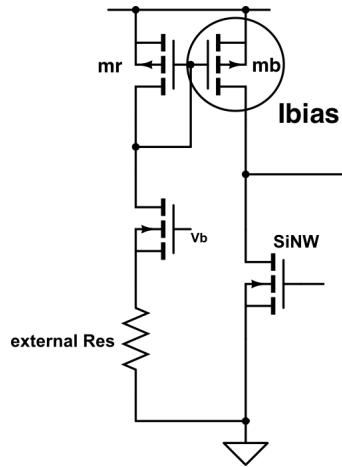


**Figure 3.13:** Results of the ac simulation of the loop gain and phase (Bode plot) with different  $g_m$  value ( $200n$ ,  $2u$ ,  $20u$ ). These  $g_m$  value is selected according to the DC-sweep mode specification we set in chapter 3 (section.2.4).

$g_m$	$20\mu$	$2\mu$	$200n$
Loop Gain	20k	2k	200
Phase Margin	80(deg)	78(deg)	81 (deg)

**Table 3.3:** The phase margin and loop gain of the fronted circuit

$I_{bias}$ .  $I_{bias}$  is generated by a simple pmos whose current is decided by an external resistor (Fig.3.14). The size ratio between pmos  $mr$  and  $mb$  is 1 : 10. This current mirror structure has a maximum output current of  $70\mu A$ . In Table.3.4, the upper limits of  $g_m$  is  $50\mu$ . According to our electrical measurement, this is the maximal  $g_m$  value that our nanowire can have when  $V_G$  is  $3V$ .

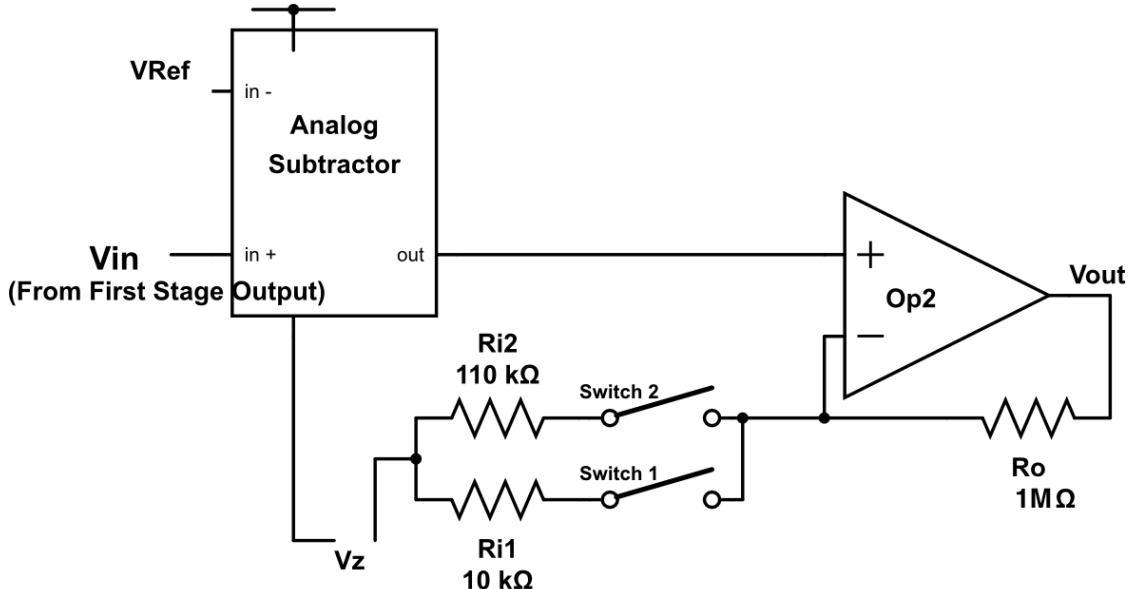
**Figure 3.14:** The current mirror structure of the current source Ibias.

	Design Spec.	Simulation result
$I_D$	$100nA - 30\mu A$	$20nA - 70\mu A$
$g_m$	$200nA - 20\mu A$	$130n - 50\mu$
$V_G$	$0.5V - 3V$	$0.45V - 3V$

**Table 3.4:** The comparison between the design specification and simulation result of the DC-sweep mode circuit.

## 3.2 The Second Stage Circuit

We discuss the second stage circuit in this section. It is notable that the second stage circuit is only used for the transient measurement.



**Figure 3.15:** Block diagram of the second stage circuit

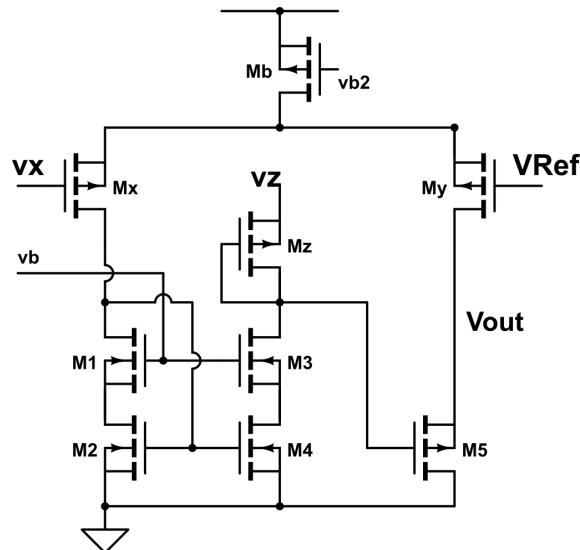
Fig.3.15 shows the block diagram of the second stage circuit. The analog subtractor shifts the voltage of  $V_{in}$  from  $V_{Ref}$  to  $V_z$ . It is followed by a resistor-based non-inverting amplifier composed of a two-stage differential operational amplifier, two switches and three resistors. The switches select the amplification gain among 100, 10 and 1.

### 3.2.1 The Analog Subtractor

Fig.3.16 shows the schematic of the analog subtractor [15]. The output voltage equals to:

$$V_x - V_{Ref} + V_z \quad (3.16)$$

A voltage signal  $\Delta v$  sent to  $v_x$  induces a current change ( $\Delta i_d$ ) in  $M_x$ . This current is mirrored to the diode-connected  $M_z$  by the cascode current mirror formed by  $M_1 \sim M_4$ .  $\Delta i_d$  changes the gate voltage of  $M_z$ , and this voltage is buffered to the output by the source follower  $M_5$ .



**Figure 3.16:** Block diagram of the second stage circuit.

$$\Delta v_{out} = \Delta v_x \frac{g_{mx}}{g_{mz}} - V_{Ref} \frac{g_{my}}{g_{m5}} + V_z \quad (3.17)$$

$$\Delta v_{out} = \Delta v_x - V_{Ref} \quad \text{For } g_{mx} = g_{mz}; g_{my} = g_{m5} \quad (3.18)$$

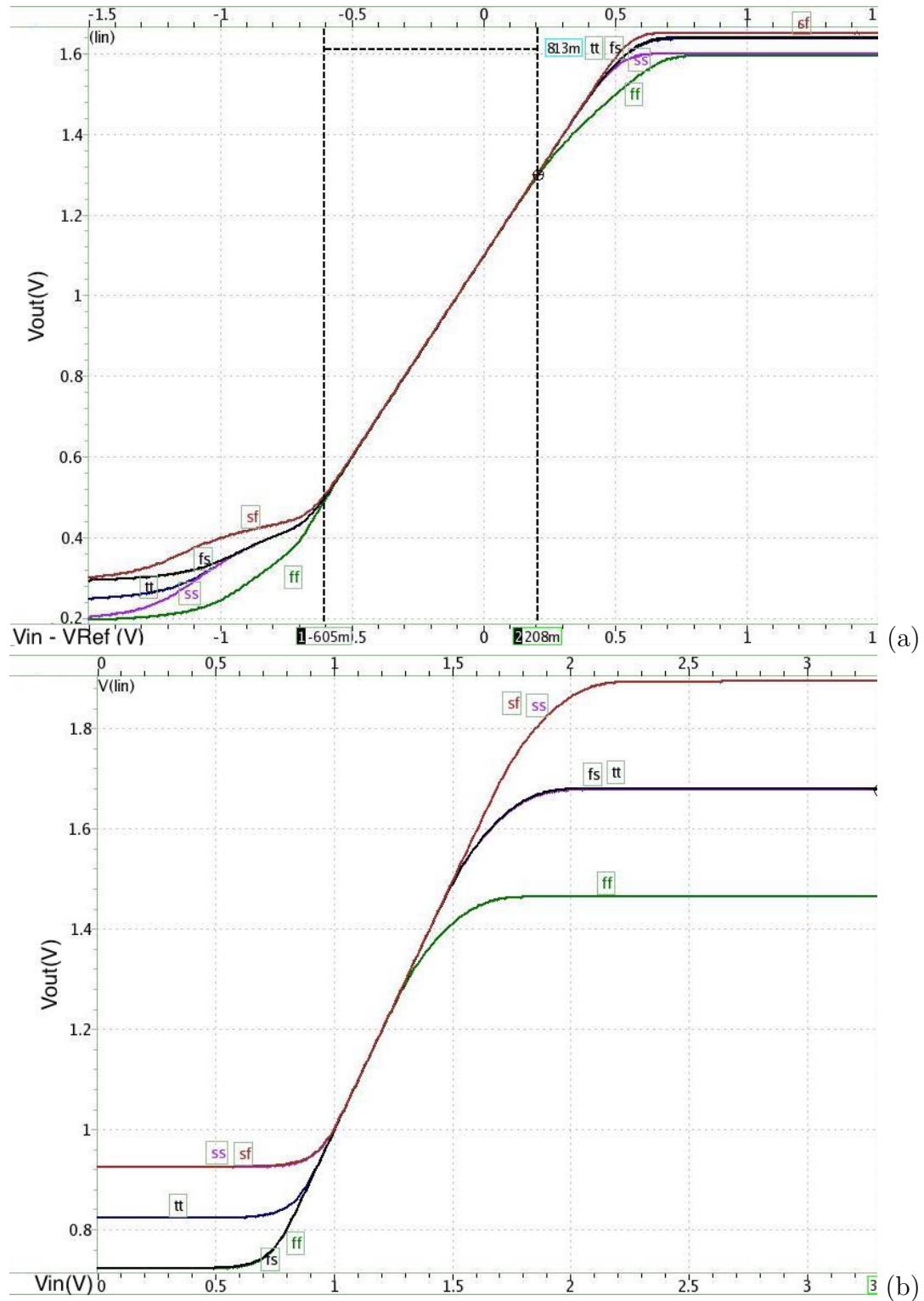
One reason for employing this block is that the  $V_{Ref}$  is an internal voltage reference which may drift with the process variation. We prefer the output offset voltage of the circuit to be constant and controllable. Therefore, we shift it to  $V_z$  controlled by an external voltage source. Another reason is to increase the output dynamic range of the next amplifier stage. This reason will be much clearer when we start discussing the amplifier circuit in the next section.

We performed DC sweep on input ( $V_X$ ) and  $V_z$  at five corners to show the linear region of the circuit (Fig.3.17, Table.3.5). The circuit has an input dynamic range of  $0.77V$  ( $-0.57V \sim +0.2V$ ) while the dynamic range for  $V_z$  is  $0.38V$ .

*In Fig.3.17(a), the result of ff corner exhibit poor upper input dynamic range.*

### 3.2.2 Non-inverting Resistor-based Amplifier

In Fig.3.16, the Op2 along with the resistors ( $R_o$ ,  $R_{i1}$ ,  $R_{i2}$ ) and the switches (Switch1, Switch2) compose our non-inverting resistor-based Amplifier. We adopt



**Figure 3.17:** DC response of the output of our analog subtractor. (a) The x-axis is the difference between positive input and negative input ( $V_x - V_{Ref}$ ). (b) The x-axis is the voltage of  $V_z$

VDD	3.3V	
Ibias	$40\mu A$	
Output voltage dynamic range	$0.2V-2.5V$	
Input voltage type	$V_x$	$V_z$
Input Dynamic Range	from $V_{Ref} - 0.57V$ to $V_{Ref} + 0.2V$	from 1V to 1.38V
Bandwidth	$675kHz$	irrelevant
SNR (@10Hz)	$8.3e10$	$8.4e10$

**Table 3.5:** The summary table of the analog subtracter circuit.

this simple structure to amplify the output signal of the subtractor. When the subtractor sends a small signal  $\Delta v$  into Vin, the output voltage ( $v_{out}$ ) is:

$$v_{out} = (\Delta v - v_f) \times A_{Op2} \quad (3.19)$$

$$v_f = v_{out} \frac{R_i}{R_o + R_i} \quad (3.20)$$

$$\frac{v_{out}}{\Delta v} = \frac{A_{Op2}}{1 + A_{Op2} \frac{R_i}{R_i + R_o}} \quad (3.21)$$

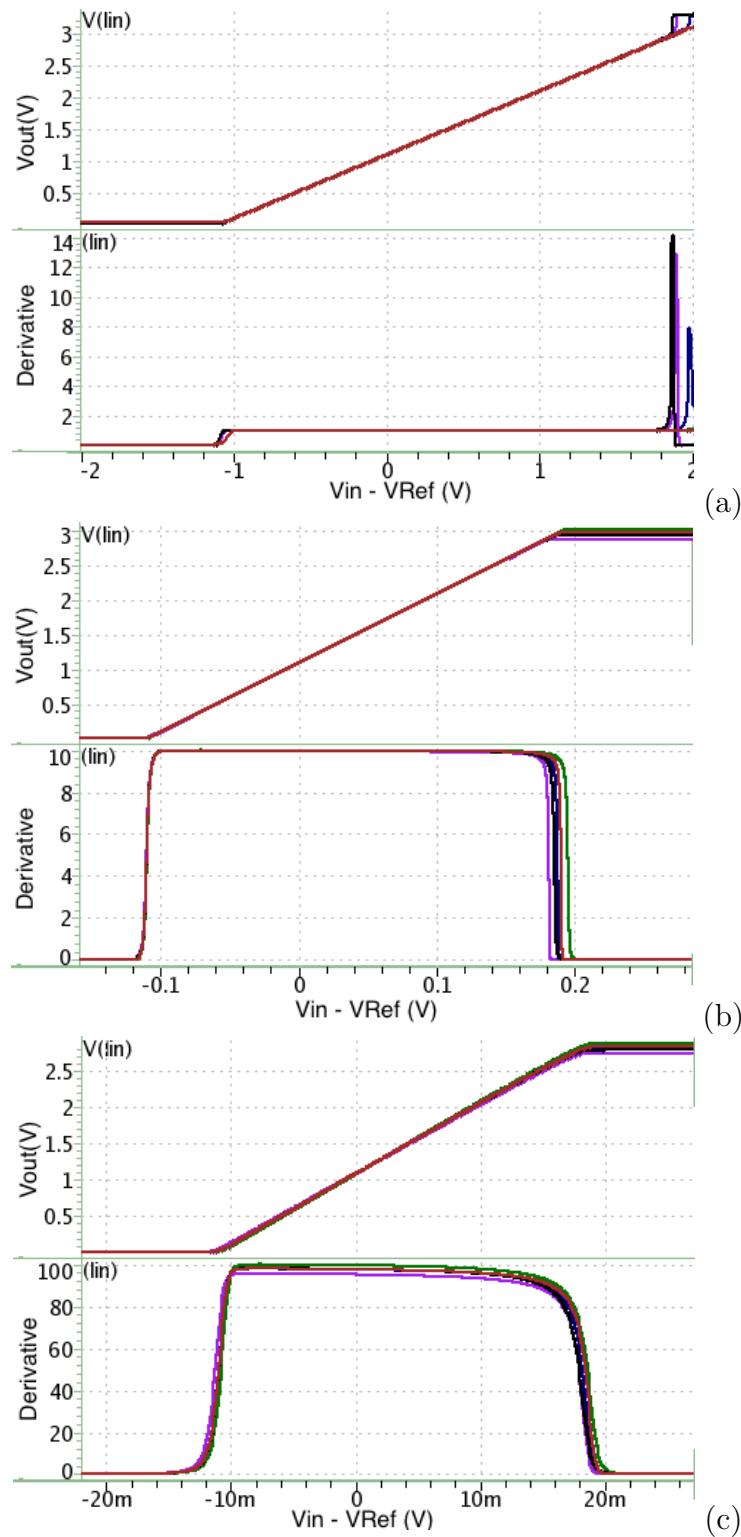
$$\approx \frac{R_i + R_o}{R_i} \quad \text{For } \frac{R_i A_{Op2}}{R_i + R_o} > 10 \quad (3.22)$$

The  $R_i$  can be  $110k\Omega$  or  $9.2k\Omega$  ( $10k\Omega || 110k\Omega$ ). When two switches is off, the circuit acts like an unit-gain buffer. Eq.(3.22) suggests that  $A_{Op2}$  should be larger than 1000 (60dB). Thus, the Op2 in Fig.3.15 adopts the structure of a two-stage amplifier (same with the operational amplifier in TIA block) due to its high gain and wide output dynamic range.

*One thing to note is that the derivation above views the  $V_z$  as the virtual ground.  $V_z$  is both the input and output offset voltage of the amplifier. It is usually applied with 1.3V. As mentioned in the subtractor section (Section.3.2.1), the subtractor increases the output dynamic range of the amplifier stage. If the subtractor is removed, the output offset voltage of this stage would be  $V_{Ref}$ , which is much lower ( $\sim 0.8V$ ), and is changeable due to the process variation.*

Fig.3.18 presents the five corners post-simulation results of the amplifier. We swept the input and measured the output under three amplification gain. And Table.3.6

is the summary table.



**Figure 3.18:** Five corners output DC response ( $v_{out}$ ) and derivative ( $dv_{out}/dvin$ ) when being operated under the amplification rate of (a)1, (b)10, (c)100.

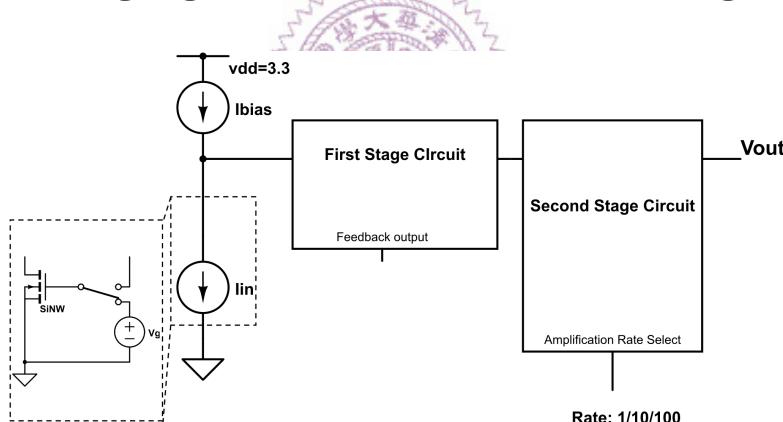
Amplification Rate	100	10	1
Error	< 7%	< 0.7%	< 0.02%
Bandwidth	10.1k Hz	24k Hz	220k Hz
Phase Margin	110 degree	110 degree	84 degree
Input Dynamic Range	from $-9mV$ to $17mV$	from $-0.11V$ to $0.14V$	from $-0.5$ to $0.3V$
Output Dynamic Range	0.1V - 3V		

**Table 3.6:** The summary table of simulation results.

### 3.3 Post-simulation Result of the Transient Measurement mode

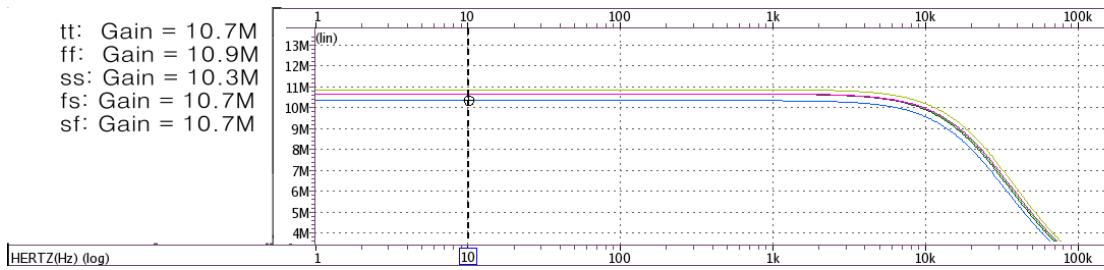
As mentioned in section 3.1.2, there are two usage of the Transient Measurement mode (Fig.3.2). There simulation results are presented separately below.

#### 3.3.1 Detecting signals of biomolecules at the gate

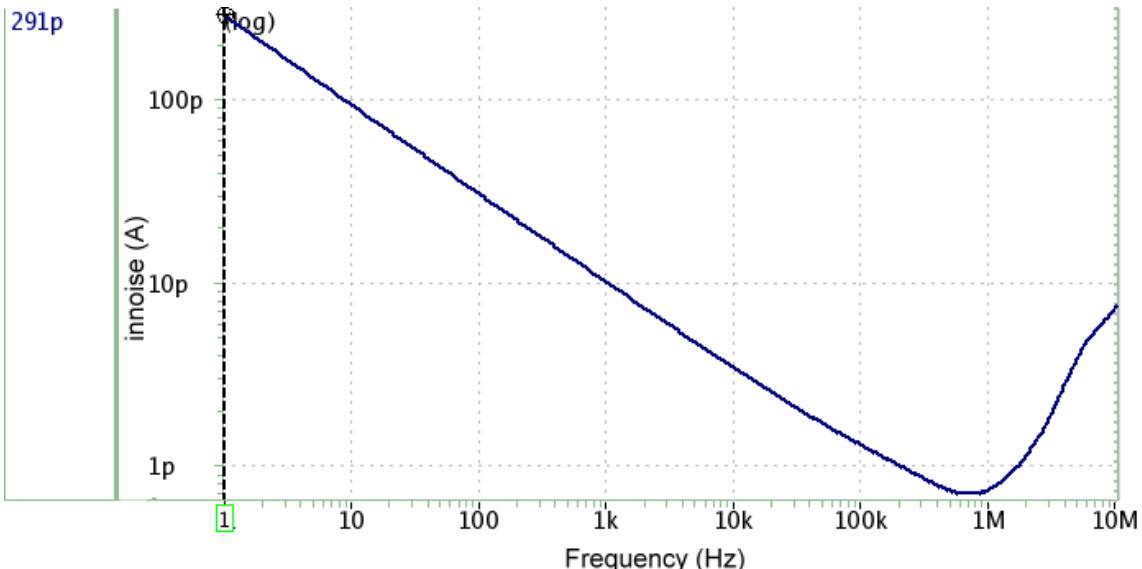


**Figure 3.19:** The block diagram of the Transient Measurement circuit. We simulate it by sending ac signal through the voltage source  $V_g$ .

The first usage is to detect the output response of input voltage signal at gate. The voltage signal is caused by the biomolecule concentration. This measurement are usually preceded by the DC-sweep mode, which initialize the  $I_D$  with the value of Ibias and set  $g_m$  to a corresponding value. Therefore, we replaced the transistor by a current signal  $I_{in}$  as in Fig.3.19. And we apply an ac signal from  $I_{in}$  to perform the ac analysis.



**Figure 3.20:** The gain of  $\frac{V_{out}}{I_{in}}$  when the voltage gain of the second stage is 100.



**Figure 3.21:** The input referred noise when the amplification rate of the second stage is 100.

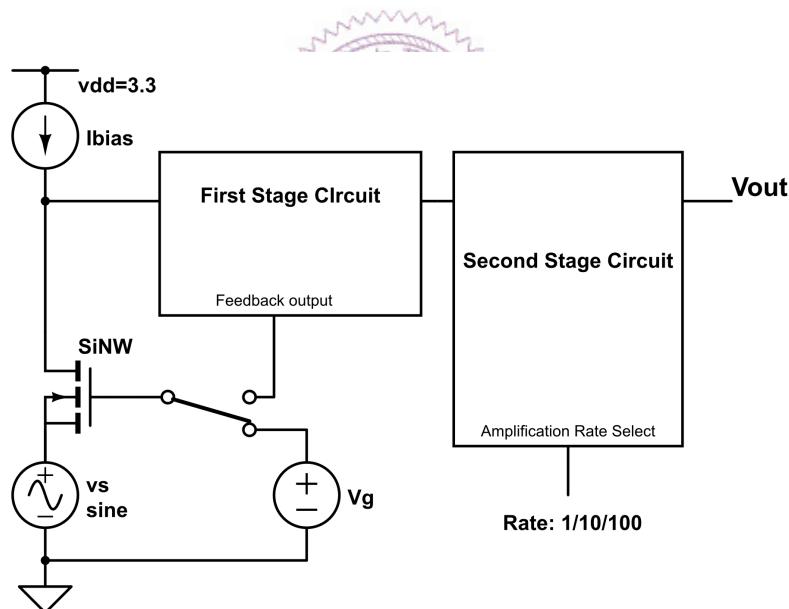
Fig.3.20 presents the maximal gain that the circuit provides at five corners. Fig.3.21 shows the input referred noise. The design specification requires the gain to be greater than 5M and the voltage noise referred to the gate of nanowire to be smaller than 2mV. The summary table (Table.3.7) computed the noise result by considering the  $g_m$  as 200n, which is the minimum  $g_m$  that may exist in our measurement.

To be noted that in the simulation of Fig.3.21, Ibias provides  $10\mu A$  which is the largest biasing current in transient measurement mode (Table.2.4). This should be when the circuit has largest noise.

	Design Spec. (Table.2.5)	Simulation Result
$I_D$ Range	600nA - 10 $\mu$ A	
$gm$ Range	1 $\mu$ - 20 $\mu$	
$\Delta V_G$	20mV - 280mV	
Dynamic Input Current Range	$\pm 2.8\mu A$	6 $\mu A$ -10 $\mu A$
Maximal Amplification Rate ( $\frac{V}{A}$ )	5M	10.3M
Bandwidth	> 1kHz	10.1kHz
Input Referred Noise ( $V_G$ )	< 2mV	= $\frac{0.291n}{200n} = 1.46mV$ @1Hz

**Table 3.7:** The summary table. The first three rows are the nanowire characteristics when applied with the Transient Measurement mode. Others are the simulation results comparing with the design specification.

### 3.3.2 Modulating biomolecule signals from the source terminal



**Figure 3.22:** The block diagram of the Transient Measurement circuit. We simulate it by sending ac signal to the source of the nanowire.

The second usage of the Transient Measurement circuit is to apply a sinusoidal signal at the source of nanowire.  $V_g$  and  $I_{bias}$  are kept constant during the measurement. The output voltage is measured and used for computing the  $g_m$  of the

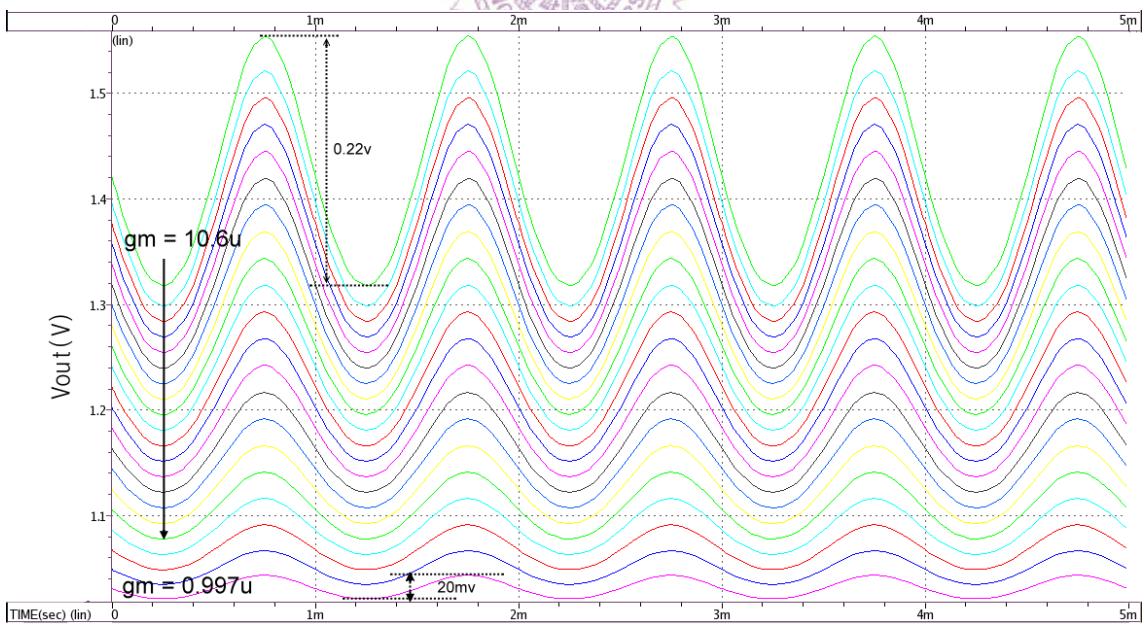
element.

$$g_m = \frac{V_{out}}{v_s \times R_{TIA} \times A_{second}} \quad (3.23)$$

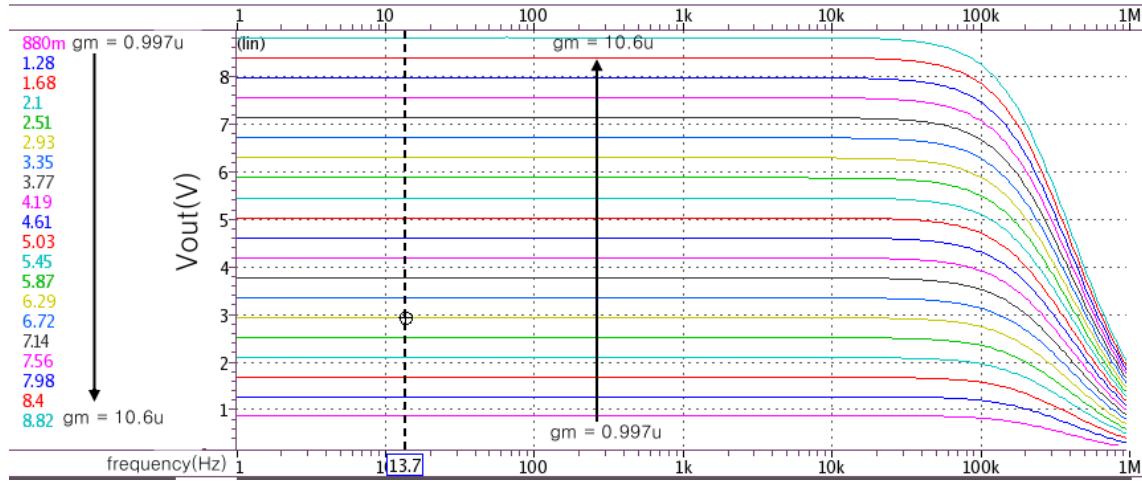
The  $v_s$  is the amplitude of the input sinusoidal signal, and  $A_{second}$  is the voltage gain of the second stage circuit.

One thing to be noted is the offset voltage of the output. The biomolecule concentration difference changes the  $I_D$  of nanowire. This  $I_D$  difference not only results in the change of  $g_m$  but also alters the offset current flowing through  $R_{TIA}$ . This current is also amplified and may cause too much current flowing into the circuit. The solution is to utilize Ibias to cancel the offset current.

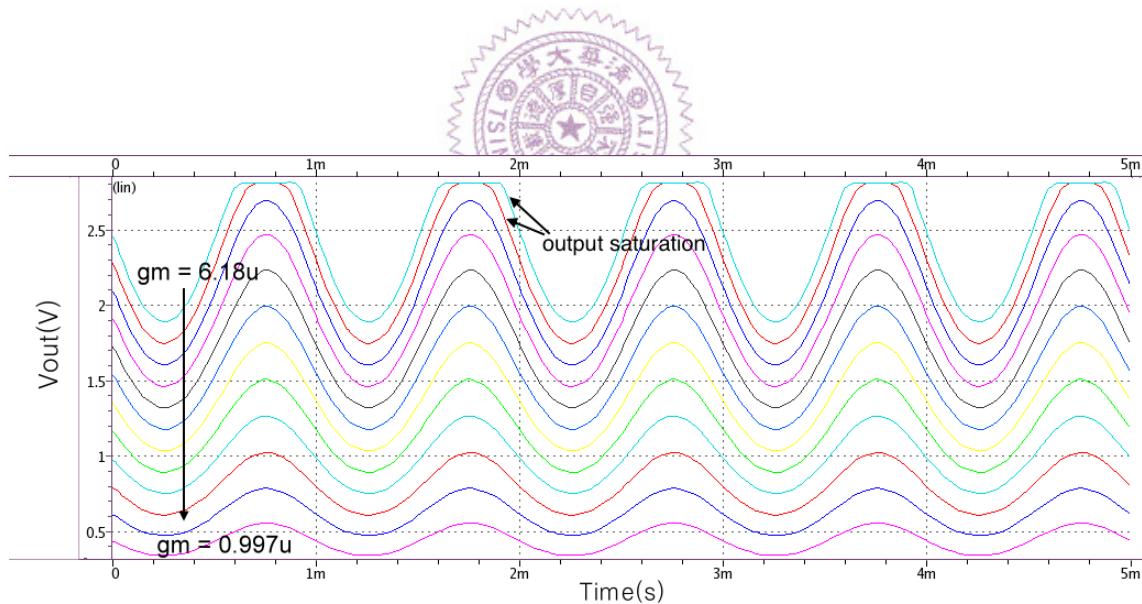
Two simulation results presented below are the transient responses of the output voltage when  $A_{amp}$  is 10 (Fig.3.23)and 100(Fig.3.25).  $g_m$  of the transistor is swept in the same time. According to the specification given in chapter 3 (Table.2.5),  $g_m$  ranges from  $1\mu$  to  $10\mu$  in transient measurement. The input sinusoidal signal has a frequency of  $1kHz$  and an amplitude of  $20mV$ . Their corresponding ac sweeps are presented in Fig.3.24 and Fig.3.26. *These results show that the circuit bandwidth is about  $10kHz$ , which is caused by the last amplifier block.*



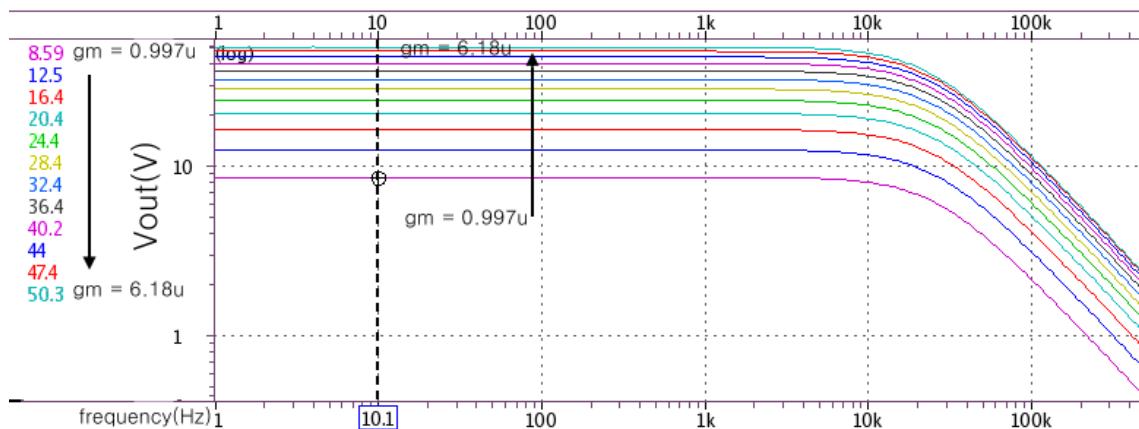
**Figure 3.23:** The transient analysis. The gain of  $A_{amp}$  is 10. The  $g_m$  is swept from  $1\mu$  to  $10\mu$ .



**Figure 3.24:** The ac analysis of the transient simulation result in Fig.3.23.



**Figure 3.25:** The transient analysis. The gain of  $A_{amp}$  is 100. The  $g_m$  is swept from  $1\mu$  to  $6\mu$ . There are two curves have the output saturation problem. This is because of the offset current flowing through  $R_{TIA}$ . One may solve it by increasing the current provided by Ibias.



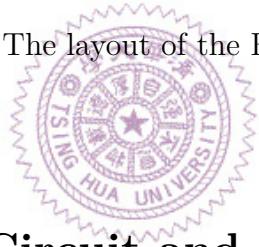
**Figure 3.26:** The ac analysis of the transient simulation result in Fig.3.25.

# Chapter 4

## Circuit Results Discussion and Summary

This chapter presents the results of our read-out circuit and the summary of this thesis. The layout of the circuit is given in 4.1

**Figure 4.1:** The layout of the Readout circuit

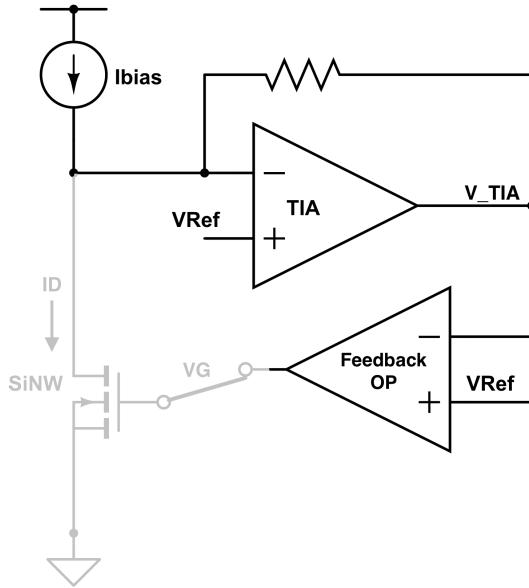
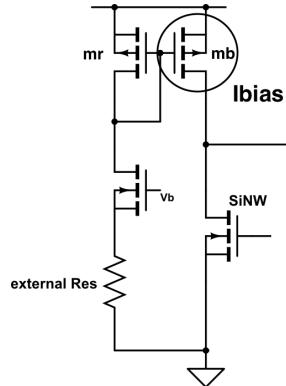


### 4.1 The Fronted Circuit and DC-sweep mode

As in Fig.4.2(a), the fronted circuit includes a biasing current source (Ibias), transimpedance amplifier (TIA) and an operational amplifier (OP). These three circuit blocks combined with the nanowire device (SiNW) form a feedback structure, which is the DC-sweep mode of our circuit.

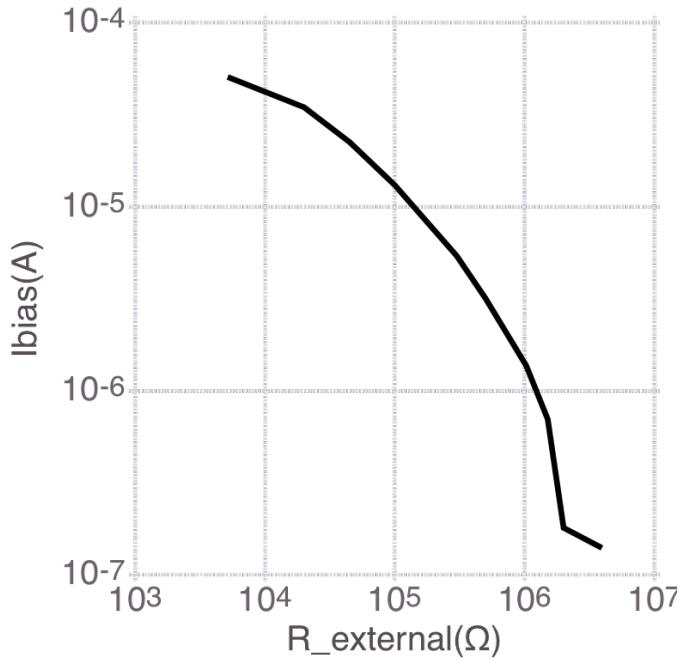
#### 4.1.1 Ibias

The Fig.4.3 is the schematic of the Ibias circuit. The relation between the resistance of the external resistor and the biasing current is shown in Fig.4.4. The Ibias circuit is able to provide a biasing current from  $100nA$  to  $50\mu A$  stably. It should be noted that this biasing current range binds the operational range of the DC-sweep mode circuit.

**Figure 4.2:** The fronted circuit**Figure 4.3:** The Ibias circuit

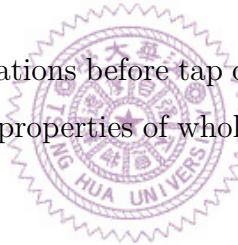
#### 4.1.2 TIA

The Fig.4.5(a) and (c) show that the dynamic input current range of TIA is  $+5.3\mu A \sim -15\mu A$ . The Fig.4.5(b) and (d) are the respective derivative ( $\frac{\partial V_{out}}{\partial I_{in}}$ ) As illustrated in these figures, the transimpedance of TIA is  $103k$ . It is notable that not all TIA on the chips have the same transimpedance. This is because the transimpedance value depends on the resistance of the resistor in TIA (Fig.4.2). This resistor is made of N-well, which should have the largest resistance-to-surface ratio among other kinds of resistor. But since the doping concentration may vary with the fabrication process, such kind of resistor has a larger resistance variance (% 30). We



**Figure 4.4:** The relation between biasing current ( $I_{\text{bias}}$ ) and resistance of the external resistor

have performed necessary simulations before tap out. It is assured that the variance does not disturb the important properties of whole read-out circuit such as stability and noise ratio.

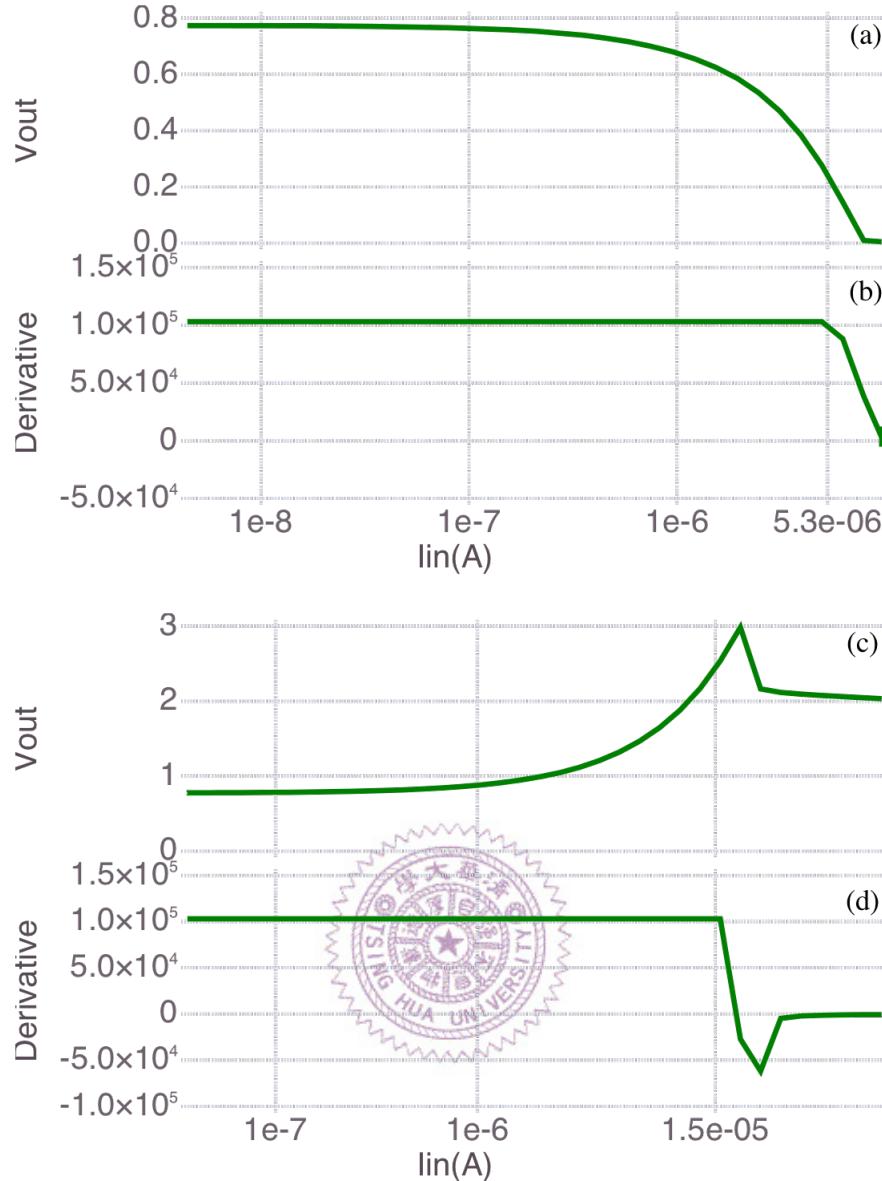


### 4.1.3 OP

A sinusoidal signal is sent to the negative input of OP and the output signal is measured in Fig.4.6. It shows that the gain of the feedback OP is only about  $1k$ . However, the gain of OP was designed to be more than  $5k$ . We will discuss this problem in the following section.

### 4.1.4 Measurement with the DC-sweep Mode Circuit and the Low-current Defect Problem

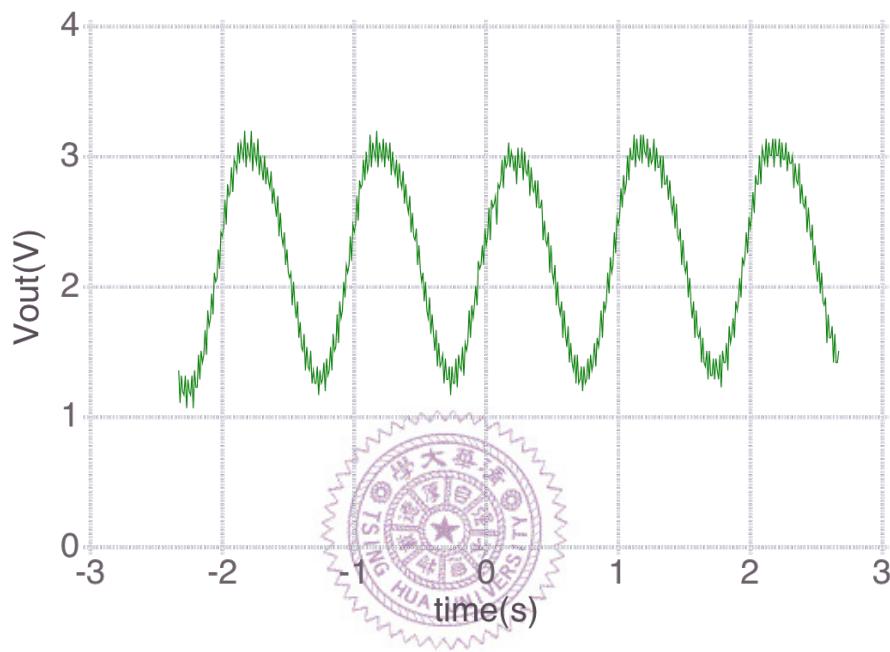
With the the DC-sweep mode circuit (Fig.4.7),  $I_{\text{bias}}$  is swept and  $V_G$  and  $I_D$  are measured to obtain the  $I_D$ - $V_G$  and  $I_{\text{bias}}$ - $V_G$  curves (Fig.4.8). The chip works well when  $I_{\text{bias}}$  is larger than  $1\mu\text{A}$ . The overlap between two curves implies that  $I_D$



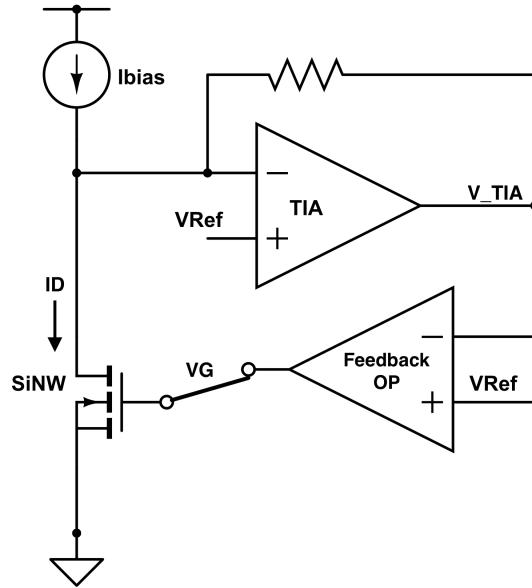
**Figure 4.5:** The dc simulation results of TIA. The x-axis represents positive/negative input current (log scale). (a) is the  $V_{\text{out}}$  responding to the positive input current while (c) is to the negative input current. (b) and (d) are the partial derivative of  $V_{\text{out}}$  with respect to input current ( $\frac{\partial V_{\text{out}}}{\partial I_{\text{in}}}$ ) from (a) and (c) respectively.

follows  $I_{\text{bias}}$  and  $V_G$  consequently alters owing to the feedback mechanism.

When current becomes low, the circuit fails to prompt nanowire to follow the biasing current. This phenomenon could be reasonable because lower  $I_D$  implies lower  $g_m$  and the feedback ability of the circuit may be not strong enough to push the gate of nanowire. However we expected this happens for  $g_m$  below  $200n$ . The

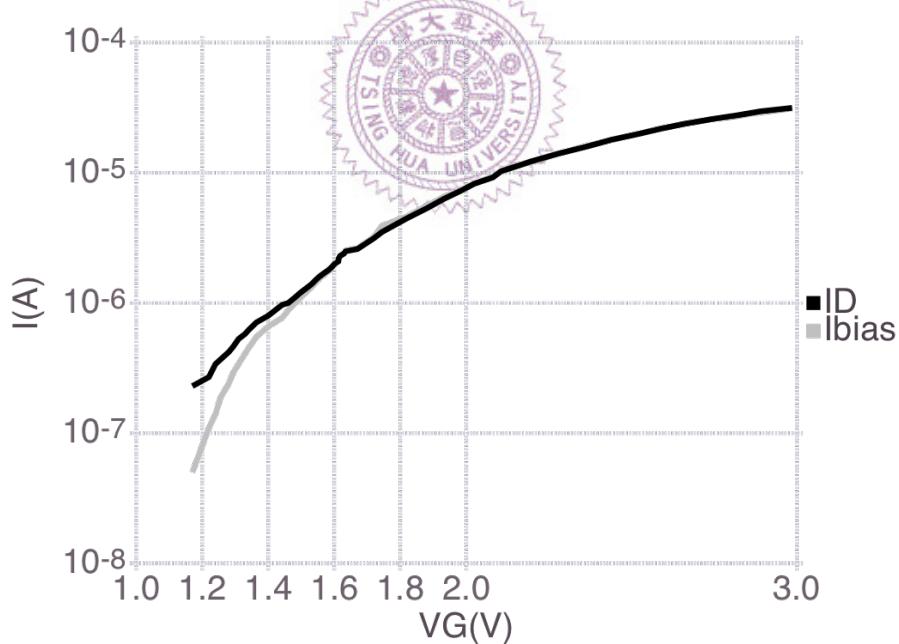


**Figure 4.6:** The output voltage of the feedback OP when the negative input is applied with a sinusoidal signal. This input sinusoidal signal has frequency of 1Hz and amplitude of 2mV. The positive input of OP is biased with a constant voltage generated by the chip (VRef in Fig.4.7). The output signal has amplitude around 2V, which means that the gain of OP is about 1k.

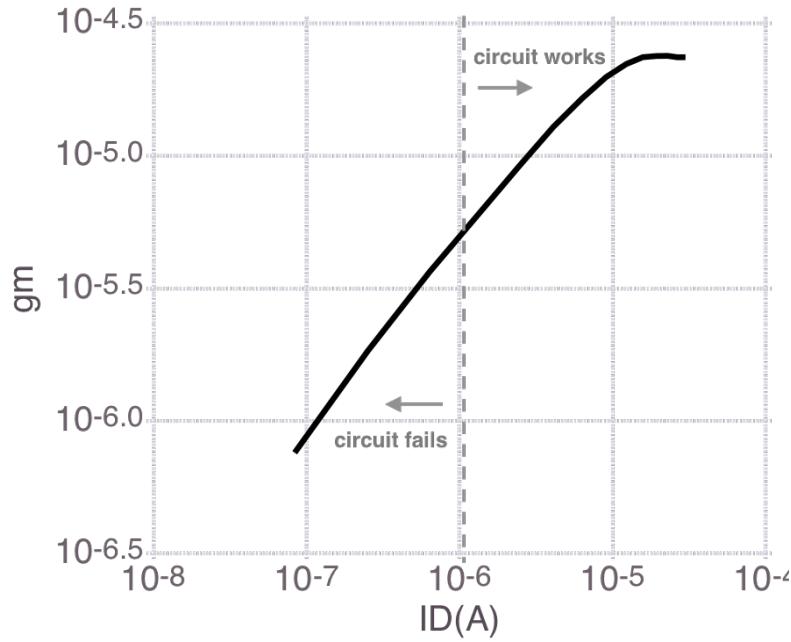


**Figure 4.7:** DC-sweep mode circuit

Fig.4.9 indicates that this happens when  $g_m$  is less than  $5\mu$  instead. We call this problem as low-current defect problem.



**Figure 4.8:** The measurement result of the DC-sweep mode circuit.  $I_{bias}$  is the biasing current.  $I_D$  is the current flowing through the nanowire device. One can observe a separation between two curves in low current section ( $< 1\mu A$ ).



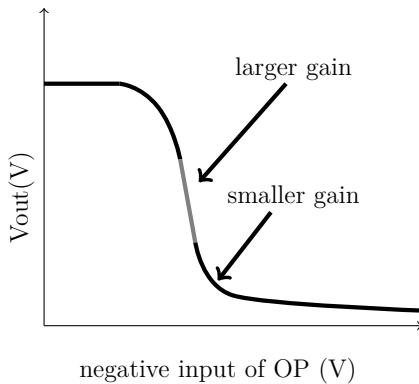
**Figure 4.9:** The  $g_m$ - $I_D$  curve. It is obtained from the  $I_D$ - $V_G$  curve in Fig.4.8. “Circuit fails” means the two curves in Fig.4.8 are separated where “circuit works” means they are overlapped.

### Insufficient Gain

We first suspected that it is caused by the insufficient gain of the feedback OP. According to the last section (Section.4.1.3), the gain is about  $1k$ . The discussion in Section.3.1.4.3 suggests that the feedback mechanism depends on the loop gain. The loop gain should be larger than 100 for the DC-sweep mode being functional. Based on Eq.(3.4) and Eq.(3.5), if  $A_{OP}$  is  $1k$ , the loop gain drops below 100 when  $g_m$  is less than  $1\mu$ . In other words, even though the gain of OP is 5 fold smaller than the gain we designed, the circuit should work well when  $g_m$  is larger than  $1\mu$ . But in fact, the circuit fails for  $gm$  below  $5\mu$ .

One possible reason is that the gain of OP varies with input. Fig.4.10 is the illustration of the input-output response of the feedback OP. As depicted by it, the slope ( $\frac{\partial V_{out}}{\partial V_{input}}$ ) in the midst of the curve is larger than the slope at the both ends (The slope can represent the gain of OP). In the measurement of Fig.4.6, the offset of the output signal is around  $2V$ . But in Fig.4.8, when the separation happens, the output voltage of OP ( $V_G$ ) is less than  $1.5V$ . Thus, we assert that the gain of

OP is less than we measured.



**Figure 4.10:** The illustration of the input-output response of the feedback OP.

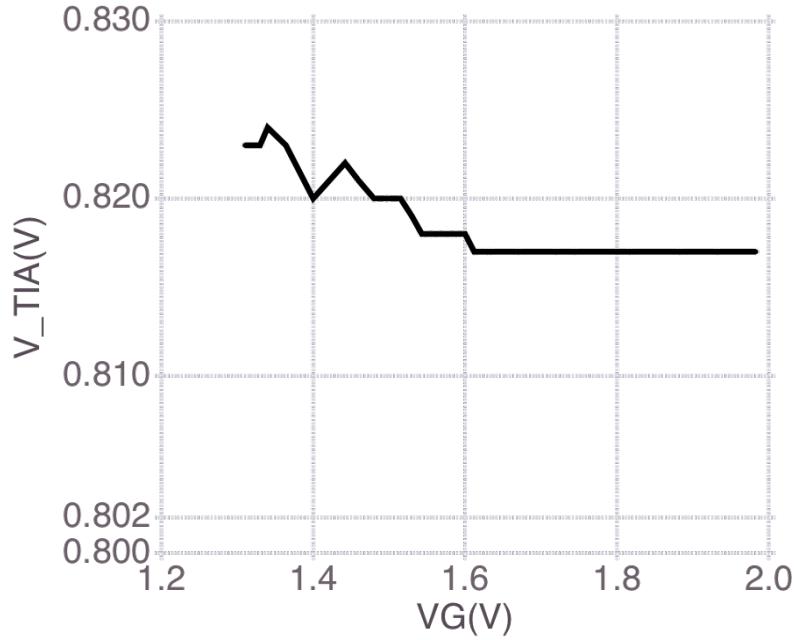
### Input Offset Voltage

Another reason may be responsible for the low-current defect is the offset voltage at the input of the feedback OP.

The output voltage of TIA ( $V_{TIA}$ ) of the DC-sweep experiment in Fig.4.8 is examined and shown in Fig.4.11. Ideally, when feedback mechanism works well,  $V_{TIA}$  should be equal to  $V_{Ref}$ (Fig.4.7). However, the value of  $V_{Ref}$  is  $0.802V$ , which is smaller than  $V_{TIA}$ . (This  $V_{Ref}$  is connected to a constant voltage point inside the chip. its value is known indirectly by measuring the drain voltage of nanowire since the drain of nanowire is kept to be same as  $V_{Ref}$  by TIA.) When the circuit works well,  $V_{TIA}$  and  $V_{Ref}$  is still different by  $15mV$ . This voltage difference can result in a  $150nA$  offset current flowing through TIA and into the nanowire device. This offset current becomes remarkable when the  $I_{bias}$  becomes small.

We suggest the reason that  $V_{TIA}$  is large than  $V_{Ref}$  is due to the offset voltage appearing at the input of the feedback OP. This speculation is reasonable with respect to the layout, which will be discussed in the next section.

Overall, the insufficient gain and the input offset may be the main reasons of the low-current defect. Both of them relate to the feedback OP. We then discuss these two reasons from the perspective of layout in the following section.



**Figure 4.11:** The  $V_{TIA}$ . The x-axis is the corresponding gate voltage. With the information from Fig.4.8, we found that the  $V_{TIA}$  is not equal to  $V_{Ref}$  no matter feedback mechanism works well or not.

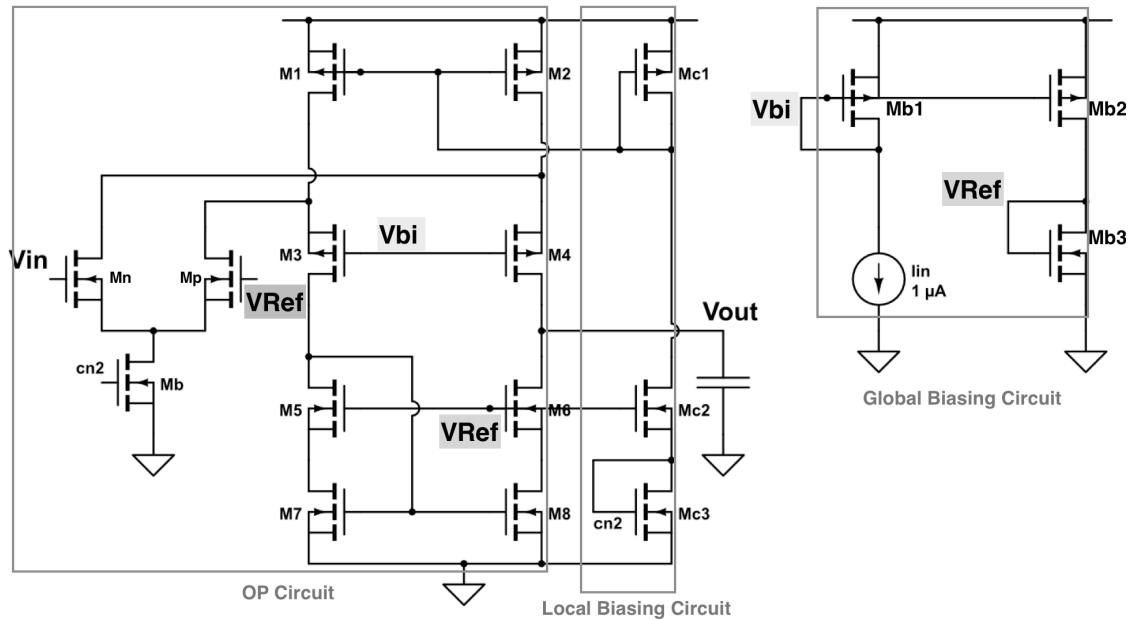
#### 4.1.5 The Layout Problems of OP

The last section mentioned that the gain of OP is lower than we expected and there may exist an input offset voltage. In this section, we will deduce that several layout flaws may be responsible for these two problems.

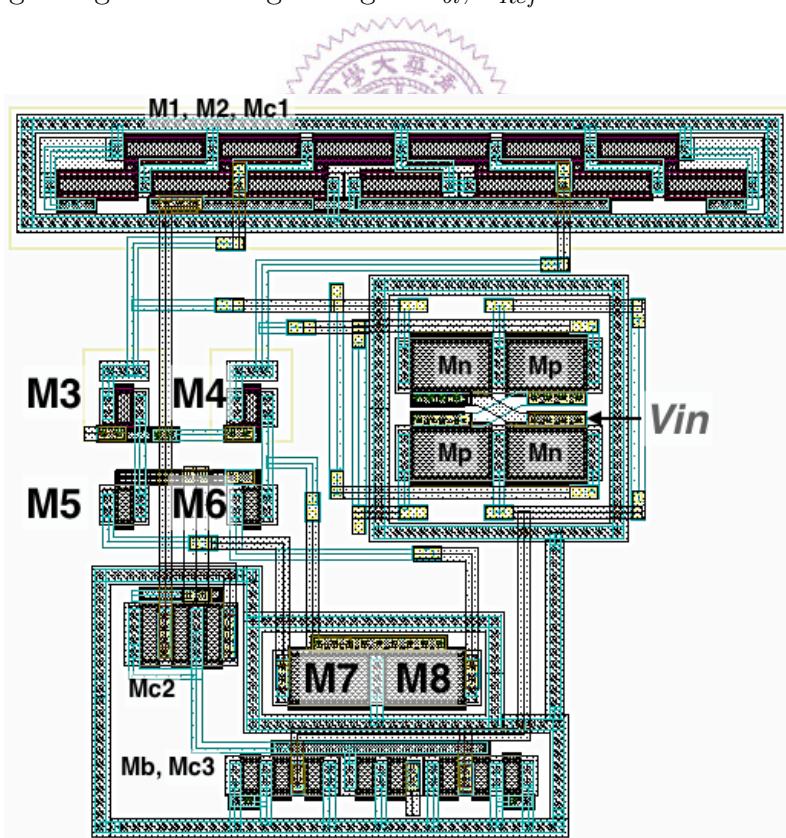
##### 4.1.5.1 The Possible Reasons for Insufficient Gain

The schematic presented in Fig.4.12 contains two sections. The left section is the body of the feedback OP and the local biasing circuit while the right one is a global biasing circuit. The global biasing circuit generated  $V_{bi}$  and  $V_{Ref}$ , which bias two pmos (M3, M4) and two nmos (M5, M6) respectively.

One layout flaw is that the M3 ~ M6 are all single transistor. They are placed alone on the chip (Fig.4.13) without any protection. In consequence their size and doping concentration are more vulnerable to the process variation than other transistors. Another layout flaw is that the global biasing circuit is placed far from the OP circuit. The extent of the process variation from which the OP circuit and global



**Figure 4.12:** The left section is the schematic of the feedback OP including the local biasing circuit and OP circuit. The right section is the global biasing circuit for generating two global biasing voltages:  $V_{bi}$ ,  $V_{Ref}$ . The  $I_{in}$  is an external current source.



**Figure 4.13:** The layout of the feedback OP including the local biasing circuit.

biasing circuit suffer may be different.

Take an example, when process variation happens in global biasing circuit,  $V_{bi}$  and  $V_{Ref}$  change respectively. Ideally, the effect of these two changes on the gain of OP are countervailing. But this may not be true if M4 and M6 suffer another process variation. The changes on  $V_{bi}$  and  $V_{Ref}$  may affect M4 and M6 in different extent. Moreover, the high output impedance of OP amplifies this difference and as a result of the gain distortion.

#### 4.1.5.2 The Possible Reasons for Input Offset

The input offset can be related to the size mismatch between M7 and M8 (Fig.4.13). The transistors were designed to be same. But there is no dummy gate or matching technique applied to the transistors. Therefore, the size mismatch may prone to happen on M7 and M8. In our case, the offset voltage is negative ( $V_{\text{negative input}} > V_{\text{positive input}}$ ). If the size mismatch is responsible for it, the size of M8 should be relatively smaller than M7.

#### 4.1.5.3 Improvement Methodology

Although all problems mentioned above relate to the layout, we do not think that simply revising the layout is a reliable solution. The feedback OP is an open-loop circuit with high output impedance. Its characteristics (such as gain and bandwidth) are hard to be control accurately considering the process variations. A better solution is to replace it with other amplifier. Since this OP serves as a high-gain and low bandwidth block, it can be substituted with a close-loop amplifier and low pass filter.

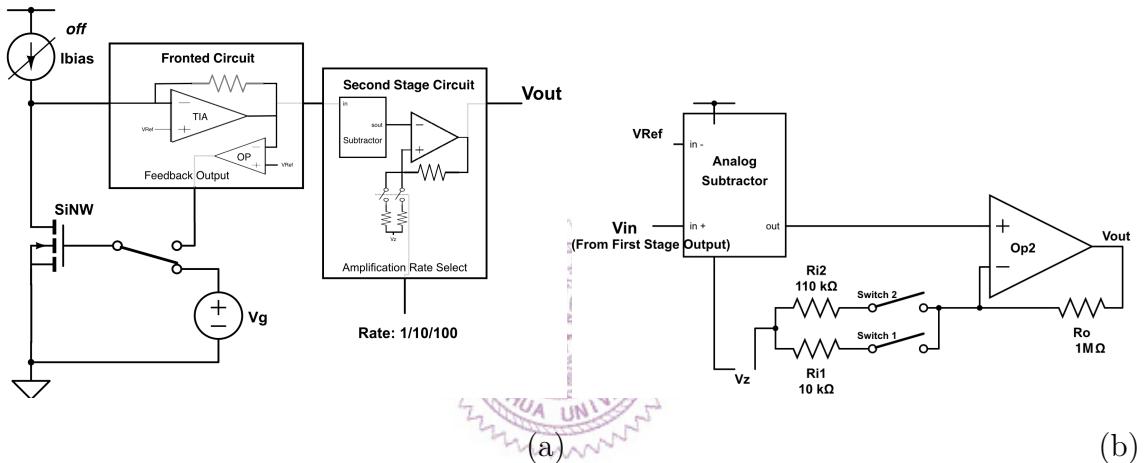
#### 4.1.5.4 Summary of DC-sweep mode

The table that compares the chip properties and the specification for DC-sweep mode is given below (Table.4.1). The chip does not meet the specification due to the low-current defect problem.

	Design Spec.	Chip Properties
$I_D$	$100nA - 30\mu A$	$1\mu A - 50\mu A$
$g_m$	$200nA - 20\mu A$	$3\mu - 20\mu A$
$V_G$	$0.5V - 3V$	$0.45V - 3V$

**Table 4.1:** The comparison between the chip properties and the specification for DC-sweep mode from chapter 3.

## 4.2 The Second Stage Circuit and Transient Measurement Mode



**Figure 4.14:** (a) The block diagram of the Transient Measurement mode circuit.  
(b) The schematic of the second stage circuit.

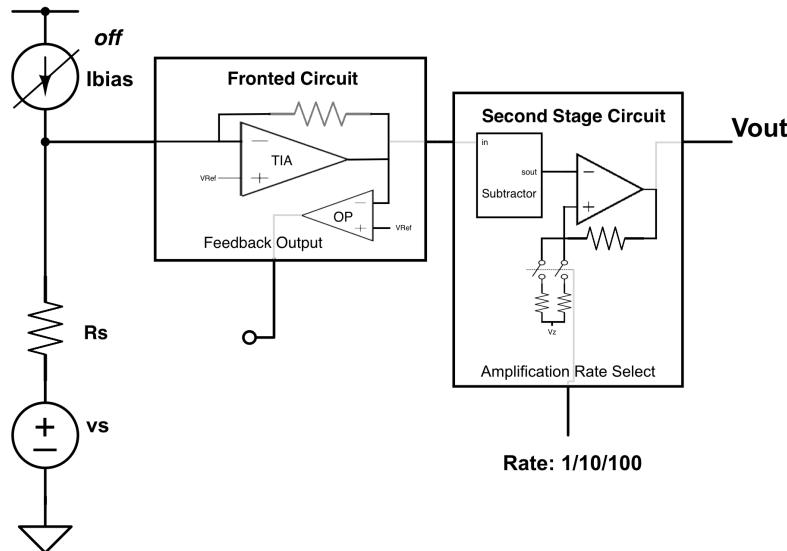
As in Fig.4.14, the Transient Measurement mode includes the second stage circuit and the Ibias and TIA from the fronted circuit. An analog subtractor and a resistor-based amplifier are included in the second stage circuit. The input signal can be sent from the gate or the source of nanowire ( $SiNW$ ).

### 4.2.1 The Second Stage Circuit

This section presents the important properties of the second stage circuit. To be notable that the performance of the subtractor and amplifier cannot be measured independently because there is no external pad connected to the output of the

subtractor. Besides, second stage input is always connected with the output of TIA. Due to the low output impedance of the TIA, it is hard to send input signal into the second stage circuit directly. Fig.4.15 is the alternative approach. The resistor  $R_s$  and the TIA compose a voltage amplifier. The input signal, which is usually triangular or sinusoidal, is injected through the  $R_s$ . It is then modulated in proportional to the ratio of  $R_s$  and TIA before being sent into the second stage circuit.

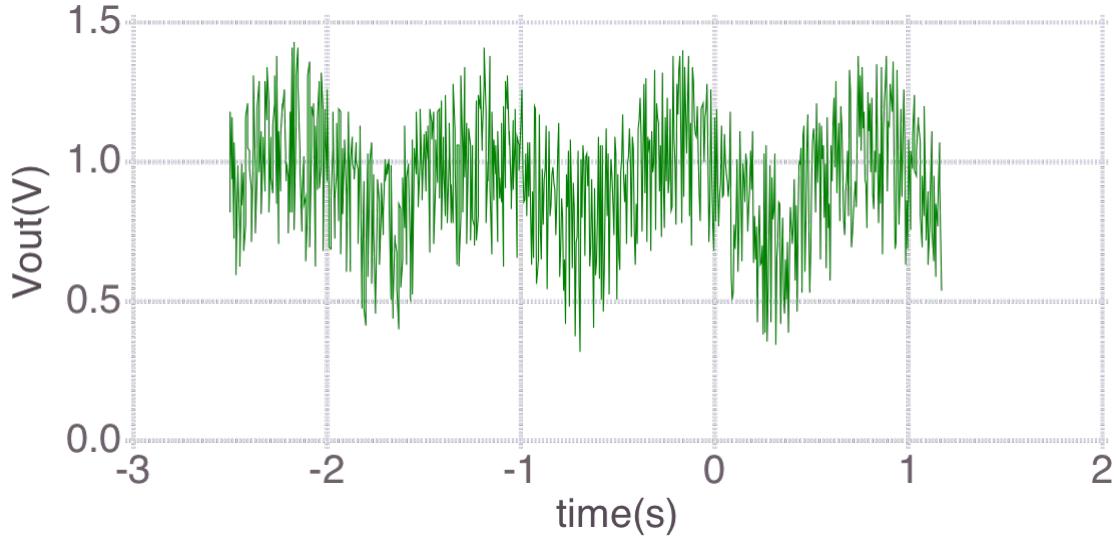
$$\text{Input of the } 2^{\text{nd}} \text{ stage circuit} = V_s \times \frac{\text{transimpedance of TIA}}{R_s} \quad (4.1)$$



**Figure 4.15:** The second stage circuit measurement approach.

#### 4.2.1.1 The Noise Oscillation Problem in Amplifier with Amplification Rate of 1

The amplifier in the second stage circuit has three amplification rate ( $A_{amp}$ ): 1, 10 and 100. The amplifier works well as the  $A_{amp}$  is 10 and 100. However, when  $A_{amp}$  is 1, the output signal is flooded with noise. In Fig.4.16, the input is a 1Hz triangle signal. Ideally, the second stage output should be a similar triangle signal. But in fact the signal is flooded with noise.

**Figure 4.16**

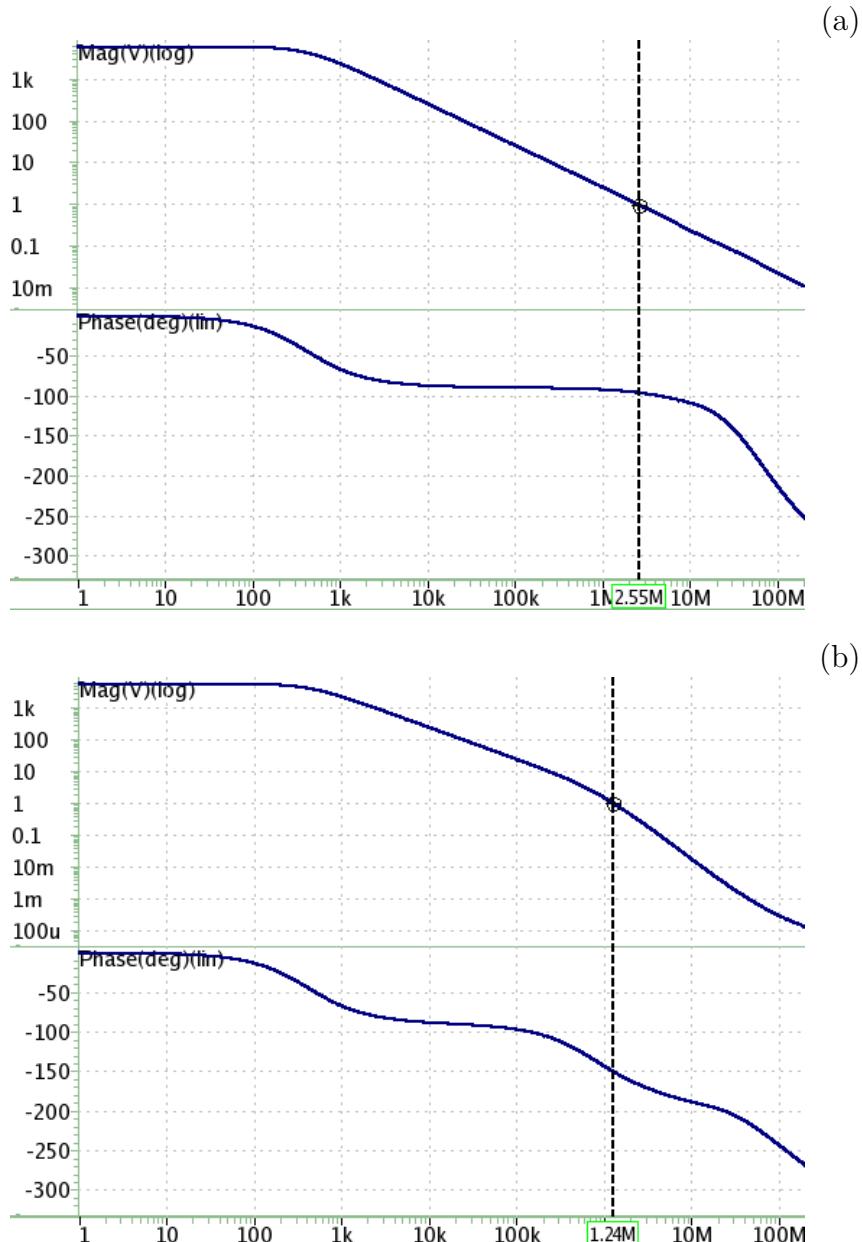
We suggest that the oscillation of noise signal should be the main cause of the problem. When designing the amplifier, we did not consider the parasitic capacitance brought by the switches and the pad (with ESD circuit) at the output. The simulation below proves our suggestion. The parasitic capacitance is modeled by a  $5pF$  capacitor. Fig.4.17(a) and (b) are the phase margin test of the amplifier before and after the capacitor is loaded on the output. The figures indicate that the second dominant pole locates at the output and the parasitic capacitors push it to the left. The phase margin is decreased subsequently.

The reason that the noise oscillation problem only happens when  $A_{amp}$  is 1 is because of the feedback mechanism. When  $A_{amp}$  is 1, the structure is similar to an unit-gain buffer (Fig.4.14(b)). In Fig.4.18, (a) is the feedback network of this structure while (c) is of the amplifier with  $A_{amp}$  is 10 and 100. To compute the loop gain, the structure is broken at the negative input and a tested signal is injected ( $V_t$ ) as illustrated in Fig.4.18 (b), (d). The loop gain ( $\frac{V_f}{V_t}$ ) of the two structure is derived as:

$$\text{when } A_{amp} = 1: \quad \frac{V_f}{V_t} = A_{op} \quad (4.2)$$

$$\text{when } A_{amp} = 10 \text{ or } 100: \quad \frac{V_f}{V_t} = A_{op} \times \frac{R_i}{R_i + R_o} \quad (4.3)$$

$A_{op}$  is the gain of the OP in the amplifier. ( $A_{op}$  is similar in two cases even if the



**Figure 4.17:** The post-simulation of the phase margin test of the amplifier when amplification rate is 1. **(a)** Without the parasitic capacitor, the phase margin is 108 degree. **(b)** With the parasitic capacitor (modeled by a  $5\text{pF}$  capacitor), the phase margin becomes 30 degree.

loading effect is taken into consideration because  $R_O \gg R_i$ .) Since the  $R_O$  is at least larger than  $R_i$  by 10-fold, two loop gains are different by 10-fold as well. The smaller loop gain increases the phase margin of amplifier by about 45 degree and diminish the oscillation (Fig.4.19).

We tried to dealt with the noise oscillation problem by the signal average tech-

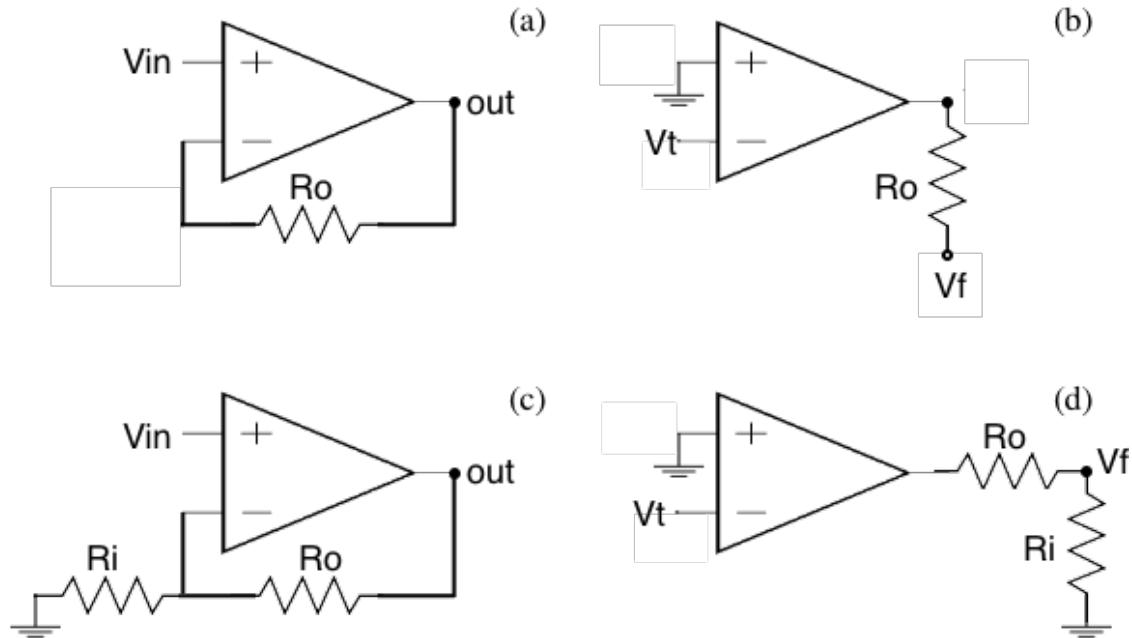
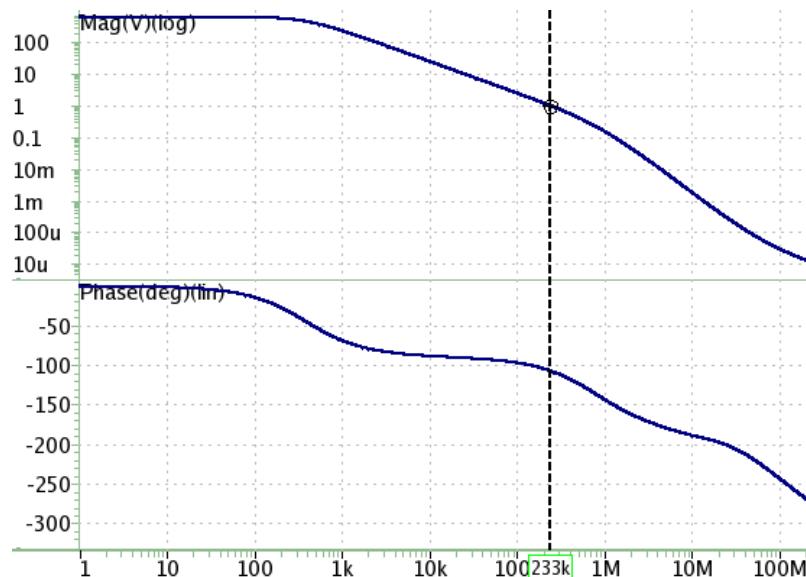


Figure 4.18



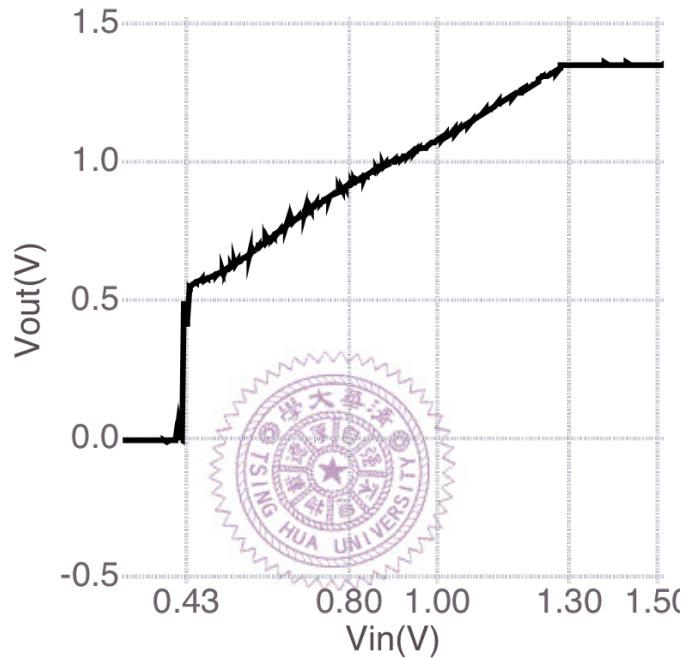
**Figure 4.19:** The post-simulation of the phase margin test of the amplifier when amplification rate is 10. With the parasitic capacitor loaded on the output(modeled by a  $5\text{pF}$  capacitor), the phase margin is 73 degree

nique. The output signal is averaged out to remove the noise component. However, the average of the signal may lie on the wrong offset. Therefore, the amplifier with  $A_{amp} = 1$  is used only when the signal trend is of interest (such as the dynamic in-

put range in Section 4.2.1.2). When the output signal is large and the amplification is not necessary, we simply measure the output of TIA.

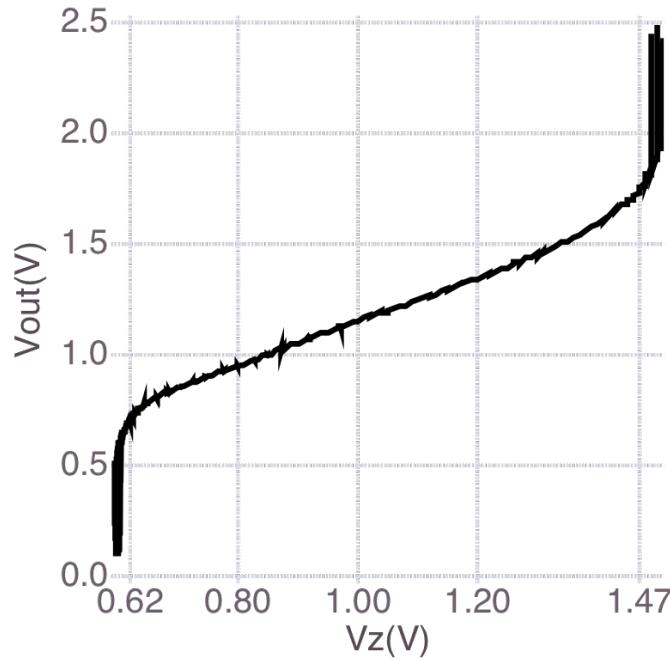
#### 4.2.1.2 Dynamic Input Range

Fig.4.20 is the input-output response of the second stage circuit ( $A_{amp} = 1$ ). It is used for finding the dynamic input range of the circuit. The linear region locates at  $V_{in} = 0.43V \sim 1.32V$ . According to chapter 5, this range is determined by the subtractor block.



**Figure 4.20:** The input-output response of the second stage circuit ( $A_{amp} = 1$ ).

Another input of the circuit is the  $V_z$  (Fig.4.14(b)). This voltage is for shifting the offset voltage. Its dynamic input range is measured and presented in Fig.4.21, which ranges from  $0.62V$  to  $1.47V$ . To be notable that ideally the input  $V_z$  should be equal to the output. But in fact an offset voltage of  $0.15V$  occurs in Fig.4.14 due to the noise oscillation problem mentioned in the last section. This offset does not exist when the  $A_{amp}$  is 10 and 100.



**Figure 4.21:** The input-output response of the second stage circuit. The input is  $V_z$ , which decides the output offset of the circuit.

Designed Amplification Rate	100	10	1
Measured Amplification Rate	93.3	9.2	1
Error Rate	7.7 %	8 %	0

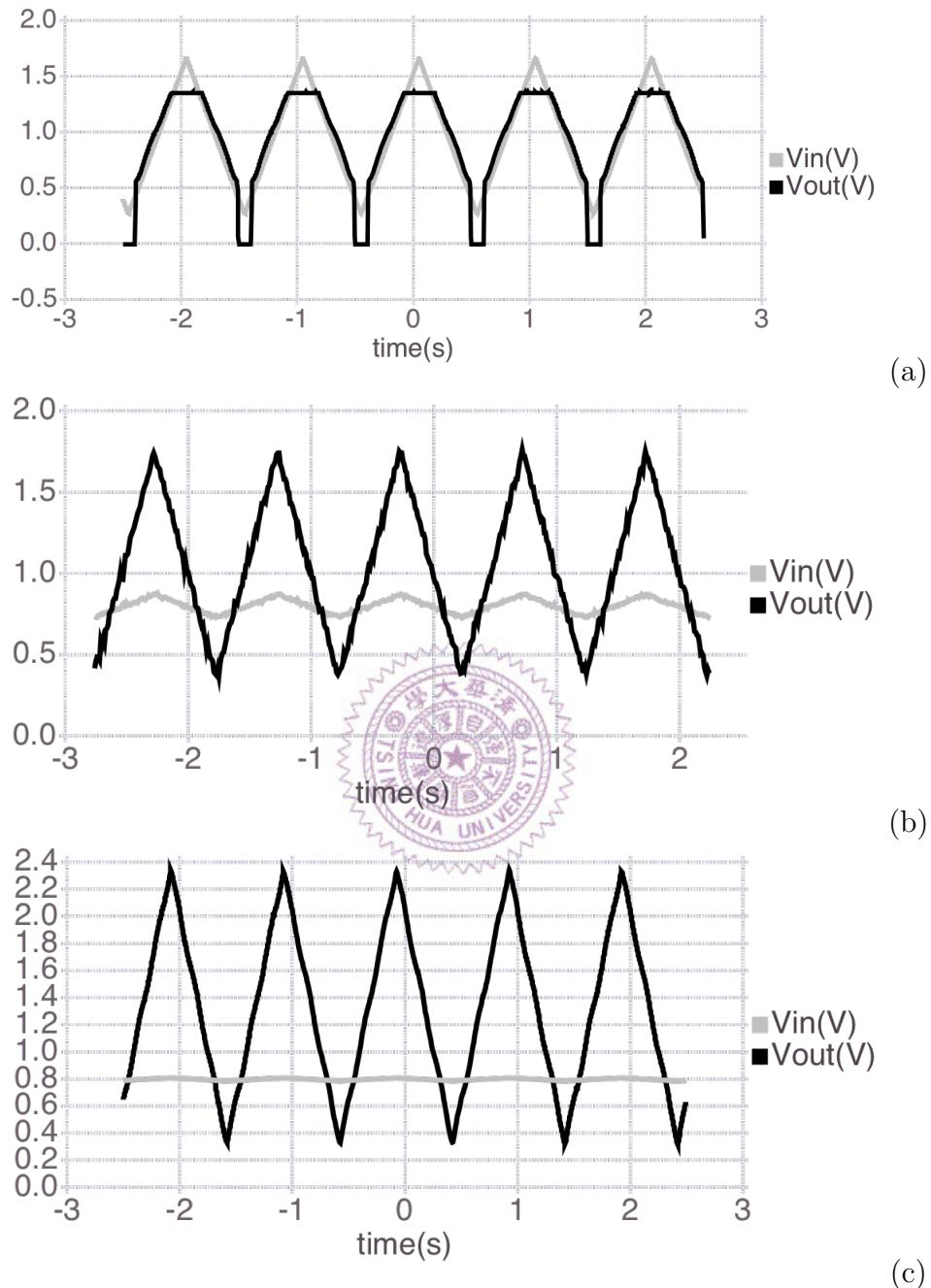
**Table 4.2:** Comparison between the designed and measured gain of the second stage circuit.

#### 4.2.1.3 The Circuit Gain

A triangle wave is sent to the end of  $R_s$  (Fig.4.15) and the input and output of the second stage circuit are recorded by an oscillation scope. Fig.4.22) (a), (b) and (c) are the time domain results when the  $A_{amp}$  is 1, 10 and 100 respectively. The exact gain values are summarized in the Table.4.2.

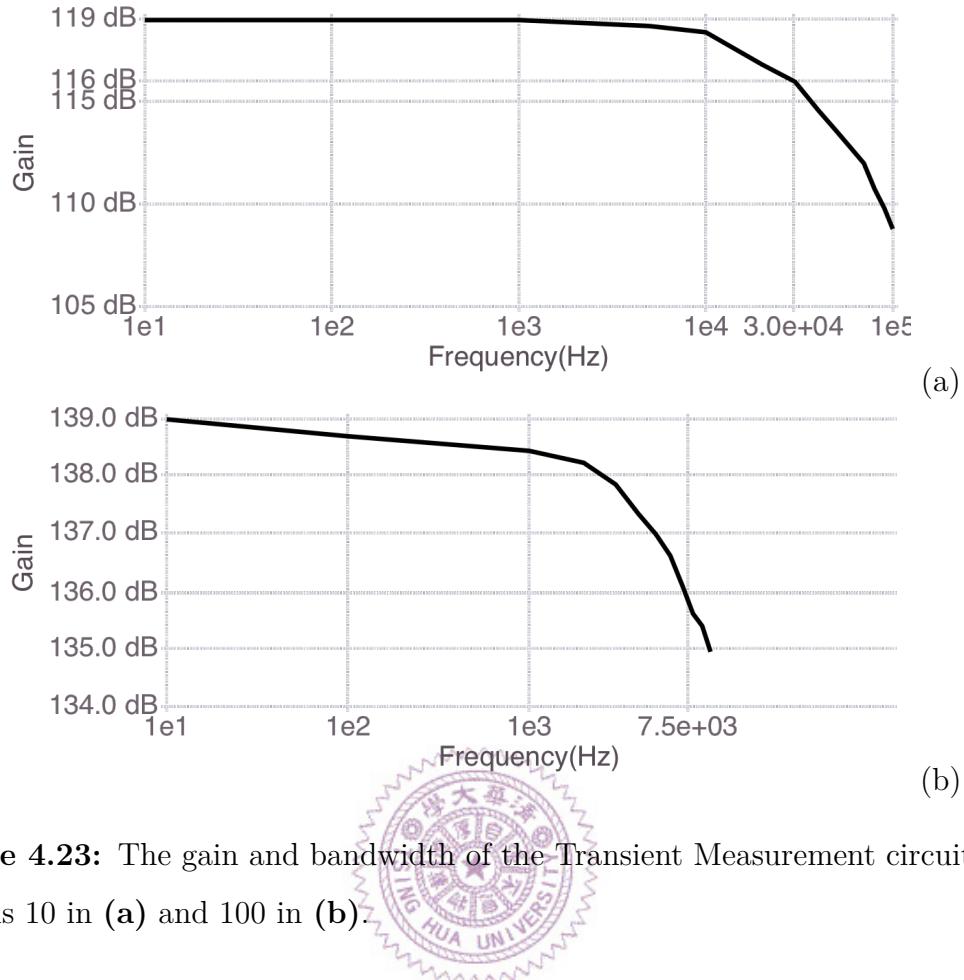
#### 4.2.2 Transient Measurement Mode

The second stage circuit and the TIA from the fronted circuit compose the circuit of Transient Measurement Mode. This section presents some of its important properties (gain, noise and bandwidth).



**Figure 4.22:** The input output signal of the second stage circuit in time domain when  $A_{amp}$  is (a) 1, (b) 10 and (c) 100.

#### 4.2.2.1 Bandwidth and Gain



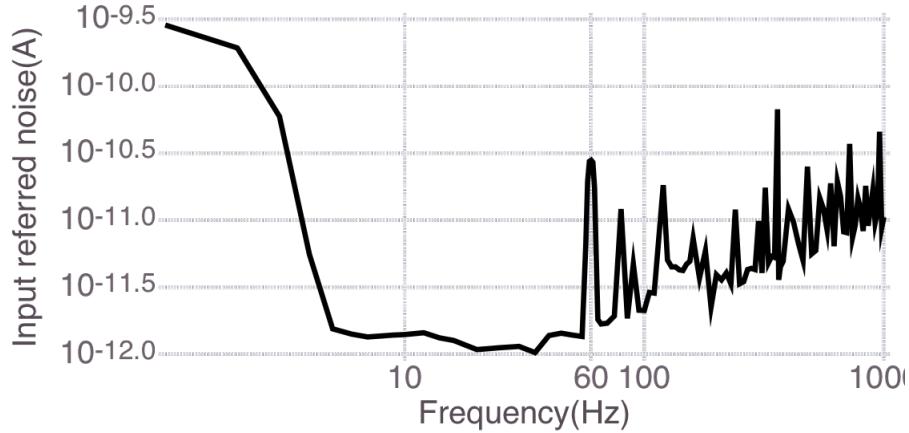
**Figure 4.23:** The gain and bandwidth of the Transient Measurement circuit. The  $A_{amp}$  is 10 in (a) and 100 in (b).

The gain is the input current to output voltage ratio. Because the noise oscillation problem may disturb the bandwidth measurement, we did not measure the circuit with  $A_{amp}$  of 1. The circuit with  $A_{amp}$  of 10 has gain of  $891k$  and bandwidth of  $30\text{kHz}$ . The circuit with  $A_{amp}$  of 100 has gain of  $8.9M$  and bandwidth of  $7.5\text{kHz}$ .

#### 4.2.2.2 Input Referred Noise

The spectrum analyzer are used to measure the noise. The power spectral density (PSD) of noise at the output of the circuit is measured and is referred to the input to show the equivalent input current noise (Fig.4.24). While measurement is performing, Ibias provides  $10\mu\text{A}$ , which is same to the condition of the post-simulation measurement (Fig.3.21). The primary type of noise are the low frequency noise (flicker noise). Other types of noise such as  $60\text{Hz}$  and  $80\text{Hz}$  come from the environment and working machines. They may be lowered by adopting better method

of experiment or equipments. Overall, the amount of noise is tolerable. The spec. from chapter 3 allows for a maximal input current noise of  $2nA$ .



**Figure 4.24:** Input referred noise of the Transient Measurement circuit.

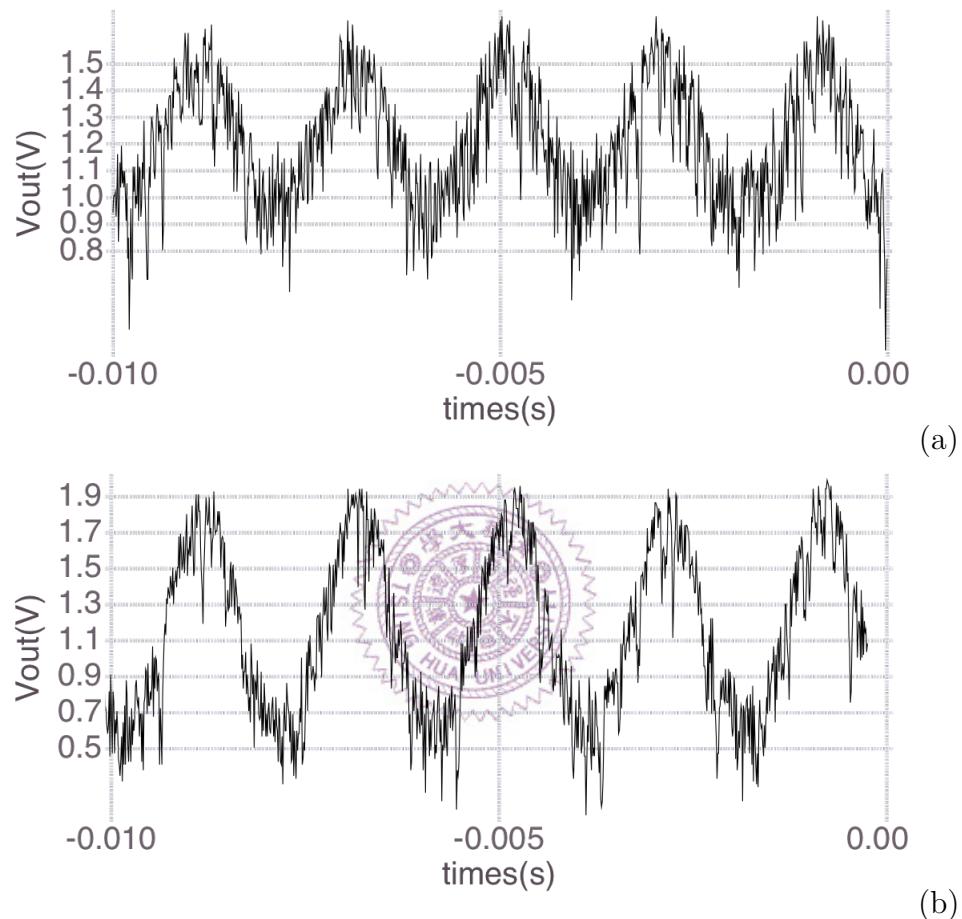
#### 4.2.2.3 Modulating biomolecule signals from the source terminal

The second usage of the Transient Measurement circuit is to apply a sinusoidal signal at the source of nanowire. In Fig.4.25, is obtained by this measurement method. The input is a sinusoidal signal with frequency of 500Hz and the amplitude of 0.5V. The nanowire was put under two solutions with different pH values in (a) and (b). After dividing the amplitude of the output signal by the transimpedance gain of the circuit (891k), we learned that the  $g_m$  of nanowire under these two pH solutions are  $1\mu$  and  $1.8\mu$ .

This method aims to modulate the biomolecule signal into higher frequency to avoid the flicker noise and other kinds of low frequency noise. However, from the result below, it can be observed that the output contains large amount of high frequency noise. We believe the noise comes from the testing solution and through the gate of nanowire. In the future, a bandpass filter with adjustable center frequency should be added to the circuit to filter the signal of the unwanted frequency.

#### 4.2.2.4 Summary of Transient Measurement mode

The Table.4.3 compares the chip properties and the specification for transient measurement mode. Although there is the noise oscillation problem, the overall perfor-



**Figure 4.25:** The output signal of the measurement using source of nanowire as input. The  $gm$  of nanowire in two figures are different by using testing solution with different pH values. The  $gm$  of nanowire is  $1\mu$  in (a) and  $1.8\mu$  in (b).

mance of the circuit is fine.

	Design Spec.	Chip Properties
IBias Current ( $I_D$ )	$600nA - 5\mu A$	$100nA - 50\mu A$
Dynamic Input Range( $\Delta I_D$ )	$\pm 2.8\mu A$	$5.3\mu A - -15\mu A$
Input Referred Current Noise	$< 2nA$	$< 0.3nA @ 1Hz$
Transimpedance Gain (max)	$5M(\frac{V}{A})$	$8.9M(\frac{V}{A})$
Bandwidth	$> 1k$ (Hz)	$7.5kHz$

**Table 4.3:** The comparison between the chip properties and the specification for Transient Measurement mode from chapter 3.

### 4.3 Dealing with the Device Variability Problem

This section presents the measurement with the proposed variability-resisting method.

Two nanowire devices (nw1-2, nw2-1) lying on the same substrate are under test. The  $I_D-V_G$  curves of two devices are obtained and substantiate that they have device variability problem (Fig.4.26(a)). These curves are then transformed into  $gm$ - $I_d$  curves (Fig.4.26(b)). Based on the conclusion of appropriate operation region (Section.2.2.1), the  $gm$  of  $2\mu$  is selected. The certain  $I_D$  under which devices are biased are therefore determined. As illustrated in Fig.4.26(b), nw1-2 is biased under  $340nA$  and nw2-1 is biased under  $900nA$ . The devices are connected with the circuit in Transient Measurement mode, where the bias current and gate voltage are set. Finally, the output response of two devices are presented in Fig.4.26(c) and (d). Two solutions with different pH values is used in substitution for the DNA solution. The pH value of solution A is lower than solution B. The lower pH value means the solution is more positive. Thus, solution B increase  $I_D$  and increases output voltage.

Two devices have similar output response, which suggest our method is functional. But still the responses are not exactly same. We can blame the inaccurate biasing current because the DC-sweep mode circuit fails in low current and the  $V_G$  is manually adjusted to make the  $I_D$  follows the biasing current. Still there may be other

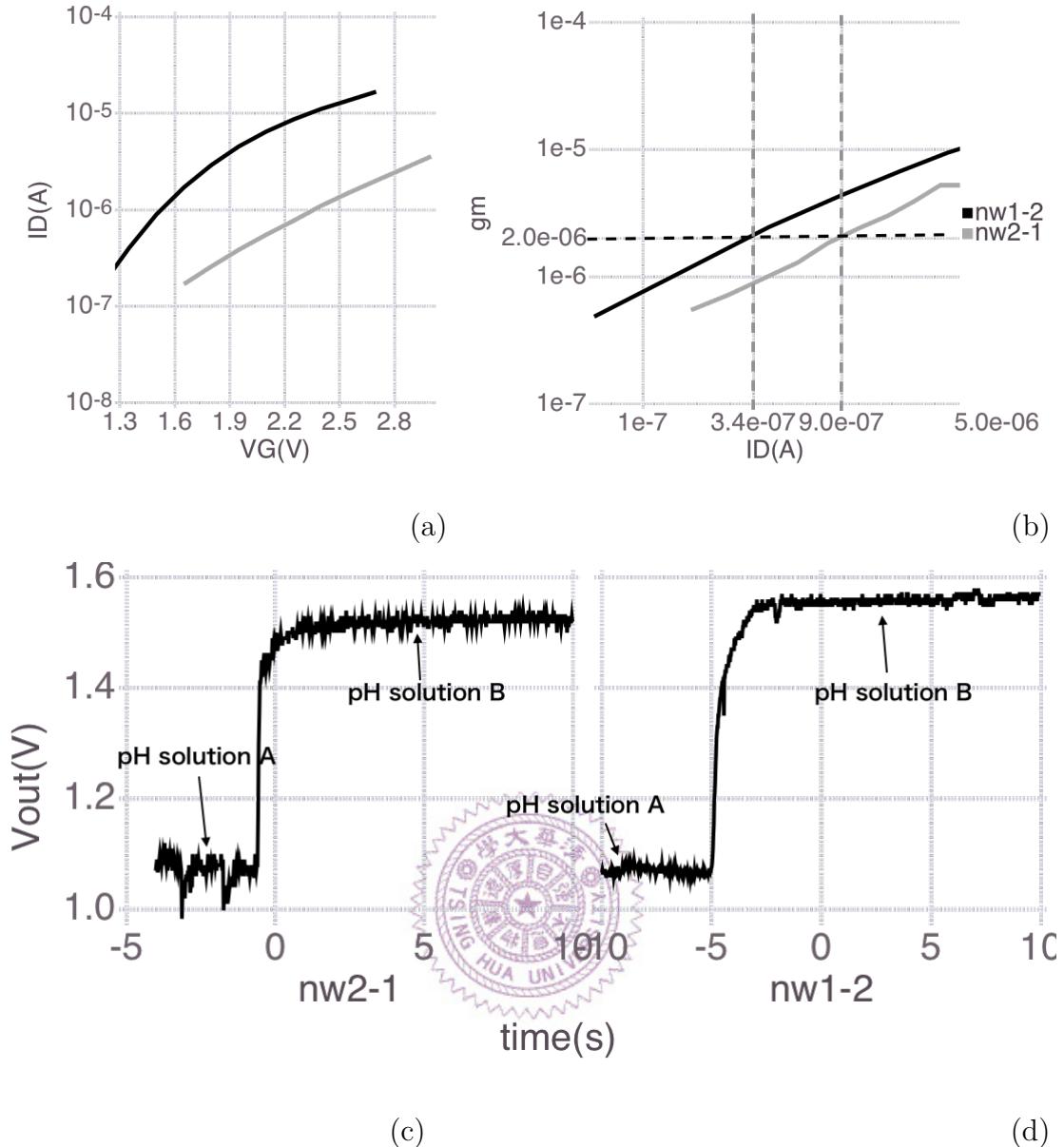


Figure 4.26

reasons.

Although we keep the devices under a same  $gm$ , the output signals can diverge if they receive incomparable input. The input of the experiment above is the equivalent voltage change induced by the concentration (pH value) difference ( $\Delta V$ ). Its value may be different because of two reasons. One is that the thickness of the each nanowire may not be same. There may be corrosion of the nanowire surface since the devices we use have been produced for more than 2 years and have been used repeatedly. The other is the gate coupling effect. The effect caused by the

double layer capacitance varies with the gate voltage, which we have mentioned in Section.1.3.

The first reason can be solved by producing a new device. The second reason need the improvement on circuit structure. This reminds us one of the advantages of source follower structure (Section.1.1.2). The structure keeps  $V_G$  constant and adjusts the source voltage of nanowire instead. But changing source voltage will as well change the drain-to-source voltage ( $V_{DS}$ ) of nanowire, which brings about the short channel effect. Therefore, in the future, if our circuit adopts the concept of source follower, the additional feedback network that keeps  $V_{DS}$  constant is required.

Overall, although our method does not entirely remove the device variability problem, it mitigates the problem. Furthermore, the improvement method is proposed and the progress can be looked forward.

## 4.4 Conclusion and Future Work

	[4]	[13]	This work
R meas range	1M - 1G	10 - 40k	
R meas error	< 2.5%	< 2%	
SNR	> 45dB	-	
Input referred noise	-	190 nV/sqrt(Hz) @ 5 kHz	
CMOS Technology	0.13um	0.18um	0.35um
Power consumption	14.82uW	2mW	1.48mW

**Table 4.4:** Specification Summary

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