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An Integrated Circuit Design for Silicon-Nanowire

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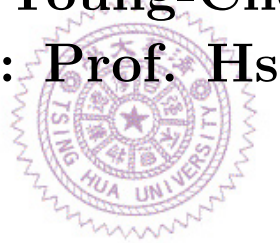

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Abstract

中　　文　　摘　　要

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Chapter 1

Introduction

1.1 Motivation

Poly-silicon nanowire(SiNW) is a well-studied and promising one-dimensional nanostructures. As reported by [4], there have been a lot of valuable research on fabrication and electrical properties. It was first introduced to the biosensor field in 2001[3] and has become a promising candidate for various features such as high surface-to-volume ratio, ultra sensitivity, label-free electrical detection and real-time measurement.

Although there have been substantial advances on nanowire structure design [6], the work of systems-level engineering is still insufficient. Systems designed for a specific purpose can help the device to meet practical needs such as noise reduction, real-time measurement, and analog-to-digital conversion. Moreover, there are still several challenges that may be overcome through a better signal acquisition system [6].

One of the challenges is that the mass production of robust nanowire elements is still improbable. Element disparity may be the main reason among others. This problem also happens to the measurement of our nanowire (Fig. 3.11). The nanowire we use is made by Professor Yang's team (National Chiao Tong University). And according to them, the nanowire use thick gate dielectric and have non-regular cross-sectional shape, which results in uncertainties of fabrication [8].

1.2 Introduction

In this project, we design a nanowire read-out circuit with two modes. In DC mode, one can use the circuit to perform a DC sweep of drain current (I_D) to show how the gate voltage (V_G) changes, or gives nanowire a constant I_D and measures the V_G response to different solution concentration. In AC mode, the circuit detects and amplifies the current variance of the nanowire with constant bias voltages applied (V_D, V_G, V_S). We also combine two modes to implement a proposed method that may mitigate the disparity problem.

Dealing with the Disparity Problem

The proposed method base on two assumptions:

1. The nanowire transconductance ($g_m = \frac{\partial I_D}{\partial V_{GS}}$) depends on I_D and independent on V_{GS}.
2. The concentration difference of biomolecule can be viewed as a voltage signal input to the gate end of a transistor.

The first assumption implies one can control the nanowire transconductance by its I_D. The second assumption means that as long as different nanowire elements have a same transconductance, the output current induced by a concentration difference should be same.

The method works as follows:

Initial stage At the beginning of each measurement event, we perform a DC sweep with the circuit in DC mode. By handling the sweep results with numerical method, we keep all nanowire elements under a selected transconductance by controlling their I_D and corresponded V_G.

Measurement stage We put the circuit in AC mode at this stage. Since the transconductance of all elements is same, they should behave uniformly based on assumption 2. At the end of the stage, we return to DC mode to reset I_D of the elements. The circuit adjusts their V_G to do so.

At the beginning of each measurement stage, an element always has a same I_D but different V_G. Based on assumption 1, its transconductance is kept constant.

The minutiae are reviewed in chapter 5. Currently, most operations are manual. We hope to make them automatic in the future, which may require digital circuit assistance.

1.3 Design Flow and Chapter Layout

In this thesis, there are six chapters sorted according to the design flow.

Chapter 2 reviews the basic theories and the literature that are related to our work. Most of those are the drain current of nanowire sweeping along the gate voltage (Id-Vg curves). We present some of the raw data and the analysis results in this part.

Chapter 3 gives a brief description of nanowire structure. It is then followed by two sections about some measurement and data analysis. The data of the first one is from the biological experiments while the second one is from the electrical measurement. We use the analysis results to design the read-out circuit.

Chapter 4 is an "accessory". This chapter contains the discrete circuit which was designed for ion-sensitive field-effect transistor (ISFET) [10]. We construct it and perform some electrical measurement. The purpose of this process is to practice the constant current method. The outcomes are deficient, and it is its reference value which we spotlight.

Chapter 5 talks about the schematic, design process and the simulation results of the read-out circuit.

Chapter 6 presents the measurement results of our integrated circuit and the conclusion of this project.

Chapter 2

Literature Review & Theory Description

As previously mentioned in the introduction section, the read-out circuit we proposed has two operation mode (DC and AC). The DC mode control the drain current (I_D) of nanowire while the AC mode is for current variance measurement. Each of them references different sources. In section 2.1, we first talk about the reason why we perform I_D-V_G sweep. Then we review the reference of our DC mode circuit design. The references of AC mode circuit design is in section 2.2. In the last section, we discuss the two assumptions mentioned in section 1.2.

2.1 DC Sweep: I_D-V_G Curves

In this section, we review the knowledge and an article that is related to our design of large signal mode (DC).

2.1.1 I_D-V_G and Transconductance

A common method for examining nanowire electrical properties is to perform DC sweep. Among all kinds of sweep method, we choose the I_D-V_G in respect of the physical characteristic. In the n-type transistor, the binding of negatively charged biomolecules induces surface-near silicon ions discharged and thus lower the threshold voltage. It is straightforward to think of these binding molecules as a voltage

signal input to the gate with its value depends on the concentration. And this voltage signal effect nanowire in the same way V_G does. So by plotting I_D-V_G curves, we can have a thumbnail of how concentration affects the I_D.

2.1.2 Source Follower

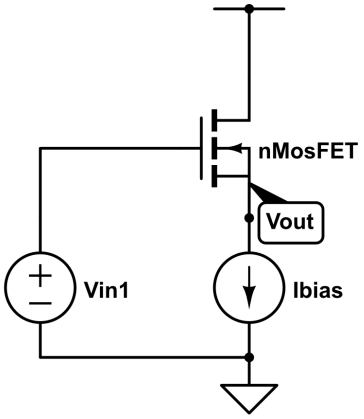


Figure 2.1: Sorce Follower

As one of the basic single stage amplifier, source follower (common drain) are employed to transfer voltage signal from gate to source while keeping drain current constant. The transfer function can be derived as:

$$\frac{V_{out}}{V_{in}} = \frac{r_{ds}g_m}{1 + r_{ds}g_m} \tag{2.1}$$

$$\approx 1 \qquad \text{for} \quad r_{ds}g_m >> 1 \tag{2.2}$$

g_m is the transconductance ($\frac{\partial I_d}{\partial V_{gs}}$) and r_{ds} is the drain-to-source resistance. Although we haven't seen the structure be applied to nanowire, there have been several applications in the read-out circuits of ISFET (Ion-sensitive Field-effect Transistor)[10, 12] for a long time.

The read-out circuit in [10] applied ISFET as a biological transducer that converts detected bio-signal into the electrical signal, which resembles our nanowire biosensor. Its adopt source follower structure as its analog front-end. The bio-signal induced voltage difference at the ISFET gate-end is converted to the source-end. This structure requires a biasing current source which may have to be stable, noiseless or wide-range on demand. Since the bias current is usually under micro-scale

even nano-scale, it is impractical to use an external current source merely. The article used two resistors and an op-amp to design a current scale down circuit. Bias current decreases in proportional to the resistance ratio (N) of one resistor to another. Moreover, by keeping Vds at a constant value (0.5v), the circuit also removes the short channel effect. Below show the schematic where two op-amp based unit gain buffer are added to force the voltage at drain-end follows the source-end.

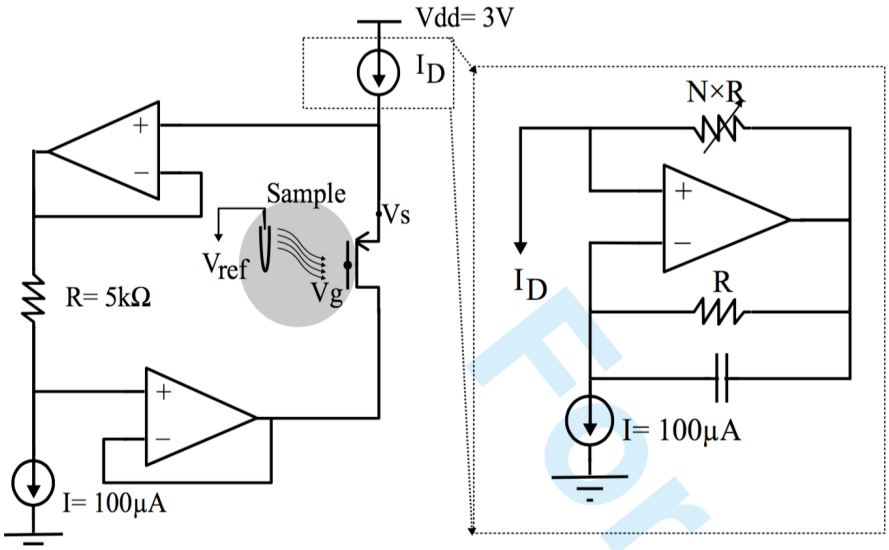


Figure 2.2: ISFET readout circuit in [10]

An issue needed to be aware is the impedance matching between the element and the current source circuit. The output impedance of current source should be much larger than the input impedance of the biasing element. The equation for the output impedance of source follower is:

$$\frac{r_{ds}}{1 + g_m r_{ds}} \tag{2.3}$$

This equation can be simplified as:

$$\frac{1}{g_m} \qquad \text{for} \qquad g_m r_{ds} >> 1 \tag{2.4}$$

The output impedance of the current source circuit is:

$$N \times R_s \tag{2.5}$$

R_s is the impedance of the right-bottom current source in Fig.2.2. In the integrated circuit, R_s is not ideal but usually close to the r_{ds} of a single MOSFET.

As mentioned, Eq.2.5 should be far larger than Eq.2.4. However, g_m is proportional to I_d, which means Eq.2.4 is inversely proportional to N. When the bias current decreases, the output impedance decreases while the input impedance at the ISFET source-end increases. Therefore, there is a lower boundary of the bias current. We observed this boundary when we construct this circuit with discrete elements. These will be presented and discussed in chapter 4.

The source follower structure provides a direct signal transition method. It is a good candidate for the read-out circuit with the aim of detecting transconductance or threshold voltage variance. Nevertheless, post-processing such as amplification and filtering are necessary. The experiment results in the article are untreated. Strong signal attenuation exists, which are mainly caused by low-frequency noise and ISFET drift [9]. The drift problem is dealt with through signal processing techniques while noise problems are left untreated.

2.2 Small Signal (AC) Measurement Method Review

In the previous section, the source follower we mentioned exhibited compelling advantages as a signal processing structure of nano-device. However, the structure overcomes obstacles when being applied to the small signal detection. Parasitic capacitors and resistors can severely influence the results.

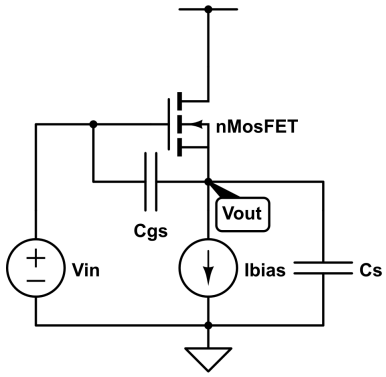


Figure 2.3: Sorce Follower with parasitic capacitance

As in figure 2.3 where the parasitic elements are included, we modified the transfer function Eq.2.2 as:

$$\frac{V_{out}}{V_{in}} = \frac{r_{ds}(sC_{gs} + gm)}{1 + r_{ds}(gm + s(C_{gs} + C_s))} \tag{2.6}$$

The equation can be similar to Eq.2.2 which roughly equals to 1 as long as C_s is far more smaller than C_{gs}. Unfortunately, C_s can be large for the output end of source follower usually connects to a next stage input or a pad. In that case, the parasitic capacitors may attenuate the signal.

We want to build another circuit structure that can not only performs AC signal measurement but also immunes from parasitic capacitance. We started by reviewing those works that try to measure the parasitic capacitance. Below, the works from two teams aim to measure drain-to-source resistance (R_{NW}) and drain-to-source capacitance (C_{NW}). The focus of the review is on the function and design theory of their read-out circuit.

2.2.1 RC Time Delay Measuring

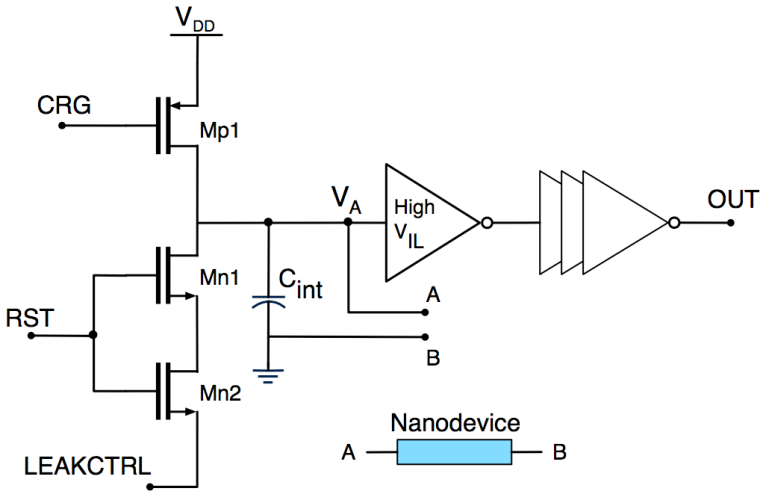


Figure 2.4: (a) Schematic of [1].

The measurement system for ZnO-nanowire based sensor array from [1] applies the Time-over-Threshold techniques to its read-out circuit (Fig.2.4). The circuit alternatively charges an on-chip capacitor (C_{int}) with a constant current and discharges it through the nano-material resistance (nanowire). An inverter with its output

switches from on to off when the capacitor is charged to its input threshold voltage, and vice versa. This behavior converts information of nanowire such as capacitance and resistance into time information. Both C_{int} and C_{NW} effect charging time and together with the R_{NW} effect the discharging time.

The work presented in [1] doesn't have enough explanation about how do they interpret the capacitance and resistance information. It merely mentioned that a microcontroller is responsible for the calculation. Besides, the work lacks simulation and experiment of using complex elements as measured target. Most of the results are the measurement of using a concrete resistor as the substitute for nanowire and regard the C_{NW} as 0p. The only nanowire experiment given at last doesn't have good performance. It seems that the design may only be applied to a pure resistance or pure capacitance type element.

The recent publican [2] by the team is more elaborate and contains the measurement of complex elements (An element composed of a discrete resistor and a discrete capacitor).

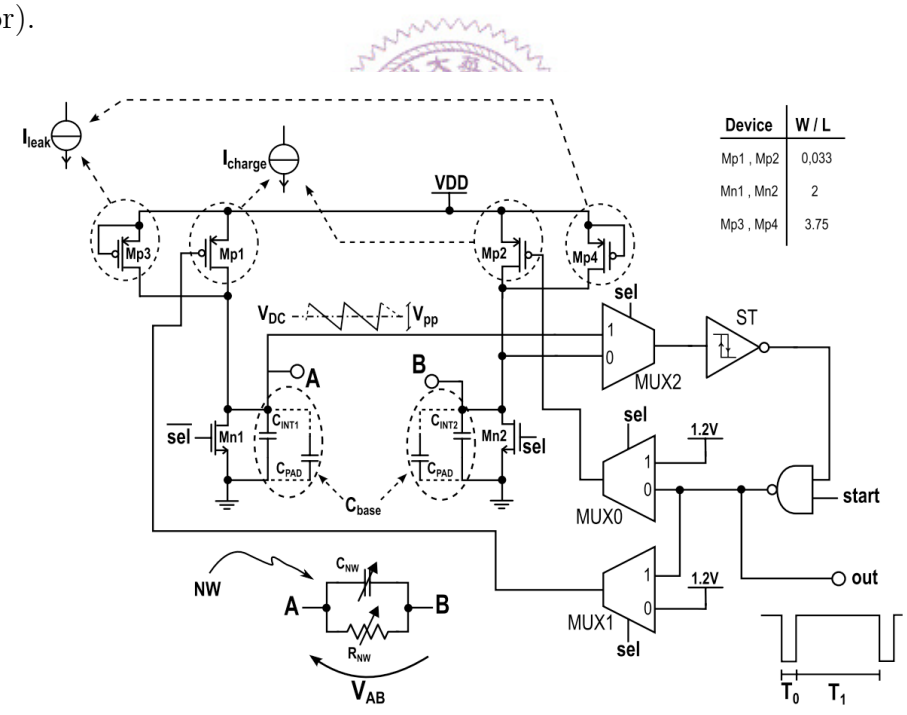


Figure 2.5: Schematic of [2].

In Fig.2.5, nanowire append between point A and B. The charging current can be applied from Mp1 or Mp2, which is determined by the "sel" signal with the aid from the MUXs. We simply assume sel = 1 and point B is virtually ground. (When

the sel = 0, the circuit measures the element with a reversed biasing current.) Now, we can see that the circuit design concept is same with [1]. The current charge both C_{int} and C_{NW}. When the voltage at A exceed the threshold voltage, the output switches to off and feedback to turn off the Mp1. (To be noted that a Schmitt trigger replaces the inverter at the output stage in [1].) Then the capacitor discharges through nanowire (r_{ds}).

The right-bottom plot in Fig.2.5 defines T_0 as the charging time and T_1 as the discharging time. The calculation of the R_{NW} and C_{NW} can be simplified as:

$$C_{NW} = T_0 - C_{base} \tag{2.7}$$

$$R_{NW} = \frac{T_1 R_{par}}{(C_{NW} + C_{base})R_{par} - T_1} \tag{2.8}$$

$$\text{where} \qquad R_{NW}||R_{par} = \frac{T_1}{C_{NW} + C_{base}} \tag{2.9}$$

C_{base} are the C_{int} plus parasitic capacitance and R_{par} the parasitic resistance. These parasitic elements come from the transistor in the integrated circuit block such as MUX and Mp. It must be noticed that we don't concern the hysteresis of the Schmitt trigger here owing to simplicity.

2.2.2 Complex Impedance Solving

The nanowire-based hydrogen sensor measurement system from [13] adopts another method. It treat It use a lock-in amplifier to realize both resistive and capacitive impedance measurement.

As the previous method, it treats nanowire as a complexed one-dimensional element. The nanowire is modeled as a parallel aligned resistor and a capacitor. The system supplies a sinusoidal voltage signal to one end of the element. Another end of the element is grounded virtually by a transimpedance amplifier (TIA). The TIA then converts the current variance into voltage output which contains complex impedance information. The resistance is in the real part while the capacitance is

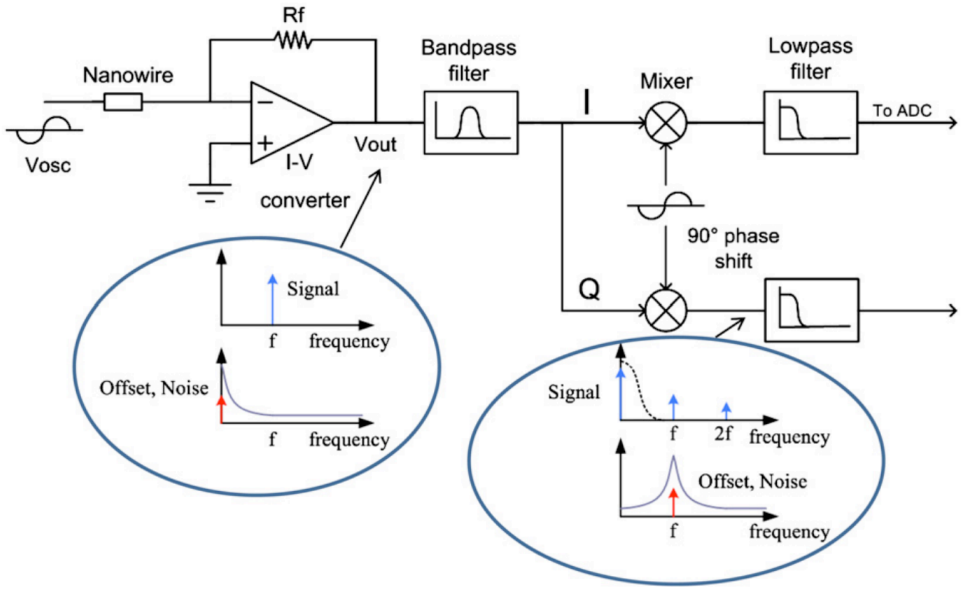


Figure 2.6: Block diagram of the lock-in amplifier in [13]

in the virtual part.

$$V_{out} = I_{NW} R_{TIA} \tag{2.10}$$

$$I_{NW} = V_{in}(\frac{1}{R_{NW}} + j2\pi f C_{NW}) \tag{2.11}$$

f is the frequency of input signal.

The output of TIA is followed by a controllable bandpass filter (BP). The BP removes high-order harmonic interferences. Then the signal is demodulated. The resistive and capacitive impedance values are resolved through two channels: I and Q with their phase different by 90 degrees. A mixer which is a linear multiplier performs the demodulation. With a radio frequency (RF) input and the input local oscillator (LO) input, it produce an output signal that consists of signals with frequencies $f_{RF} + f_{LO}$ and $f_{RF} - f_{LO}$. Incidentally, the signal is immune from the perturbation of low-frequency noise which is a common problem for the biosensor.

2.2.3 Comparison and Conclusion

We compare Method 1 (Sec.2.2.1) and Method 2 (Sec.2.2.2) here. Both of them focus on detecting the R_{NW} difference. According to the comparison table below (2.1), we can see the resistor measurement range of Method 1 is different from

Method 2 by a large extent. This may because the maximum and minimum bias current of nanowire provided by the circuits are different. The current in Method 1 is limited by the pmos(I charge) and the leakage current. In Method 2, it is limited by the TIA. Our method adopts this TIA block and will discuss this problem in section.5.1.1.1.

Method 2 perform well when it comes to noise suppression. In fact, the circuit in Method 1 doesn't provide noise reduction ability. The particular structure it uses (The article [1] mentioned it as M4N approach) is the one responsible for that.

Method 1 has a lower power consumption. However, it doesn't include the power of microcontroller and may underestimate.

	[2]	[13]
R meas range	1M - 1G	10 - 40k
R meas error	$< 2.5\%$	$< 2\%$
C meas range	100fF - 1uF	0.5 - 1.8nF
C meas error	$< 3\%$	$< 3\%$
SNR	> 45dB	-
Input refered noise	-	190 nV/sqrt(Hz) @ 5 kHz
CMOS Technology	0.13um	0.18um
Power consumption	14.82uW	2mW

Table 2.1: Specification Summary

In our project, capacitance measurement is not our object. But we still need to consider the parasitic capacitor effect in our circuit design. Method 1 converts the resistance information into time (frequency) information. If one want to avoid the effect of the parasitic capacitor, he should apply a C_{int} that is much larger than C_{NW}. However, it is not practical in integrated design because the chip size is limited.

Method 2 uses a TIA to measure resistance and capacitance together first and then resolve the complex value. We can write the complex impedance value as:

$$\frac{R_{NW}}{1 + i2\pi f R_{NW} C_{NW}} \tag{2.12}$$

In Eq.2.12, i is the imaginary unit and f is the signal frequency. The equation can be simplified as R_{NW} when $i2\pi f R_{NW} C_{NW} < 0.1$. The simplification can be applied when the signal frequency or $C_{NW}R_{NW}$ is small enough. Thus, one needs to select the appropriate signal frequency or to determine the R_{NW} detecting range.

Another reason that makes Method 2 more attractive is that it is more flexible. One can add other analog blocks such as noise filter or amplifier to it.

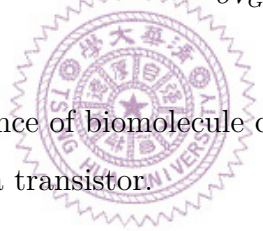
Overall, Method 1 has the advantage in detecting range and accuracy while Method 2 has better noise suppression and flexibility.

2.3 Two assumption for Dealing with Disparity Problem

In chapter 1, to deal with disparity problem, we assume that:

1. The nanowire transconductance ($g_m = \frac{\partial I_D}{\partial V_{GS}}$) depends on I_D and independent on V_{GS}.

2. The concentration difference of biomolecule can be viewed as a voltage signal input to the gate end of a transistor.



We discuss them in this section.

2.3.1 Transconductance and I_D

With the MOSFET model of weak and strong inversion, we have the I_D equations of MOSFET:

$$\text{weak inversion:} \quad I_D = I_0 e^{\kappa V_{GS}/\phi_t}(1 - e^{-V_{DS}/\phi_t}) \tag{2.13}$$

$$= I_0 e^{\kappa V_{GS}/\phi_t} \quad \text{where } V_{DS} > 4\phi_t \tag{2.14}$$

$$\text{strong inversion:} \quad I_D = \mu C_{ox}\frac{W}{L}((V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}) \tag{2.15}$$

$$= \mu C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2 \quad \text{where } V_{DS} > V_{GS} - V_{th} \tag{2.16}$$

C_{ox} is the oxide capacitance and μ is the electron mobility. Both of them depends on doping concentration. W and L are the width and length of the transistor. ϕ_t is the thermal voltage depending on temperature. The κ is the gate coupling coefficient. It will be discuss in the next paragraph. To be noted that we ignore the short channel effect, which doesn't effect our discussion since we always keep V_{DS} constant.

We then derive g_m:

$$\text{weak inversion:} \quad g_m = \frac{\kappa I_D}{\phi_t} \tag{2.17}$$

$$\text{strong inversion:} \quad g_m = \sqrt{2\mu C_{ox}(\frac{W}{L})I_D} \tag{2.18}$$

$$\tag{2.19}$$

For the strong inversion, the Eq.2.19 shows that the assumption 1 is correct. However, the assumption is not completely right for transistor in weak inversion. According to the Eq.2.18, the g_m is effect not only by I_D but also by the κ. It is a non-linear parameter effected by V_G and other factors. Its value is range from 0.4 to 0.9. In our circuit, this problem is currently left unsolved. We present its effect in chapter 6.

2.3.2 A Simple Model for Concentration Affect

In [5], the team plot the I_D-V_G curves and study how the curve changes with the concentration of biomolecules. We observe that in the plot (Fig.2.7) with a log scale

for the y-axis, curves with different concentration exhibit a same rising trend when I_D is low (< 100nA). Each curve seems to be different with the other by a constant fold. By applying the weak inversion current equation of MOSFET, we found that the assumption can explain this concentration effect.

$$I_D1 = I_0 e^{\kappa(V_{GS}-V_{th})/\phi_t} \tag{2.20}$$

$$I_D2 = I_0 e^{\kappa(V_{GS}-(V_{th}-v_c))/\phi_t} \tag{2.21}$$

$$\rightarrow I_D2 = f(v_c) \times I_D1 \quad \text{where} \quad f(\Delta v_g) = e^{v_c/\phi_t} \tag{2.22}$$

The I_D1 and I_D2 are the current of two nanowire elements placed in solutions of different concentration. The (v_c) is a concentration related variable we create. The Eq.2.22 implies that when nanowire is in weak inversion region, its $\log I_D$ difference is independent of V_g.

$$\log I_D2 - \log I_D1 = \log \frac{I_D2}{I_D1} = \log f(v_c) = v_c/\phi_t \tag{2.23}$$

As for strong inversion region which refer to the large current section in Fig.2.7, the difference of the curves diminish as V_G increasing. The strong inversion equation (Eq.2.16) shows that if V_{GS} is far larger then v_c, the concentration effect can be ignored.

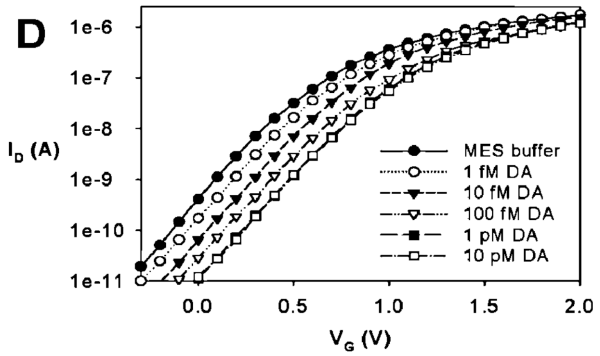


Figure 2.7: Concentration-dependent electric response($I_D - V_G$) of biotin-modified poly-Si NWFET following biotin–streptavidin interaction.[5]

We will further prove the two assumptions by the data of biology experiment in section.3.2.2.

Chapter 3

Nanowire Structure and Measurement

In this chapter, we present the experiment data and some analysis which are the foundation of our circuit design. The first section gives a brief description of our silicon nanowire element. The second section provides the data of the biology experiments. The last section presents the data of the electrical measurement, on which our circuit design spec depends.

3.1 Brief Description of Nanowire Structure

The nanowire we use is made by Prof.Yang's team (National Chiao Tong University)[7]. Fig.3.1 is the sectional view of the nanowire structure. The fabrication process is based on the poly silicon sidewall spacer technique. The n-Type doped poly-SiNW FET has two to ten poly silicon channels. Each channel is 80nm in width and 2μm in length. A Large portion of the channel surface is exposed to environment. The exposed region, through several post-process, capture the DNA probe and serve as the sensing site for DNA molecules.[7, 8]

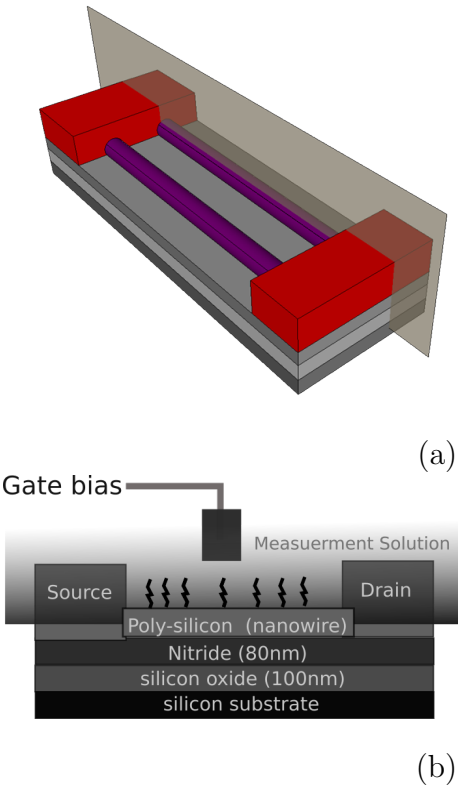
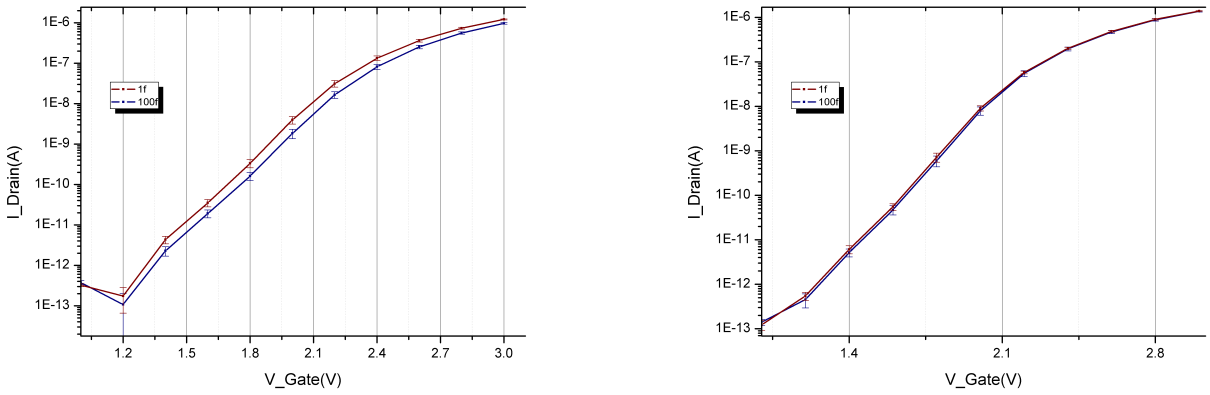


Figure 3.1: Nanowire Structure. (a) A nanowire element with two poly silicon channels. (b) is the sectional view of the cutting plane in (a).

3.2 Biology Experiment

The biology experiment data are provided by Prof.Yang's team. These data are the Id-Vg measurement of the same biomolecule placed under different circumstances or with different nanowire elements. With each measurement repeated three times, we find the mean and standard deviation (SD) of them and consider the SD value as the intrinsic noise of nanowire. We want to ensure that such noise should not be greater than the signal. To be more specific, we examine whether the Id-Vg curves of different concentration overlap with each other or not. We present an example below:

Fig.3.2 are concentration-dependent measurements (1 femto mole(fM) and 100fM biomolecule solution) obtained with two elements ((a) and (b)). The two curves in the (a) are distinguishable from the other after gate voltage of 1.4v They are not distinguishable in the (b) since they overlap each other. We thus assert that the element of (b) can't detect the concentration difference between 1fM and 100fM.



(a) (b)

Figure 3.2: Concentration-dependent I_D-V_G curves of two equivalent nanowire elements. In (a), the measurement result of 1fM and 100fM biomolecule solution is distinguishable. There is no overlap between two curves. This is not true in (b).

The noise is stronger than the signal (The signal means the I_D difference caused by the concentration difference). The element of (a) can do so if it is biased at gate voltage larger than 1.4v or drain current larger than 1E-11.

In Fig.3.3, I_D increase with the biomolecule concentration. One can find that there is only a few "space" between PBS buffer and solution containing biomolecule with the concentration of 100aM. Hence the 100aM should be the limit of detection.

It is worth noting that there is more space between 100aM and 10fM than the space between 10fM and 1pM. And the noise rate: $SD/Mean$ is independent of concentration (Fig.3.4). Hence we say that the "resolution" for detecting concentration ranging from 100aM to 10fM may be better than the that ranging from 10fM to 1pM.

3.2.1 Appropriate operation region

In [8], the team found that "the induced change of current (I_D) following biomolecule was dependent on the applied gate voltage (VG)" (Fig.). In other words, a "biomolecule concentration resolution" seems to depend on V_G The team tried to find a bias gate voltage range which can induce more current response. In our opinion, the induced change of current (I_D) following biomolecule is not directly dependent on V_G. Based on the our assumption 2 (section1.2), it depends on the transconductance. The phe-

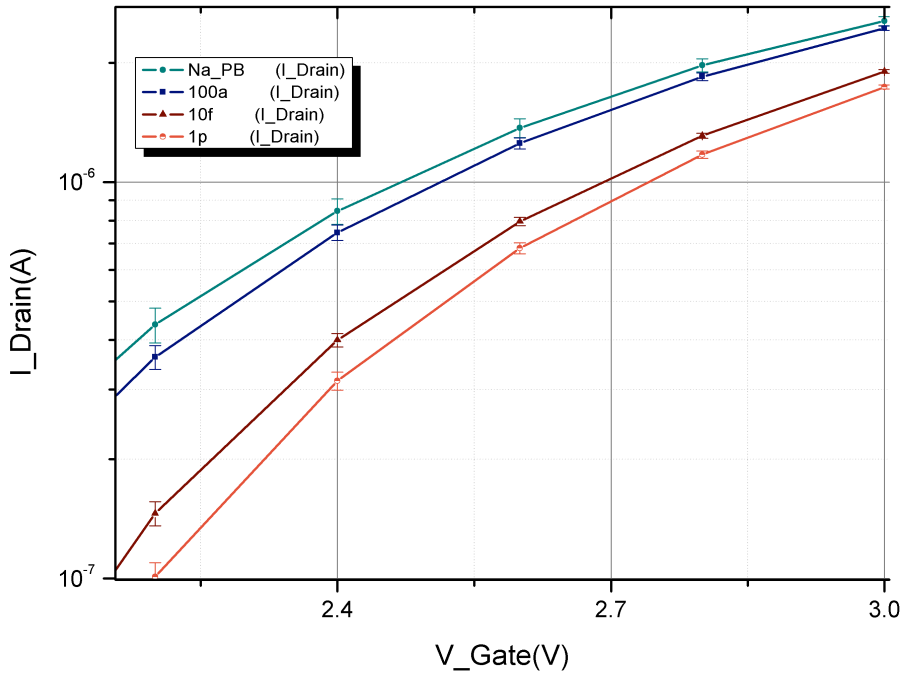


Figure 3.3: Concentration-dependent I_D-V_G curves with concentration of Na_PB(Buffer solution only), 100aM, 10pM, 1pM. Since the biomolecule is negative-charged, the lower the concentration is, the higher the curve is. To be noticed, the 10fM curve is closer to the curve of 1pM than 100aM.

nomenon is found by I_D-V_G curves, which means the V_G also affect the I_D which cause different transconductance.

Furthermore, we think the noise effect should be taken into consideration. Some kinds of noise have positive correlations with transconductance.

Still, we want to find an appropriate operation region of nanowire that has the largest concentration resolution. We proposed a comprehensive method that one should choose the operation region with more "noise tolerance". The noise tolerance is defined as:

$$noise \quad tolerance = \frac{I_D1 - SD1 - (I_D2 + SD2)}{I_D2} \tag{3.1}$$

I_D and SD are the mean and standard deviation of a curve. The larger the noise tolerance implies there is more space between two curves. And more space implies the less chance of overlapping between to concentration curves may happens.

We present analysis results from three nanowire elements. Fig.3.5(a), (c), (e) are the I_D-V_G curves of three elements and Fig.3.5(b), (d), (f) are the noise tolerance

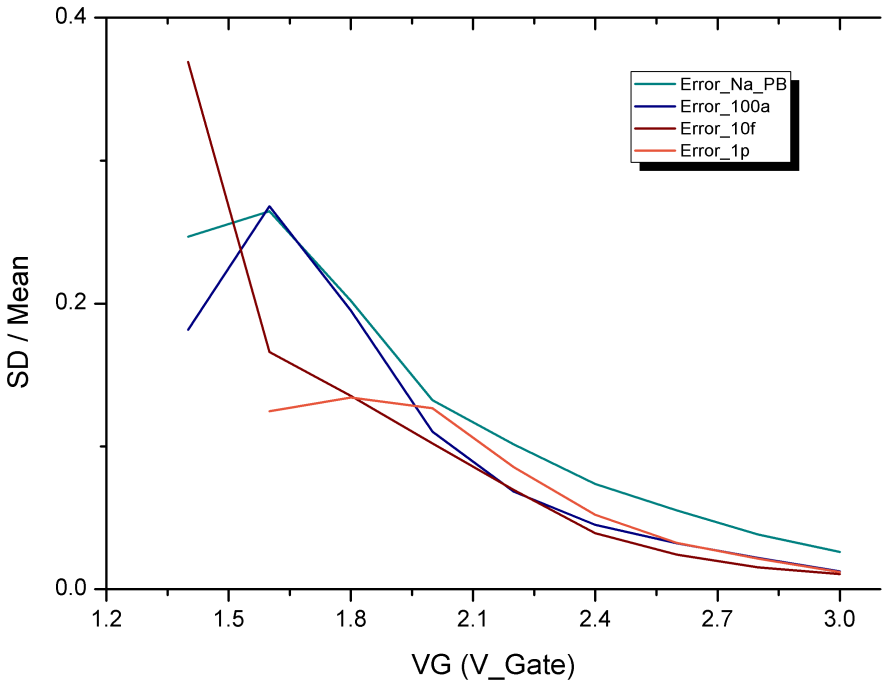
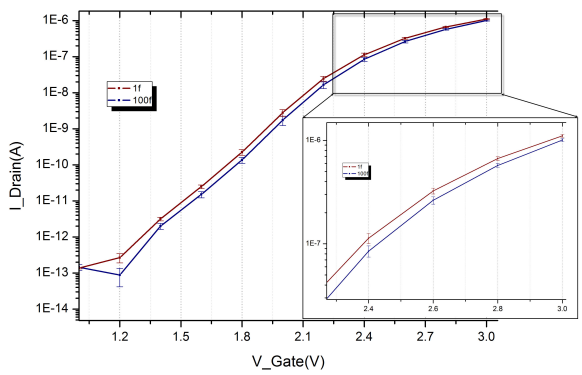
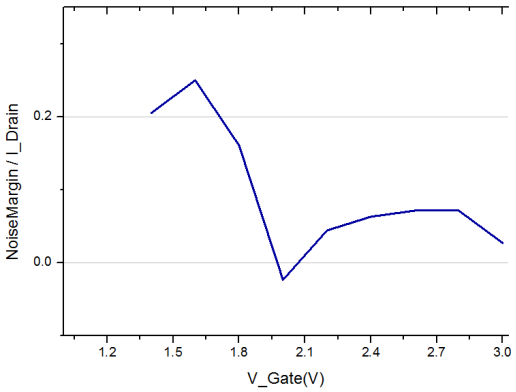


Figure 3.4: The noise rate of Fig.3.3. The noise rate is obtained by dividing SD by Mean.

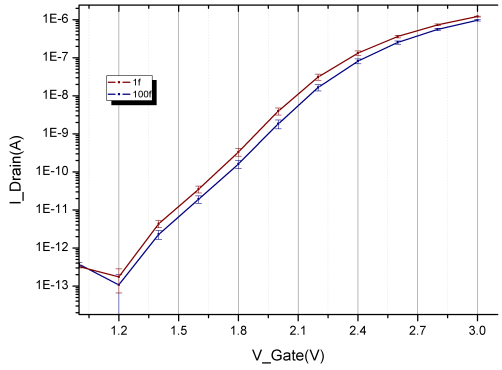
respectively. One can observe in (b) and (d) that there is first a rising trend then followed by a drop as gate voltage decreases. The drop doesn't exist in (f) may because the weak inversion is too narrow. The transistor enters into the reverse region before the drop appears. The highest points of (b) and (d) locate in the weak inversion region and is close to the transition region (The region between strong inversion and weak inversion region). We therefore suggest that in this section nanowire should has the largest concentration resolution.



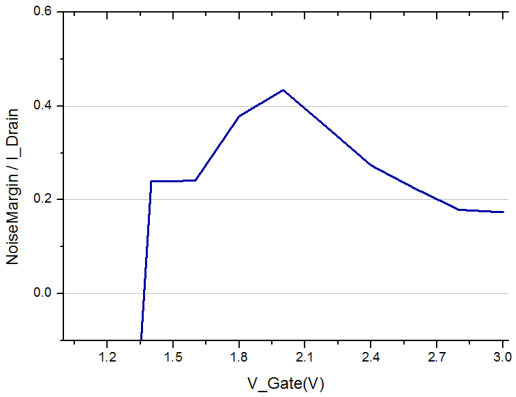
(a)



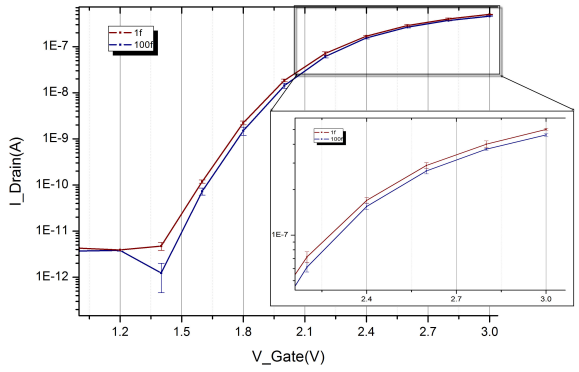
(b)



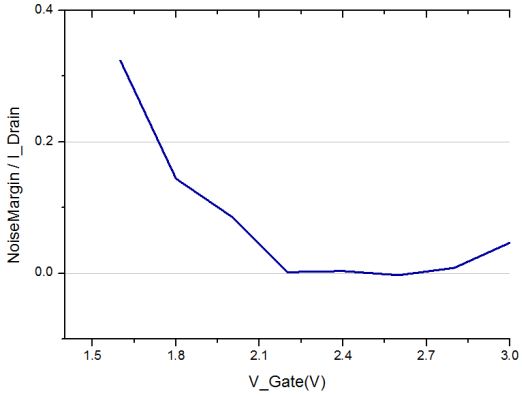
(c)



(d)



(e)



(f)

Figure 3.5

3.2.2 g_m-I_D Plot

We plot the g_m-I_D curve with the data in Fig.3.3. It clearly proves our two assumptions for dealing the disparity problem, which we have discussed in section.2.3.

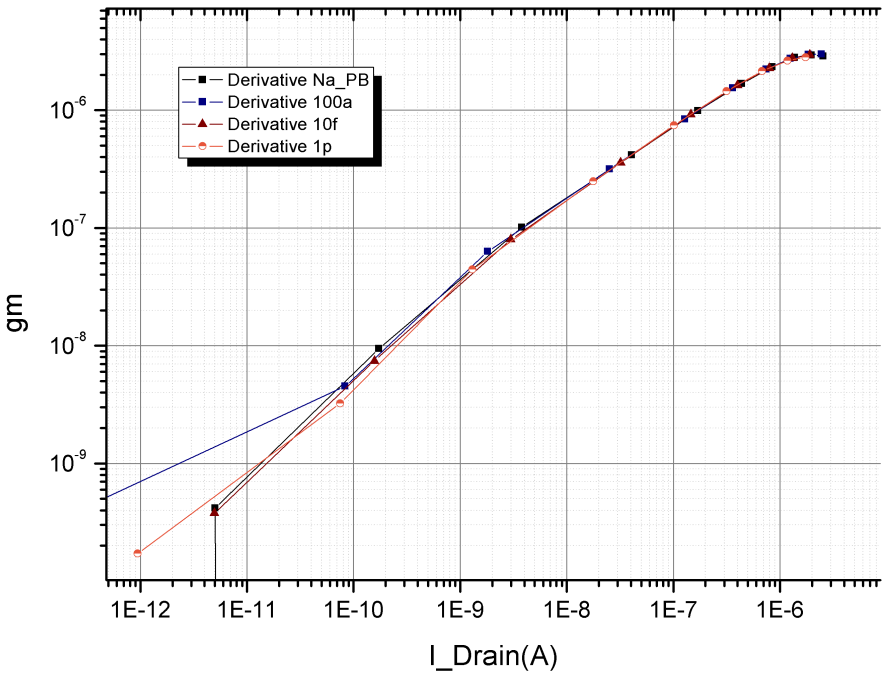


Figure 3.6: The g_m-I_D curve obtained by the I_D-V_G curve in Fig.3.3. The curves start splitting after $I_D > 1\mu$A where the element may enter into strong inversion region.

In Fig.3.6, when I_D is from 0.1nA to 1μA, we can observe that the g_m of nanowire is almost independent of concentration and merely depends on I_D. In fact, the curves start splitting after $I_D > 1\mu$A. It means the element is no longer in weak inversion region but enters into strong inversion region.

With the data from Fig.3.6, we may find the equivalent voltage value generated by the concentration difference based on the assumption 2 (section.2.3). The values

Concentration Difference	Na_PB - 100aM	100aM - 10fM	10fM - 1pM
Equivalent voltage value	$30mV - 40mV$	$200mV - 280mV$	$38mV - 60mV$

Table 3.1: The equivalent voltage value generated by the concentration difference. We obtained the data by the data from Fig.3.6. We divided the I_D difference of different concentration by their g_m ($\Delta I_D = g_m \Delta V_G$).

is changeable, which may result from the gate-coupling coefficient (Eq.2.14).

3.3 Electrical Measurements

This section presents the data analysis results. The data are obtained from our measurements with the source meter (Keithley 2602). To exclude the ion effect, we placed nanowire elements in dd-water instead of biomolecule solution. And there is no DNA probe on the poly-Si channel surfaces.

3.3.1 Front Gate and Back Gate

Our nanowire has two gates available: floating gate (liquid gate) and back-gate. We choose floating gate as the operation gate mainly because the floating gate can induce larger drain-current. In other words, it has higher transconductance (Fig.3.7). In our circuit design, nanowire is placed in a feedback loop where its transconductance is proportional to the loop gain (chapter 5).

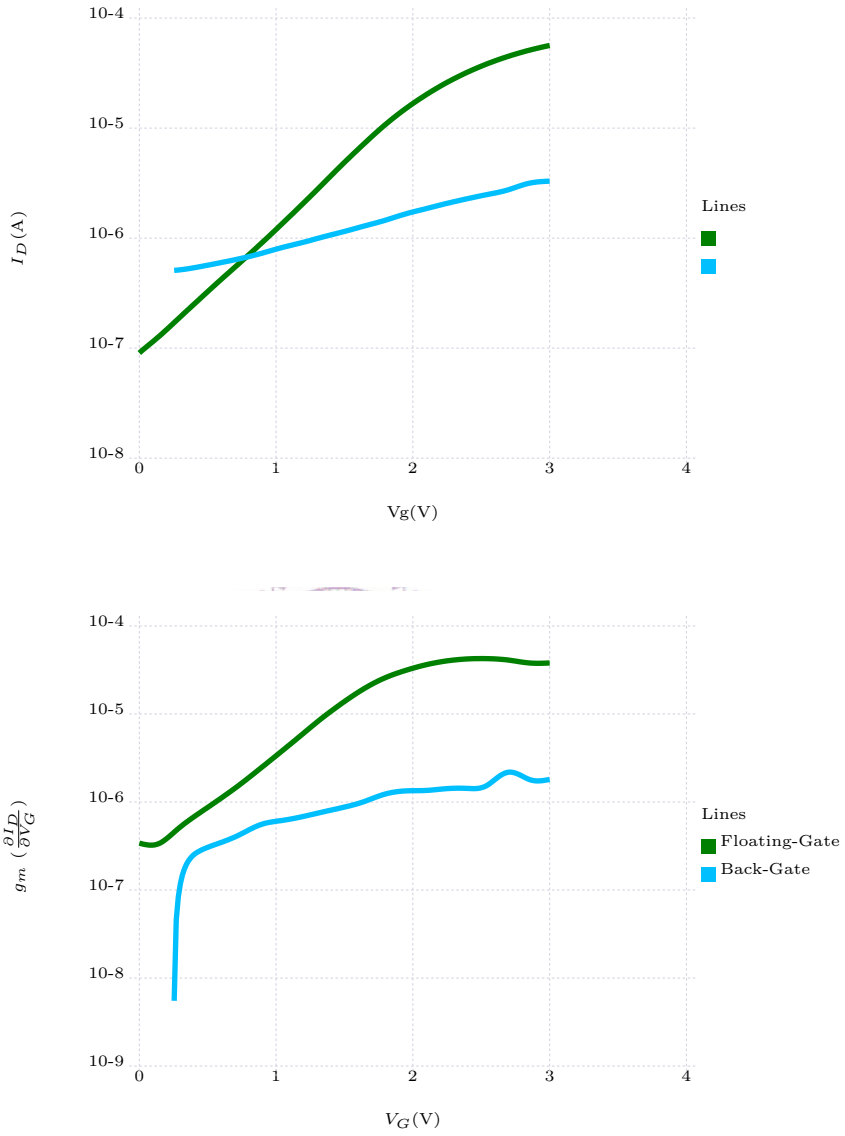
There are some advantages of back-gate. One of them is the ability to lower the 1/f noise [14, 11]. But this only happens in a very high gate voltage, which is not practical in the integrated circuit design.

3.3.2 Transconductance

The most crucial parameter for our circuit design is the transconductance (g_m). We acquire it by finding the partial derivative of I_D of V_G. Since in section.2.3.1 we proved that g_m is related to I_D, we plot the g_m-I_D curve to reveal their relation (Fig.3.8(b)).

The g_m-I_D plot indicates that there is a "linear region" where g_m is proportional to I_D. This corresponds to our induction (Eq.2.18). We can recognize that our nanowire element is operated in weak inversion region when I_D is less than 10μA. Therefore, by the section.3.2.1, we decide our the I_D of our nanowire should be operated below 10μA.

We also proved that the transconductance under this region is unaffected by the V_{DS}.



(b)

Figure 3.7: Comparison between the DC sweep of voltage on the floating gate and back gate. (a) I_D (b) Transconductance (g_m): the derivative of I_D. The traansconductance of the floating gate is larger than the back gate.

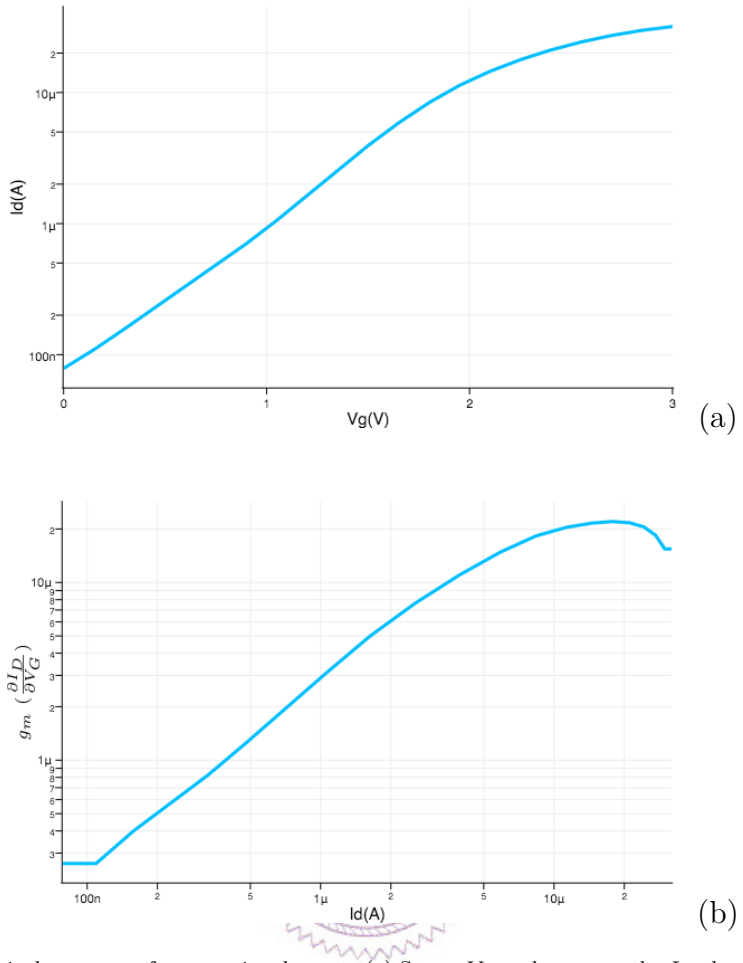


Figure 3.8: Eelectrical response of a nanowire element. (a) Sweep V_G and measure the I_D changes. And by finding the transconductance (g_m): the derivative of I_D of V_G, we plot (b) the g_m-I_D curve

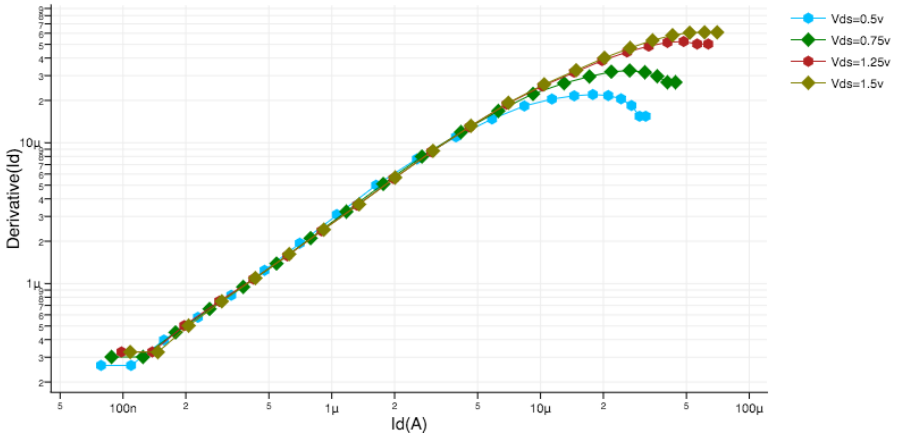


Figure 3.9: Id-transconductance with Vds variance

3.3.3 Drain-to-source impedance (r_{ds})

In our circuit design, we keep V_{DS} constant. By the measurement in last section, 0.7 is enough to keep nanowire in saturation region for V_G range from 0v to 3v. However, due to the fabrication variance, the value varies from 0.75v to 1v.

We concern about how the I_D effect r_{ds}. The way we obtained r_{ds} is as follows:

1. Perform I_D-V_G sweep with two different V_D.
2. Find the difference of I_D at each V_G sweep point and divide it by the difference of V_D.

The result is as Fig.3.10

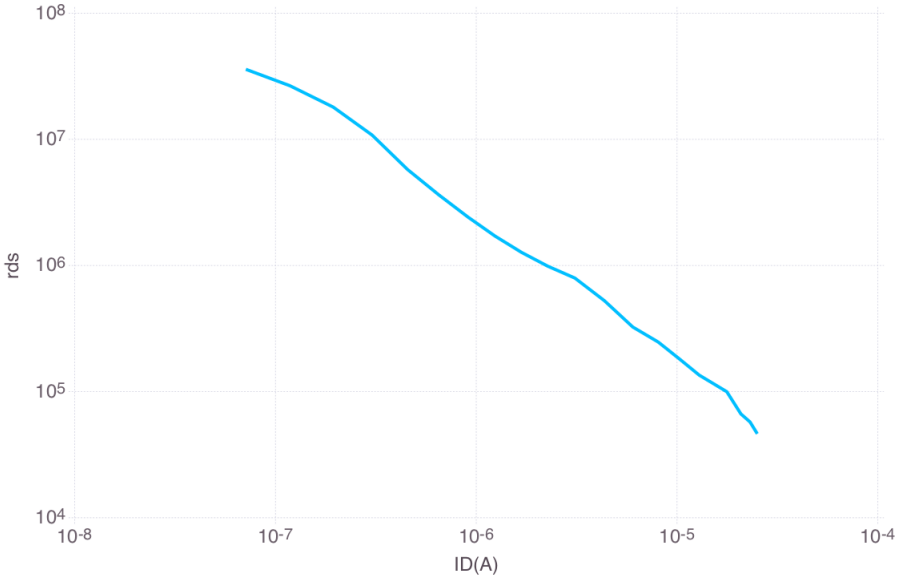


Figure 3.10: I_D-r_{ds} plot

3.4 Disparity Problem exists

We measured two nanowire elements which lie on the same wafer and are immersed with the same testing PBS solution. Below, the g_m-I_D plot (Fig.3.11) shows that even the environment is same, two elements exhibit different electrical response.

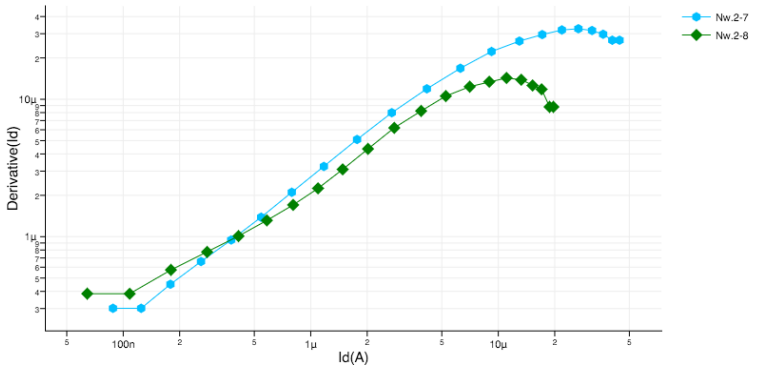


Figure 3.11: Dusparity problem casue nanowire elements with same environment can exhibit different electrical responses.

3.5 Conclusion and Design Spec

Table.3.2 concludes the electrical characteristics of our nanowire.

Operation Region	I_D	V_G	g_m	r_{ds}
Cut off	$< 100nA$	$< 0V$	-	-
weak inversion	$100nA$ - $10\mu A$	$0V$ - $2.5V$	$200n$ - 20μ	$50M\Omega$ - $200k\Omega$
strong inversion	$> 1\mu A$	$> 2.2V$	20μ - 30μ	$< 200k\Omega$

Table 3.2: Element electrical characteristics. There are overlaps due to the element disparity

We hence decide the detecting spec of the DC mode as in the table.3.3.

I_D	g_m
$100nA$ - $30\mu A$	$200n$ - 20μ

Table 3.3: Detecting Spec of DC mode

As for the AC mode, section.3.2.1 suggests that the element should operated in the weak inversion region adjacent to the strong inversion region. The table.3.1 tells that the minimum equivalent input voltage (ΔV_G) brought by concentration difference is $20mV$. We integrate these informatino in table.3.4. The Spec for AC

I_D	g_m	ΔV_G (min)
$600nA$ - $5\mu A$	1μ - 10μ	$20mV$

Table 3.4: The summation of the nanowire characteristics when applied with AC mode circuit

Input referred Noise(V)	Amplification Rate (max)
$< 2mV$	$10^7(\frac{V}{A})$

Table 3.5: Spec of AC mode circuit

mode circuit is as in table.3.5.

Chapter 4

Discrete Circuitry Design

This chapter contains the discrete circuit which has been briefly reviewed in section 2.1.2. We build this circuit to practice the constant current method.

4.1 Transforming the design from p-type measuring into n-type measuring

In [10], the circuit is for p-type ISFET element (Fig.4.1). Our nanowire element is n-type. Hence we transform the circuit as Fig.4.2.

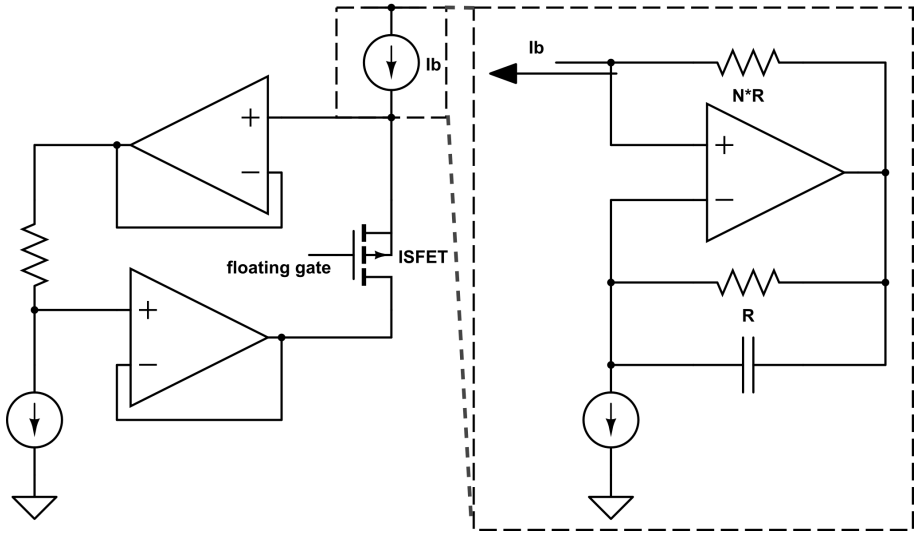


Figure 4.1: The schematic of read-out circuit from [10]. The ISFET is a p-type element. It is controlled by the current source I_b whose sub-circuit is shown at right.

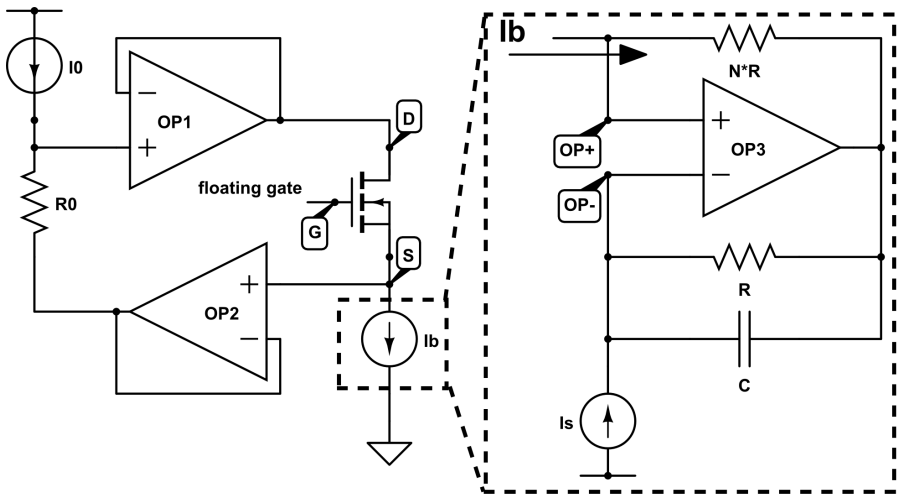


Figure 4.2: The our circuit schematic transformed from Fig.**??**. The center transistor is a n-type element. It is controlled by the current source I_b whose sub-circuit is shown at right.

4.2 Circuit Description

The circuit is divided into two sections: the circuit body and the biasing current source (Ib).

Circuit Body

The circuit body section is a source follower structure. The input of the circuit is at the floating gate (G) of the center transistor, where the output is at its source (S).

The I_D of the transistor is controlled by the Ib. The leakage current flowing into the negative input of OP2 is less than 0.1nA. Thus the I_D of the transistor should always be same as bias current I_b.

The V_{DS} is always equal to the potential difference ($I_0 \times R_0$) across the resistor R_0. This is achieved by two OP-based unity gain buffer. They connected serially with R_b and cause the voltage at drain end D follows the voltage at S.

biasing current source (Ib)

The Ib is in fact a current scale down circuit. By concerning the OP as ideal, the node $OP+$ has the same voltage with $OP-$. This equalize the potential difference across two resistors whose resistance are different by N-fold. As the result, the current of Ib and Is are also different by N-fold. $I_b = I_s/N$.

The capacitor is for filtering. It filter the high frequency noise out to create a stable output current.

4.3 Discrete Element

We use tlc2264 made by Texas Instrument (TI) as our OP. This OP element has working voltage of $\pm 5v$ and can perform rail-to-rail output operation. Its gain (Large-signal differential voltage amplification rate) is 170 for the output load greater than 50k.

For the current source Is and I0, we use lm334 made by National Semiconductor. It is a 3-terminal adjustable current sources with wide dynamic voltage range of 1v to 40v and current accuracy of $\pm 3\%$. In out experiment, the current I_s is fixed at $1\mu A$ where its output impedance is $1.2G\Omega$.

4.4 Circuit Performance and Conclusion

We examined the performance of our circuit by plotting its I_D-V_G curve. The I_0, R_0 and V_G were kept constant. We swept the I_D by changing the N value with a variable resistor. The N ranges from 1 to 1000. And the Ib circuit should produces bias current I_b from $1\mu A$ to $1nA$.

We measured the output voltage at S and subtracted this value from V_G to get the respective V_{GS}. These two value gave result to the I_D-V_G curve in Fig.4.3.

The measurement result shows that when I_D is larger than $10nA$, the circuit is functional. The I_D-V_G curve obtained by the circuit is same as the one obtained by directly sweeping V_G and measuring I_D with Source Meter (Keithley 2602).

The circuit fails when I_D is smaller than $10nA$. This is caused by the unmatched impedance, which we have discussed in section.2.1.2.

The output impedance of Ib circuit is:

$$N \times R_s \tag{4.1}$$

R_s is the output impedance of current source Is which equals to $1.2G\Omega$. And the

input impedance of transistor is:

$$\frac{1}{g_m} \tag{4.2}$$

We plot the I_D-Impedance plot in Fig.4.4.

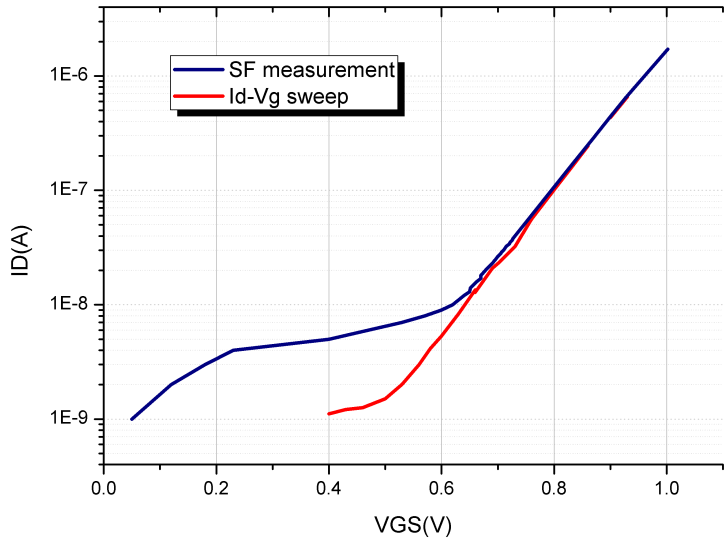


Figure 4.3: The measuremet result ("SF_measurement") compares with the direct I_D-V_G sweep ("Id-Vg sweep").

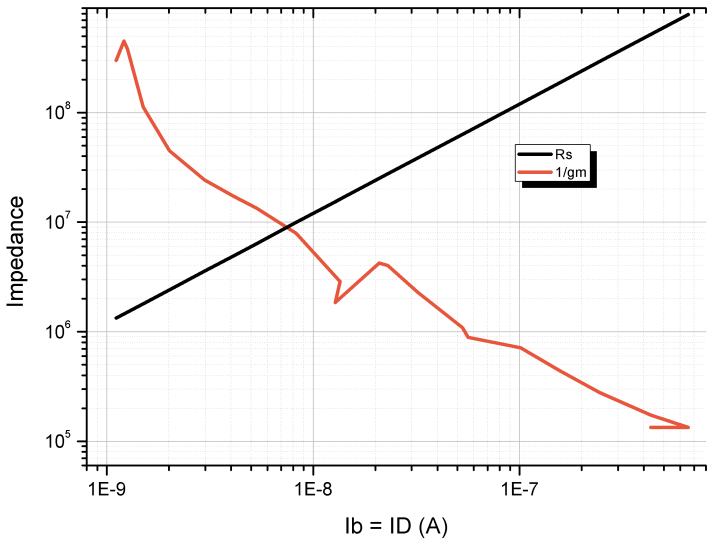


Figure 4.4: Input impedance of transistor ("1/gm") and output impedance of Ib circuit ("Rs"). The former is found by the derivative of I_D of V_{Gs}. The latter is obtained by Eq.4.1.

Fig.4.4 proves that the R_s is close to the input impedance of transistor around $I_D = 10nA$, where the g_m of transistor is around $1/10M$. The result means that we overestimate the I_b.

Overall, the constant current method is feasible. What one needs to noticed when applying the constant current method is the impedance matching. In source follower structure, its current input impedance varies with the bias current. The varying range effect the dynamic range and need more design concern.

Chapter 5

Integrated Circuitry Design

This chapter presents the design of the read-out circuit and the simulation results.

5.1 Architecture

The review of source follower in section.2.1.2 suggests the constant current method for the circuit of DC measurement. The data analysis from chapter 3 supports it by the linear relation between I_D and g_m. However, the section.2.2 shows that source follower is not suitable for AC measurement. It alternatively recommends the circuit in Fig.2.6 which measures ac current signal and converts it into voltage output. This circuit is appealing because of its noise suppression, simplicity and flexibility.

We combined these two method into one circuit structure and introduce them below.

5.1.1 Circuit Schematic: First Stage

DC mode Fig.5.1 is the first stage of our read-out circuit connected in DC mode. As in the source follower, there is a bias current source (Ibias) for controlling the I_D. The difference is that the Ibias inputs the current into drain instead of source. In addition to this, we apply the TIA from section.2.2 ([13]). Its output connects to a rail-to-rail OP amplifier, which forms a negative feedback loop. When the I_D is greater than the current of Ibias, it lowers the output voltage of TIA and raise the

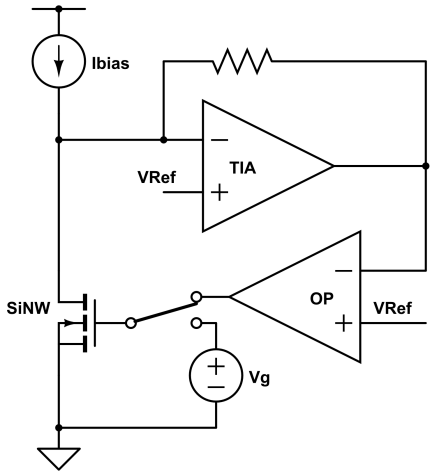
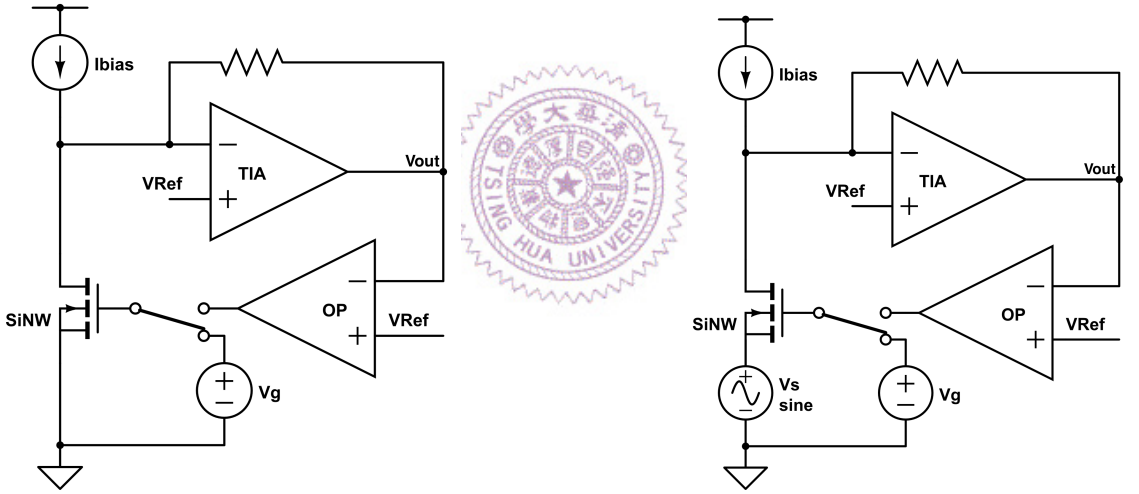


Figure 5.1

gate voltage V_G. And vice versa. This is to say that the feedback mechanism forces the I_D be equal to the current of Ibias by adjusting the V_G.



(a) (b)

Figure 5.2

AC mode In Fig.5.2(a), the switch in Fig.5.1 turns to a simple voltage source (Vg) which bias nanowire with the gate voltage. The OP is nonfunctional with its output connected floating. When performing measurement, we directly find how the solution concentration changes the output voltage (V_{out}). This output voltage will input into the second stage circuit which is for the amplification.

Dealing with the Disparity Problem As mentioned in chapter 1, we combine DC mode and AC mode to perform a disparity-resisting measurement. Assuming there are two nanowire elements having disparity problem. Initially, they are applied with DC mode to perform the I_D-V_G sweeping. We calculate their g_m by the derivative of I_D of V_G and find the g_m-I_D relation of these elements. Then we select a g_m value. For the two elements, this value corresponds to two I_D. And these two I_D corresponds to two V_G. We set the Ibias and Vg to these values. Finally, after these initialization steps, we add the measuring solutions and detect the difference of V_{out}. Since elements have same g_m, they should produce same voltage differences. Before the next measuring solutions is added, we return to DC mode to find new V_G. This reset I_D of the elements to the value of Ibias, which also reset the g_m to the value we selected.

Another Usage of AC mode There is another way to perform measurement with AC mode, which resembles the method in [13]. This method measures the g_m of nanowire. As in Fig.5.2(b), the source of nanowire is applied with an ac signal (v_s). An ac output in V_{out} is equal to $v_s g_m \times R_{TIA}$. The values of Ibias and Vg can be arbitrary. But one need to be aware that the values should not saturate the output of TIA or the second stage circuit.

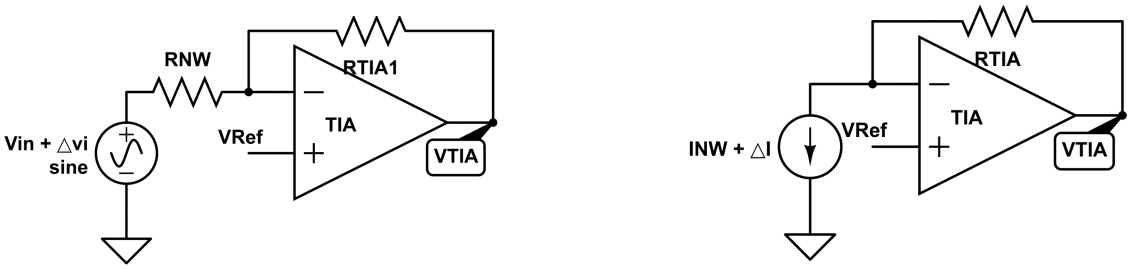
Below, we talk about some design concept.

5.1.1.1 Detecting Range Improvement (AC mode)

In section.2.2.3 about the TIA subcricuit as Fig.5.3(a), we mentioned that the detecting range of R_{NW} is limited. There are same limits in our circuit which detects the current variance of nanowire. We now discuss the causes of these limits and show the strategies we use. To be noticed that the TIA block is a two-stage differential input and single output op-amp in the flowing discussion.

Lower Limit: According to Fig.5.3(b), the TIA output voltage is:

$$V_{TIA} = V_{Ref} + I_{NW} R_{TIA} + \Delta i R_{TIA} \tag{5.1}$$



(a) (b)

Figure 5.3: (a) The transimpedance block (TIA) of the readout circuit from [13]. The circuit input a voltage signal into resistive nanowire element R_{NW}. To compare it with our circuit (Fig.5.4), we transform the voltage input into an equivalent current input in **(b)**. The $I_{NW} = (V_{Ref} - V_{in})/R_{NW}$ and $\Delta i = \Delta vi/R_{NW}$

Two reasons which result in the lower limit of the detecting range relate to a large offset current I_{NW}. One is that the output current provided by the TIA is restricted by design. The other is that the restriction of the current flowing through the resistor R_{TIA}:

$$\frac{V_{Ref}}{R_{TIA}} < I_{NW} < \frac{VDD - V_{Ref}}{R_{TIA}} \tag{5.2}$$

Both reasons leads to the output saturation of TIA.

A naive way to handle the first reason is to increase the output current which TIA can provide. The side effects of this method are the increases in power consumption and chip area. As for the second reason, using smaller R_{TIA} can ease the restriction on I_{NW} and reduce the lower limit. Unfortunately, it reduces the upper limit as well. This will be discussed in the paragraph of "upper limit".

Our strategy for decreasing the lower limit is by utilizing the bias current source of nanowire. According to Fig.5.4, the Eq.5.1 is transformed into:

$$V_{TIA} = V_{Ref} + (I_{NW} - I_{bias})R_{TIA} + \Delta i R_{TIA} \tag{5.3}$$

Now we can diminish the large I_{NW} by Ibias. In conclusion, the large offset current cause the saturation of the output of TIA. We use the biasing current source to diminish that offset current, which increase the detecting range.

Upper Limit: The upper limit issues from the output resolution. If the signal $\Delta i R_{TIA}$ from Eq.5.4 is too small, it may be defeated by the noise. One may be raise up the SNR by using large R_{TIA}. However, the chip area constrain the size of

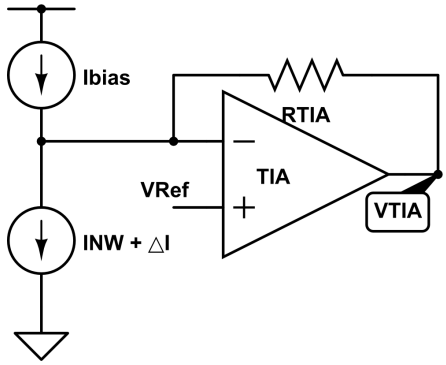


Figure 5.4

resistors. In our circuit design, we cannot make the resistance value out of $100k\Omega$. Furthermore, even if the resistor can be greater, one need to concern for the noise brought by the large resistance.

Our strategy is to boost the SNR of TIA by designing its input MOSFETs in a large area. And we also amplify the output signal through the second stage circuit.

5.1.1.2 Input impedance Matching (DC mode)

From the chapter 4, we learned that for the constant current method, the impedance matching between current source Ibias and nanowire element is important. The matching decides the limit of the biasing current. Here we calculate the input impedance of the circuit.

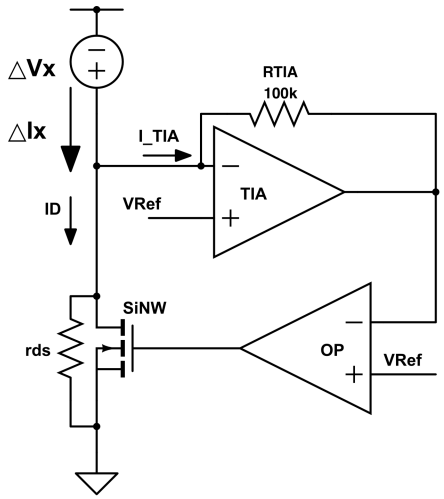


Figure 5.5

In Fig.5.5, by applying and input voltage Δv_x, we find the Δi_x. The input

impedance of the circuit is $\Delta v_x/\Delta i_x$.

$$\Delta i_x = i_D + i_{TIA} \tag{5.4}$$

$$i_D = \frac{\Delta v_x}{r_{ds}} + \Delta v_x A_{TIA} A_{OP} g_m \tag{5.5}$$

$$i_{TIA} = \frac{\Delta v_x}{R_{TIA}/(1 + A_{TIA})} \tag{5.6}$$

$$\Delta v_x/\Delta i_x = (\frac{1}{r_{ds}} + \frac{1 + A_{TIA})}{R_{TIA}})^{-1} \tag{5.7}$$

The A_{TIA} is the gain of the opAmp in TIA block. The A_{OP} is the gain of OP. The r_ds is the drain-to-source resistance of nanowire which is large than $100k\Omega$. From the Eq.5.7, we conclude that the input impedance of the circuit is equal to:

$$\frac{1/g_m}{A_{TIA} \times A_{OP}} || r_{ds} || \frac{R_{TIA}}{1 + A_{TIA})} \tag{5.8}$$

In out design, the Ibias is an simple pmos. Its output impedance roughly ranges from $1M\Omega$ to $1G\Omega$. Since the r_{ds} is large than $100k\Omega$. The input impedance is clearly smaller than 1/100 fold of the r_{ds}, which means the impedance matching successes.

The result above seems implies that our design can achieve a lower biasing current than the circuit in chapter 4. Unfortunately, it is not true. A portion of the current given by Ibias leaks into the R_{TIA}. We calculate the current ratio between i_{TIA} and i_D:

$$\frac{i_D}{i_{TIA}} = R_{TIA} \times g_m \times A_{OP} \tag{5.9}$$

Another section will shows that this value may not be over 10k (80dB) due to the stability. Thus we can see that when g_m is getting lower than 0.1μ, the ratio is smaller than 100 and the leakage current is not ignorant anymore. This limit of the biasing current is same with the one of the circuit in chapter 4(Fig.4.4).

5.1.2 Architecture: Second Stage

We discuss the second stage circuit in this section. To be noted that the second stage circuit is only for AC mode.

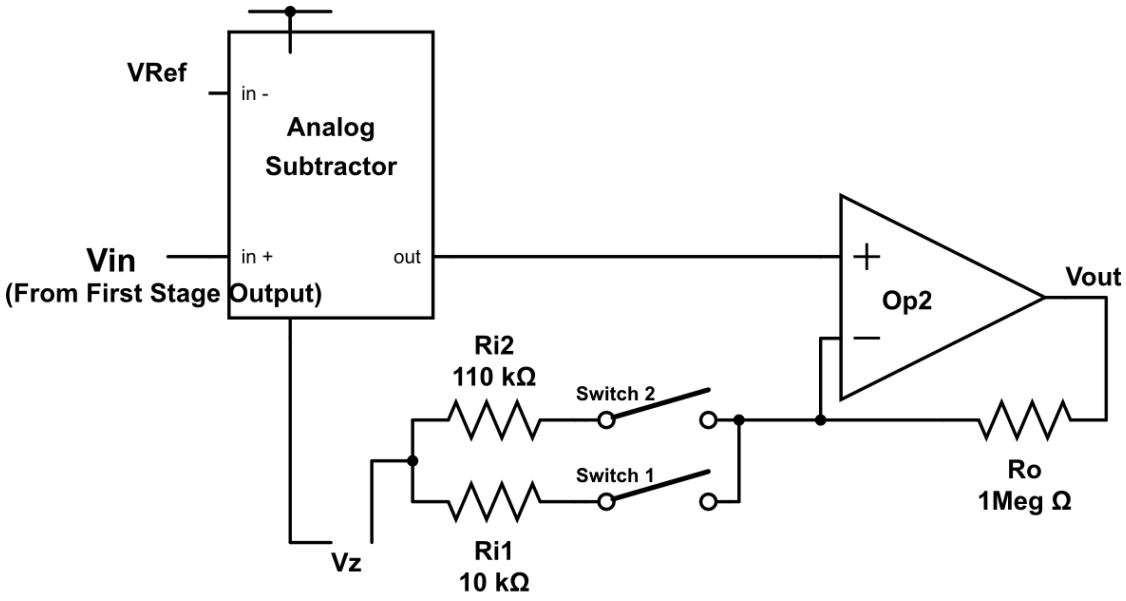


Figure 5.6

Fig.5.6 is the block diagram of the second stage circuit. The analog subtractor shifts the voltage of the V_{in} from V_{Ref} to V_z. It follows by a resistor-based non-inverting amplifier composed of an two-stage differential OpAmp, two switches and three resistors. The switches select the amplification rate among 100, 10 and 1.

5.1.3 Design Spec and Calculation

Chapter 6

Discussion and Conclusions

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