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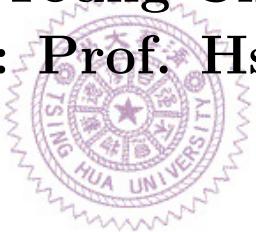
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An Integrated Circuit Design for Silicon-Nanowire

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2016

Abstract



中 文 摘 要

關鍵詞：



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Abstract

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Chapter 1

Introduction

1.1 Motivation

Poly-silicon nanowire(SiNW) is a well-studied and promising one-dimensional nanostructures. As reported by [4], there have been a lot of valuable research on fabrication and electrical properties. It was first introduced to the biosensor field in 2001[3] and has become a promising candidate for various features such as high surface-to-volume ratio, ultra sensitivity, label-free electrical detection and real-time measurement.

Although there have been substantial advances on nanowire structure design [6], the work of systems-level engineering is still insufficient. Systems designed for a specific purpose can help the device to meet practical needs such as noise reduction, real-time measurement, and analog-to-digital conversion. Moreover, there are still several challenges that may be overcome through a better signal acquisition system [6].

One of the challenges is that the mass production of robust nanowire elements is still improbable. Element disparity may be the main reason among others. This problem also happens to the measurement of our nanowire (Fig. 3.11). The nanowire we use is made by Professor Yang's team (National Chiao Tong University). And according to them, the nanowire use thick gate dielectric and have non-regular cross-sectional shape, which results in uncertainties of fabrication [8].

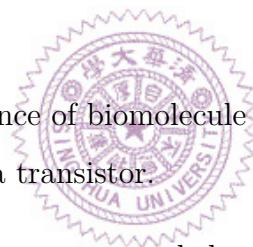
1.2 Introduction

In this project, we design a nanowire read-out circuit with two modes: DC Sweep mode and Transient Measurement mode. In the DC Sweep mode, one can use the circuit to perform a DC sweep of drain-to-source current (I_D) to show how the gate voltage (V_G) changes, or gives nanowire a constant I_D and measures the V_G response to different solution concentration. In the Transient Measurement mode, the circuit detects and amplifies the variance of (I_D) with constant bias voltages applied (V_D , V_G , V_S). We also combine two modes to implement a proposed method that may mitigate the disparity problem.

Dealing with the Disparity Problem

The proposed method base on two assumptions:

1. The nanowire transconductance ($g_m = \frac{\partial I_D}{\partial V_{GS}}$) depends on I_D and independent on V_{GS} .
2. The concentration difference of biomolecule can be viewed as a voltage signal input to the gate end of a transistor.



The first assumption implies one can control the nanowire transconductance by its I_D . The second assumption means that as long as different nanowire elements have a same transconductance, the output current induced by a concentration difference should be same.

The method works as follows:

Initial stage At the beginning of each measurement event, we perform a DC sweep with the DC Sweep mode. By handling the sweep results with numerical method, we keep all nanowire elements under a selected transconductance by controlling their I_D and corresponded V_G .

Measurement stage We put the circuit in the Transient Measurement mode at this stage. Since the transconductance of all elements is same, they should behave

uniformly based on assumption 2. At the end of the stage, we return to the DC Sweep mode to reset I_D of the elements. The circuit adjusts their V_G to do so.

At the beginning of each measurement stage, an element always has a same I_D but different V_G . Based on assumption 1, its transconductance is kept constant.

The minutiae are reviewed in chapter 5. Currently, most operations are manual. We hope to make them automatic in the future, which may require digital circuit assistance.

1.3 Design Flow and Chapter Layout

In this thesis, there are six chapters sorted according to the design flow.

Chapter 2 reviews the basic theories and the literature that are related to our work. Most of those are the drain current of nanowire sweeping along the gate voltage (I_d - V_g curves). We present some of the raw data and the analysis results in this part.

Chapter 3 gives a brief description of nanowire structure. It is then followed by two sections about some measurement and data analysis. The data of the first one is from the biological experiments while the second one is from the electrical measurement. We use the analysis results to design the read-out circuit.

Chapter 4 is an “accessory”. This chapter contains the discrete circuit which was designed for ion-sensitive field-effect transistor (ISFET) [10]. We construct it and perform some electrical measurement. The purpose of this process is to practice the constant current method. The outcomes are deficient, and it is its reference value which we spotlight.

Chapter 5 talks about the schematic, design process and the simulation results of the read-out circuit.

Chapter 6 presents the measurement results of our integrated circuit and the conclusion of this project.

Chapter 2

Literature Review & Theory

Description

As previously mentioned in the introduction section, the read-out circuit we proposed has two operation mode (DC and AC). The DC Sweep mode control the drain current (I_D) of nanowire while the Transient Sweep mode is for current variance measurement. Each of them references different sources. In section 2.1, we first talk about the reason why we perform I_D - V_G sweep. Then we review the reference of our DC Sweep mode circuit design. The references of the Transient Sweep mode circuit design is in section 2.2. In the last section, we discuss the two assumptions mentioned in section 1.2.

2.1 DC Sweep: I_D - V_G Curves

In this section, we review the knowledge and an article that is related to our design of large signal mode (DC).

2.1.1 I_D - V_G and Transconductance

A common method for examining nanowire electrical properties is to perform DC sweep. Among all kinds of sweep method, we choose the I_D - V_G in respect of the physical characteristic. In the n-type transistor, the binding of negatively charged biomolecules induces surface-near silicon ions discharged and thus lower the thresh-

old voltage. It is straightforward to think of these binding molecules as a voltage signal input to the gate with its value depends on the concentration. And this voltage signal effect nanowire in the same way V_G does. So by plotting I_D - V_G curves, we can have a thumbnail of how concentration affects the I_D .

2.1.2 Source Follower

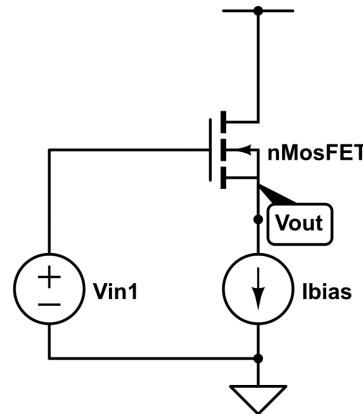


Figure 2.1: Sorce Follower

As one of the basic single stage amplifier, source follower (common drain) are employed to transfer voltage signal from gate to source while keeping drain current constant. The transfer function can be derived as:

$$\frac{V_{out}}{V_{in}} = \frac{r_{ds}g_m}{1 + r_{ds}g_m} \quad (2.1)$$

$$\approx 1 \quad \text{for} \quad r_{ds}g_m \gg 1 \quad (2.2)$$

g_m is the transconductance ($\frac{\partial I_d}{\partial V_{gs}}$) and r_{ds} is the drain-to-source resistance. Although we haven't seen the structure be applied to nanowire, there have been several applications in the read-out circuits of ISFET (Ion-sensitive Field-effect Transistor)[10, 12] for a long time.

The read-out circuit in [10] applied ISFET as a biological transducer that converts detected bio-signal into the electrical signal, which resembles our nanowire biosensor. Its adopt source follower structure as its analog front-end. The bio-signal induced voltage difference at the ISFET gate-end is converted to the source-end. This structure requires a biasing current source which may have to be stable, noiseless or wide-range on demand. Since the bias current is usually under micro-scale

even nano-scale, it is impractical to use an external current source merely. The article used two resistors and an op-amp to design a current scale down circuit. Bias current decreases in proportional to the resistance ratio (N) of one resistor to another. Moreover, by keeping V_{ds} at a constant value (0.5v), the circuit also removes the short channel effect. Below show the schematic where two op-amp based unit gain buffer are added to force the voltage at drain-end follows the source-end.

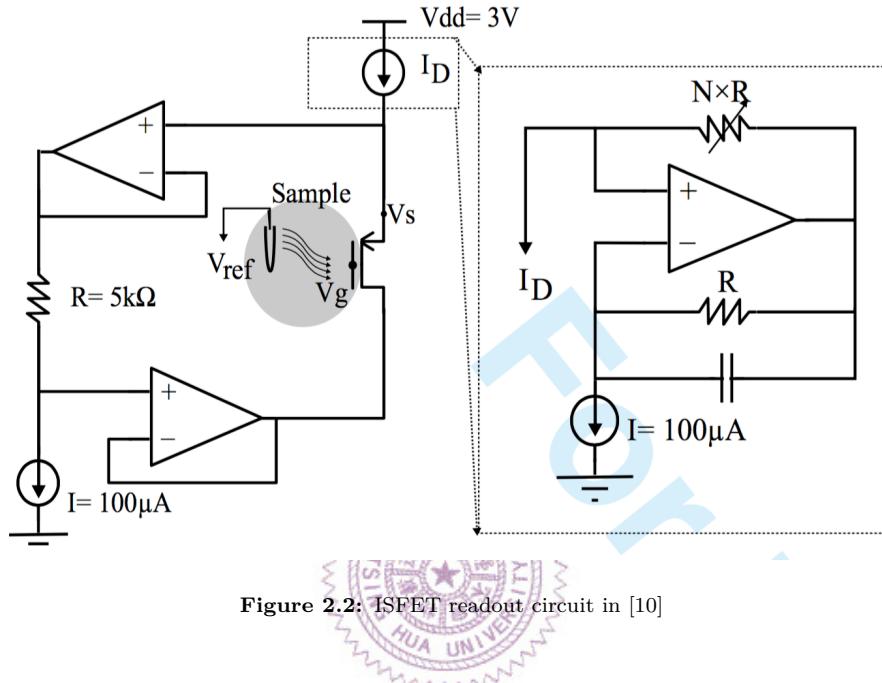


Figure 2.2: ISFET readout circuit in [10]

An issue needed to be aware is the impedance matching between the element and the current source circuit. The output impedance of current source should be much larger than the input impedance of the biasing element. The equation for the output impedance of source follower is:

$$\frac{r_{ds}}{1 + g_m r_{ds}} \quad (2.3)$$

This equation can be simplified as:

$$\frac{1}{g_m} \quad \text{for} \quad g_m r_{ds} \gg 1 \quad (2.4)$$

The output impedance of the current source circuit is:

$$N \times R_s \quad (2.5)$$

R_s is the impedance of the right-bottom current source in Fig.2.2. In the integrated circuit, R_s is not ideal but usually close to the r_{ds} of a single MOSFET.

As mentioned, Eq.2.5 should be far larger than Eq.2.4. However, g_m is proportional to I_d , which means Eq.2.4 is inversely proportional to N. When the bias current decreases, the output impedance decreases while the input impedance at the ISFET source-end increases. Therefore, there is a lower boundary of the bias current. We observed this boundary when we construct this circuit with discrete elements. These will be presented and discussed in chapter 4.

The source follower structure provides a direct signal transition method. It is a good candidate for the read-out circuit with the aim of detecting transconductance or threshold voltage variance. Nevertheless, post-processing such as amplification and filtering are necessary. The experiment results in the article are untreated. Strong signal attenuation exists, which are mainly caused by low-frequency noise and ISFET drift [9]. The drift problem is dealt with through signal processing techniques while noise problems are left untreated.

2.2 Small Signal (AC) Measurement Method Review

In the previous section, the source follower we mentioned exhibited compelling advantages as a signal processing structure of nano-device. However, the structure overcomes obstacles when being applied to the small signal detection. Parasitic capacitors and resistors can severely influence the results.

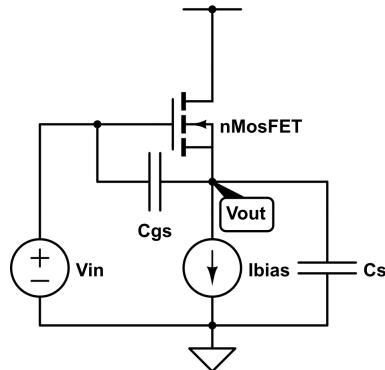


Figure 2.3: Sorce Follower with parasitic capacitance

As in figure 2.3 where the parasitic elements are included, we modified the transfer function Eq.2.2 as:

$$\frac{V_{out}}{V_{in}} = \frac{r_{ds}(sC_{gs} + gm)}{1 + r_{ds}(gm + s(C_{gs} + C_s))} \quad (2.6)$$

The equation can be similar to Eq.2.2 which roughly equals to 1 as long as C_s is far more smaller than C_{gs} . Unfortunately, C_s can be large for the output end of source follower usually connects to a next stage input or a pad. In that case, the parasitic capacitors may attenuate the signal.

We want to build another circuit structure that can not only performs AC signal measurement but also immune from parasitic capacitance. We started by reviewing those works that try to measure the parasitic capacitance. Below, the works from two teams aim to measure drain-to-source resistance (R_{NW}) and drain-to-source capacitance (C_{NW}). The focus of the review is on the function and design theory of their read-out circuit.

2.2.1 RC Time Delay Measuring

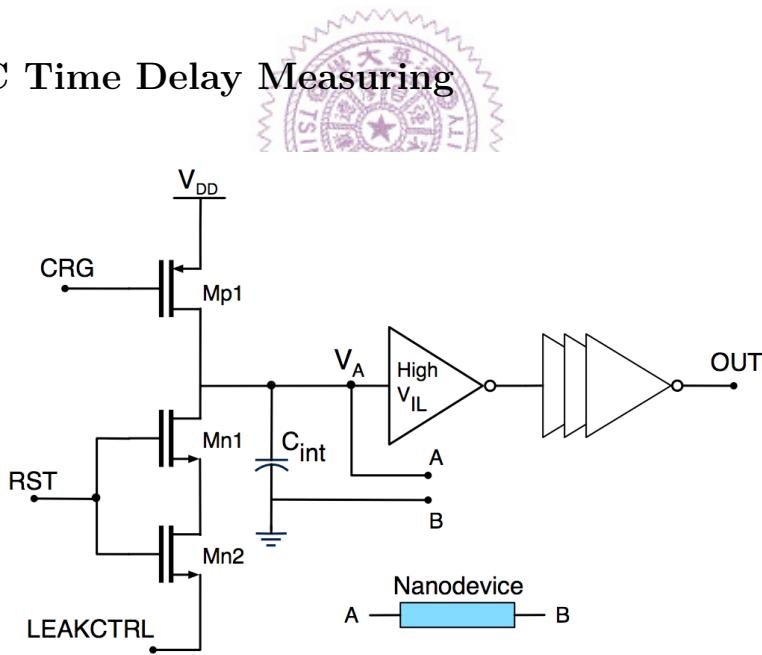


Figure 2.4: (a) Schematic of [1].

The measurement system for ZnO-nanowire based sensor array from [1] applies the Time-over-Threshold techniques to its read-out circuit (Fig.2.4). The circuit alternatively charges an on-chip capacitor (C_{int}) with a constant current and discharges it through the nano-material resistance (nanowire). An inverter with its output

switches from on to off when the capacitor is charged to its input threshold voltage, and vice versa. This behavior converts information of nanowire such as capacitance and resistance into time information. Both C_{int} and C_{NW} effect charging time and together with the R_{NW} effect the discharging time.

The work presented in [1] doesn't have enough explanation about how do they interpret the capacitance and resistance information. It merely mentioned that a microcontroller is responsible for the calculation. Besides, the work lacks simulation and experiment of using complex elements as measured target. Most of the results are the measurement of using a concrete resistor as the substitute for nanowire and regard the C_{NW} as 0p. The only nanowire experiment given at last doesn't have good performance. It seems that the design may only be applied to a pure resistance or pure capacitance type element.

The recent publican [2] by the team is more elaborate and contains the measurement of complex elements (An element composed of a discrete resistor and a discrete capacitor).

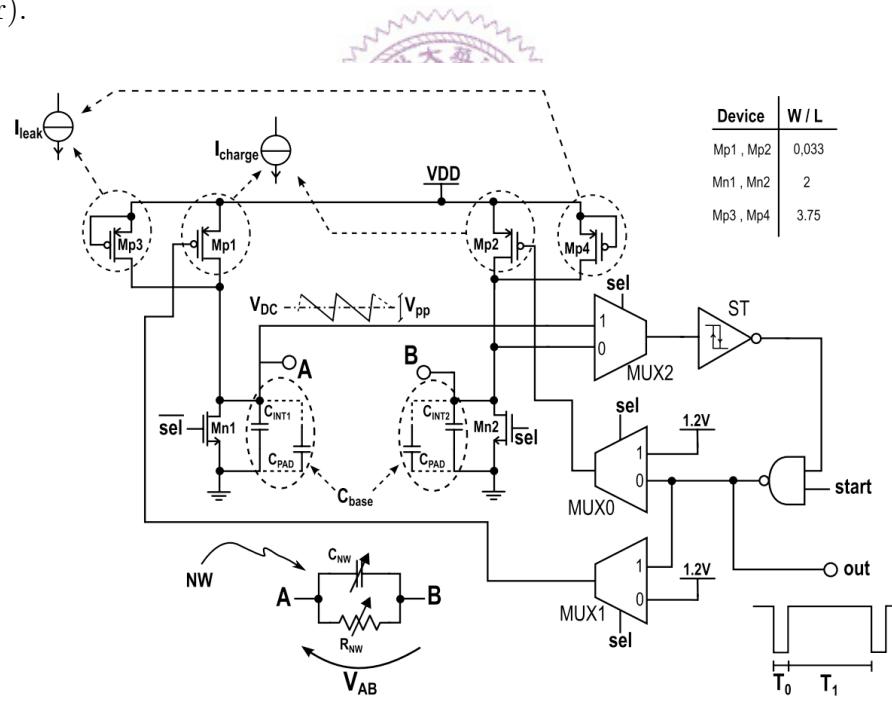


Figure 2.5: Schematic of [2].

In Fig.2.5, nanowire append between point A and B. The charging current can be applied from Mp1 or Mp2, which is determined by the “sel” signal with the aid from the MUXs. We simply assume sel = 1 and point B is virtually ground. (When

the sel = 0, the circuit measures the element with a reversed biasing current.) Now, we can see that the circuit design concept is same with [1]. The current charge both C_{int} and C_{NW} . When the voltage at A exceed the threshold voltage, the output switches to off and feedback to turn off the Mp1. (To be noted that a Schmitt trigger replaces the inverter at the output stage in [1].) Then the capacitor discharges through nanowire (r_{ds}).

The right-bottom plot in Fig.2.5 defines T_0 as the charging time and T_1 as the discharging time. The calculation of the R_{NW} and C_{NW} can be simplified as:

$$C_{NW} = T_0 - C_{base} \quad (2.7)$$

$$R_{NW} = \frac{T_1 R_{par}}{(C_{NW} + C_{base}) R_{par} - T_1} \quad (2.8)$$

$$\text{where } R_{NW} || R_{par} = \frac{T_1}{C_{NW} + C_{base}} \quad (2.9)$$

C_{base} are the C_{int} plus parasitic capacitance and R_{par} the parasitic resistance. These parasitic elements come from the transistor in the integrated circuit block such as MUX and Mp. It must be noticed that we don't concern the hysteresis of the Schmitt trigger here owing to simplicity.

2.2.2 Complex Impedance Solving

The nanowire-based hydrogen sensor measurement system from [13] adopts another method. It treat It use a lock-in amplifier to realize both resistive and capacitive impedance measurement.

As the previous method, it treats nanowire as a complexed one-dimensional element. The nanowire is modeled as a parallel aligned resistor and a capacitor. The system supplies a sinusoidal voltage signal to one end of the element. Another end of the element is grounded virtually by a transimpedance amplifier (TIA). The TIA then converts the current variance into voltage output which contains complex impedance information. The resistance is in the real part while the capacitance is

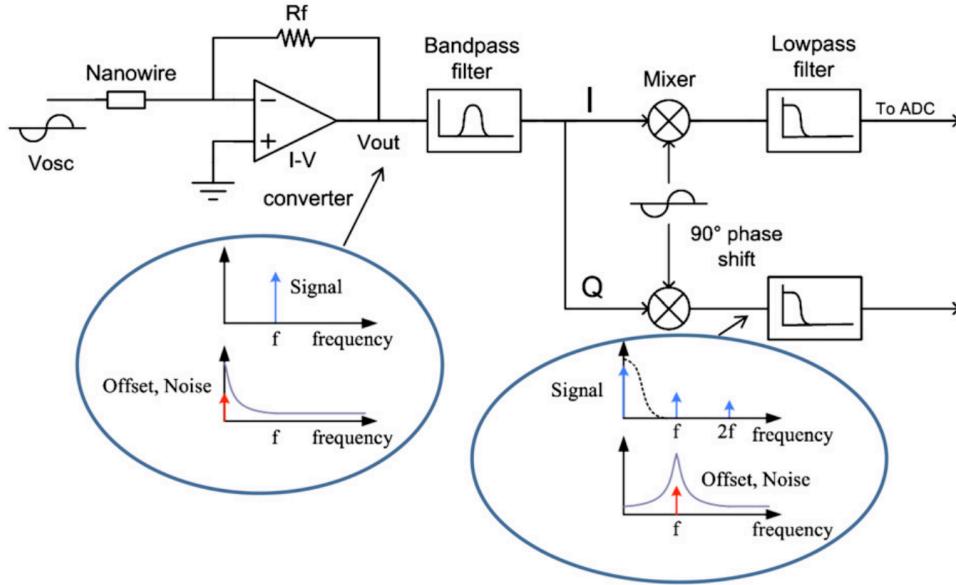


Figure 2.6: Block diagram of the lock-in amplifier in [13]

in the virtual part.

$$V_{out} = I_{NW} R_{TIA} \quad (2.10)$$

$$I_{NW} = V_{in} \left(\frac{1}{R_{NW}} + j2\pi f C_{NW} \right) \quad (2.11)$$

f is the frequency of input signal.

The output of TIA is followed by a controllable bandpass filter (BP). The BP removes high-order harmonic interferences. Then the signal is demodulated. The resistive and capacitive impedance values are resolved through two channels: I and Q with their phase different by 90 degrees. A mixer which is a linear multiplier performs the demodulation. With a radio frequency (RF) input and the input local oscillator (LO) input, it produce an output signal that consists of signals with frequencies $f_{RF} + f_{LO}$ and $f_{RF} - f_{LO}$. Incidentally, the signal is immune from the perturbation of low-frequency noise which is a common problem for the biosensor.

2.2.3 Comparison and Conclusion

We compare Method 1 (Sec.2.2.1) and Method 2 (Sec.2.2.2) here. Both of them focus on detecting the R_{NW} difference. According to the comparison table below (2.1), we can see the resistor measurement range of Method 1 is different from Method 2

by a large extent. This may because the bias current of nanowire that caprovided by the circuits are different. The current in Method 1 is limited by the pmos(I charge) and the leakage current. In Method 2, it is limited by the TIA. Our method adopts this TIA block and will discuss this problem in section.5.1.4.1.

Method 2 perform well when it comes to noise suppression. In fact, the circuit in Method 1 doesn't provide noise reduction ability. The particular structure it uses (The article [1] mentioned it as M4N approach) is the one responsible for that.

Method 1 has a lower power consumption. However, it doesn't include the power of microcontroller and may underestimate.

	[2]	[13]
R meas range	1M - 1G	10 - 40k
R meas error	< 2.5%	< 2%
C meas range	100fF - 1uF	0.5 - 1.8nF
C meas error	< 3%	< 3%
SNR	> 45dB	-
Input refered noise	-	190 nV/sqrt(Hz) @ 5 kHz
CMOS Technology	0.13um	0.18um
Power consumption	14.82uW	2mW

Table 2.1: Specification Summary

In our project, capacitance measurement is not our object. But we still need to consider the parasitic capacitor effect in our circuit design. Method 1 converts the resistance information into time (frequency) information. If one want to avoid the effect of the parasitic capacitor, he should apply a C_{int} that is much larger than C_{NW} . However, it is not practical in integrated design because the chip size is limited.

Method 2 uses a TIA to measure resistance and capacitance together first and then resolve the complex value. We can write the complex impedance value as:

$$\frac{R_{NW}}{1 + i2\pi f R_{NW} C_{NW}} \quad (2.12)$$

In Eq.2.12, i is the imaginary unit and f is the signal frequency. The equation can be simplified as R_{NW} when $i2\pi f R_{NW} C_{NW} < 0.1$. The simplification can be

applied when the signal frequency or $C_{NW}R_{NW}$ is small enough. Thus, one needs to select the appropriate signal frequency or to determine the R_{NW} detecting range.

Another reason that makes Method 2 more attractive is that it is more flexible. One can add other analog blocks such as noise filter or amplifier to it.

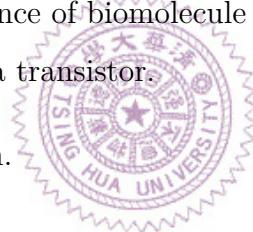
Overall, Method 1 has the advantage in detecting range and accuracy while Method 2 has better noise suppression and flexibility.

2.3 Two assumption for Dealing with Disparity Problem

In chapter 1, to deal with disparity problem, we assume that:

1. The nanowire transconductance ($g_m = \frac{\partial I_D}{\partial V_{GS}}$) depends on I_D and independent on V_{GS} .
2. The concentration difference of biomolecule can be viewed as a voltage signal input to the gate end of a transistor.

We discuss them in this section.



2.3.1 Transconductance and I_D

With the MOSFET model of weak and strong inversion, we have the I_D equations of MOSFET:

$$\text{weak inversion: } I_D = I_0 e^{\kappa V_{GS}/\phi_t} (1 - e^{-V_{DS}/\phi_t}) \quad (2.13)$$

$$= I_0 e^{\kappa V_{GS}/\phi_t} \quad \text{where } V_{DS} > 4\phi_t \quad (2.14)$$

$$\text{strong inversion: } I_D = \mu C_{ox} \frac{W}{L} ((V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2}) \quad (2.15)$$

$$= \mu C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2 \quad \text{where } V_{DS} > V_{GS} - V_{th} \quad (2.16)$$

C_{ox} is the oxide capacitance and μ is the electron mobility. Both of them depends on doping concentration. W and L are the width and length of the transistor. ϕ_t is the thermal voltage depending on temperature. The κ is the gate coupling coefficient. It will be discuss in the next paragraph. To be noted that we ignore the short channel effect, which doesn't effect our discussion since we always keep V_{DS} constant.

We then derive g_m :

$$\text{weak inversion: } g_m = \frac{\kappa I_D}{\phi_t} \quad (2.17)$$

$$\text{strong inversion: } g_m = \sqrt{2\mu C_{ox} \left(\frac{W}{L}\right) I_D} \quad (2.18)$$

$$(2.19)$$

For the strong inversion, the Eq.2.19 shows that the assumption 1 is correct. However, the assumption is not completely right for transistor in weak inversion. According to the Eq.2.18, the g_m is effect not only by I_D but also by the κ . It is a non-linear parameter effected by V_G and other factors. Its value is range from 0.4 to 0.9. In our circuit, this problem is currently left unsolved. We present its effect in chapter 6.

2.3.2 A Simple Model for Concentration Affect

In [5], the team plot the I_D - V_G curves and study how the curve changes with the concentration of biomolecules. We observe that in the plot (Fig.2.7) with a log scale for the y-axis, curves with different concentration exhibit a same rising trend when I_D is low ($< 100\text{nA}$). Each curve seems to be different with the other by a constant fold. By applying the weak inversion current equation of MOSFET, we found that the assumption can explain this concentration effect.

$$I_{D1} = I_0 e^{\kappa(V_{GS} - V_{th})/\phi_t} \quad (2.20)$$

$$I_{D2} = I_0 e^{\kappa(V_{GS} - (V_{th} - v_c))/\phi_t} \quad (2.21)$$

$$\rightarrow I_{D2} = f(v_c) \times I_{D1} \quad \text{where } f(\Delta v_g) = e^{v_c/\phi_t} \quad (2.22)$$

The I_{D1} and I_{D2} are the current of two nanowire elements placed in solutions of different concentration. The (v_c) is a concentration related variable we create. The Eq.2.22 implies that when nanowire is in weak inversion region, its $\log I_D$ difference is independent of V_g .

$$\log I_{D2} - \log I_{D1} = \log \frac{I_{D2}}{I_{D1}} = \log f(v_c) = v_c/\phi_t \quad (2.23)$$

As for strong inversion region which refer to the large current section in Fig.2.7, the difference of the curves diminish as V_G increasing. The strong inversion equation (Eq.2.16) shows that if V_{GS} is far larger then v_c , the concentration effect can be ignored.

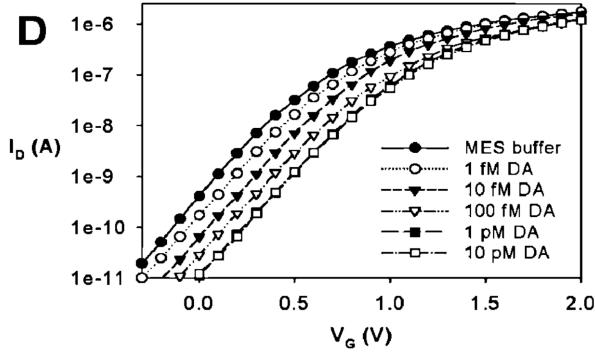


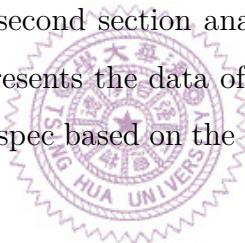
Figure 2.7: Concentration-dependent electric response($I_D - V_G$) of biotin-modified poly-Si NWFET following biotin-streptavidin interaction.[5]

We will further prove the two assumptions by the data of biology experiment in section.3.2.2.

Chapter 3

Nanowire Structure and Measurement

In this chapter, we present the experiment data and some analysis which are the foundation of our circuit design. The first section gives a brief description of our silicon nanowire element. The second section analyzes the data of the biology experiments. The third section presents the data of the electrical measurement. The last section provides the design spec based on the information given by the previous sections.



3.1 Brief Description of Nanowire Structure

The nanowire we use is made by Prof.Yang's team (National Chiao Tong University)[7]. Fig.3.1 is the sectional view of the nanowire structure. The fabrication process is based on the poly silicon sidewall spacer technique. The n-Type doped poly-SiNW FET has two to ten poly silicon channels. Each channel is 80nm in width and 2 μ m in length. A Large portion of the channel surface is exposed to environment. The exposed region, through several post-process, capture the DNA probe and serve as the sensing site for DNA molecules.[7, 8]

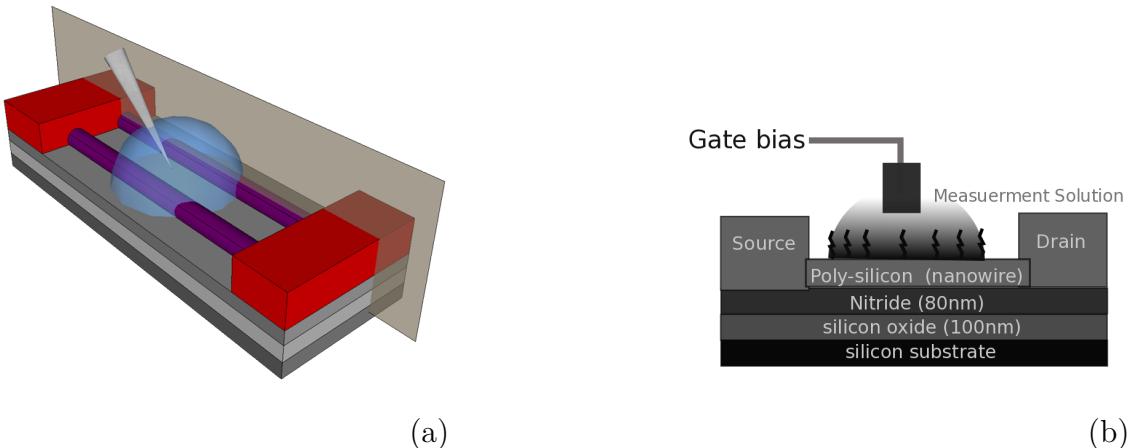


Figure 3.1: Nanowire Structure. (a) A nanowire element with two poly silicon channels. (b) is the sectional view of the cutting plane in (a).

3.2 Biology Experiment

The biology experiment data are provided by Prof.Yang's team. These data are the Id-Vg measurement of the same biomolecule placed under different circumstances or with different nanowire elements. With each measurement repeated three times, we find the mean and standard deviation (SD) of them and consider the SD value as the intrinsic noise of nanowire. We want to ensure that such noise should not be greater than the signal. To be more specific, we examine whether the Id-Vg curves of different concentration overlap with each other or not. We present an example below:

Fig.3.2 are concentration-dependent measurements (1 femto mole(fM) and 100fM biomolecule solution) obtained with two elements ((a) and (b)). The two curves in the (a) are distinguishable from the other after gate voltage of 1.4v They are not distinguishable in the (b) since they overlap each other. We thus assert that the element of (b) can't detect the concentration difference between 1fM and 100fM. The noise is stronger than the signal (The signal means the I_D difference caused by the concentration difference). The element of (a) can do so if it is biased at gate voltage larger than 1.4v or drain current larger than 1E-11.

In Fig.3.3, I_D increase with the biomolecule concentration. One can find that there is only a few “space” between PBS buffer and solution containing biomolecule with the concentration of 100aM. Hence the 100aM should be the limit of detection.

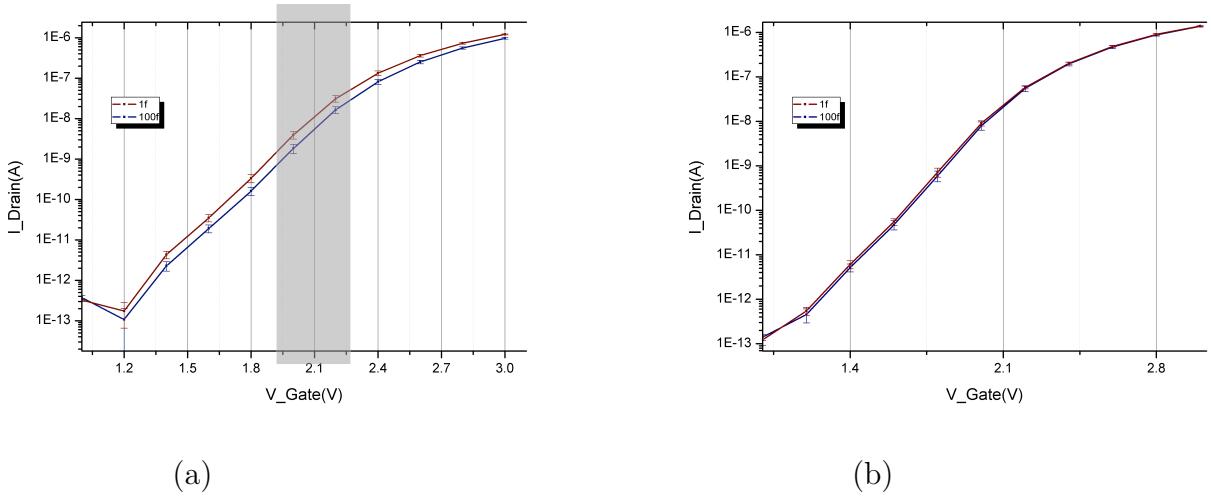


Figure 3.2: Concentration-dependent I_D - V_G curves of two equivalent nanowire elements. In (a), the measurement result of 1fM and 100fM biomolecule solution is distinguishable. There is no overlap between two curves. This is not true in (b).

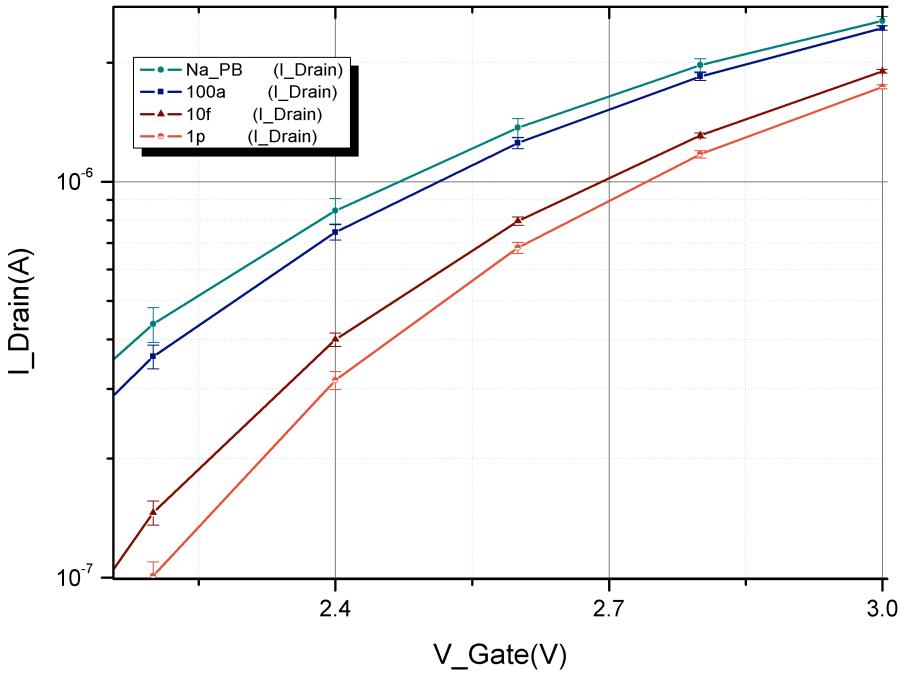


Figure 3.3: Concentration-dependent I_D - V_G curves with concentration of Na_PB(Buffer solution only), 100aM, 10pM, 1pM. Since the biomolecule is negative-charged, the lower the concentration is, the higher the curve is. To be noticed, the 10fM curve is closer to the curve of 1pM than 100aM.

It is worth noting that there is more space between 100aM and 10fM than the space between 10fM and 1pM. And the noise rate: $SD/Mean$ is independent of

concentration (Fig.3.4). Hence we say that the “resolution” for detecting concentration ranging from 100aM to 10fM may be better than the that ranging from 10fM to 1pM.

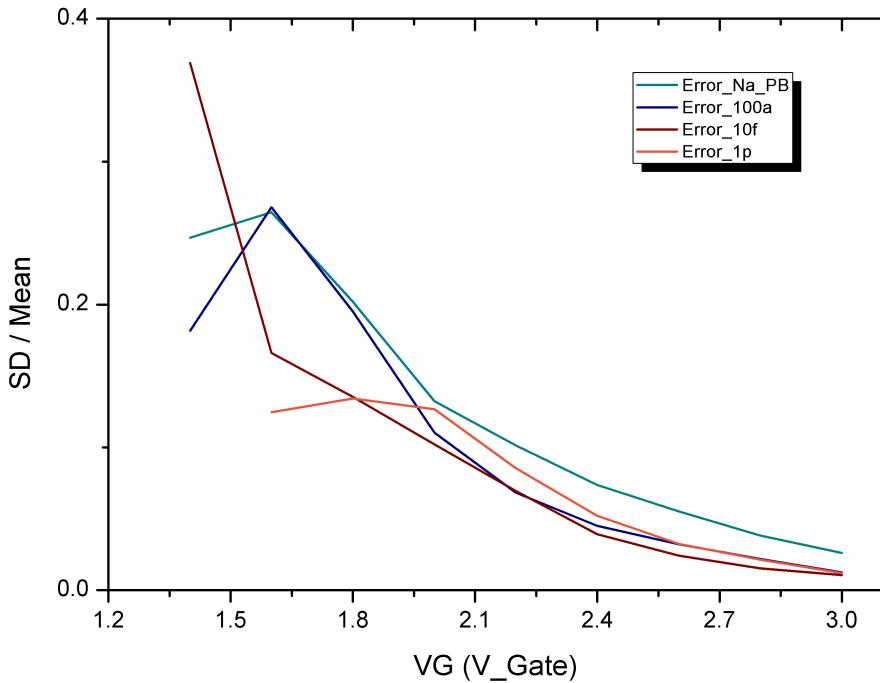
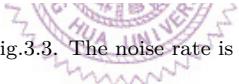


Figure 3.4: The noise rate of Fig.3.3. The noise rate is obtained by dividing SD by Mean.



3.2.1 Appropriate operation region

In [8], the team found that “the induced change of current (I_D) following biomolecule was dependent on the applied gate voltage (V_G)”. In other words, a “biomolecule concentration resolution” seems to depend on V_G . The team tried to find a bias gate voltage range which can induce more current response.

We also want to operate the nanowire under the condition that the element has the largest concentration resolution. Differently, we suppose that one should find the appropriate operation region instead of bias V_G range. And we take the noise effect in to consideration. The comprehensive method we proposed below proved that nanowire has the largest concentration resolution when operated in the weak inversion region adjacent to the transition region.

Our method is that we choose the operation region with more “noise tolerance”. The noise tolerance is defined as:

$$\text{noise tolerance} = \frac{I_{D1} - SD1 - (I_{D2} + SD2)}{I_{D2}} \quad (3.1)$$

I_D and SD are the mean and standard deviation of several I_D - V_G curves obtained in a same experimental condition. The larger the noise tolerance implies there is more space between two curves. And more space implies the less chance of overlapping that may happen between two concentration curves.

We present analysis results from three nanowire elements in Fig.3.5. Figure (a), (c), (e) are the I_D - V_G curves of three elements and Fig.3.5(b), (d), (f) are the noise tolerance respectively. One can observe in (b) and (d) that there is first a rising trend then followed by a drop as gate voltage decreases. The drop doesn't exist in (f) may because the measurement failed before the drop appears (The failure is because the I_D is too small to be detected.). But one can still observe the rising trend. The highest points of (b) and (d) locates in the weak inversion region and is adjacent to the transition region (The region between strong inversion and weak inversion region). We therefore suggest that in this section nanowire should have the largest concentration resolution.

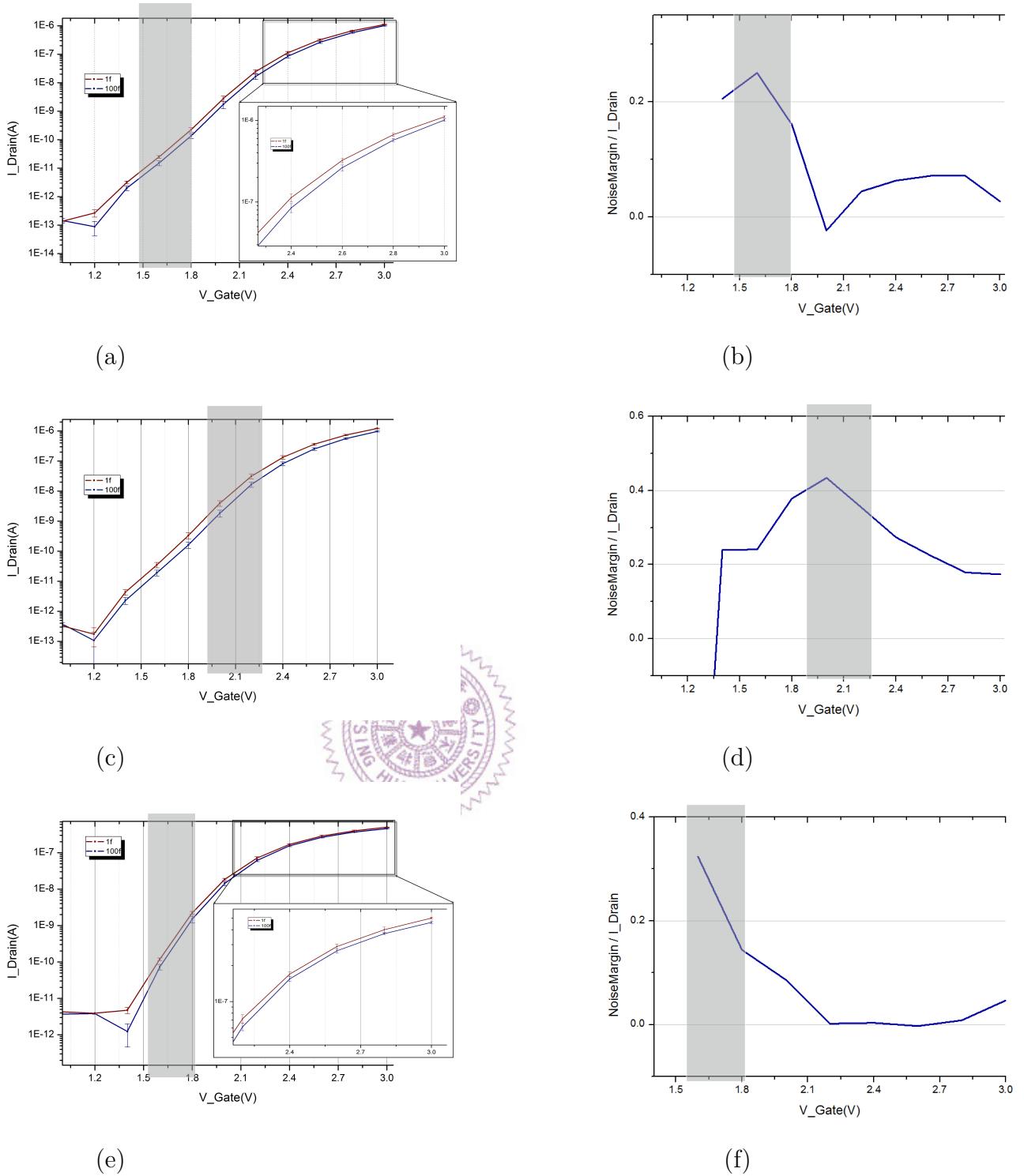


Figure 3.5

3.2.2 g_m - I_D Plot

We plot the g_m - I_D curve with the data in Fig.3.3. It clearly proves our two assumptions for dealing the disparity problem, which we have discussed in section.2.3.

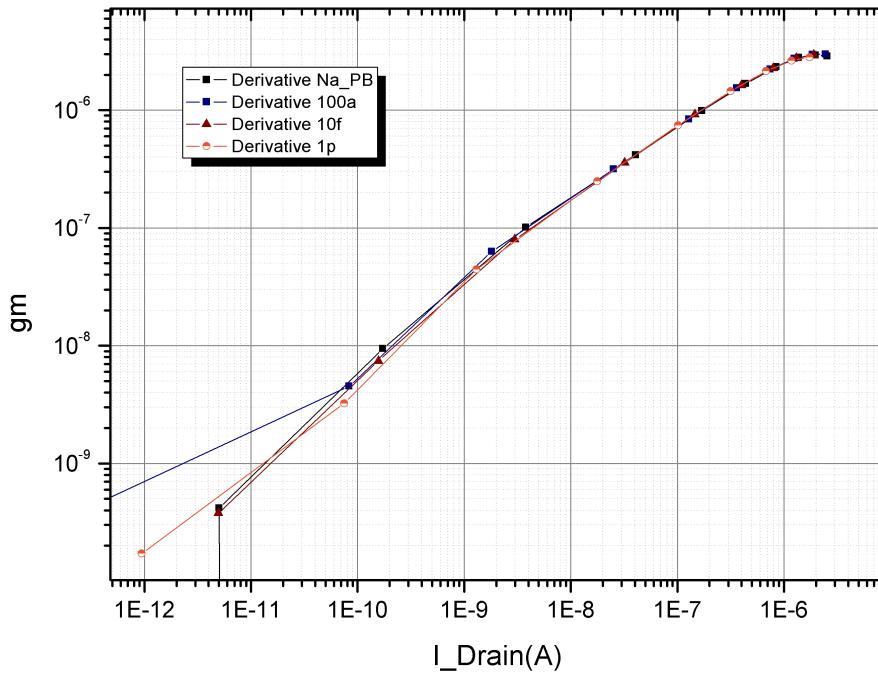


Figure 3.6: The g_m - I_D curve obtained by the I_D - V_G curve in Fig.3.3. The curves start splitting after $I_D > 1\mu\text{A}$ where the element may enter into strong inversion region.

In Fig.3.6, when I_D is from 0.1nA to $1\mu\text{A}$, we can observe that the g_m of nanowire is almost independent of concentration and merely depends on I_D . In fact, the curves start splitting after $I_D > 1\mu\text{A}$. It means the element is no longer in weak inversion region but enters into strong inversion region.

With the data from Fig.3.6, we may find the equivalent voltage value generated by the concentration difference based on the assumption 2 (section.2.3). The values

Concentration Difference	Na_PB - 100aM	100aM - 10fM	10fM - 1pM
Equivalent voltage value	$30mV - 40mV$	$200mV - 280mV$	$38mV - 60mV$

Table 3.1: The equivalent voltage value generated by the concentration difference. We obtained the data by the data from Fig.3.6. We divided the I_D difference of different concentration by their g_m ($\Delta I_D = g_m \Delta V_G$).

is changeable, which may result from the gate-coupling coefficient (Eq.2.14).

3.3 Electrical Measurements

This section presents the data analysis results. The data are obtained from our measurements with the source meter (Keithley 2602). To exclude the ion effect, we placed nanowire elements in dd-water instead of biomolecule solution. And there is no DNA probe on the poly-Si channel surfaces.

3.3.1 Front Gate and Back Gate

Our nanowire has two gates available: floating gate (liquid gate) and back-gate. We choose floating gate as the operation gate mainly because the floating gate can induce larger drain-current. In other words, it has higher transconductance (Fig.3.7). In our circuit design, nanowire is placed in a feedback loop where its transconductance is proportional to the loop gain (chapter 5).

There are some advantages of back-gate. One of them is the ability to lower the 1/f noise [14, 11]. But this only happens in a very high gate voltage, which is not practical in the integrated circuit design.

3.3.2 Transconductance

The most crucial parameter for our circuit design is the transconductance (g_m). We acquire it by finding the partial derivative of I_D of V_G . Since in section.2.3.1 we proved that g_m is related to I_D , we plot the g_m - I_D curve to reveal their relation (Fig.3.8(b)).

The g_m - I_D plot indicates that there is a “linear region” where g_m is proportional to I_D . This corresponds to our induction (Eq.2.18). We can recognize that our nanowire element is operated in weak inversion region when I_D is less than $10\mu\text{A}$. Therefore, by the section.3.2.1, we decide our the I_D of our nanowire should be operated below $10\mu\text{A}$.

We also proved that the transconductance under this region is unaffected by the V_{DS} .

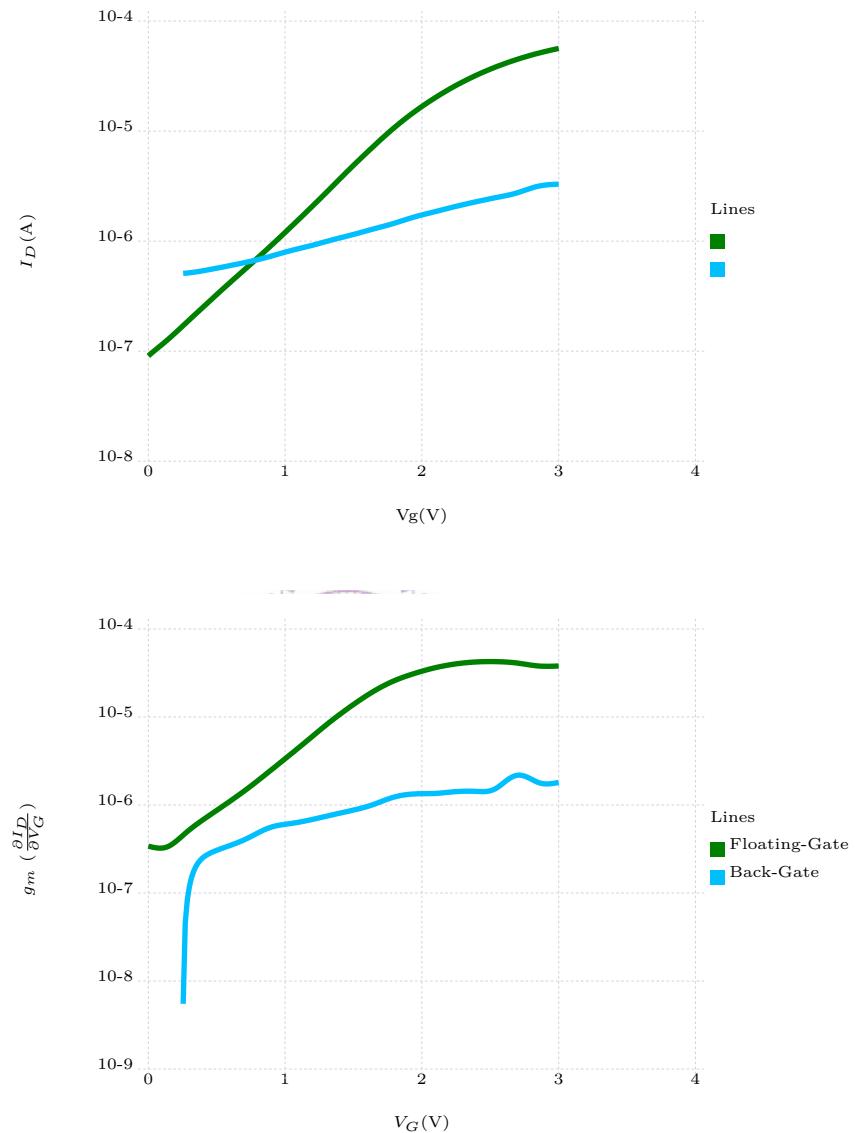


Figure 3.7: Comparison between the DC sweep of voltage on the floating gate and back gate. (a) I_D (b) Transconductance (g_m): the derivative of I_D . The transconductance of the floating gate is larger than the back gate.

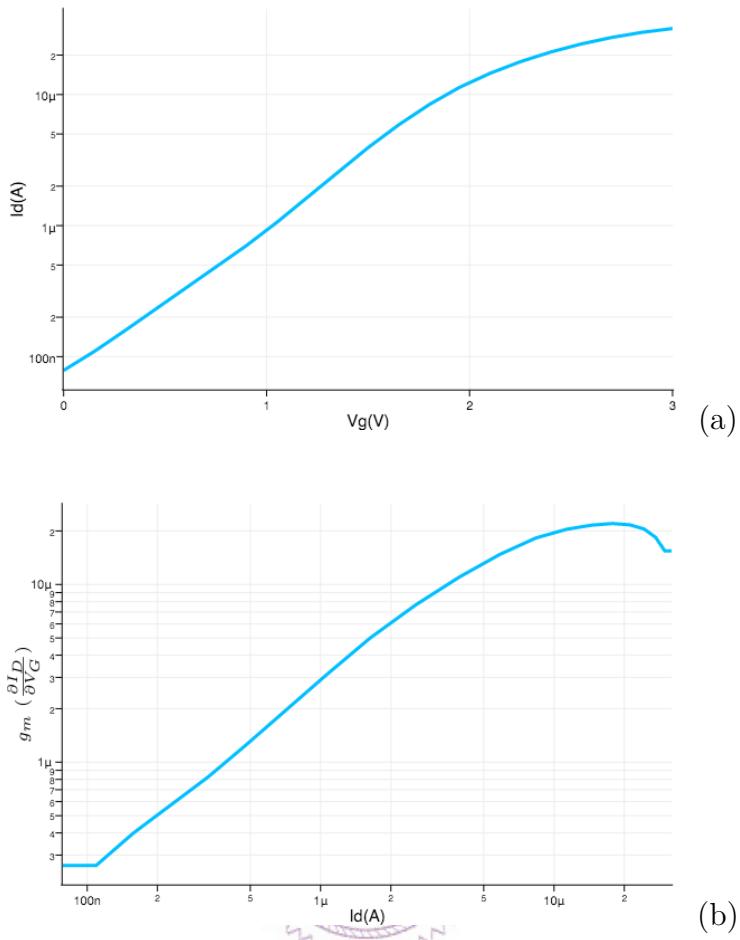


Figure 3.8: Electrical response of a nanowire element. (a) Sweep V_G and measure the I_D changes. And by finding the transconductance (g_m): the derivative of I_D of V_G , we plot (b) the g_m - I_D curve

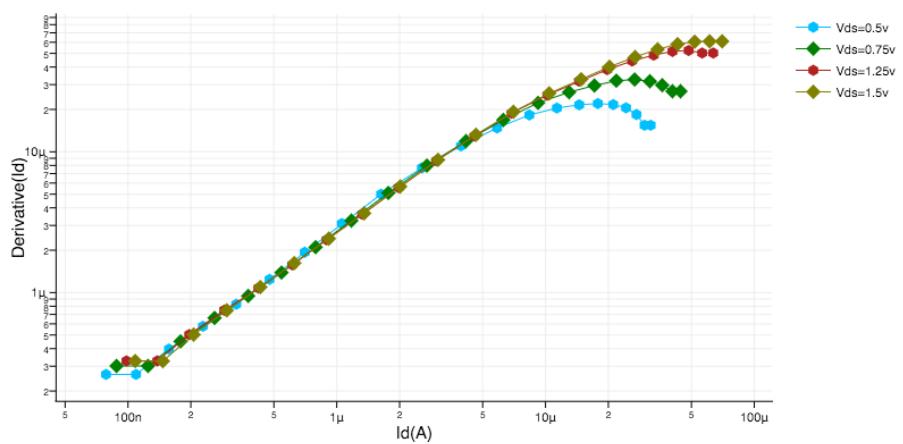


Figure 3.9: I_D -transconductance with V_{DS} variance

3.3.3 Drain-to-source impedance (r_{ds})

In our circuit design, we keep V_{DS} constant. By the measurement in last section, 0.7 is enough to keep nanowire in saturation region for V_G range from 0v to 3v. However, due to the fabrication variance, the value varies from 0.75v to 1v.

We concern about how the I_D effect r_{ds} . The way we obtained r_{ds} is as follows:

1. Perform I_D - V_G sweep with two different V_D .
2. Find the difference of I_D at each V_G sweep point and divide it by the difference of V_D .

The result is as Fig.3.10

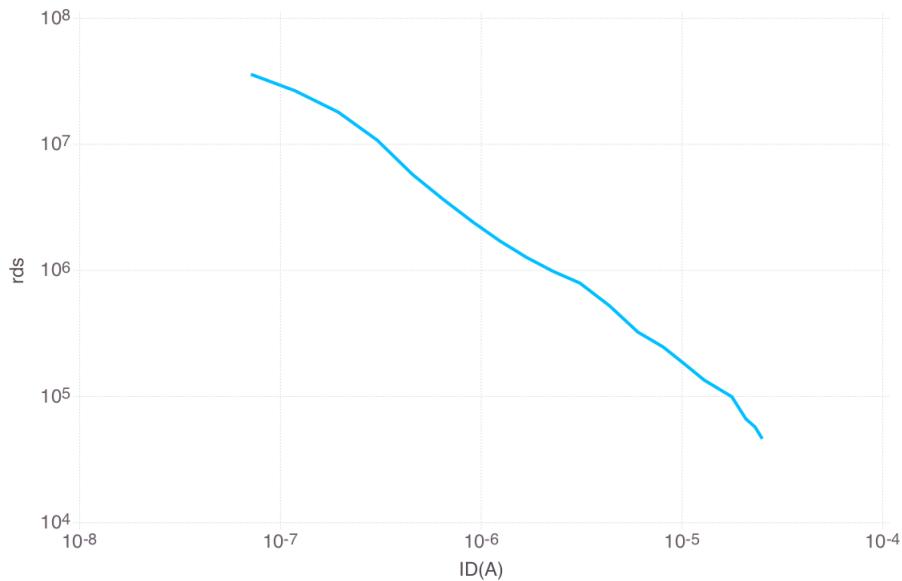


Figure 3.10: I_D - r_{ds} plot

3.3.4 Disparity Problem exists

We measured two nanowire elements which lie on the same wafer and are immersed with the same testing PBS solution. Below, the g_m - I_D plot (Fig.3.11) shows that even the environment is same, two elements exhibit different electrical response.

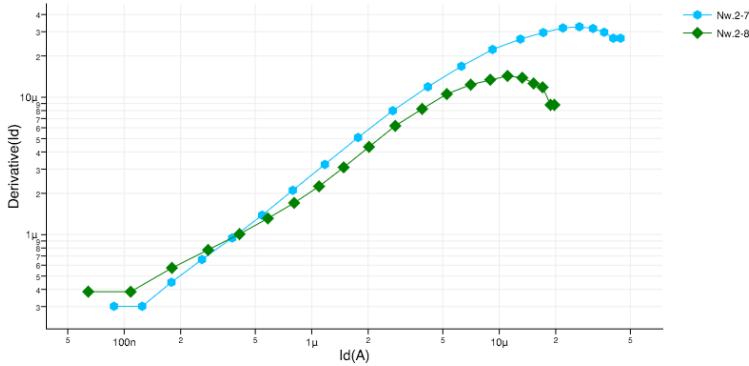


Figure 3.11: Disparity problem cause nanowire elements with same environment can exhibit different electrical responses.

3.4 Conclusion and Design Spec

Table 3.2 summarizes the electrical characteristics of our nanowire.

Operation Region	I_D	V_G	g_m	r_{ds}
Cut off	$< 100nA$	$< 0V$	-	-
weak inversion	$100nA - 10\mu A$	$0V - 2.5V$	$200n - 20\mu$	$50M\Omega - 200k\Omega$
strong inversion	$> 1\mu A$	$> 2.2V$	$20\mu - 30\mu$	$< 200k\Omega$

Table 3.2: Element electrical characteristics. There are overlaps due to the element disparity

We hence decide the detecting spec for the DC Sweep mode as in the table 3.3.

I_D	g_m
$100nA - 30\mu A$	$200n - 20\mu$

Table 3.3: Detecting Spec for the DC Sweep mode

As for the Transient Measurement mode, section 3.2.1 suggests that the element should be operated in the weak inversion region adjacent to the strong inversion region. And the table 3.1 tells that the minimum equivalent input voltage (ΔV_G) brought by concentration difference is $20mV$. To reach a better resolution, we require the input referred noise (referred to the gate) of our circuit to be less than 10% of this value ($< 2mV$). We also require the total input current to output voltage ratio to be $5M$. This is because the minimum g_m is $200n$ and the minimum current difference is $4nA$ ($20mV \times 200n$). We expect the output voltage larger than $20mV$.

We integrate these informatino in table.3.4. The Spec for the Transient Measure-

I_D	g_m	ΔV_G (min)
$600nA - 5\mu A$	$1\mu - 10\mu$	$20mV$

Table 3.4: The summation of the nanowire characteristics when applied with the Transient Measurement mode circuit

ment mode circuit is as in table.3.5.

Input referred Noise(V)	Amplification Rate (max)
$< 2mV$	$5E6(\frac{V}{A})$

Table 3.5: Spec for the Transient Measurement mode circuit



Chapter 4

Discrete Circuitry Design

This chapter contains the discrete circuit which has been briefly reviewed in section 2.1.2. We built this circuit to apply the constant current method to our nanowire element.

4.1 Transforming the design from p-type measuring into n-type measuring

In [10], the circuit is for p-type ISFET element (Fig.4.1). Our nanowire element is n-type. Hence we transformed the circuit into the one in Fig.4.2.

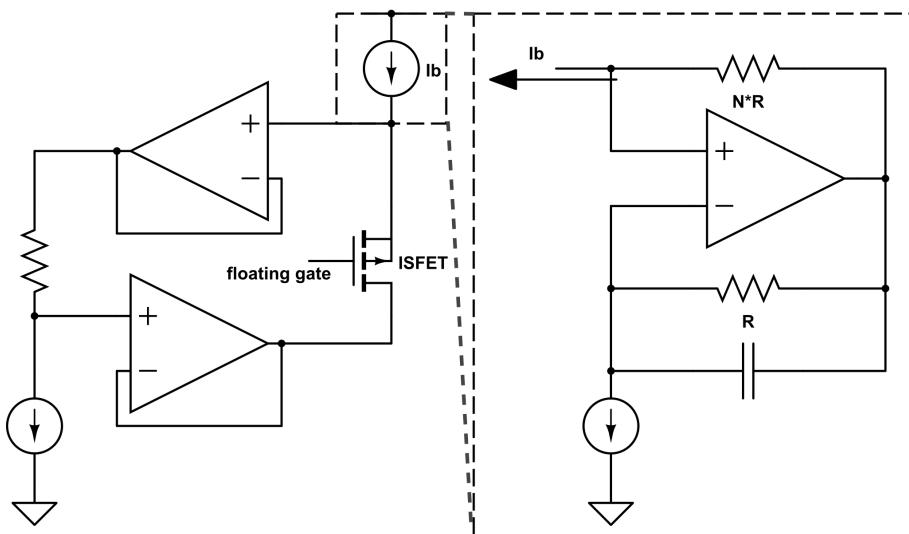


Figure 4.1: The schematic of read-out circuit from [10]. The ISFET is a p-type element. It is controlled by the current source I_b whose sub-circuit is shown at right.

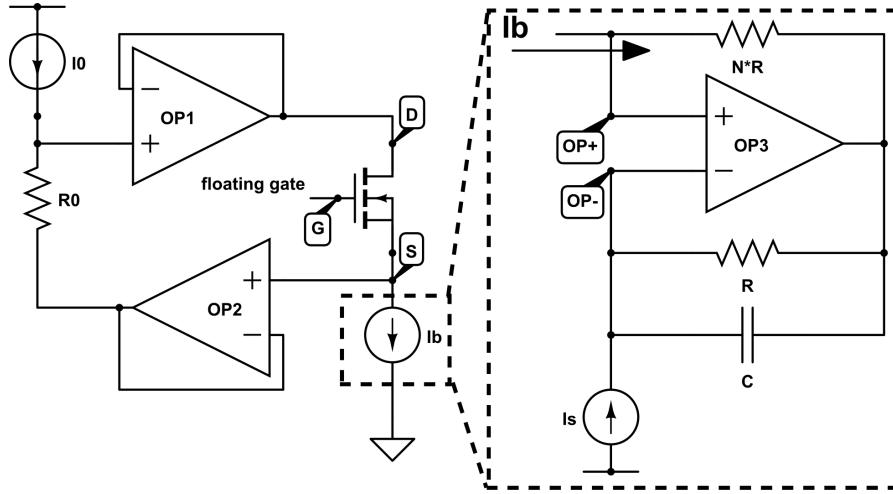


Figure 4.2: Our circuit schematic transformed from Fig.4.1. The center transistor is a n-type element. It is controlled by the current source I_b whose sub-circuit is shown at right.

4.2 Circuit Description

The circuit is divided into two sections: the circuit body and the biasing current source (I_b).

Circuit Body



The circuit body section is a source follower structure. The input of the circuit is at the floating gate (G) of the center transistor, where the output is at its source-end (S).

The I_D of the transistor is controlled by the I_b . Because the leakage current flowing into the negative input of OP2 is less than 0.1nA, the I_D of the transistor should always be same as the current provided by I_b .

The V_{DS} is always equal to the potential difference ($I_0 \times R_0$) across the resistor R_0 . This is achieved by two OP-based unity gain buffer. They connected serially with R_b and cause the voltage at the drain-end (D) follows the voltage at the source-end (S).

biasing current source (I_b)

The I_b is in fact a current scale down circuit. By concerning the OP as ideal, the node $OP+$ has the same voltage with $OP-$. This equalize the potential difference

across two resistors whose resistance are different by N -fold. As the result, the current of I_b and I_s are also different by N -fold. $I_b = I_s/N$.

The capacitor is for filtering. It filter the high frequency noise out to create a stable output current.

4.3 Discrete Element

We use tlc2264 made by Texas Instrument (TI) as our OP. This OP element has working voltage of $\pm 5v$ and can perform rail-to-rail output operation. Its gain (Large-signal differential voltage amplification rate) is 170 for the output load greater than 50k.

For the current source I_s and I_0 , we use lm334 made by National Semiconductor. It is a 3-terminal adjustable current sources with wide dynamic voltage range of 1v to 40v, and current accuracy of $\pm 3\%$. In our experiment, the current I_s is fixed at $1\mu A$ where its output impedance is $1.2G\Omega$.



4.4 Circuit Performance and Conclusion

We examined the performance of our circuit by plotting its I_D - V_G curve. The I_0 , R_0 and V_G were kept constant. We swept the I_D by changing the N value with a variable resistor. The N ranges from 1 to 1000. And the I_b circuit should produce bias current I_b from $1\mu A$ to $1nA$.

We measured the output voltage at S and subtracted this value from V_G to get the respective V_{GS} . These two value gave result to the I_D - V_G curve in Fig.4.3. We compare this curve with the curve obtained by directly sweeping V_G and measuring I_D with Source Meter (Keithley 2602).

The result shows that when I_D is larger than $10nA$, the circuit is functional. Two curves are same as each other.

The circuit fails when I_D is smaller than $10nA$. This is caused by the unmatched impedance, which we have discussed in section.2.1.2.

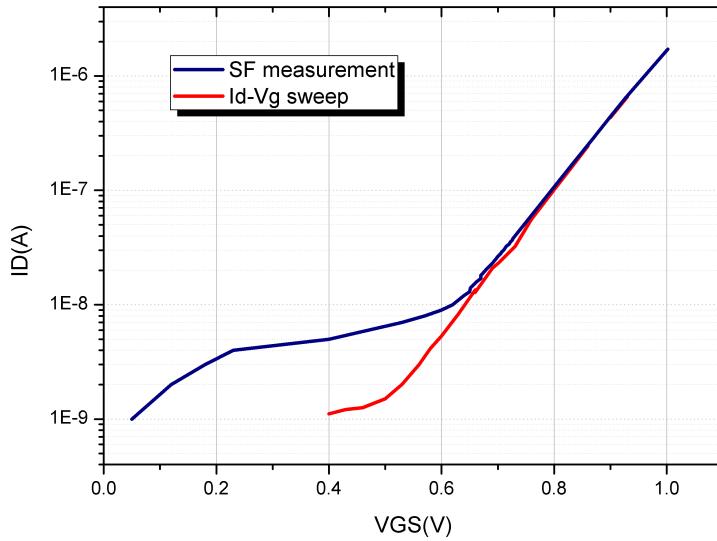


Figure 4.3: The measurement result (“SF_measurement”) compares with the direct I_D - V_G sweep (“Id-Vg sweep”).

The output impedance of Ib circuit is:

$$N \times R_s \quad (4.1)$$

R_s is the output impedance of current source I_s which equals to $1.2G\Omega$. And the current input impedance at the S of the circuit body is:

$$\frac{1}{g_m} \quad (4.2)$$

We plot the I_D -Impedance plot in Fig.4.4.

It shows that the output impedance of Ib is close to the input impedance of transistor when current is $10nA$ ($N = 100$). The impedance is unmatched.

Overall, the constant current method is feasible. What one needs to notice when applying the constant current method is the impedance matching. In source follower structure, its current input impedance varies with the bias current. It effects the dynamic range and need more design concern.

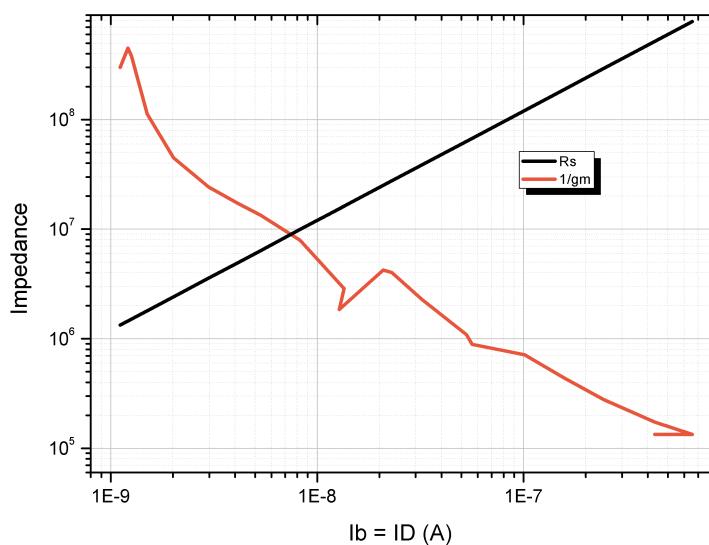


Figure 4.4: Input impedance of transistor (“1/gm”) and output impedance of Ib circuit (“Rs”). The former is found by the derivative of I_D of V_{Gs} . The latter is obtained by Eq.4.1.

Chapter 5

Integrated Circuitry Design

This chapter presents the design of the read-out circuit and the post-simulation results.

5.1 First Stage Circuit Design

The review of the source follower in section.2.1.2 suggests the constant current method for the circuit of DC Sweep mode. The data analysis from chapter 3 supports it by the linear relation between I_D and g_m . However, the section.2.2 shows that source follower is not suitable for AC measurement. It alternatively recommends the circuit in Fig.2.6 which measures the transient current signal and converts it into the voltage output.

The first stage circuit combined these two methods into one circuit structure with two modes available: the DC Sweep mode and the Transient Measurement mode.

5.1.1 DC Sweep mode

Fig.5.1 is the first stage circuit operated in the DC Sweep mode. The switch turns the circuit into DC Sweep mode by connecting with the gate of nanowire.

As in the source follower, our circuit contains a bias current source (I_{bias}) for controlling the I_D . The difference is that the I_{bias} inputs the current into drain instead of source. In addition to this, we apply the TIA from section.2.2 ([13]). Its output connects to a rail-to-rail OP amplifier and forms a negative feedback loop.

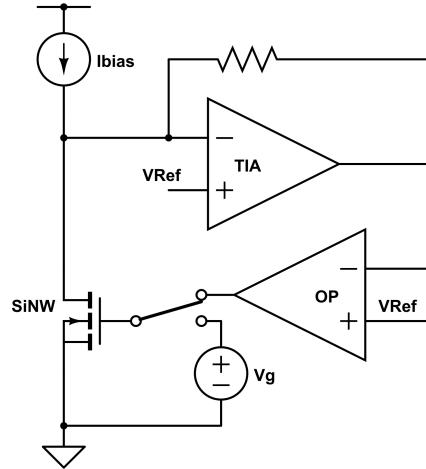


Figure 5.1

When I_D is less than the current of I_{bias} , the output voltage of TIA falls and the gate voltage V_G rises to increase I_D . On the contrary, output voltage of TIA rises and the gate voltage (V_G) drops if the current of I_{bias} is smaller than I_D . Finally, the feedback mechanism forces I_D be equal to the current of I_{bias} by adjusting V_G .

5.1.2 Transient Measurement mode

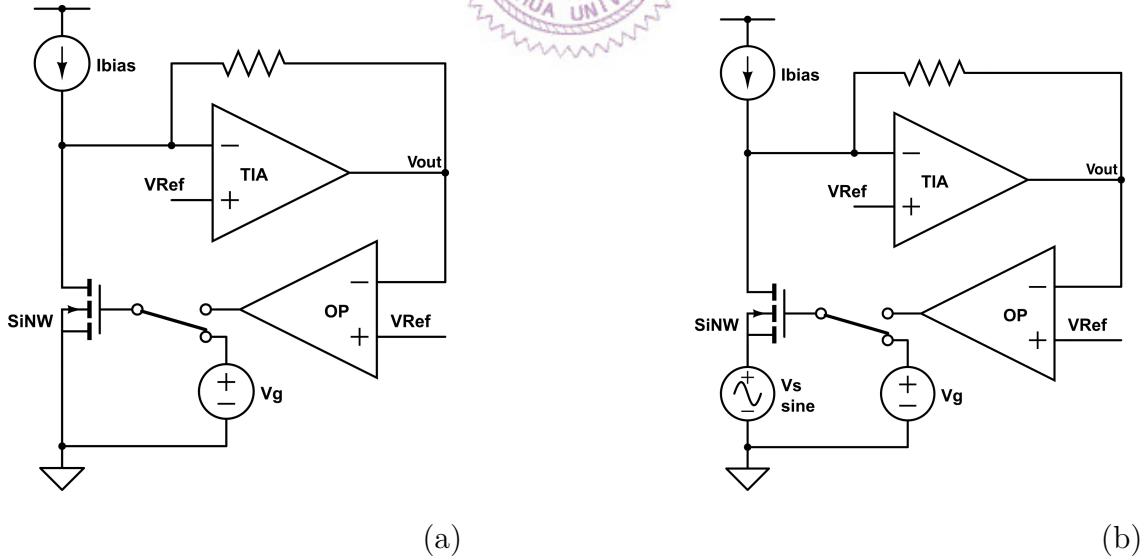


Figure 5.2

In Fig.5.2(a), the switch turns to a simple voltage source (V_g) that provides the gate of nanowire constant voltage bias. The feedback OP is nonfunctional in this

mode. When performing measurement, we directly find how the biomolecule concentration changes the output voltage (V_{out}). This output voltage will be input into the second stage circuit which is for the amplification.

Another Usage of Transient Measurement mode There is another method to perform measurement with Transient Measurement mode, which resembles the measurement in [13]. This method measures the g_m of nanowire. As in Fig.5.2(b), a sine wave signal with an amplitude of v_s is input to the source end of nanowire. The output response (V_{out}) is a sine wave of the same frequency with its amplitude equals to $v_s g_m \times R_{TIA}$. The values of Ibias and Vg can be arbitrary. But one need to be aware that their values should not cause the saturation of the output of TIA or the second stage circuit.

5.1.3 Dealing with the Disparity Problem

As mentioned in chapter 1, we combine DC Sweep mode and Transient Measurement mode to perform a disparity-resisting measurement.

Method Procedure Assuming there are two nanowire elements and the disparity problem exists between them. Initially, we use these element to perform the I_D-V_G sweep in the DC Sweep mode. We use the sweep results to find the g_m of each element. ($g_m = \frac{\partial I_D}{\partial V_G}$) When we turns to the Transient Measurement mode, we control these two elements under a same selected g_m by setting the Ibias and Vg to the corresponding values. After we add the measuring solutions, a same voltage differences at the output (V_{out}) should be detected because they have the same g_m . Before the next measuring solutions is added, we return to DC Sweep mode again. This is for finding the new bias V_G values to reset their I_D to be same with Ibias. This implies that every times when we apply the Transient Measurement mode to the elements, they always have the same I_D and g_m as the initial one.

5.1.4 Design Description

In this section, we first talk about the TIA block and focus on how we improve the detecting limits of this block. It is followed by the design of the TIA circuit. Then we analyze the feedback mechanism of the DC Sweep mode circuit and its input impedance. After that, we discuss the stability issue. Finally, we show the design of the feedback OP block.

5.1.4.1 Strategies for lowering current detecting limits

In section 2.2.3 about the TIA subcircuit as Fig.5.3(a), we mentioned that the detecting range of R_{NW} is limited by the I_{NW} provided by TIA. We now discuss the causes of the upper and lower limits, and show the strategies we use against them.

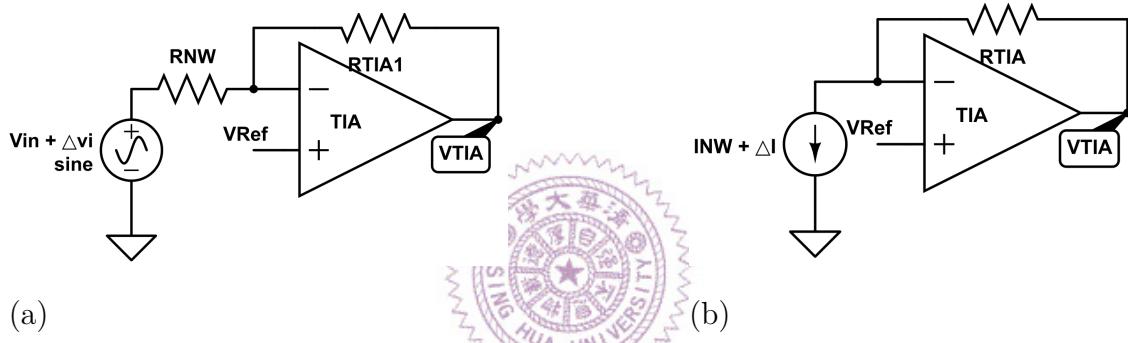


Figure 5.3: (a) The transimpedance block (TIA) of the read-out circuit from [13]. The circuit input a voltage signal into resistive nanowire element R_{NW} . To compare it with our circuit (Fig.5.4), we transform the voltage input into an equivalent current input in (b). The $I_{NW} = (V_{Ref} - V_{in})/R_{NW}$ and $\Delta i = \Delta vi/R_{NW}$

Lower Limit: In Fig.5.3(b), the TIA output voltage is:

$$V_{TIA} = V_{Ref} + I_{NW}R_{TIA} + \Delta i R_{TIA} \quad (5.1)$$

Two reasons which result in the lower limit of the detecting range relate to a large offset current I_{NW} . One is that the output current provided by the TIA is restricted by design. The other is that the restriction of the current flowing through the resistor R_{TIA} :

$$\frac{V_{Ref} - V_{SS}}{R_{TIA}} < I_{NW} < \frac{V_{DD} - V_{Ref}}{R_{TIA}} \quad (5.2)$$

Both reasons lead to the output saturation of TIA.

A naive way to handle the first one is to increase the output current which TIA can provide. The side effects of this method are the increases in power consumption and chip area. As for the second one, using smaller R_{TIA} can ease the restriction on I_{NW} . Unfortunately, this is unpreferable because it reduces the current-to-voltage ratio of TIA.

Our strategy for decreasing the lower limit is to utilize the bias current source (I_{bias}) of nanowire. As in Fig.5.4, the Eq.5.1 is transformed into:

$$V_{TIA} = V_{Ref} + (I_{NW} - I_{bias})R_{TIA} + \Delta i R_{TIA} \quad (5.3)$$

Now we can diminish the large I_{NW} by I_{bias} .

In conclusion, the large offset current causes the saturation of the output of TIA. We use the biasing current source to diminish that offset current, hence increases the detecting range.

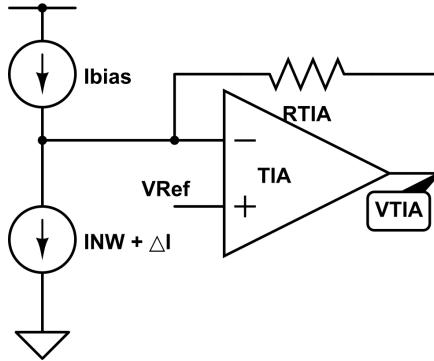


Figure 5.4

Upper Limit: The upper limit issues from the output resolution. When the input current signal Δi in fig.5.4 is too small, the output response may be defeated by the noise. This may be solved by raising up the SNR through a larger R_{TIA} . However, the chip area constrains the size of resistors. In our circuit design, we cannot make this resistance value out of $100k\Omega$. Furthermore, even if the resistor can be greater, one need to concern for the noise brought by the large resistance.

Our strategy is to boost the SNR of TIA by designing its input MOSFETs in a large area. We also amplify the output signal through the second stage circuit.

5.1.4.2 TIA (Transimpedance Amplifier) Design

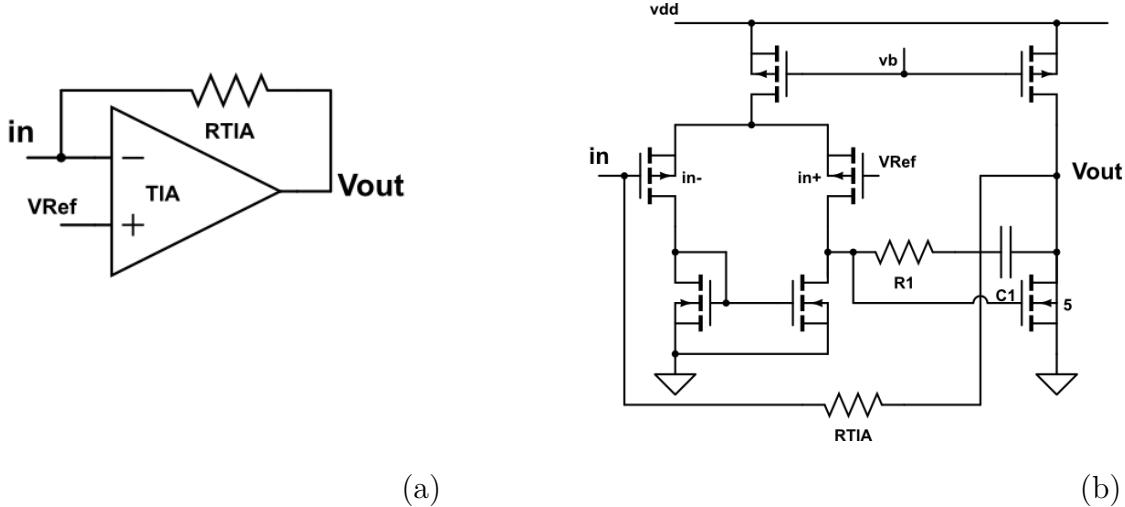


Figure 5.5: (a)The transimpedance block and the (b) schematic

Fig.5.5 is the circuit of our Transimpedance Amplifier circuit. We implement the operational amplifier in TIA with the two-stage differential pair single output structure. This structure prevails other structure such as folded cascode or single stage OP because:

1. Larger output current tolerance As we mentioned in the last section, one of the methods to decrease the lower limit is to increase the output current that TIA can provide. We use large size pmos and nmos at the output stage of OP. This allows the OP can tolerate a larger output current. Moreover, separation between the output stage and the input stage minimizes the effect of the substantial current variance on the OP gain.

2. Rail-to-Rail Output The dynamic range of $Vout$ limits the maximum of the input current. The structure can provide the greatest output dynamic range among others.

The Fig.5.6 and Fig.5.7 show the dc and ac post-simulation of the TIA. The table.5.1 is the summation of the simulation result.

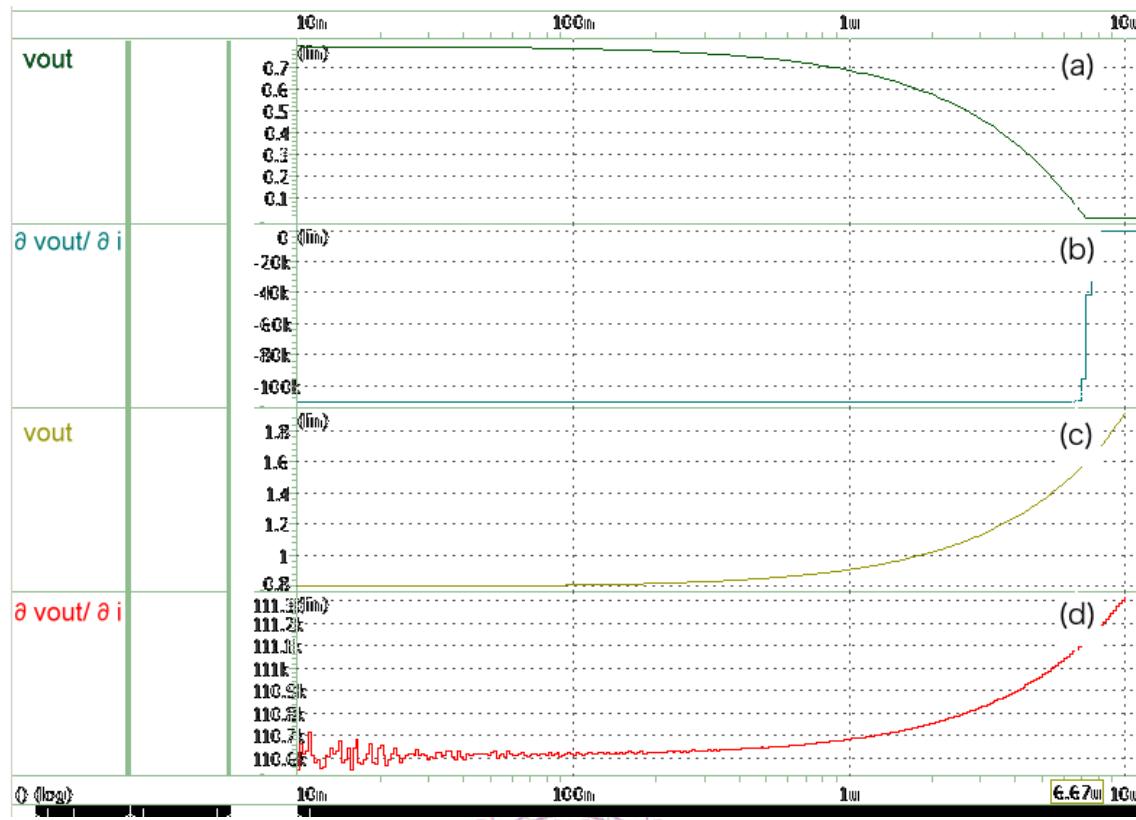


Figure 5.6: The dc simulation results of TIA. The x-axis represents positive/negative input current (log scale). (a) is the V_{out} responding to the positive input current while (c) is to the negative input current. (b) and (d) are the derivative of V_{out} of input current ($\frac{\partial V_{out}}{\partial I_{in}}$) from (a) and (c) respectively.

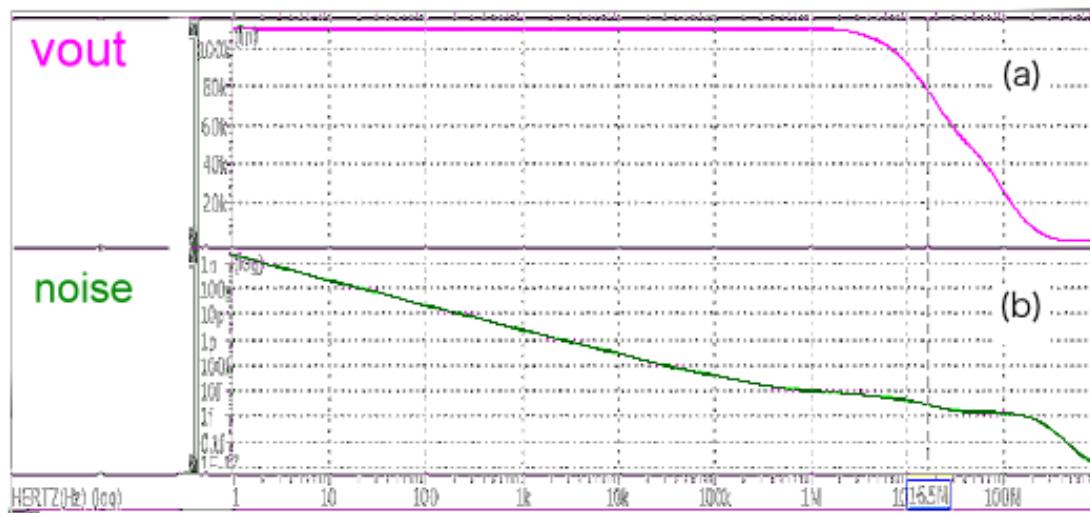


Figure 5.7: The ac simulation results of TIA. The x-axis is the input signal frequency. (a) is the V_{out} and (b) is the output-referred noise.

Input Current range	from $6\mu A$ to $-10\mu A$
Bandwidth	7M Hz
Output referred noise (@10Hz)	$0.01mV$

Table 5.1: Post-simulation result of TIA

5.1.4.3 Feedback Mechanism

The DC Sweep mode circuit forms a negative feedback loop. Fig.5.8 is the block diagram of the circuit.

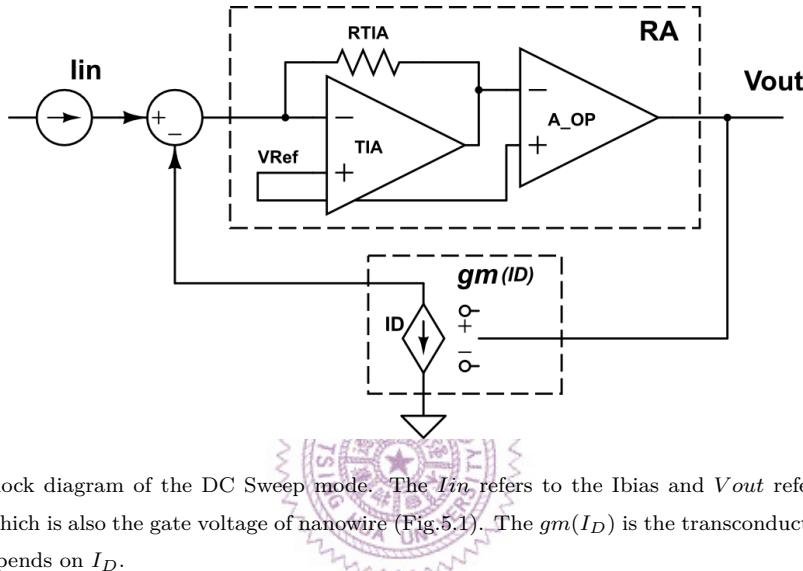


Figure 5.8: Block diagram of the DC Sweep mode. The I_{in} refers to the Ibias and V_{out} refers to the output voltage of OP, which is also the gate voltage of nanowire (Fig.5.1). The $gm(I_D)$ is the transconductance of nanowire whose values depends on I_D .

From the block diagram, we can compute the loop gain (LG) and the transfer function (TF):

$$R_A = R_{TIA} \times A_{OP} \quad (5.4)$$

$$LG = R_A \times g_m \quad (5.5)$$

$$TF = \frac{V_{out}}{I_{in}} = \frac{R_A}{1 + LG} \quad (5.6)$$

$$\approx \frac{1}{g_m} \quad \text{If } LG \geq 100 \quad (5.7)$$

The transfer function suggests that if we want to obtained a I_D-V_G sweeping results with the error less than %1, our loop gain should be greater than 100. According to chapter 3, the spec for g_m detection ranges from $200n$ to $20u$. This implies that

the A_{OP} should be at least greater than 5k. We will show that the ultimate A_{OP} is 10k in the next section.

The post-simulation result is presented in Fig.5.9. We performed AC analysis by sending a small current signal to I_{in} and detected the AC response of V_{out} . Meanwhile the g_m of nanowire is kept at certain values. Afterwards, we compared the g_m values with the $\frac{I_{in}}{V_{out}}$. The comparison are summarized in table.5.2.

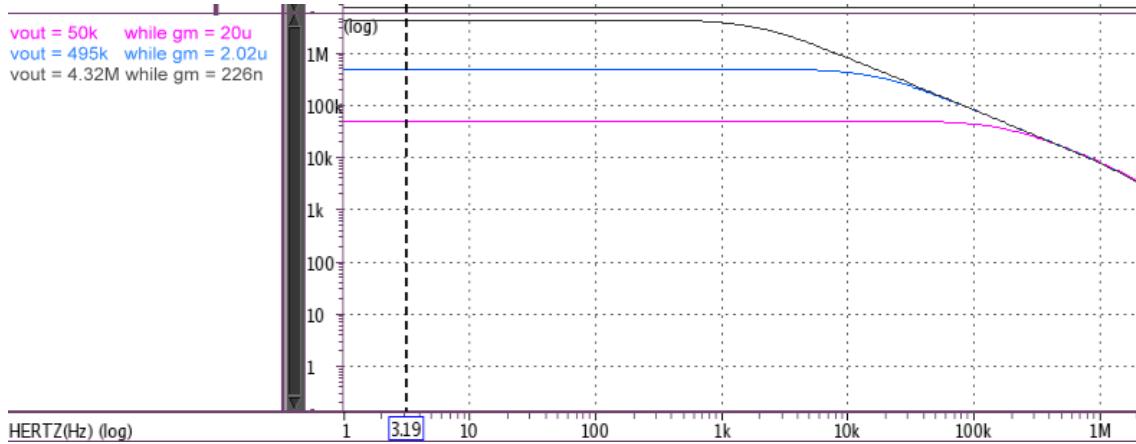


Figure 5.9: The simulation results of $\frac{\Delta v_{out}}{i_{in}}$

	V_{out}	$\frac{I_{in}}{V_{out}}$	error
$g_m = 20\mu$	50k	20μ	Unable to detect
$g_m = 2.02\mu$	495k	2.02μ	Unable to detect
$g_m = 226n$	4.32M	$231.5n$	1.02%

Table 5.2: The the comparison of g_m and $\frac{I_{in}}{V_{out}}$

5.1.4.4 Input Impedance (DC Sweep mode)

From chapter 4, we have discussed the impedance matching between current source and nanowire element. Here we compute the input impedance of the circuit.

In Fig.5.10, we apply an input voltage Δv_x and find the Δi_x . The input impedance

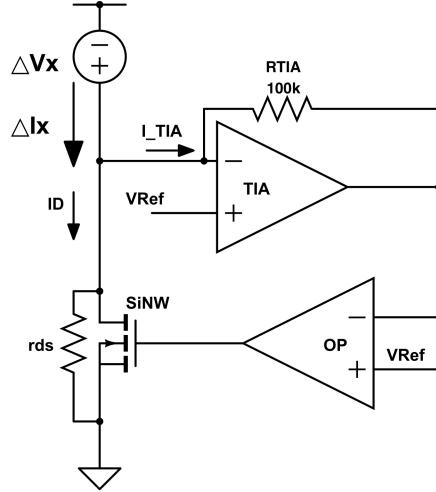


Figure 5.10

of the circuit is $\Delta v_x / \Delta i_x$.

$$\Delta i_x = i_D + i_{TIA} \quad (5.8)$$

$$i_D = \frac{\Delta v_x}{r_{ds}} + \Delta v_x A_{TIA} A_{OP} g_m \quad (5.9)$$

$$i_{TIA} = \frac{\Delta v_x}{R_{TIA}/(1 + A_{TIA})} \quad (5.10)$$

$$\Delta v_x / \Delta i_x = \left(\frac{1}{r_{ds}} + A_{TIA} A_{OP} g_m + \frac{1 + A_{TIA}}{R_{TIA}} \right)^{-1} \quad (5.11)$$

$$= \frac{R_{TIA}}{(1 + A_{TIA})(1 + R_{TIA} A_{OP} g_m)} \quad (5.12)$$

The A_{TIA} is the gain of the opAmp in TIA block. The A_{OP} is the gain of the feedback OP. The r_{ds} is the drain-to-source resistance of nanowire, which is larger than $100k\Omega$.

The Eq.5.12 can be rewritten into:

$$\frac{Z_{in}}{1 + LG} \quad (5.13)$$

where the Z_{in} is the input impedance of TIA.

The OpAmp of TIA holds the gain of 1000 (60dB), which makes the Z_{in} of 100. The LG is greater than 5k from the last section. In our design, the Ibias is a simple pmos. Its output impedance ranges from $1M\Omega$ to $1G\Omega$. It is obvious that the input impedance is much smaller than the r_{ds} . The result tells that the impedance matching is fine.

5.1.4.5 Stability and Feedback OP Design

To decide the structure of the feedback OP, we must discuss the stability of the feedback loop in the DC Sweep mode. The OP plays a crucial role in the stability issue because it not only decides the loop gain but also contains the dominant pole at its output.

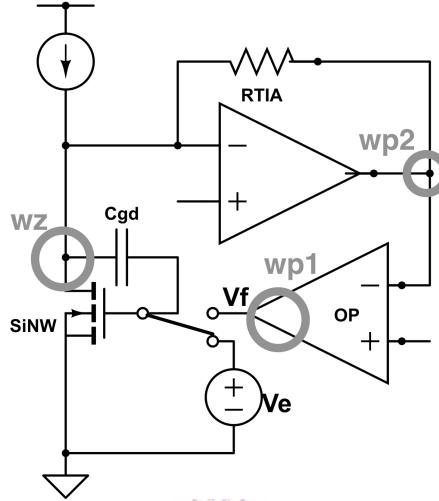


Figure 5.11

In Fig.5.11, we mark the dominant pole (w_{p1}), second order dominant pole w_{p2}) and the zero (w_z). We can write the loop gain as:

$$\frac{v_f}{v_e} = R_{TIA} \times A_{OP} \times g_m \frac{1 - s/w_z}{(1 + s/w_{p1})(1 + s/w_{p2})} \quad (5.14)$$

$$w_z = \frac{g_m}{C_{gd}} \quad (5.15)$$

The parasitic capacitance C_{gd} , at the conservative estimate, has a maximum value of $1pF$ (The estimation is based on the fabrication information from [5] and [8]). And because the lower bound of g_m in our design spec (table.3.3) is $200n$, the w_z can be as small as $20k$. To force the total loop gain to drop to 1 before $s > 2k$, we have to move the first dominant pole left.

We choose the w_{p1} as the first dominant pole. From section.5.1.4.3, we learned that the A_{OP} should be larger than $5k$. Thus, we choose a folded cascode structure which provides high output impedance and gain.

We designed a folded cascode OP with gain of $10k$ (80dB) and bandwidth less than 3Hz (Fig.5.12, Table.5.3). A higher gain prevents the circuit from the fabrica-

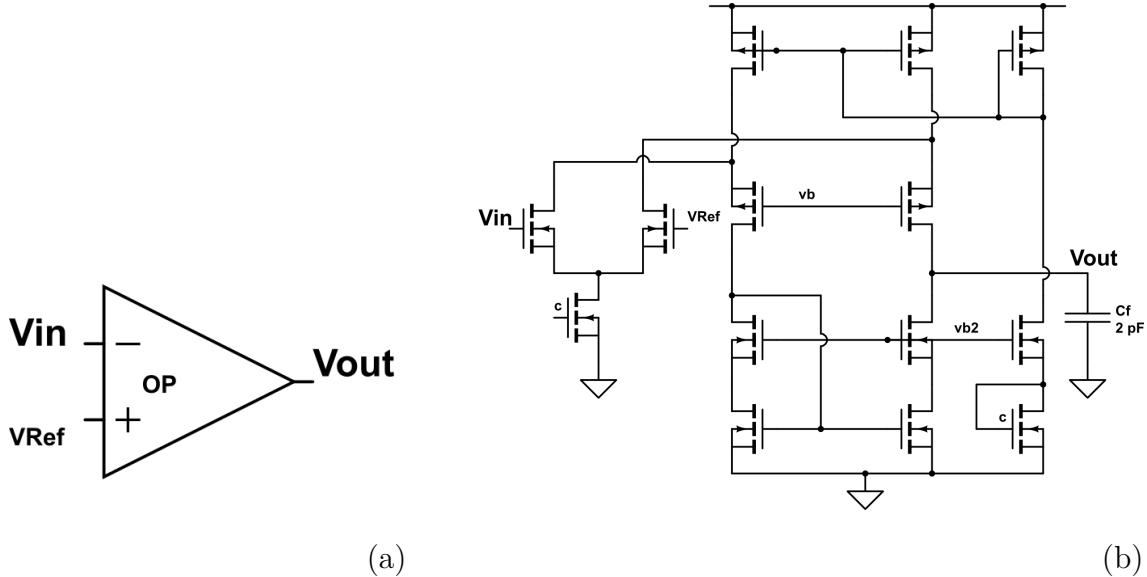


Figure 5.12: (a)The feedback OP block and its (b) schematic

tion flaw (30% deviation of the impedance of the R_{TIA} in TIA block). The low bandwidth is owing to the large capacitance (C_f) appended to the output. This capacitance results in a lower slew rate, which is fine because the circuit is for DC signal and there is no need for high speed operation.

BandWidth	2 Hz
Max Gain	81dB
Output Dynamic Range	0.45V - 2.6V

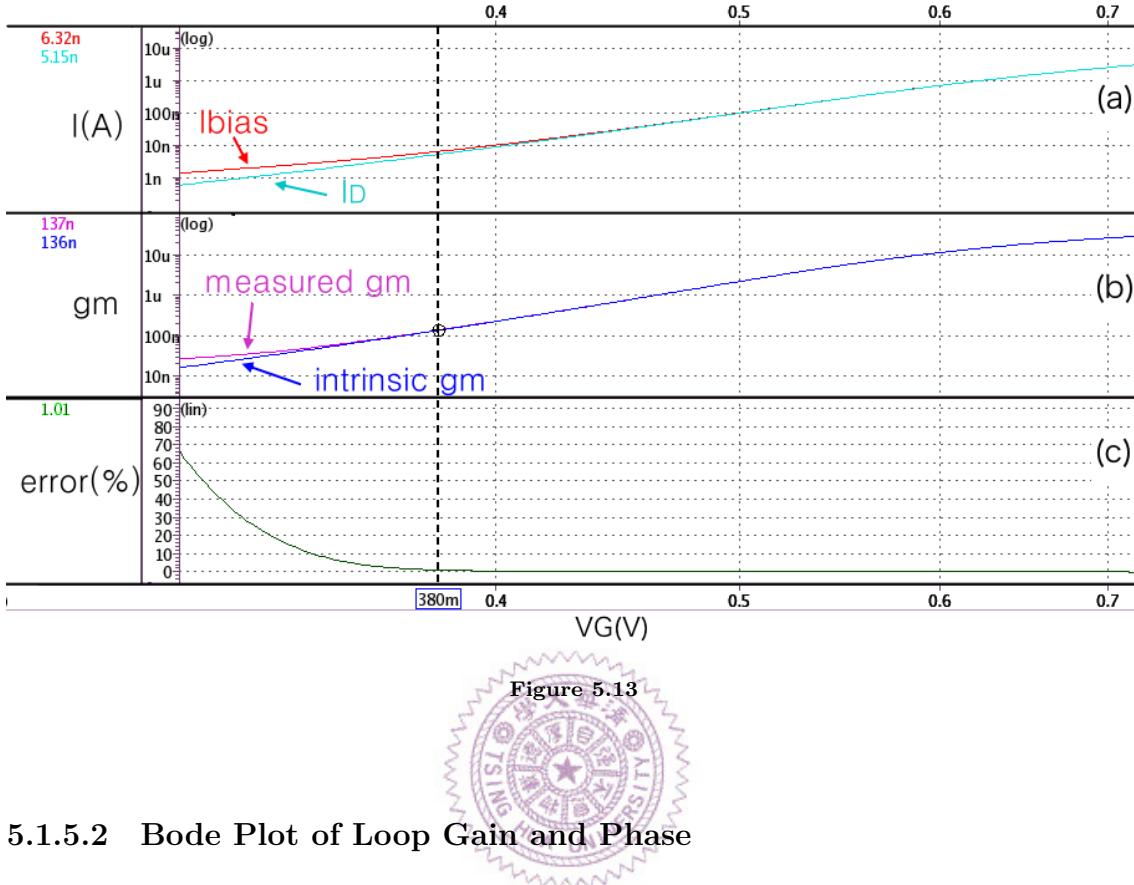
Table 5.3: Post-simulation result of feedback OP

5.1.5 The Post-simulation Result of the DC Sweep mode circuit

5.1.5.1 DC Current (Ibias) Sweep

We swept the Current of Ibias and measured the output voltage of the feedback OP which is also the V_G . We also measured the I_D of the transistor. (Because we don't have nanowire model, we performed the simulation by using an alternative mosfet.) The curve of I_{bias} - V_G is compared with the curve of I_D - V_G (Fig.5.13 (a)). Moreover, we compare the measured g_m ($\frac{I_{bias}}{V_G}$) with the intrinsic g_m ($\frac{I_D}{V_G}$) (Fig.5.13(b)).

This is according to the section of the feedback mechanism (section.5.1.4.3). The result in Fig.5.13(c) shows that the error is over 1% when the g_m of the transistor is less than $130n$.



5.1.5.2 Bode Plot of Loop Gain and Phase

The simulation here is according to the stability section (section.5.1.4.5). We present the Bode plot of the loop gain and the phase (Fig.5.14). The summarization table is also given (Table.5.4). We adjusted the transistor to the specific g_m values by selecting the Ibias and corresponding V_G . We also appended a $1pF$ capacitance to model the C_{gd} .

g_m	20μ	2μ	$200n$
Loop Gain	20k	2k	200
Phase Margin	80(deg)	78(deg)	81 (deg)

Table 5.4: The phase margin and loop gain of the first stage circuit

The table.5.5 is for comparing the design spec and the simulation result. To be noted that the upper limit of I_D and g_m of our circuit is unclear because they depends on two factors. One is the gate voltage. Tbale.5.3 shows that the maximal

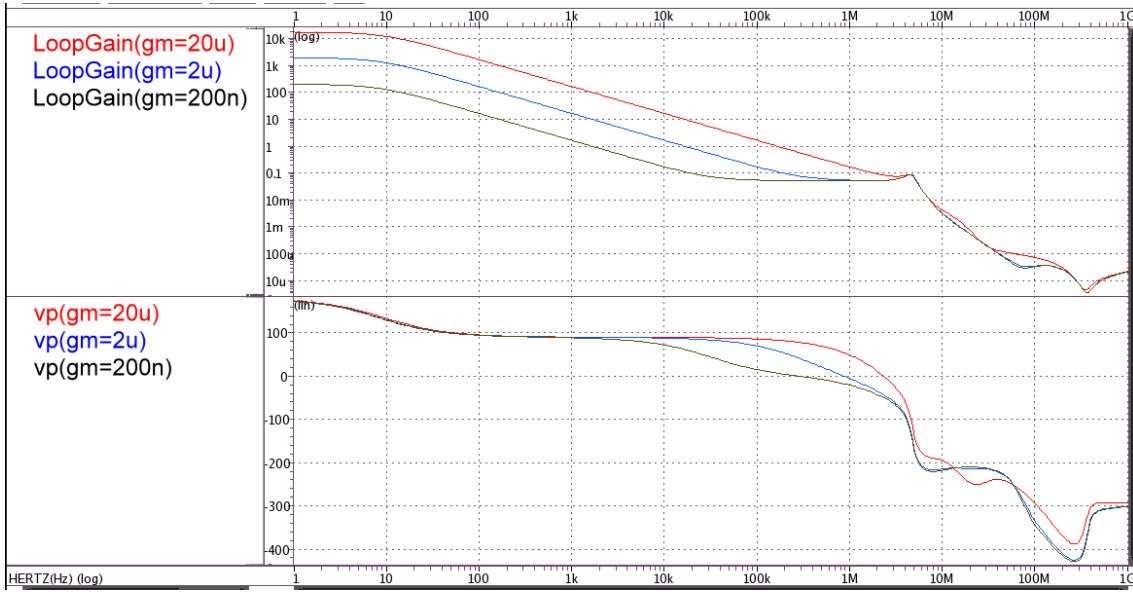


Figure 5.14: Results of the ac simulation of the loop gain and phase (Bode plot) with different g_m value ($200n$, $2u$, $20u$). These g_m value is selected according to the DC Sweep mode spec we set in chapter 3 (section.3.4).

gate voltage that the Feedback OP can provides is $2.6V$. The other is the current bias. The Ibias is a simple pmos whose current is decided by an external resistor (Fig.5.15). This current mirror structure has a maximum output current of $70\mu A$.

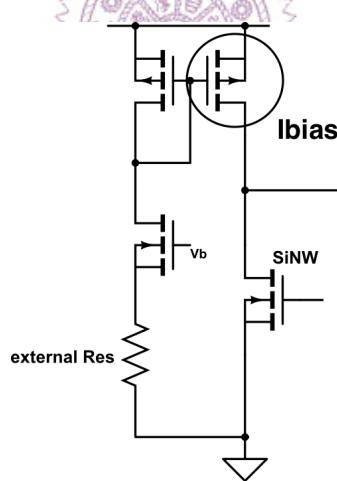


Figure 5.15: The current mirror structure of the current source Ibias.

	Design Spec	Simulation result
I_D	$100nA - 30\mu A$	$> 20nA$
g_m	$200n - 20\mu$	$> 130n$

Table 5.5: The comparison between the design spec and simulation result of the DC Sweep mode circuit.

5.2 Second Stage Circuit Design

We discuss the second stage circuit in this section. To be noted that the second stage circuit is only for Transient Measurement mode.

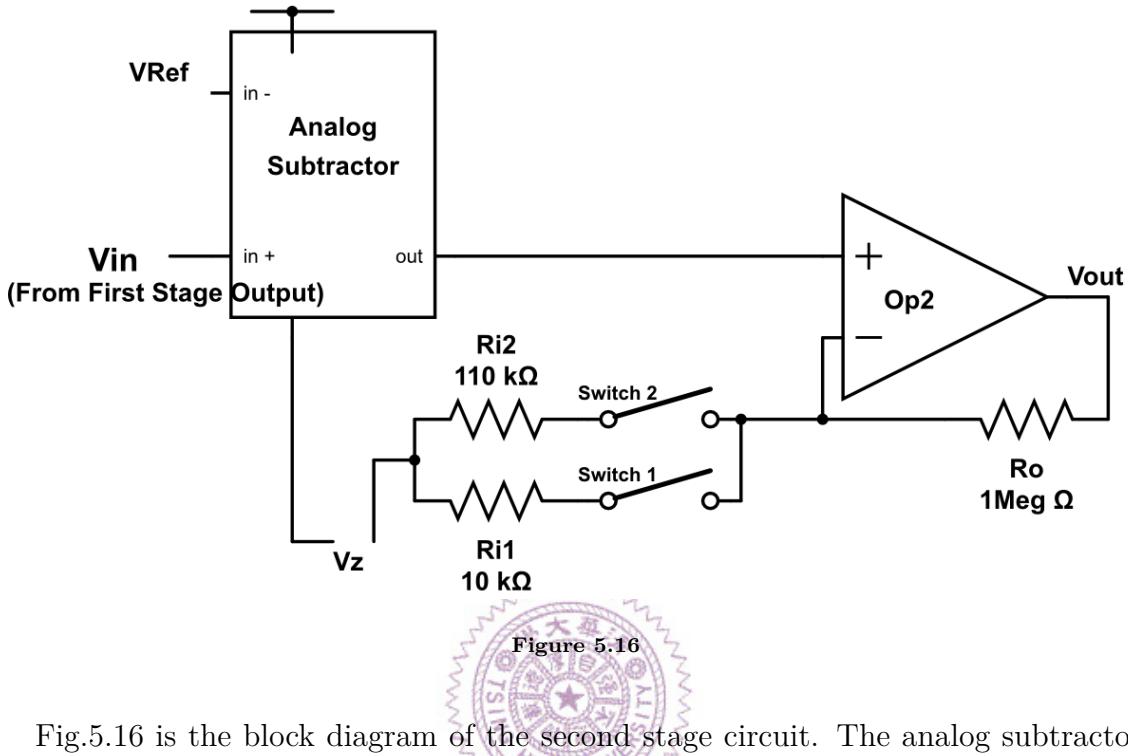


Fig.5.16 is the block diagram of the second stage circuit. The analog subtractor shifts the voltage of the V_{in} from V_{Ref} to V_z . It follows by a resistor-based non-inverting amplifier composed of a two-stage differential operational amplifier, two switches and three resistors. The switches select the amplification rate among 100, 10 and 1.

5.2.1 Analog Subtractor

Fig.5.17 is the schematic of our analog subtractor which references [15]. The output voltage equals to:

$$v_x - V_{Ref} + v_z \quad (5.16)$$

A voltage signal Δv sent to v_x induces a current difference (Δi_d) of M_x . This current is mirrored to the diode-connected M_z by the cascode current mirror formed by M_1 to M_4 . The changing of the current changes the gate voltage of M_z . And this voltage is buffered to the output by the source follower M_5 .

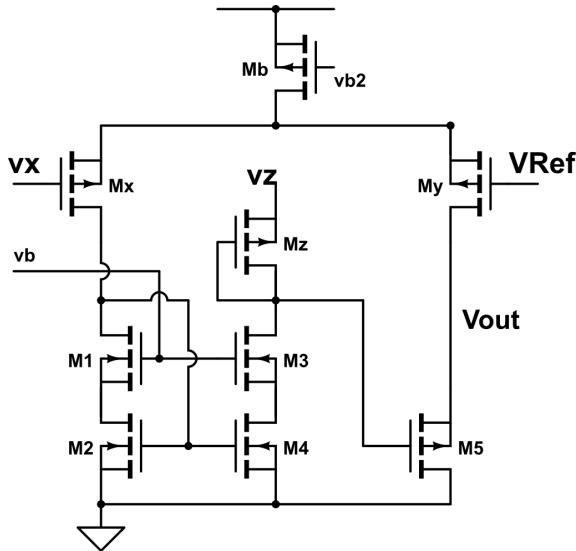


Figure 5.17: Block diagram of the second stage circuit.

$$\Delta v_{out} = \Delta v_x \frac{g_{mx}}{g_{mz}} - V_{Ref} \frac{g_{my}}{g_{m5}} + v_z \quad (5.17)$$

$$\Delta v_{out} = \Delta v_x - V_{Ref} \quad \text{For } g_{mx} = g_{mz}; g_{my} = g_{m5} \quad (5.18)$$

One of the reasons that we apply this block is because the V_{Ref} is an internal voltage reference which may drift by the process variance. We prefer the output offset voltage of the circuit to be constant and controllable. In such a way, we shift it to v_z which is controlled by an external voltage source. Another reason is to increase the input dynamic range of the next amplifier block. This reason will be much clearer when we start discussing the amplifier block in the next section.

We performed DC sweep on input (v_X) and v_z at five corners to show the linear region of the circuit (Fig.5.18, Table.5.6). The circuit has input dynamic range of $0.77V$ while the dynamic range for v_z is $0.38V$.

To be more specific, the input dynamic range is from $-0.5V$ to $+0.2$. When the current flowing through the TIA block is greater than $+5\mu A$ or smaller than $-2\mu A$, the output of the second stage circuit is saturated.

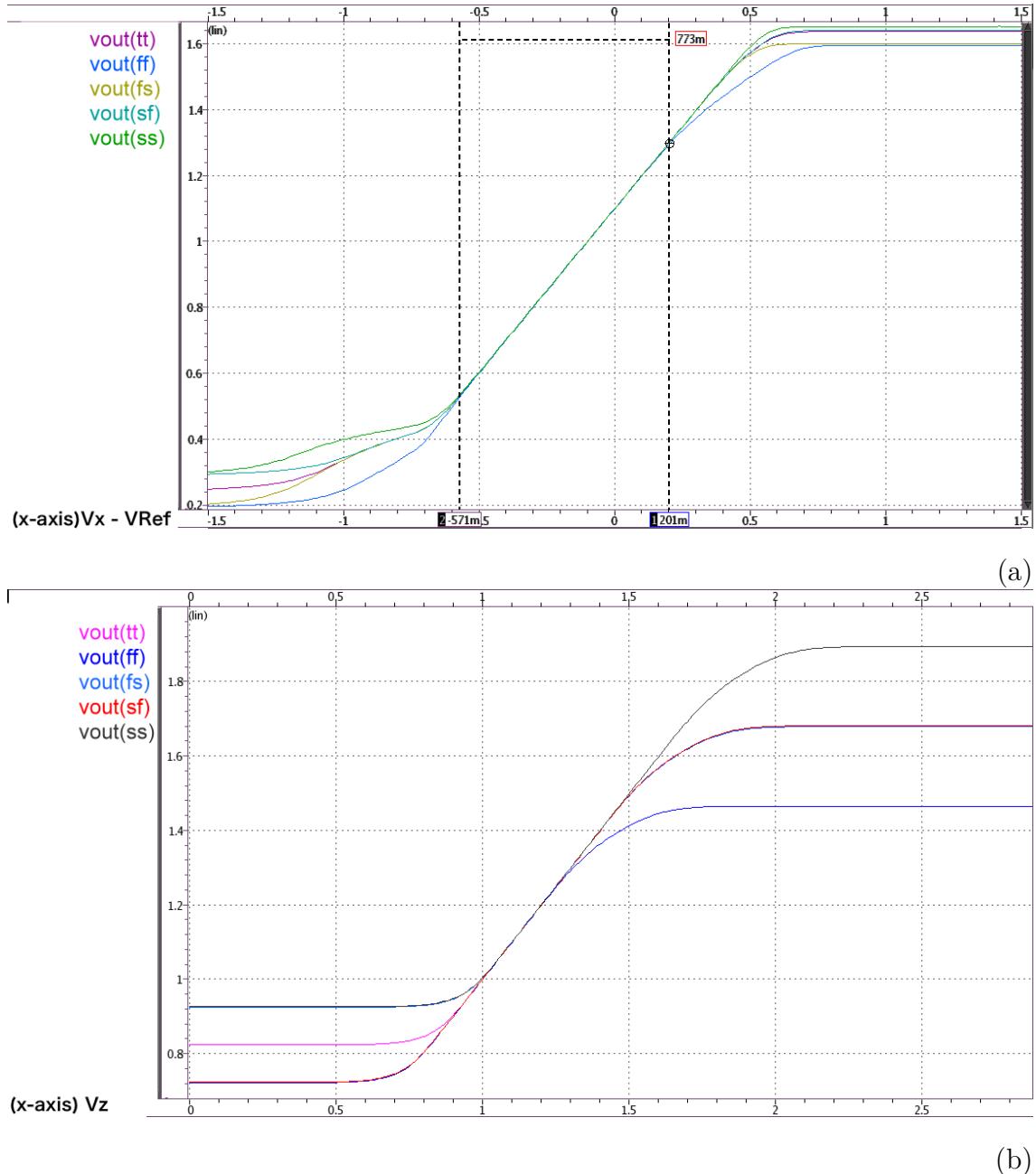


Figure 5.18: DC response of the output of our analog subtractor. (a)The x-axis is the difference between positive input and negative input ($V_x - V_{Ref}$). (b) The x-axis is the voltage of v_z

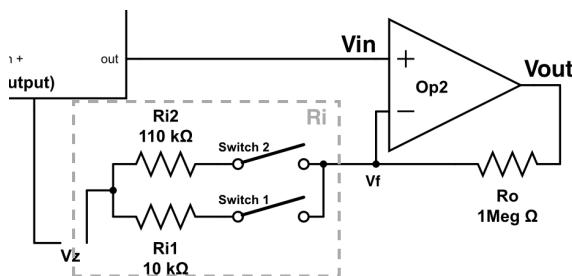


Figure 5.19: The non-inverting resistor-based amplifier circuit

	V_x	V_z
Input Dynamic Range	$V_{Ref} - 0.57V_{Ref} + 0.2$	1-1.38
Bandwidth	675k Hz	-
SNR (@10Hz)	8.3e10	8.4e10

Table 5.6: The summary table of the analog subtracter circuit.

5.2.2 Non-inverting Resistor-based Amplifier

Fig.5.19 is the last block of the second stage circuit. It is a non-inverting resistor-based Amplifier. We adopt this simple structure to amplify the output signal of the subtractor. When the subtractor sends a small signal Δv into V_{in} , the output voltage (v_{out}) is:

$$v_{out} = (\Delta v - v_f) \times A_{Op2} \quad (5.19)$$

$$v_f = v_{out} \frac{R_i}{R_o + R_i} \quad (5.20)$$

$$\frac{v_{out}}{\Delta v} = \frac{A_{Op2}}{1 + A_{Op2} \frac{R_i}{R_i + R_o}} \quad (5.21)$$

$$\approx \frac{R_i + R_o}{R_i} \quad \text{For } \frac{R_i A_{Op2}}{R_i + R_o} > 10 \quad (5.22)$$

The R_i can be $110k\Omega$ or $9.2k\Omega$ ($10k\Omega || 110k\Omega$). (When two switches is off, the circuit act like a unit-gain buffer.) Eq.5.22 suggests that the A_{Op2} should be larger than 1000 (60dB). Thus, the Op2 in Fig.5.19 adopts the structure of two-stage differential pair (same with the operational amplifier in TIA block) due to its high gain and wide output dynamic range (rail-to-rail).

One thing to note is that the derivation above views the V_z as the virtual ground. The V_z equals to the offset voltage of V_{in} . And it is the output offset voltage of the amplifier as well. In fact, this results in the input dynamic range of $\frac{\pm V_z}{AmplificationRate}$. (As long as the Op2 is a rail-to-rail operational amplifier). This emphasizes the importance of the subtractor block. If we directly connect the input of the amplifier to the fist stage output, the input dynamic range will be $\frac{\pm V_{Ref}}{AmplificationRate}$. The V_{Ref} is around $\pm 1V$ and is lower than V_z .

Fig.5.20 presents the five corners post-simulation results of the amplifier. We swept the input and measured the output under three amplification rate. And table.5.7 is

the summary table.

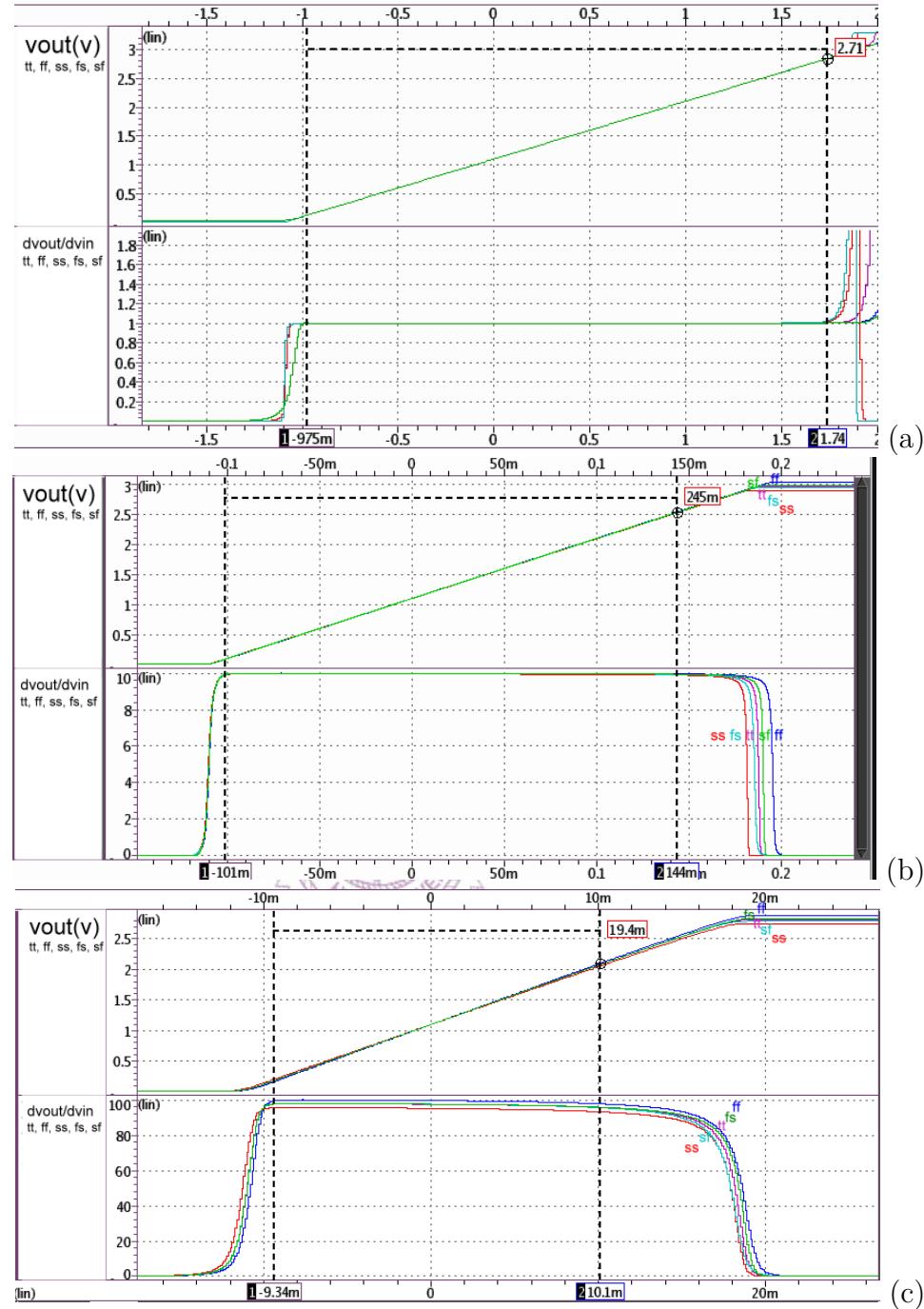


Figure 5.20: Five corners output DC response (v_{out}) and derivative ($dv_{out}/dvin$) when being operated under the amplification rate of (a)1, (b)10, (c)100.

Amplification Rate	100	10	1
Error	< 7%	< 0.7%	< 0.02%
Bandwidth	210k Hz	190k Hz	2M Hz
Input Dynamic Range	from $-9mV$ to $17mV$	from $-0.11V$ to $0.14V$	from -0.5 to $0.3V$
Output Dynamic Range	$0.1V - 3V$		

Table 5.7: The summary table of simulation results.

5.3 post-simulation Result of the Transient Measurement mode circuit

As mentioned in section 5.1.2, there are two usage of the Transient Measurement mode circuit (Fig.5.2). There simulation results are presented separately below.

5.3.1 Input from Gate

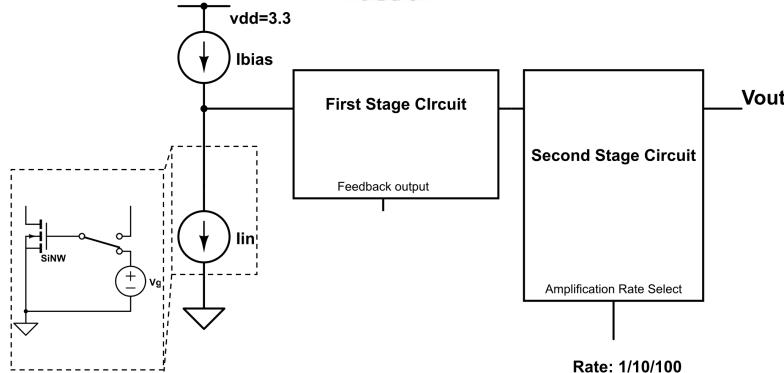


Figure 5.21: The block diagram of the Transient Measurement circuit. We simulate it by sending ac signal through the voltage source V_g .

The first usage is to detect the output response of input voltage signal at gate. The voltage signal is caused by the biomolecule concentration. This measurement are usually preceded by the DC Sweep mode, which initialize the I_D with the value of Ibias and set g_m to a corresponding value. Therefore, we replaced the transistor elements and V_g by a current signal I_{in} as in Fig.5.24. And we apply an ac signal from I_{in} to perform the ac analysis.

Fig.5.22 presents the maximum gain that the circuit in five corners provides. And Fig.5.23 is input referred noise analysis. The design spec requires the gain to be

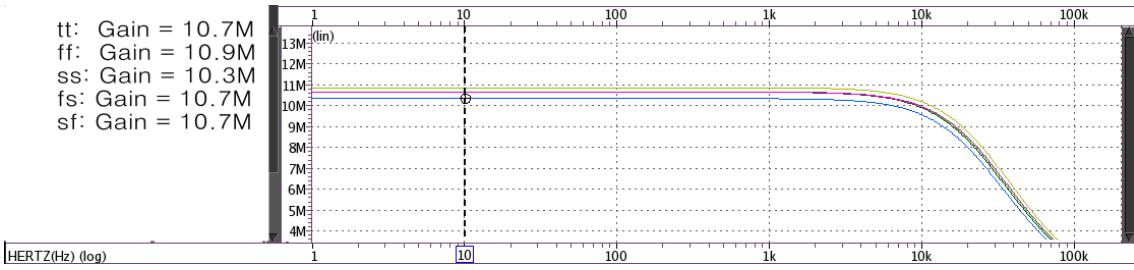


Figure 5.22: The gain of $\frac{V_{out}}{V_{in}}$ when the amplification rate of the second stage is 100.

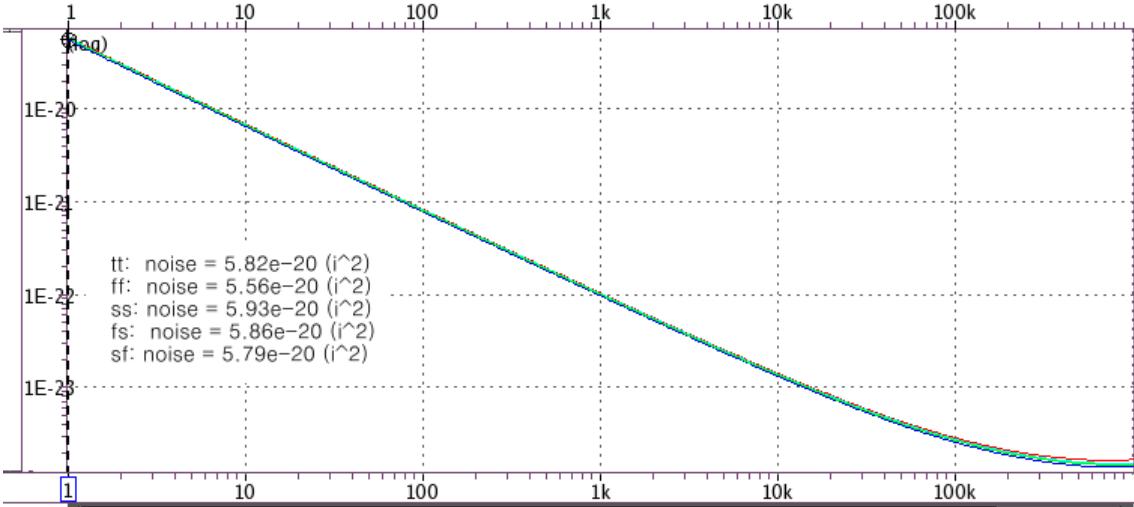


Figure 5.23: The input referred noise when the amplification rate of the second stage is 100.

greater than $5E6$ and the voltage noise referred to the gate of nanowire to be smaller than $2mV$. The summary table (Table.5.8) computed the noise result by considering the g_m as $200n$, which is the minimum g_m that may exist in our measurement.

	Design Spec (table.3.5)	Simulation Result
Amplification Rate (max)	$5E6$	$1.03E7$
Input Referred Noise	$< 2mV$	$= \frac{\sqrt{5.8E-20}}{200n} = 1.2mV @1Hz$

Table 5.8: The summary table. The simulation results are compared with the design spec.

5.3.2 Input from Source

The second usage of the Transient Measurement mode circuit is to apply a sine wave voltage signal at the source of nanowire. The V_g and I_{bias} are fixed at constant during the measurement. The output voltage is measured and used for computing

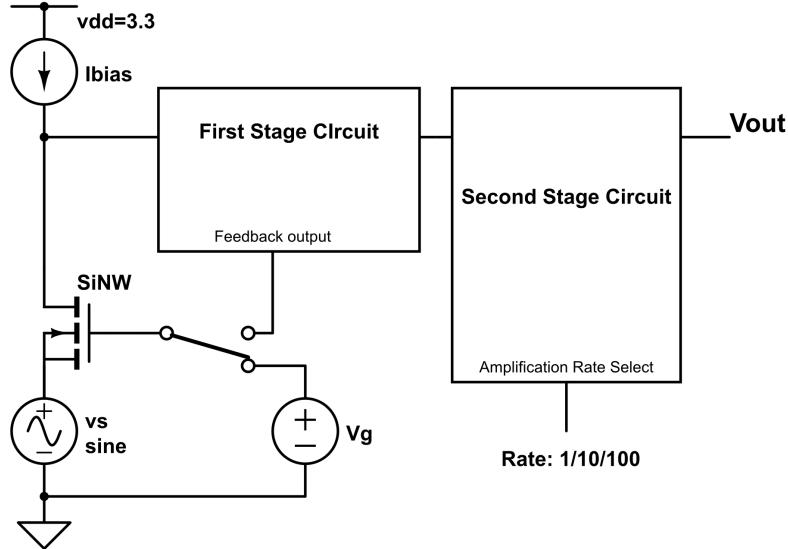


Figure 5.24: The block diagram of the Transient Measurement circuit. We simulate it by sending ac signal to the source of the nanowire.

the g_m of the element.

$$g_m = \frac{V_{out}}{v_s} \times R_{TIA} \times A_{second} \quad (5.23)$$

The v_s is the amplitude of the input sine wave. And the A_{second} is the amplification rate of the second stage circuit.

One thing to be noted is the offset voltage of the output. The biomolecule concentration difference changes the I_D of nanowire. This I_D difference not only results in the changes of g_m but also alter the offset current flowing through the R_{TIA} . This current is also amplified and may cause the output saturation. The solution is to utilize Ibias to cancel the offset current.

We can find the limit of the offset current. Since the output dynamic range of the resistor-based amplifier is from $0V$ to $3V$, the limit is $\pm \frac{1.5V}{A_{amp} \times R_{TIA}}$ where the A_{amp} is 1, 10 or 100.

Two simulation results presented below are the transient response of the output voltage when the A_{amp} is 10 (Fig.5.25) and 100(Fig.5.27). The g_m of the transistor is swept in the same time. The input sine wave has frequency of 1kHz and amplitude of $20mV$. Their corresponding ac sweep is presented in Fig.5.26 and Fig.5.28. This results show that the circuit bandwidth is about $10k$.

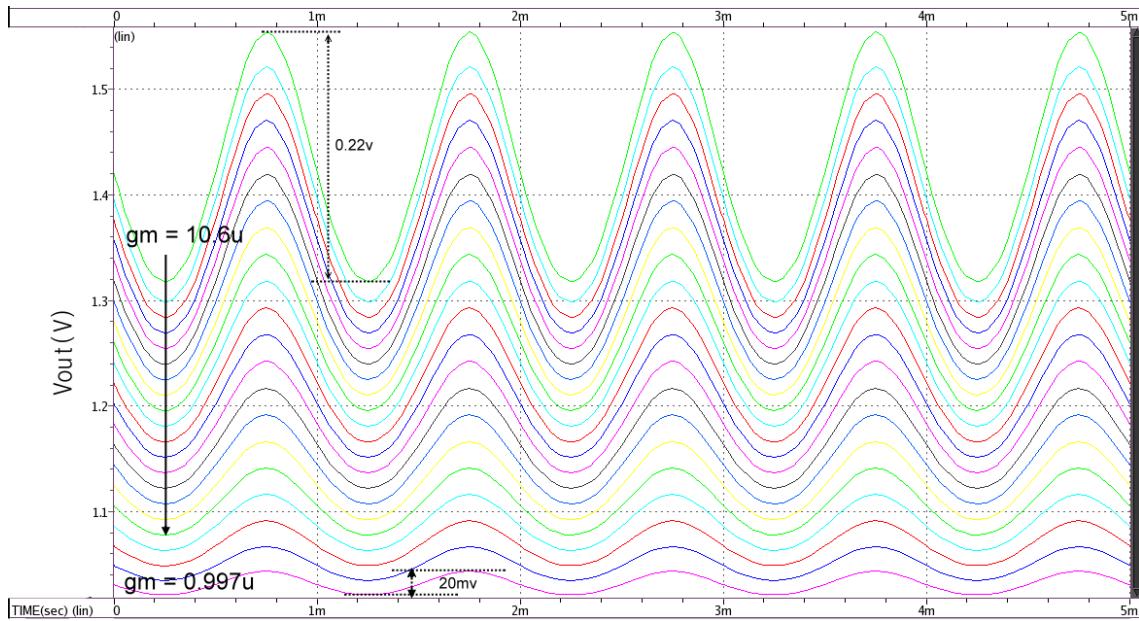


Figure 5.25: The transient analysis. The amplification rate of A_{amp} is 10. The g_m is swept from 1μ to 10μ .

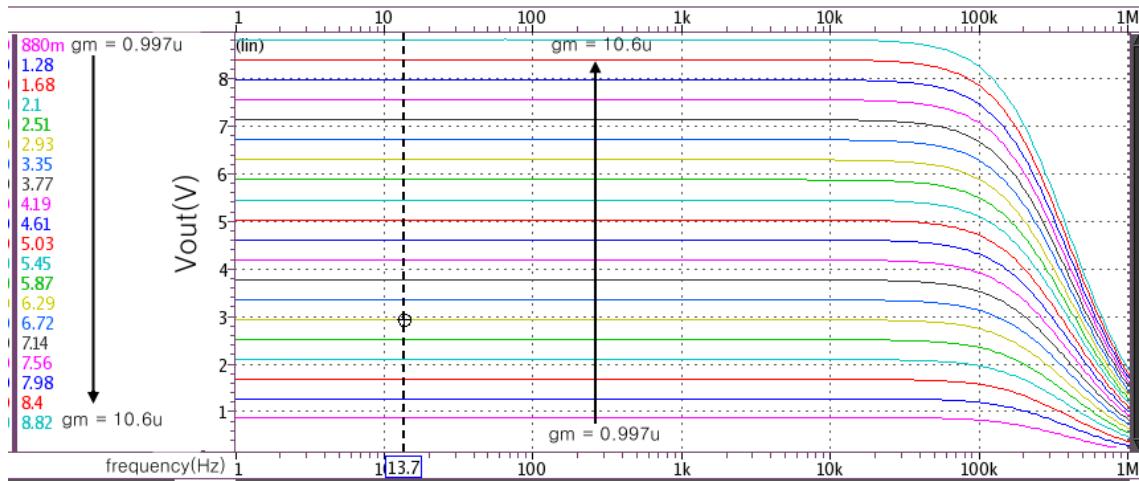


Figure 5.26: The ac analysis of the transient simulation result in Fig.5.25.

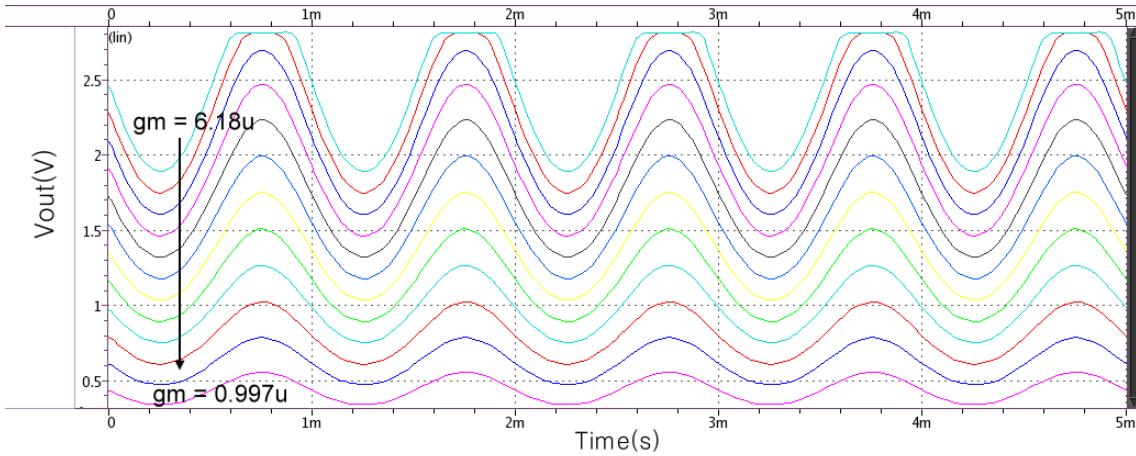


Figure 5.27: The transient analysis. The amplification rate of A_{amp} is 100. The g_m is swept from 1μ to 6μ . There are two curves have the output saturation problem. One solve it by increasing the current provided by Ibias.

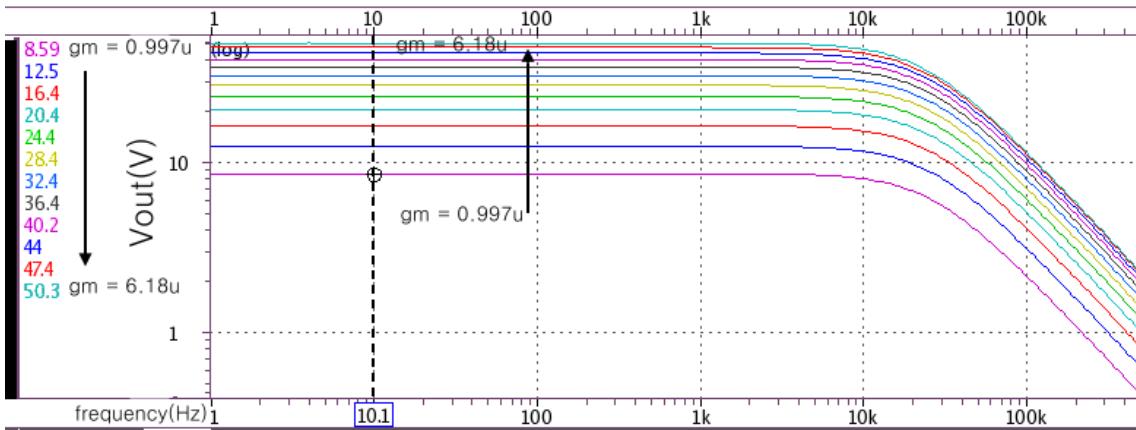


Figure 5.28: The ac analysis of the transient simulation result in Fig.5.27.

Chapter 6

Discussion and Conclusions



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