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An Integrated Circuit Design for Silicon-Nanowire

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Abstract



中 文 摘 要

關鍵詞：



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Abstract

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Chapter 1

Introduction

1.1 Motivation

Poly-silicon nanowire(SiNW) is an interesting and promising one-dimensional nano-structures. Many research of fabrication and electrical properties have been conducted [4]. It was first introduced to the biosensor field in 2001[3] and has become a promising candidate for various features such as high surface-to-volume ratio, ultra sensitivity, label-free electrical detection and real-time measurement.

Although there has been some great advances on nanowire structure design [6], the work of systems-level engineering is still insufficient. Systems designed for specific purpose can help the device to meet practical needs such as noise reduction, real-time measuring and conversion to digital output. Moreover, there are still several challenges that may be overcome through a better signal acquisition system [6].

One of the challenges is that the mass production of robust nanowire is still improbable. Element disparity may be a main reason among others. This problem also happens to the measurement of our own nanowire (Fig. 3.9). The nanowire we use is made by Professor Yang's team (National Chiao Tung University). And according to them, the nanowire use thick gate dielectric and have non-regular cross-sectional shape, which result in uncertainties of fabrication [8].

1.2 Introduction

In this project, we design a nanowire readout circuit with two modes that perform large signal (DC) and small signal (AC) measurement. In DC mode, one can use the circuit to perform a DC sweep of drain current (I_D) to show how the gate voltage (V_G) changes, or gives nanowire a constant I_D and measures the V_G response to different solution concentration. In AC mode, the circuit detects and amplifies the current variance of nanowire with constant bias voltages applied (V_D , V_G , V_S). We also combine two modes to implement a proposed method that may mitigate the disparity problem.

Dealing with the disparity problem

The proposed method base on two assumptions.

1. The nanowire transconductance ($g_m = \frac{\partial I_D}{\partial V_{GS}}$) is proportional to I_D .
2. The changing of the concentration of targeted biomolecule can be viewed as a voltage signal input to the gate end of a transistor.

The first assumption implies one can control the nanowire transconductance by the biasing I_D . The second assumption means that as long as different nanowire elements have a same transconductance, the output current induced by a concentration difference should be same. We testify these assumption in chapter 3.

The method works as follows: In the beginning of each measurement event, we set circuit under DC mode and perform a DC sweep. By handling the sweep results with numerical method, we keep all nanowire elements under a selected transconductance by controlling their I_D and corresponded V_G . This complete the initial stage. It then follows by the measurement stage where the AC mode is used, all elements should behave uniformly based on assumption 2. In the end of the stage, we return to DC mode to reset I_D of the elements. The circuit adjusts their V_G to do so. In the beginning of each measurement stage, an element always has a same I_D value and so does its g_m value according to the assumption 1.

Some minutiae is reviewed in chapter 5. Currently, most operations are manual.

We hope to make them automatic in the future, which may require digital circuit assistance.

1.3 Design Flow and Chapter Layout

There are six chapters in this thesis, which are sorted according to the design flow.

Chapter 2 are divided into two part. The first part is the literature review. ... The other is the analysis of measurement data from Yang's team. Most of those are the drain current of nanowire sweeping along the gate voltage (I_d - V_g curves). We present some of the raw data and the analysis results in this part.

Chapter 3 gives a brief description of nanowire structure. It is then followed by some analysis of data from biology experiment and electrical measurement. The biology experiment are done by Prof. Yang's team while electrical measurement are performed by ourselves.

Chapter 4 is an "accessory". We construct an discrete circuit which was designed for ion-sensitive field-effect transistor (ISFET) [10]. The purpose of this process is to practice the constant current method. The outcomes are deficient and it is its reference value which we spotlight.

Chapter 5

None

Figure 1.1: Design Flow

Chapter 2

Literature Review &

As previously mentioned in the introduction section, the read-out circuit we proposed has two operation mode (DC and AC). The DC mode control the drain current (I_D) of nanowire while the AC mode is for current variance measurement. Each of them references different sources.

2.1 DC Sweep and Source Follower

In this section, we review the knowledge and an article that is related to our design of large signal mode (DC).

2.1.1 I_D - V_G and Transconductance

A common method for examining nanowire electrical properties is to perform DC sweep. In [5], the team plot the I_D - V_G curves and study how the curve changes with the concentration of bio-molecules. In n-type transistor, the binding of negative charged bio-molecule induce surface-near silicon ions discharged and thus lower the threshold voltage. We may think of this as an additional voltage applied onto the gate:

$$\text{strong inversion: } I_D = KP(V_G - (V_{th} - v_g))^2 \quad (2.1)$$

$$\text{weak inversion: } I_D = I_0 e^{\kappa(V_{GS} - (V_{th} - \Delta v_g))/\phi_t} \quad (2.2)$$

2.1.2 Source Follower

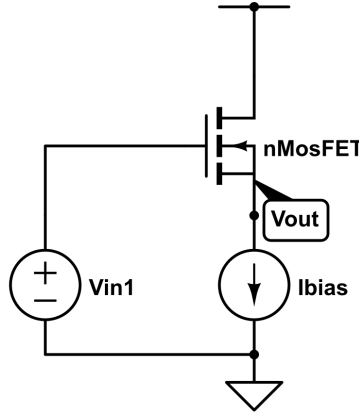


Figure 2.1: Source Follower

As one of the basic single stage amplifier, source follower (common drain) are employed to transfer voltage signal from gate to source while keeping drain current constant. The transfer function can be derived as:

$$\frac{V_{out}}{V_{in}} = \frac{r_{ds}g_m}{1 + r_{ds}g_m} \quad (2.3)$$

$$\approx 1 \quad \text{for} \quad r_{ds}g_m \gg 1 \quad (2.4)$$

g_m is the transconductance ($\frac{\partial I_d}{\partial V_{gs}}$) and r_{ds} is the drain-to-source resistance. Although we haven't seen it is applied to nanowire, there have been several applications in the read-out circuits of ISFET (Ion-sensitive Field-effect Transistor)[10, 12] for a long time.

In [10], ISFET is applied as a biological transducer that convert detected bio-signal into it's input signal on the gate-end, which is resemble to our biosensor of nanowire. An read-out circuit of source follower is served as the analog front-end. The bio-signal induced voltage difference at the ISFET gate-end are converted to the source-end. There is no need for an extra current-to-voltage converter which may import more signal fluctuation such as shot noise or flicker noise. But on the other hand, the circuit requires a biasing current source. This current source may have to be stable, noiseless or wide-range on demand. And since the current value are usually under micro-scale even nano-scale, it is impractical to merely use external current source. The article use two resistors and an op-amp to design a current scale

down circuit. Bias current decreases in proportional to the resistance ratio (N) of one resistor to another. Moreover, by keeping V_{ds} at a constant value (0.5v), the circuit also removes the channel affect which is a factor that may effect linearity of the results. It is showed in the schematic below that two op-amp based unit gain buffer are added to force the voltage at drain-end follows the source-end.

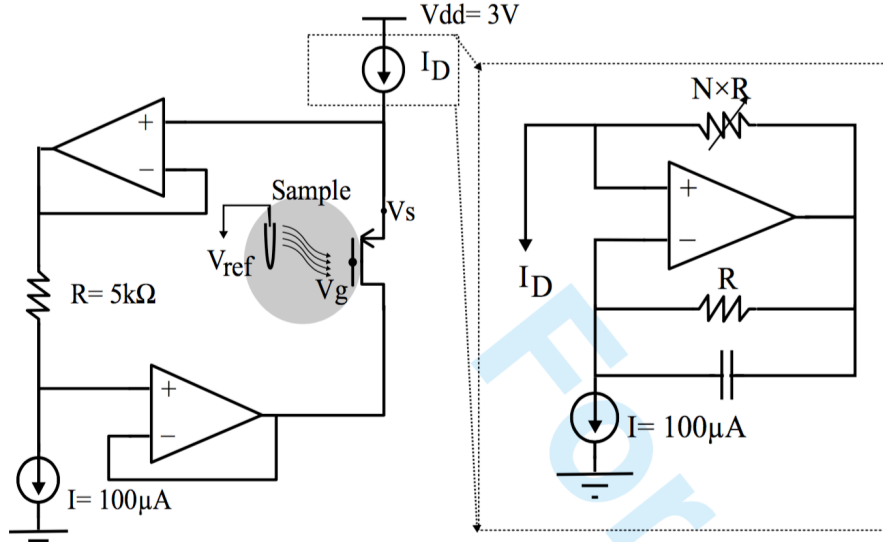


Figure 2.2: ISFET readout circuit in [10]

An issue need to be noticed is the impedance matching between the element and the current source circuit. It is known that the output impedance of current source should be much larger than the input impedance of the biased element. The equation for the output impedance of source follower is:

$$\frac{r_{ds}}{1 + g_m r_{ds}} \quad (2.5)$$

This equation can be simplified as:

$$\frac{1}{g_m} \quad \text{for} \quad g_m r_{ds} \gg 1 \quad (2.6)$$

We also compute the output impedance of the current source circuit:

$$N \times R_i \quad (2.7)$$

R_i is the impedance of the right-bottom current source in Fig.2.2. In the integrated circuit, R_i is not ideal but usually close to the r_{ds} of a single MOSFET.

As mentioned, Eq.2.7 should be far larger than Eq.2.6. However, g_m is proportional to the I_d , which means Eq.2.6 is inversely proportional to N . When the bias current decreases, the output impedance decreases while the input impedance at the ISFET source-end increases. This creates a lower boundary of the bias current.

The source follower structure provides a direct signal transition method. It is a good candidate for the read-out circuit with the aim of detecting transconductance or threshold voltage variance. Nevertheless, post-processing such as amplification and filtering are necessary. The experiment results in the article are untreated. Some strong signal attenuation exist, which are mainly caused by low-frequency noise and ISFET drift [9]. The drift problem are dealt with through some signal processing techniques while noise problems are left untreated.

We constructed this circuit with discrete elements and applied it to our nanowire. The results are presented in chapter 4.

2.2 Small Signal (AC) Measurement Method Review

In previous section, the source follower we mentioned exhibited compelling advantages as a signal processing structure of nano-device. However, the structure overcomes obstacles when being applied to the small signal detection. Parasitic capacitors and resistors can severely influence the results.

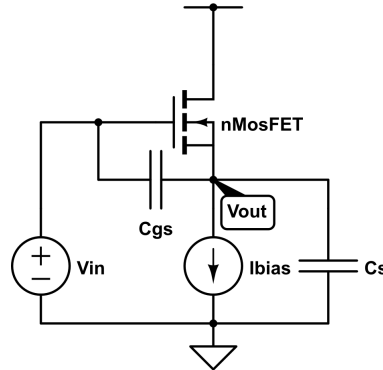


Figure 2.3: Source Follower with parasitic capacitance

As in figure 2.3 where the parasitic elements are included, we modified the transfer

function Eq.2.4

$$\frac{V_{out}}{V_{in}} = \frac{r_{ds}(sC_{gs} + gm)}{1 + r_{ds}(gm + s(C_{gs} + C_s))} \quad (2.8)$$

The equation can be similar to Eq.2.4 which roughly equals to 1 as long as C_s is far more smaller than C_{gs} . Unfortunately, C_s can be large since the output end of source follower usually connects to the next stage input or a pad. In that case, the parasitic capacitors may attenuate the signal.

We want to build another circuit structure that can not only performs ac signal measurement but also immunes from parasitic capacitance affect. This is achieved by reviewing those works that try to measure the parasitic capacitance first. Below, the works from two teams aims to measure drain-to-source resistance (R_{NW}) and drain-to-source capacitance (C_{NW}). Base on the reviews, we adopted and modified the method from one of it (2.2.2). This will be described briefly in section 2.2.3 and thoroughly in chapter 5.

2.2.1 RC Time Delay Measuring

The measurement system for ZnO-nanowire based sensor array from [1] applies the Time-over-Threshold techniques to its read-out circuit (Fig.2.4). The circuit alternatively charges an on-chip capacitor (C_{int}) with a constant current and discharges it through the nano-material resistance (nanowire). An inverter with its output switches from on to off when the capacitor is charged to its input threshold voltage, and vice versa. This behavior convert information of nanowire such as capacitance and resistance into time information. Both C_{int} and C_{NW} effect charging time and together with the R_{NW} effect the discharging time.

The work presented in [1] doesn't have enough explanation about how do they interpret the capacitance and resistance information. It simply mentioned that a microcontroller is responsible for these calculation. Besides, the work lacks simulation and experiment of using complex elements as measure target. Most of the results are measurement of using concrete resistor as the substitute for nanowire and regard the C_{NW} as 0p. The only nanowire experiment given at last doesn't has good performance. It seems that the design may only be applied to a complete-resistor

or complete-capacitor element.

The recent publications [2] by the team is more elaborate and have measurement of complex element (An element composed of both resistor and capacitor). In Fig.2.5, nanowire append between point A and B. The charging current is able to be applied from Mp1 or Mp2, which is determined by the “sel” signal with the aid from the MUXs. This is simply mean to perform a reverse measurement and we ignore it by assume $sel = 1$ and point B is virtually ground. Now, we can see that the circuit design concept is actually same. The current charge both C_{int} and C_{NW} . When the voltage at A exceed the threshold voltage, the output switches to off and feedback to turn off the Mp1. (To be noted that the inverter at the output satge in [1] is replaced by a schmitt trigger.) Then the capacitor discharges through nanowire (r_{ds}). The right-bottom plot in Fig.2.5 defines T_0 as the charging time and T_1 as the discharging time. The derivation of the R_{NW} and C_{NW} in the work can be simplified as:

$$C_{NW} = T_0 - C_{base} \quad (2.9)$$

$$R_{NW} = \frac{T_1 R_{par}}{(C_{NW} + C_{base}) R_{par} - T_1} \quad (2.10)$$

$$\text{where } R_{NW}||R_{par} = \frac{T_1}{C_{NW} + C_{base}} \quad (2.11)$$

C_{base} are the C_{int} plus parasitic capacitance and R_{par} the parasitic resistance. These parasitic elements comes from the transistor in the integrated circuit block such as MUX and Mp. It must be noted that owing to simplicity, we doesn't concern the hysteresis of the schmitt trigger here.

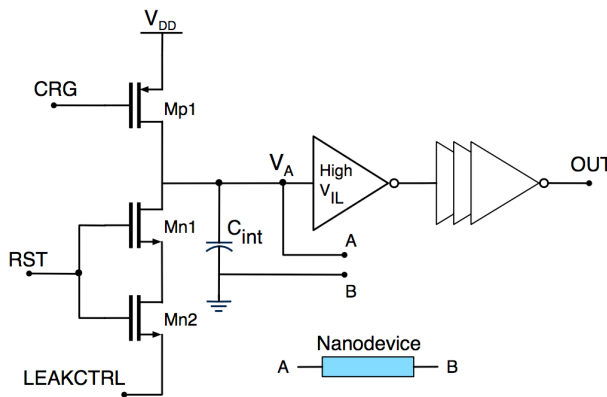


Figure 2.4: (a) Schematic of [1]

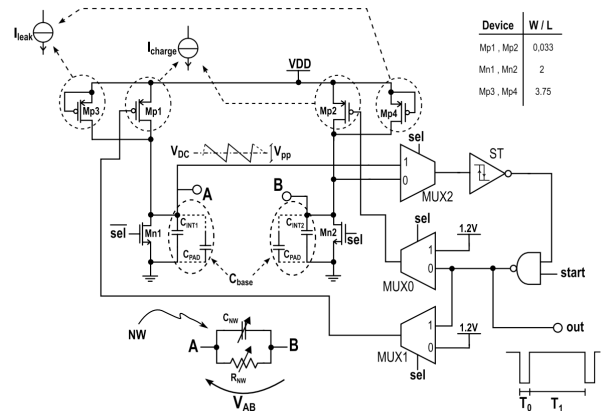


Figure 2.5: (b) Schematic of [2]

None

Figure 2.6: Draw mos with $(C_{gd} + C_d)$ and r_{ds} is modeled by R_{nw} and C_{nw}

2.2.2 Complex Impedance Solving

The nanowire-based hydrogen sensor measurement system from [13] adopt another method. It use a lock-in amplifier to realize both resistive and capacitive impedance measurement.

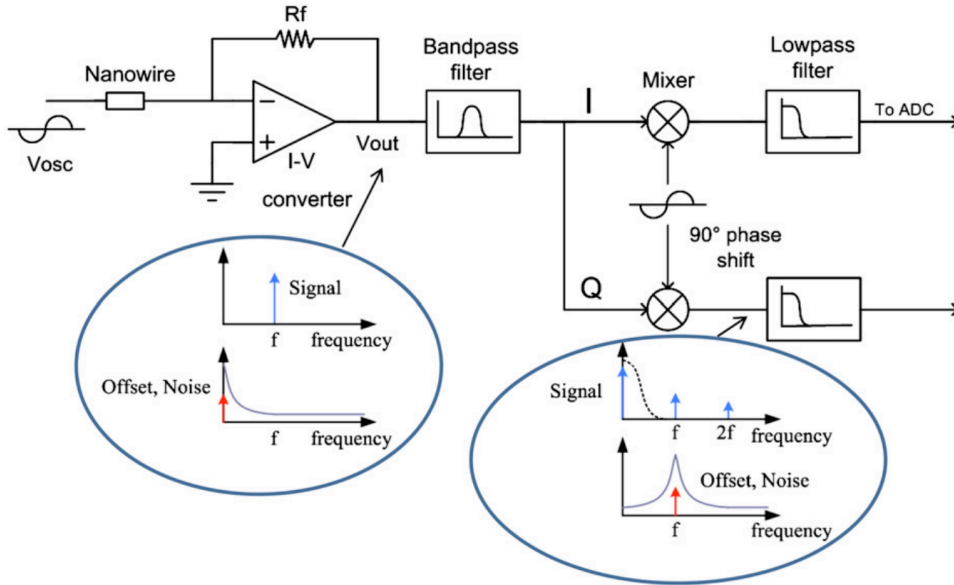


Figure 2.7: (b) Block diagram of the lock-in amplifier in [13]

The system started by supplying nanowire with a sinusoidal voltage signal to one end while the other end is grounded virtually by a transimpedance amplifier (TIA). The TIA then converts the output current of nanowire into voltage signal which contains complex impedance information. The resistance is in the real part while the capacitance is in the virtual part

$$V_{out} = I_{NW} R_{TIA} \quad (2.12)$$

$$I_{NW} = V_{in} \left(\frac{1}{R_{NW}} + j2\pi f C_{NW} \right) \quad (2.13)$$

f is the frequency of input signal.

After remove high-order harmonic interferences by a controllable bandpass filter, the signal is demodulated. The resistive and capacitive impedance values are resolved through channel I and Q with phase different by 90 degree. The mixer is a linear multiplier that use for demodulation. With a radio frequency (RF) input and the input local oscillator (LO) input, it produce an output signal that consists of signals with frequencies $f_{RF} + f_{LO}$ and $f_{RF} - f_{LO}$. Incidentally, the signal are immune from the perturbation of low frequency noise which is a common problem for biosensor.

2.2.3 Comparison and Conclusion

We compare method 1 (Sec.2.2.1) and method 2 (Sec.2.2.2) here. Both of them focus on detecting the R_{NW} difference. According to the comparison table below (2.2.3), we can see the resistor measurement range of method 1 is different from 2 by a large extent. This may because the minimum bias current of nanowire provided by the circuits are different. The minimum current in method 1 is limited by the pmos(I charge) and the leakage current. In method 2, it is limited by the TIA. Since our method adopt this TIA block, we will discuss this problem in chapter 5.

As for the C_{NW} detection, the measure range is much worse. Reason

Method 2 perform well when it comes to noise suppression. In fact, the circuit in method 1 doesn't provide noise reduction ability. The special structure it use (The article [1] mentioned it as M4N approach) is the one responsible for that.

Method 1 has a lower power consumption. However, it is under estimated since the microcontroller power is not included.

In our project, capacitance measurement is not our object. But we will still need to consider the parasitic capacitor effect in our circuit design. Method 1 convert the resistance information into time (frequency) information. If one want to avoid the affect from parasitic capacitor, he should apply a C_{int} that is much larger than C_{NW} . However, it is not practical in integrated design because the chip size is limited.

Method 2 uses a TIA to measure resistance and capacitance together first and then resolve the complex value. We notice that the capacitance value is much larger

	[2]	[13]
R meas range	1M - 1G	10 - 40k
R meas error	< 2.5%	< 2%
C meas range	100fF - 1uF	0.5 - 1.8nF
C meas error	< 3%	< 3%
SNR	> 45dB	-
Input refered noise	-	190 nV/sqrt(Hz) @ 5 kHz
CMOS Technology	0.13um	0.18um
Power consumption	14.82uW	2mW

Table 2.1: Specification Summary

than the resistance value. This difference may be revised downward in our silicon nanowire case. The resistance can be more than 100M. However, since C_{NW} is parallel to R_{NW} , we wonder the C value can be ignored. Besides, our circuit measure the g_m instead of R_{NW} . The value can be smaller than R_{NW} . In fact, we can even control the I_d of nanowire to lower the g_m further.

Another reason that make method 2 more attractive is because the method is more flexible. One can simply add other analog blocks such as noise filter or amplifier to it.

Overall, method 1 has advantage in detecting range and accuracy while method 2 has better noise suppression and flexibility.

Chapter 3

Nanowire Structure and Measurement

In this chapter, we present the experiment data and some analysis which are the foundation of our circuit design. The first section gives a brief description of the our silicon nanowire element. The second section provides the data of the biology experiments. These data are use for ensure that the SNR of nanowire is lower enough. The last section presents the data of the electrical measurement. Our circuit design spec are base on the analysis from this section.

3.1 Brief Description of Nanowire Structure

The nanowire we use is made by Prof.Yang's team (National Chiao Tong University)[7]. A sectional view of the nanowire structure is given below. The fabrication process is based on the poly-silicon sidewall spacer technique. The n-Type doped poly-SiNW FET has 2 to 10 poly-silicon channels. Each channel is 80nm in width and 2 μ m in length. Large portion of the channel surface is exposed to environment. The exposed region, through several post-process, capture the DNA probe and serve as the sensing site for DNA molecules.[7, 8]

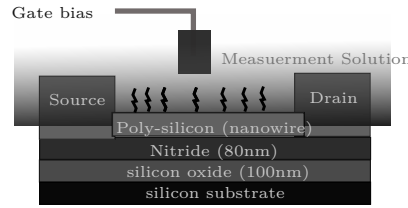
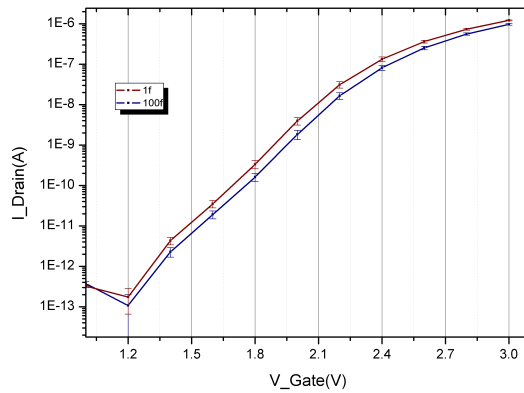


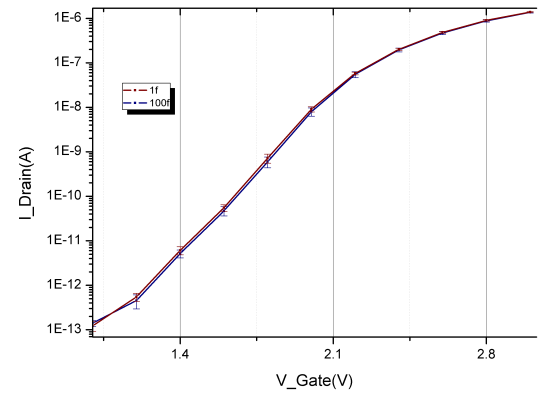
Figure 3.1: Nanowire Structure

3.2 Biology Experiment

The biology experiment data are provided by Prof. Yang's team. These data are the Id-Vg measurement of the same biomolecule placed under different circumstances or with different nanowire elements. With each measurement repeated three times, we find the mean and standard deviation (SD) of them and consider the SD value as the intrinsic noise of nanowire. We want to ensure that such noise should not be greater than the signal. To be more specific, we examine whether the Id-Vg curves of different concentration overlap with each other or not. We present an example below:



(a)



(b)

Figure 3.2:

The Fig.3.2 are concentration-dependent measurements (1 femto mole(fM) and 100fM biomolecule solution) obtained with two elements ((a) and (b)). The two curves in the (a) are distinguishable from the other after gate voltage of 1.4v. They are not distinguishable in the (b) since they overlap each other. We thus assert that the element of (b) can't detect the concentration difference between 1fM and 100fM.

The noise is stronger than the signal (The signal means the I_D difference caused by the concentration difference). The element of (a) is able to do so if it is biased at gate voltage larger than 1.4v or drain current larger than 1E-11.

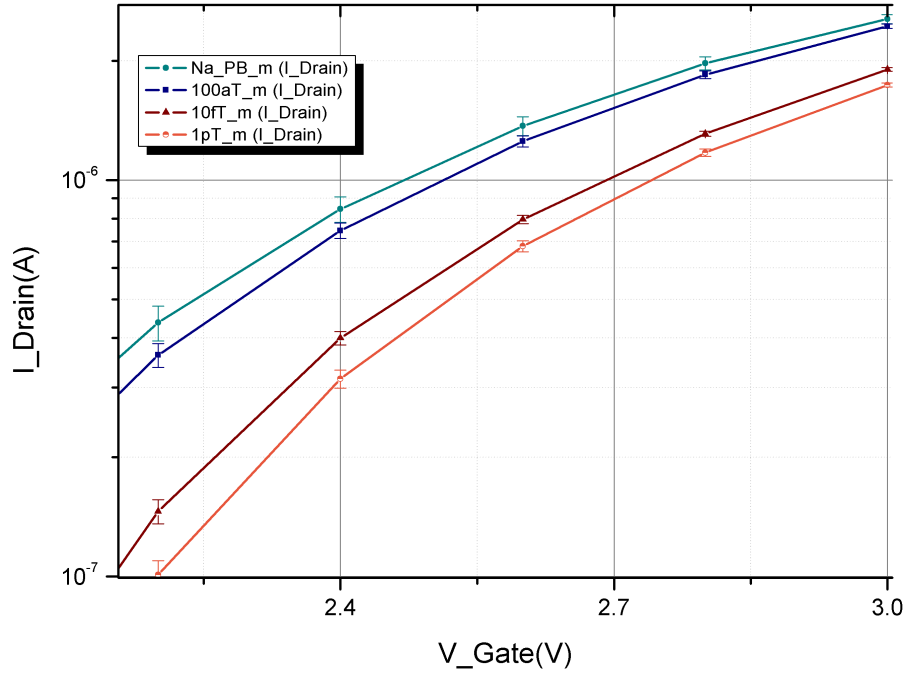


Figure 3.3:

In Fig.3.3, the I_D increase with the biomolecule concentration. One can find that there are only few “space” between PBS buffer and solution containing biomolecule with concentration of 100aM. Hence the 100aM should be the limit of detection.

It is worth noting that there are more space between 100aM and 10fM than the space between 10fM and 1 pico mole(pM). We calculate the noise rate: $SD/Mean$ which seems independent of concentration (Fig.3.4). These implies that the “resolution” for detecting concentration ranging from 100aM to 10fM may be better than the that ranging from 10fM to 1pM.

Appropriate Bias Gate Voltage

In [8], the team found that “the induced change of current (I_D) following biomolecule was dependent on the applied gate voltage (VG)”. The team tried to find a bias

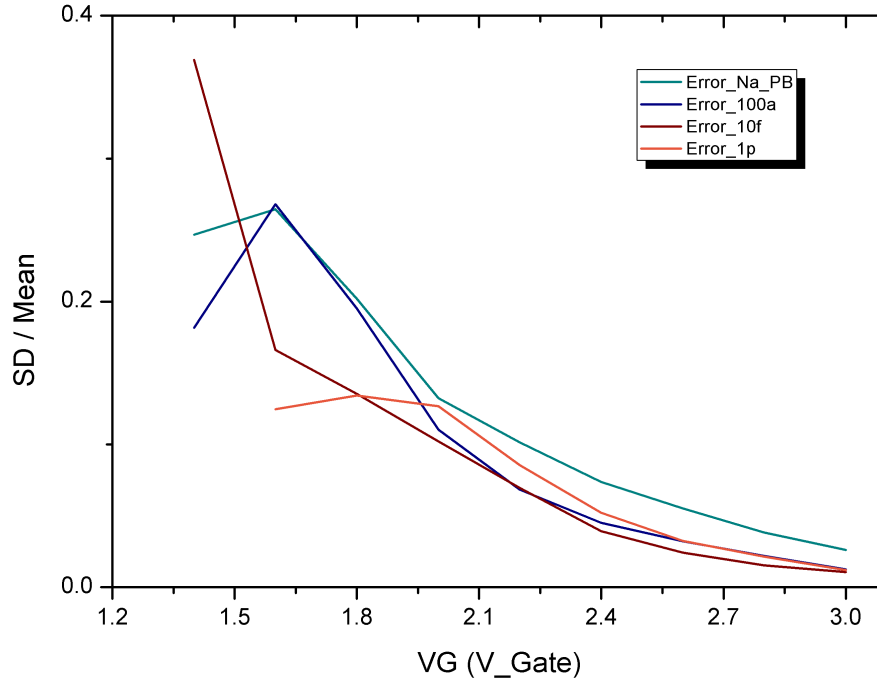


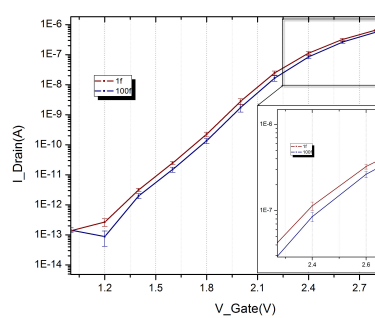
Figure 3.4:

gate voltage range which can induce more current response. By taking noise into consideration, we proposed that one should choose the region with more “noise tolerance”. We define the noise tolerance as below:

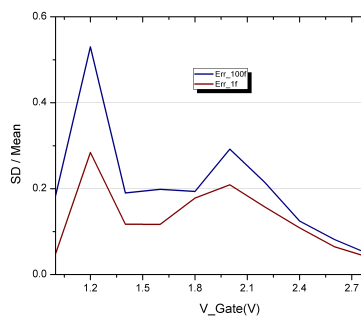
$$\text{noise tolerance} = \frac{I_{D1} - SD1 - (I_{D2} + SD2)}{I_{D2}} \quad (3.1)$$

I_D and SD are the mean and standard deviation of a curve. The larger the noise tolerance implies there are more space between two curves.

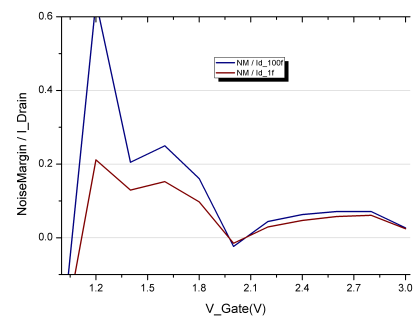
The Fig.3.5(c), (f), (i) are the noise tolerance of Fig.3.5(a), (d), (g). The Fig.3.5(b), (e), (h) are the noise rate respectively. We observe a rising trend in both noise rate and noise tolerance as gate voltage decrease. Moreover, a small peak appears in (c) and (f) located around the section where transistor switches from weak inversion region to strong inversion region. We therefore suggest that this section should be the best region under which nanowire should be operated.



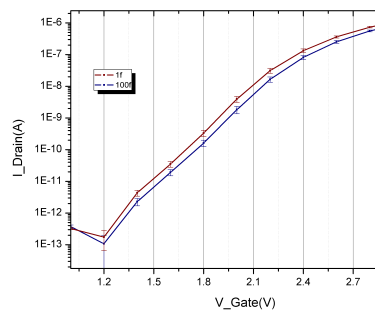
(a)



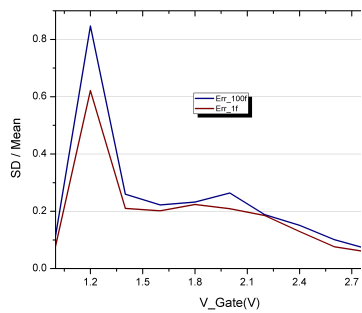
(b)



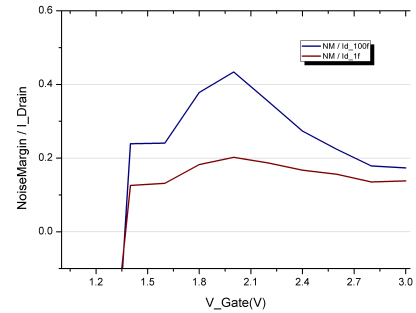
(c)



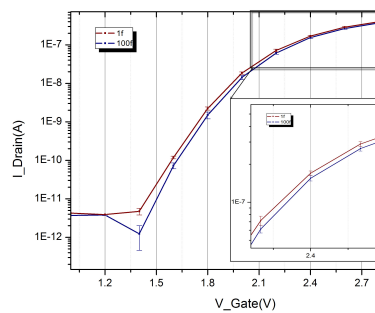
(d)



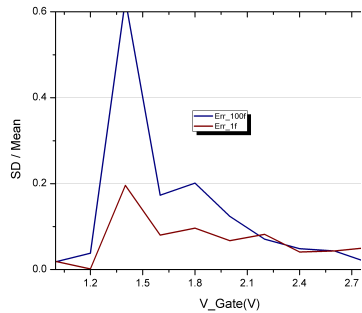
(e)



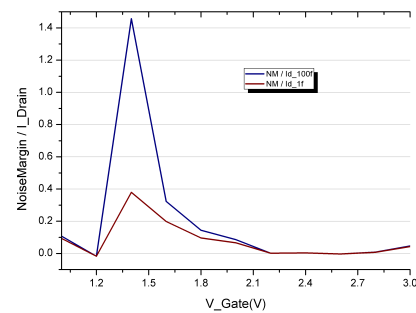
(f)



(g)



(h)



(i)

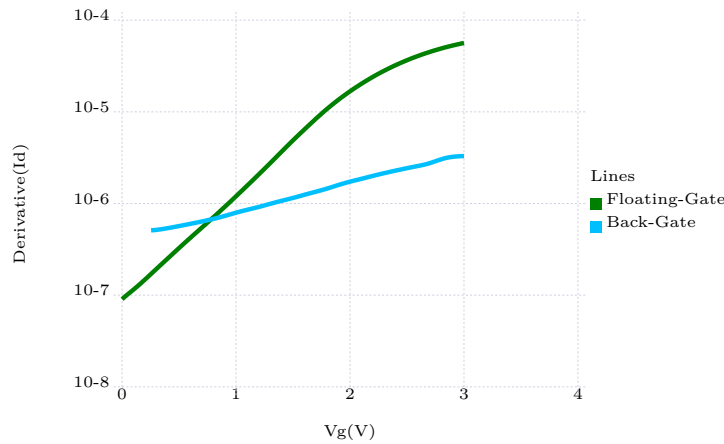
Figure 3.5:

3.3 Electrical Measurements

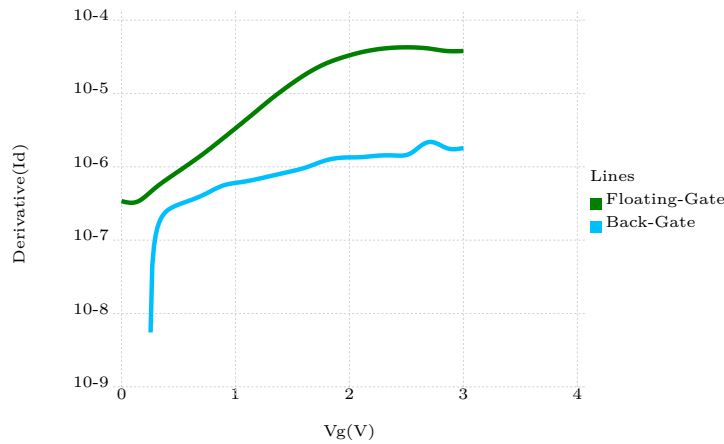
This section presents the results.

Front Gate and Back Gate

Two gates are available: floating gate (liquid gate) and back-gate. We choose floating gate as the operation gate in spite of some advantages that back-gate has. One of them is the ability to lower the $1/f$ noise [14, 11]. However, this only happens in a very high gate voltage, which is not practical in the integrated circuit design. Moreover, the floating gate induces larger drain-current. In other words, it has higher transconductance. And a high transconductance leads to a stronger feedback ability in our design.



(a)



(b)

Figure 3.6:

3.3.1 Parameters

The most crucial parameter for our circuit design is the transconductance (gm). The gm is acquired by finding the relation between drain-to-source current (I_d) and gate-source voltage (V_g), and perform differentiation: $\frac{\partial I_d}{\partial V_g}$. use standard PBS as

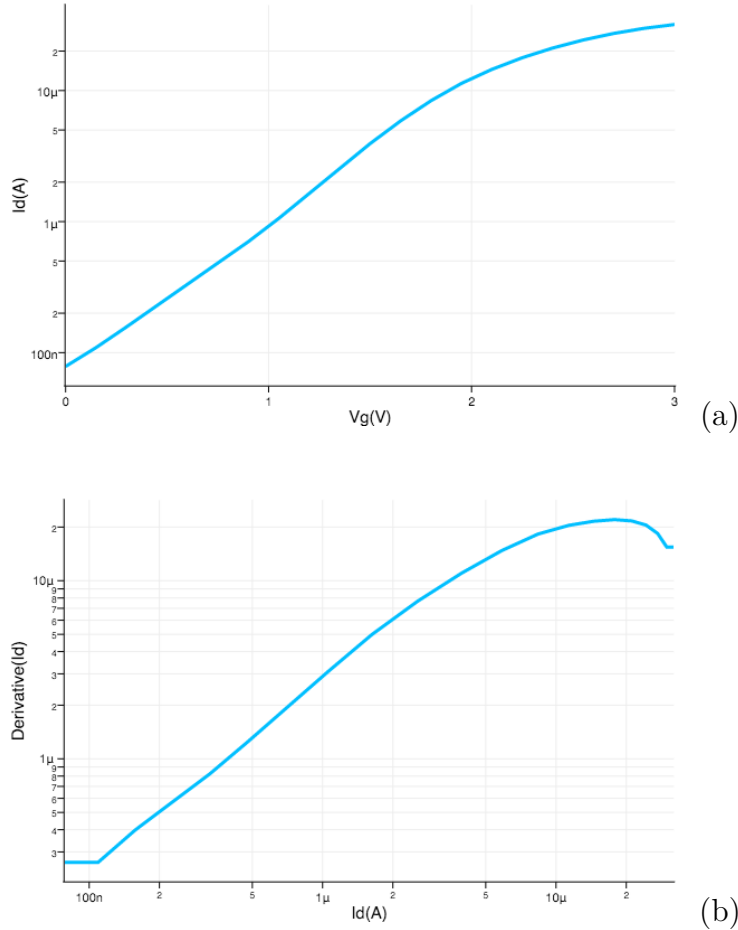
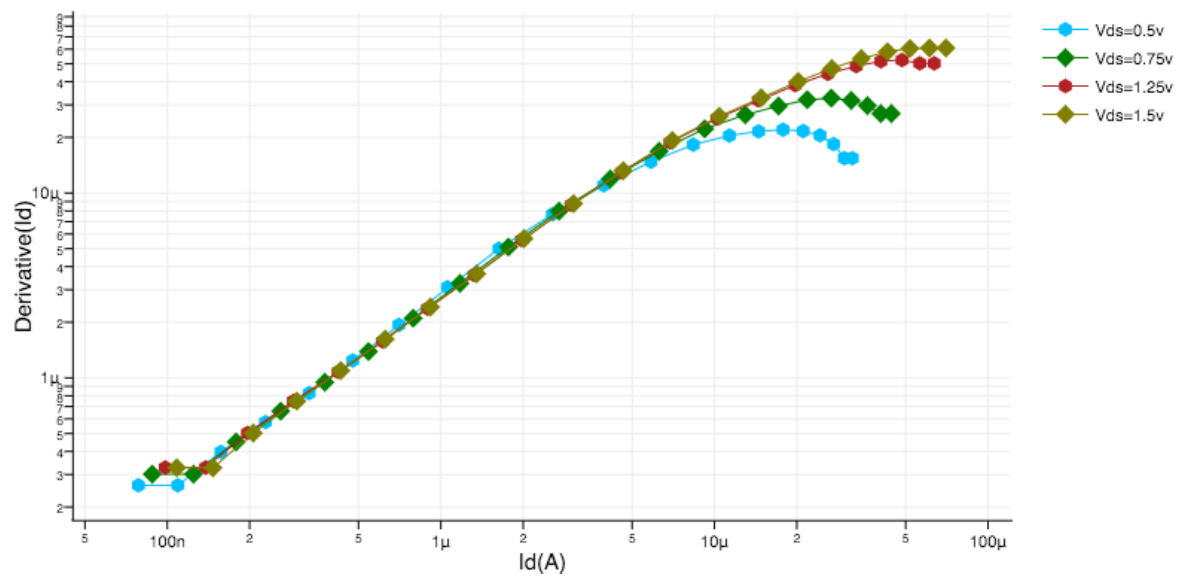


Figure 3.7:

The I_d -Derivative figures indicates there is a “linear region” where gm is proportional to I_d . This property implies the transconductance can be controlled in simple way. As mentioned in introduction, we may find specific bias I_d for distinct elements and adjust their transconductance to a same value.

We also prove that the transconductance under this region is unaffected by the drain-source voltage variance.

By measuring two nanowire element which lie on the same wafer and are immersed

Figure 3.8: Id-transconductance with V_{ds} variance

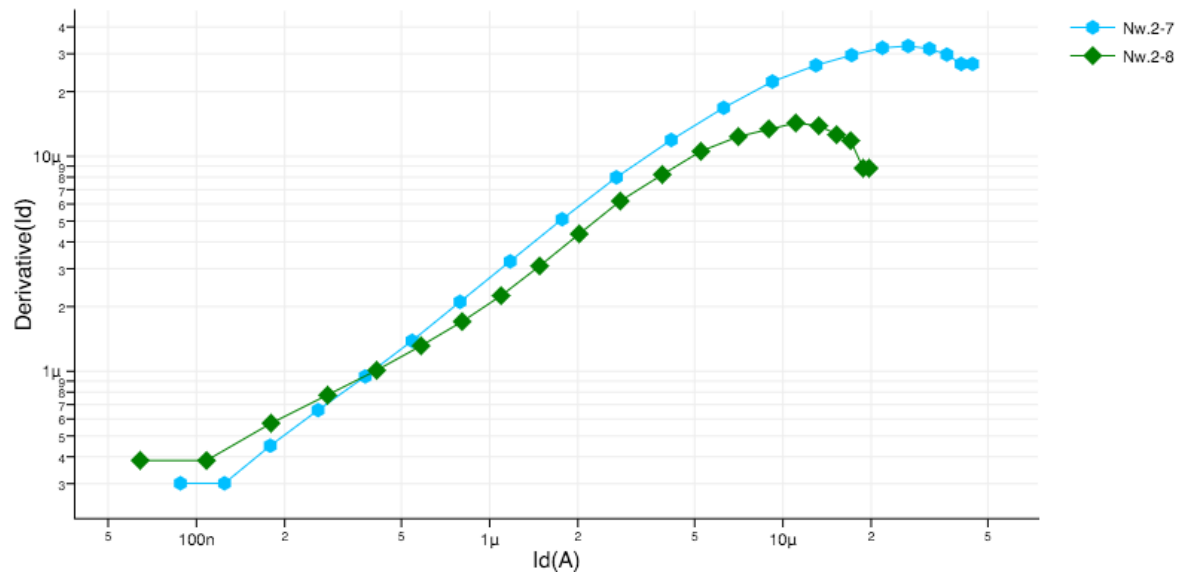


Figure 3.9: Distinct element with a line indicate they have same transconductance

with the same testing PBS solution



Chapter 4

Discrete Circuitry Design



Chapter 5

Integrated Circuitry Design

5.1 Signal Acquisition Method



Chapter 6

Discussion and Conclusions



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