國立清華大學

碩士論文

積體化電路設計之矽基體奈米線

An Integrated Circuit Design

for Silicon-Nanowire

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Abstract

Poly-silicon nanowire (SiNW) is a well-studied and interesting one-dimensional nanostructure. Since it was introduced to the biosensor field in 2001, it has become a promising candidate for ultra-sensitive, real-time and label-free sensor device. Nevertheless, many physical and chemical challenges constrain nanowire from being robust and practical. Nowadays, many studies adopt the integrated-circuit techniques to solve the problems. Circuits with different design concepts and purposes are proposed to meet practical needs.

In this thesis, based on the nanowire designed by Prof.Yang (National Chiao Tong University), we design our own read-out circuit. This research first analyzes biological experiments results (From Prof.Yang) and the electrical characteristics of the nanowires. The circuit specification and design is then based on these data analysis.

The circuit is capable of performing both DC-sweep (I_D-V_G sweep) and transient measurement. Moreover, we proposed a measurement method a combining of these two functions. We believe this method mitigates the device variability induced by the fabrication process. Currently, most operations in this method are manual. We hope to make them automatic in the future by inducing digital circuits and constructing a system-level structure.

中　　文　　摘　　要

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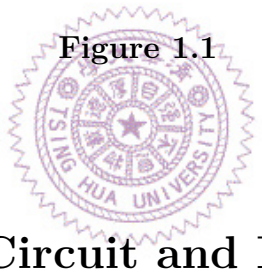
List of Figures

Chapter 1

Circuit Results Discussion and Summary

This chapter presents the results of our read-out circuit and the summary of this thesis. The layout of the circuit is given in 1.1

Figure 1.1



1.1 The Fronted Circuit and DC-sweep mode

As in Fig.1.2(a), the fronted circuit includes a biasing current source (Ibias), transimpedance amplifier (TIA) and an operational amplifier (OP). These three circuit blocks combined with the nanowire device (SiNW) form a feedback structure, which is the DC-sweep mode of our circuit.

1.1.1 Ibias

The Fig.1.3 is the schematic of the Ibias. By changing the resistance of the external Res and measuring the current, we obtained the result shown in Fig.**??**.

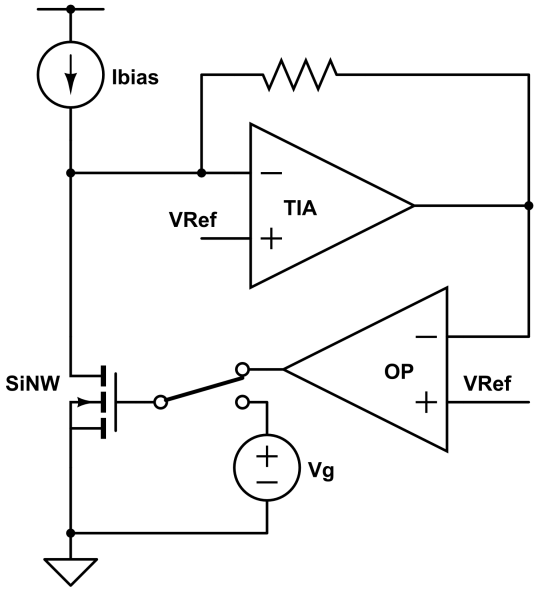


Figure 1.2: The fronted circuit

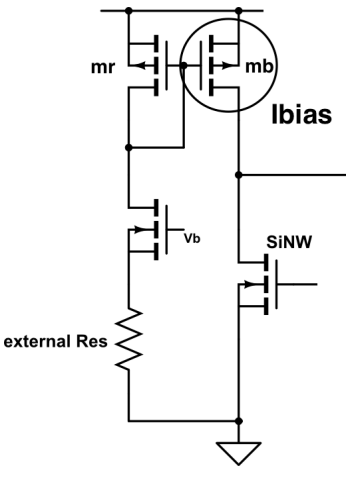


Figure 1.3: The fronted circuit

1.1.2 Ibias

1.1.3 TIA

The Fig.1.4(a) and (c) shows that the input current range of TIA is$+5.3\mu A \sim -15\mu A$. The Fig.1.4(b) and (d) are the respective derivative ($\frac{\partial V_{out}}{\partial I_{in}}$), which indicates the TIA has transimpedance of $103k$. It is notable that not all TIA on the chips have the same transimpedance. This is because the transimpedance value depends on the resistance of the resistor (Fig.1.2). *We use N-well to implement this resistor, which should have the largest resistance-to-surface ratio among other kinds of resistor.* But since the doping concentration may vary with the fabrication process, such kind of resistor has a larger resistance variance (% 30). We have performed necessary simulation before tap out. It is assured that the variance does not disturb the important characteristics of whole read-out circuit such as stability and noise ratio.

1.1.4 OP

By applying a sinusoidal signal to the negative input of OP, we found that the gain of OP is about $2k$ (Fig.1.5). However, the gain of OP was designed to be more than $5k$.

We will discuss this problem in the following section.

1.1.5 Measurement with the DC-sweep Mode Circuit and the Low-current Defect Problem

With the the DC-sweep mode circuit (Fig.1.6), we swept Ibias and measured V_G and I_D to obtain the I_D-V_G and I_{bias}-V_G curves (Fig.1.7). The chip works well when I_bias is larger than $1\mu A$. The overlap between two curves implies that I_D follows Ibias and V_G consequently alters due to the feedback mechanism.

When current becomes low, the circuit fails to prompt nanowire follows the biasing current. This phenomenon could be reasonable because the g_m becomes low and the feedback ability of the circuit may be not strong enough to push the gate of

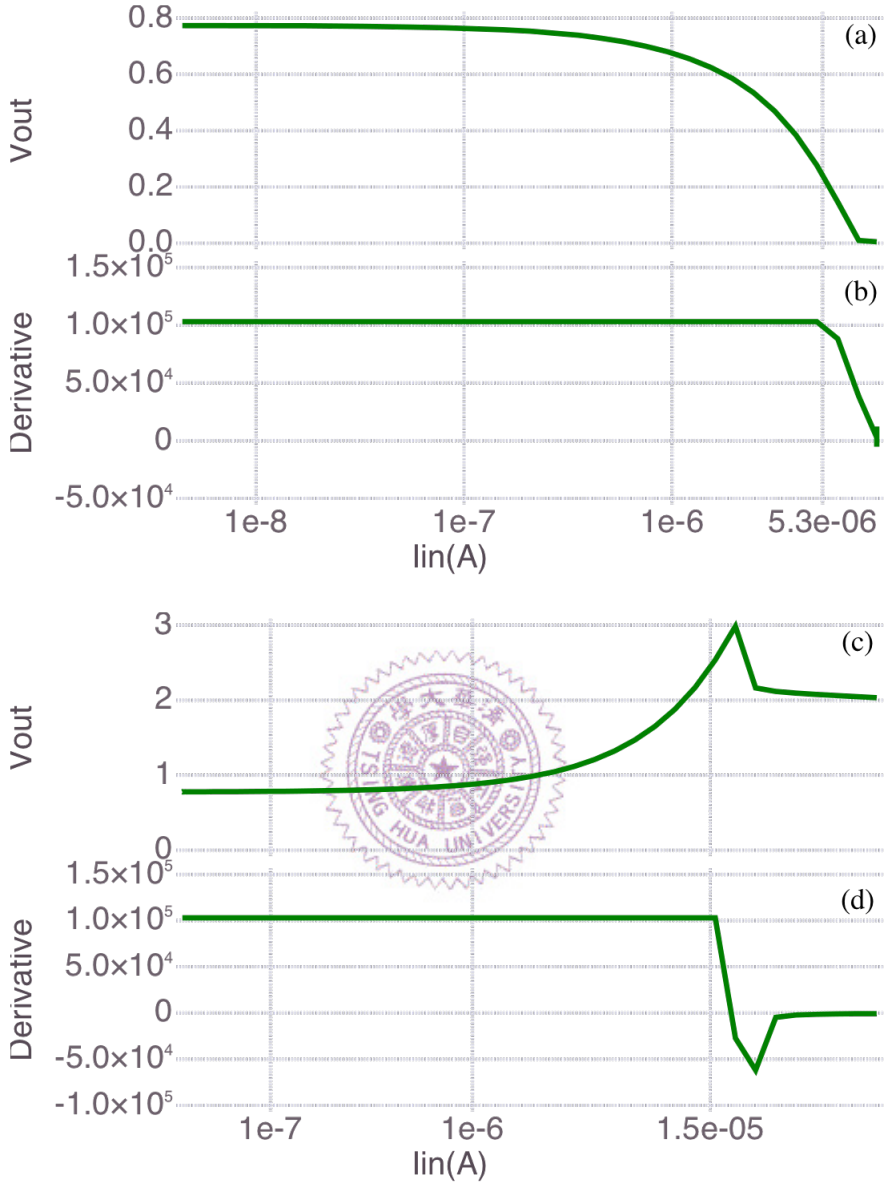


Figure 1.4: The dc simulation results of TIA. The x-axis represents positive/negative input current (log scale). **(a)** is the V_{out} responding to the positive input current while **(c)** is to the negative input current. **(b)** and **(d)** are the derivative of V_{out} of input current ($\frac{\partial V_{out}}{\partial I_{in}}$) from **(a)** and **(c)** respectively.

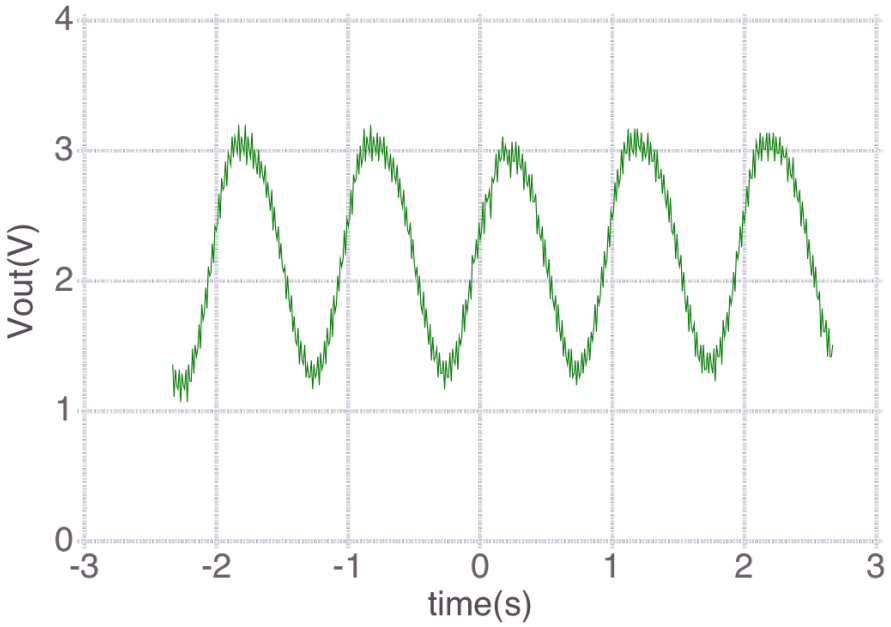


Figure 1.5: The output voltage of the OP when the negative input is applied with a sinusoidal signal. This input sinusoidal signal has frequency of 1Hz and amplitude of $1mV$. The positive input of OP is biased with a constant voltage generated by the chip. The output signal has amplitude around $2V$, which means that the gain of OP is about $2k$.

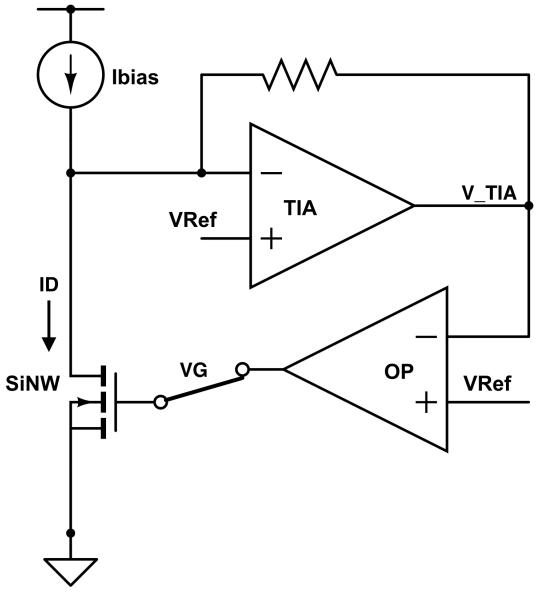


Figure 1.6: DC-sweep mode circuit

nanowire. However, when design the circuit (chapter 5), we expected this happens for g_m below $200n$. The Fig.1.8 indicates the circuit fails when g_m is less than 5μ. We call this problem as the low-current defect.

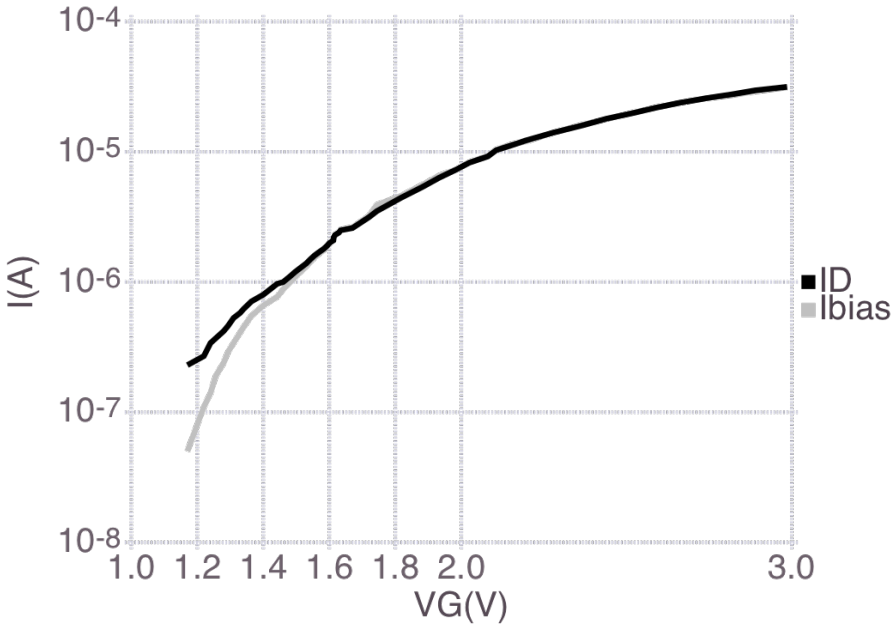


Figure 1.7: The measurement result of the DC-sweep mode circuit. I_{bias} is the biasing current. I_D is the current flowing through the nanowire device. One can observe a separation between two curves in low current section ($< 1\mu A$).

Insufficient Gain

We first suspected that it is caused by the insufficient Op gain (Fig.1.6). According to the last section (Section.1.1.4), the gain is about $2k$. The discussion in Section.**??** suggests the feedback mechanism depends on the loop gain of the circuit. The loop gain should be larger than 100 for the DC-sweep mode being functional. Based on Eq.(**??**) and Eq.(**??**), if A_{OP} is $2k$, the loop gain drops below 100 when g_m is less than $500n$. In other words, even though the gain of OP is 2.5 fold smaller than the gain we designed, the circuit should work well when g_m is larger than $500n$.

One reason may explain is that the gain of OP varies with input. As depicted in Fig.1.9, the slope ($\frac{\partial V_{out}}{V_{input}}$) at the midst is larger than the slope at the both end (The slope can represent the gain of OP). In the measurement of Fig.1.5, the offset of the output signal is around $2V$. But in Fig.1.7, when the separation happens, the

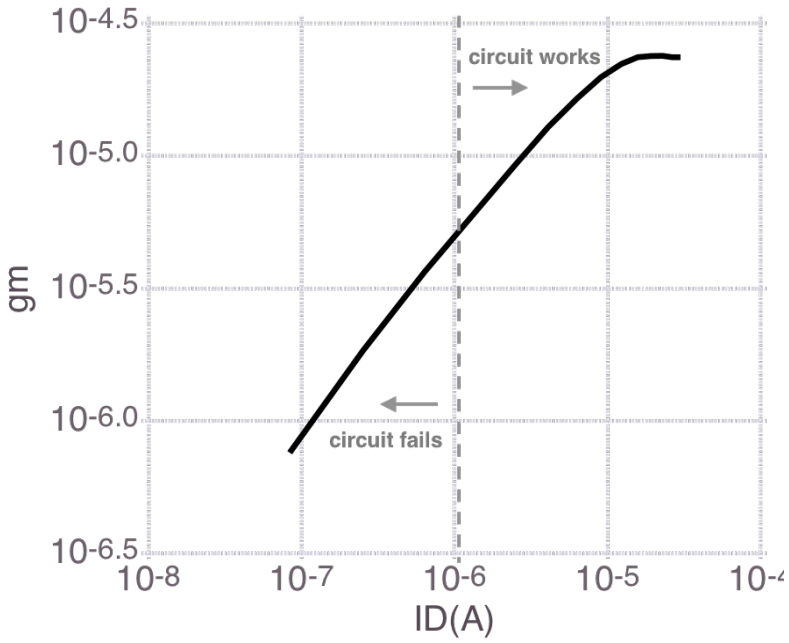


Figure 1.8: The g_m-I_D curve. It is obtained from the I_D-V_G curve in Fig.1.7. "Circuit fails" means the two curves in Fig.1.7 are separated where "circuit works" means they are overlapped.

output voltage of OP (V_G) is less than $1.5V$. Thus, we assert that the gain of OP is less than $2k$.

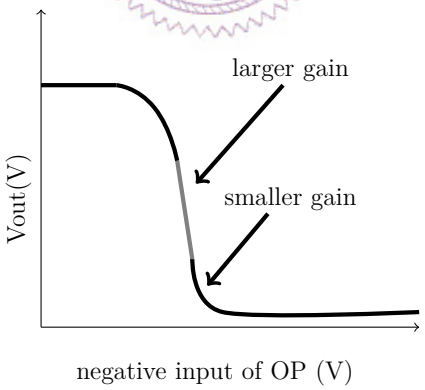


Figure 1.9

Input Offset Voltage

Another reason may be responsible for the low-current defect is the offset voltage at the input of the OP.

We examined the output voltage of TIA (V_{TIA}) of the Fig.1.7 DC-sweep experiment. It is shown in Fig.1.10. Ideally, when feedback mechanism works well, V_{TIA} should be equal to V_{Ref}(Fig.1.6). However, the value of V_{Ref} is $0.802V$, which is smaller than V_{TIA}. (This V_{Ref} is connected to a constant voltage point inside the chip. We know its value indirectly by measuring the drain voltage of nanowire since the drain of nanowire is kept to be same as V_{Ref} by TIA.) When the circuit works well, V_{TIA} and V_{Ref} is still different by $15mV$. This voltage difference can result in an $150nA$ offset current flowing through TIA and into the nanowire device. This offset current becomes remarkable when the I_{bias} is less than $1\mu A$.

We suggest the reason that V_{TIA} is large than V_{Ref} is due to the offset voltage appearing at the input of the OP. This speculation is reasonable through with respect to the layout, which will be discussed in the next section.

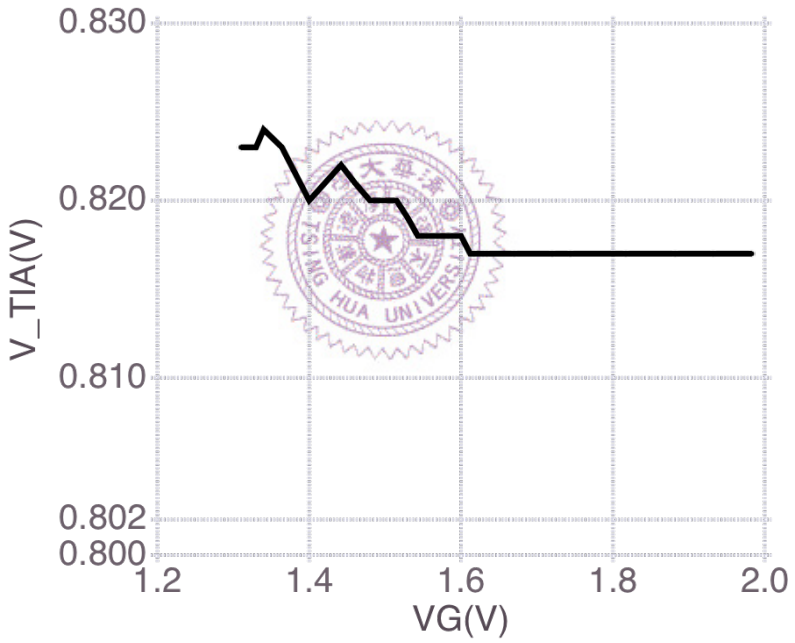


Figure 1.10: The V_{TIA}. The x-axis is the corresponding gate voltage. With the information from Fig.1.7, we found that the V_{TIA} is not equal to V_{Ref} no matter feedback mechanism works well or not.

Overall, the insufficient gain and the input offset may be the main reasons of the low-current defect. Both of them relate to the OP block. We then discuss these two reasons from the perspective of layout.

1.1.6 The Design and Layout Problems of OP

In the last section, me mentioned that the gain of OP is lower than we expected and there may exist an input offset voltage. In this section, we will deduce that several layout flaws may be responsible for these two problems.

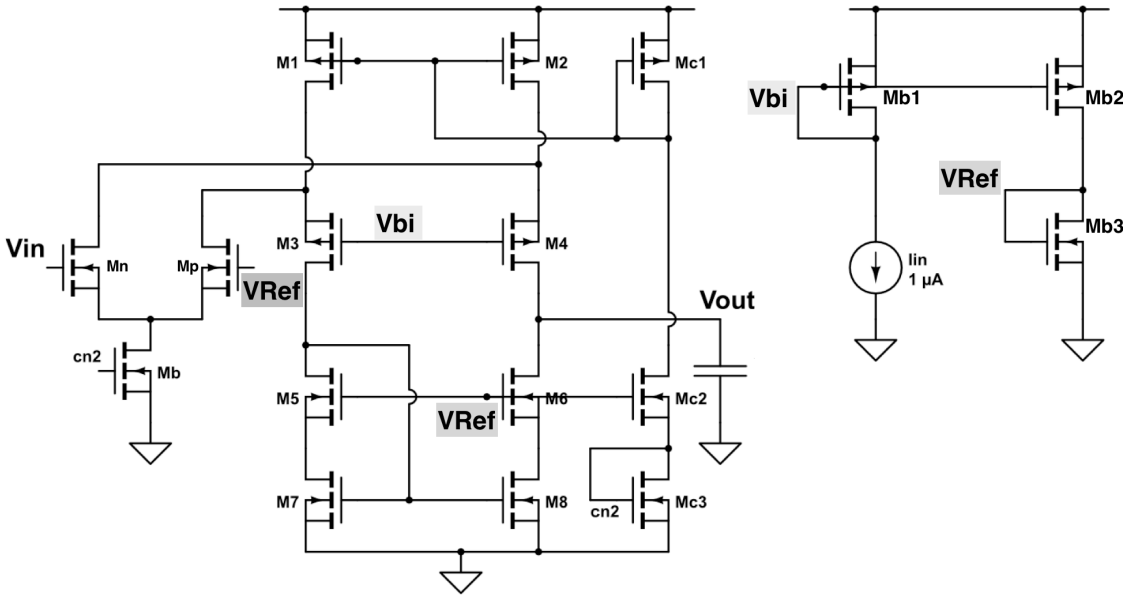


Figure 1.11: The left section is the schematics of the OP and the local biasing circuit. The right section is the global biasing circuit for generating two global biasing voltages: V_{bi}, V_{Ref}. The Iin is an external current source.

1.1.6.1 The Possible Reasons for Insufficient Gain

The schematic presented in Fig.1.11 contains two sections. The left section is the body of the OP, while the right one is a global biasing circuit. The global biasing circuit generated V_{bi} and V_{Ref}, which bias two pmos (M3, M4) and two nmos (M5, M6) respectively.

One layout flaw is that the M3 $\sim$ M6 are all single transistor. They are placed alone on the chip (Fig.1.12) without any protection, which cause their size and doping concentration to be vulnerable to the process variation. Another layout flaw is that the global biasing circuit is not placed next to the OP circuit. The extent of the process variation from which the OP circuit and global biasing circuit suffer may be different.

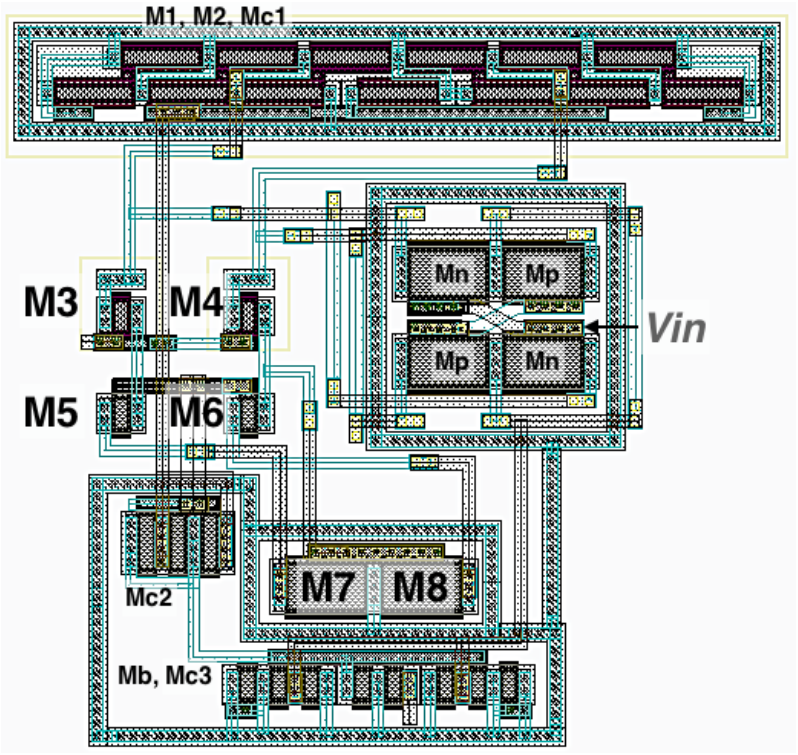


Figure 1.12: The layout of the OP including the local biasing circuit (The transistor Mc1∼3 in Fig.1.11)

Take an example, when process variation happens in global biasing circuit, V_{bi} and V_{Ref} change respectively. Ideally, the effect of these two changes on the gain of OP are countervailing. But this may not be true if M4 and M6 suffer distinct process variation and response differently to the gate voltage difference. Moreover, the high output impedance of OP amplifies this difference. Hence, the gain of the OP we design is more sensitive to the process variation.

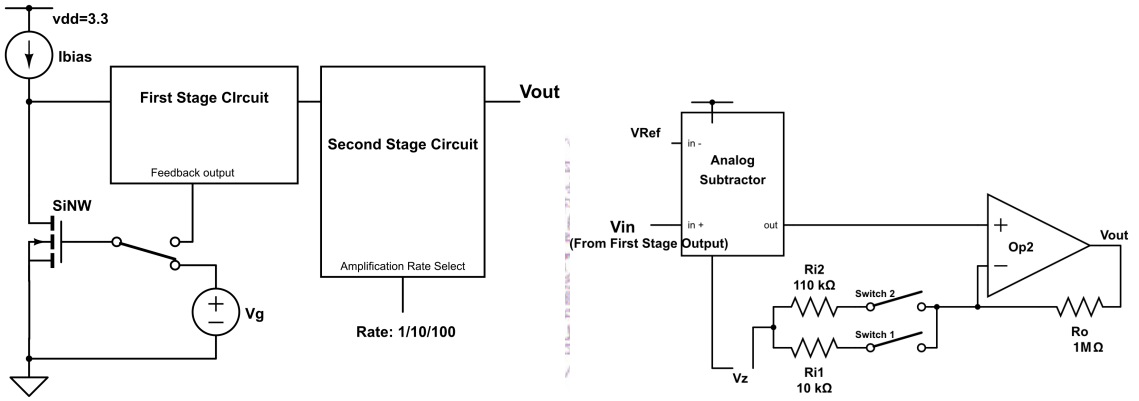
1.1.6.2 The Possible Reasons for Input Offset

The input offset can be related to the size mismatch between M7 and M8 (Fig.1.12). There is no dummy gate or matching technique applied to the transistors. Therefore, the size mismatch may prone to happen on M7 and M8. In our case, the offset voltage is negative ($V_{\text{negative input}} > V_{\text{positive input}}$). This means that the size of M8 may be relatively smaller than M7 (We designed them to be same).

1.1.6.3 Improvement Methodology

Although all problems mentioned above relate to the layout, we do not think that simply revising the layout is a reliable solution. The OP is a high an open-loop circuit with high output impedance. Its characteristics (such as gain) are hard to be control accurately considering the process variations. A better solution will be replace the OP. This OP served as a high-gain and low bandwidth block. In the future, we can substitute a close-loop amplifier and low pass filter for it.

1.2 The Second Stage Circuit and Transient Measurement Mode



(a) (b)

Figure 1.13: (a) The block diagram of the Transient Measurement mode circuit. **(b)** The schematic of the second stage circuit.

As in Fig.1.13, the Transient Measurement mode includes the Ibias and TIA from the fronted circuit and the second stage circuit. An analog subtractor and a resistor-based amplifier are included in the second-stage circuit. The input signal can be sent from the gate or the source of nanowire (SiNW) as mentioned in chapter 5.

1.2.1 The Second Stage Circuit

We present the important circuit properties in this section. To be notable that we did not measure the performance of the subtractor and amplifier independently

because there is no any external pad connected to the output of the subtractor. Besides, the output of TIA is always connected with the second stage input. Due to the low output impedance of the TIA, it is hard to give the input signal of the second stage circuit directly. Fig.1.14 is the alternative approach. The resistor Rs and the TIA compose a voltage amplifier. By injecting input signal through the Rs, we can therefore obtain the correct input and output signal of the second stage circuit.

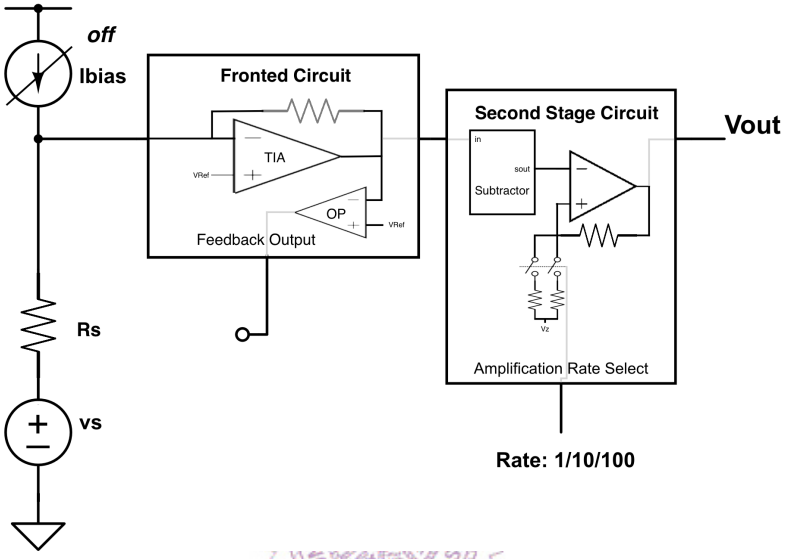


Figure 1.14

1.2.1.1 Noise Oscillation Problem in Amplifier with Amplification Rate of 1

The amplifier in the second stage circuit has three amplification rate (A_{amp}): 1, 10 and 100. The amplifier works well as the A_{amp} is 10 and 100. However, when A_{amp} is 1, the output signal is flooded with noise. In Fig.1.15, a 1Hz triangle signal is sent to the Rs. By the voltage amplifier composed of Rs and TIA, the signal is then sent into the second stage circuit. Ideally, the second stage output should be a triangle signal as well. But in fact the signal is flooded with noise.

We suggest that the oscillation of noise signal should be the main cause of the problem. The simulation we performed in chapter 5 did not consider the parasitic capacitance brought by the pad (with ESD circuit) at the output and switches. The

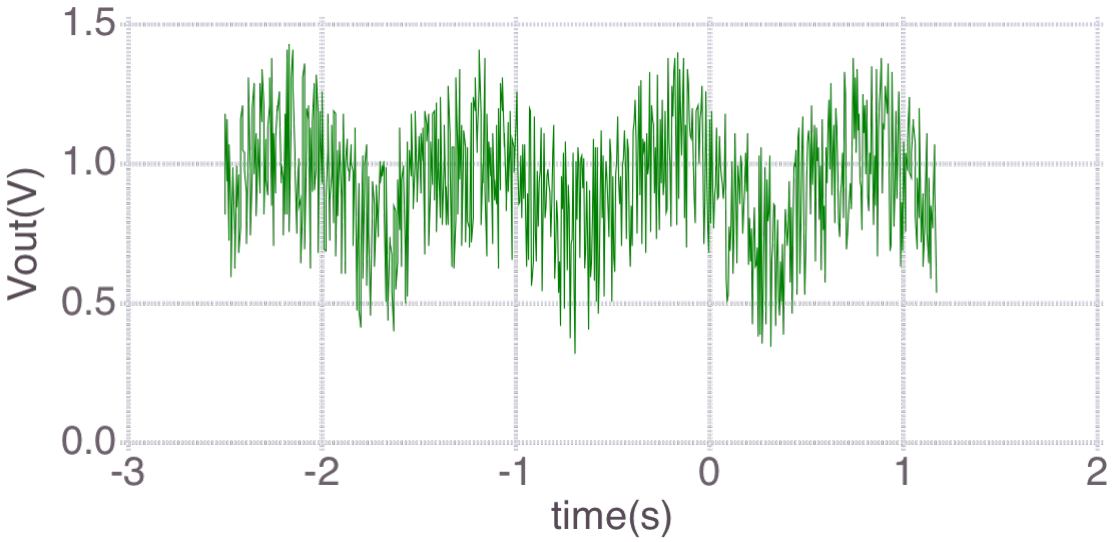


Figure 1.15

new simulation proves our suggestion. The second dominant pole locates at the output. The parasitic capacitors push it to the left and decrease the phase margin.

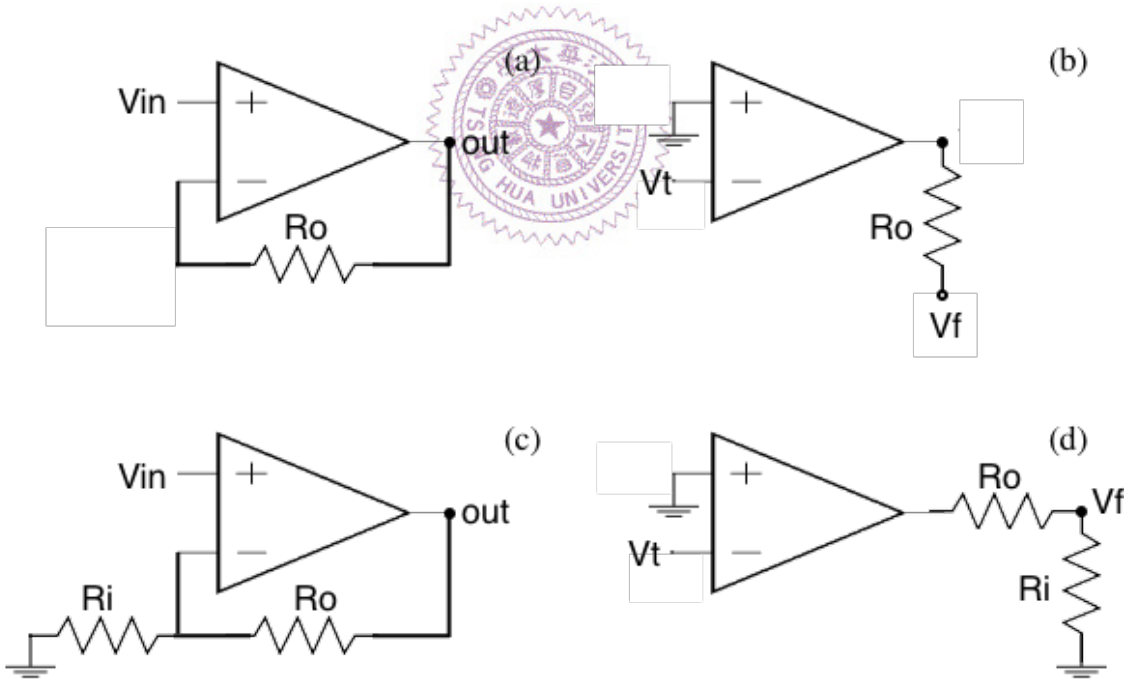


Figure 1.16

The reason that the noise oscillation problem only happens when A_{amp} is 1 is because of the feedback mechanism. The two switches of amplifier are turned off (Fig.1.13(b)). The structure is similar to an unit-gain buffer. In Fig.1.16, (a) is the

feedback network of this structure while (c) is of the amplifier with gain of 10 and 100. To compute the loop gain, the structure is broken at the negative input and a test signal is injected (Vt) as illustrated in Fig.1.16 (b), (d). The loop gain ($\frac{V_f}{Vt}$) of the two structure is derived as:

$$\text{when } A_{amp} = 1: \qquad \frac{V_f}{Vt} = A_{op} \tag{1.1}$$

$$\text{when } A_{amp} = 10 \text{ or } 100: \qquad \frac{V_f}{Vt} = A_{op} \times \frac{R_i}{R_i + R_o} \tag{1.2}$$

A_{op} is the gain of the OP in the amplifier where the loading effect has been taken into consideration. Since the R_O is at least larger than R_i by 10-fold, the two loop gain is different by 10-fold as well. The smaller loop gain increases the phase margin of amplifier by about 45 degree and diminish the oscillation.

Although the noise oscillation problem exist, we can still recognize the trend of the output signal by applying the signal average technique. The side effect of this technique is that it induce an offset ($\approx 0.15V$) to the output signal. This will appears in the following section where the input dynamic range is measured.

1.2.1.2 Dynamic Input Range

Fig.1.17 is the input-output response of the second stage circuit ($A_{amp} = 1$). We find the dynamic input range of the circuit with it. As illustrated in the figure, the linear region locates at $Vin = 0.62V \sim 1.32V$. According to chapter 5, this range is determined by the subtractor block.

Another input of the circuit is the Vz (Fig.1.13). This voltage is for shifting the offset voltage. Its dynamic input range is measured and presented in Fig.1.18, which ranges from $0.43V$ to $1.28V$. To be notable that ideally the input Vz should be equal to the output. But in fact an offset voltage occurrs in Fig.1.13 due to the noise oscillation problem mentioned in the last section. This offset does not exist when the A_{amp} is 10 and 100.

1.2.1.3 The Circuit Gain

The second stage circuit has three gain: 1, 10 and 100. We send a triangle wave to the end of Rs (Fig.1.14) and measure the input and output of the second stage circuit.

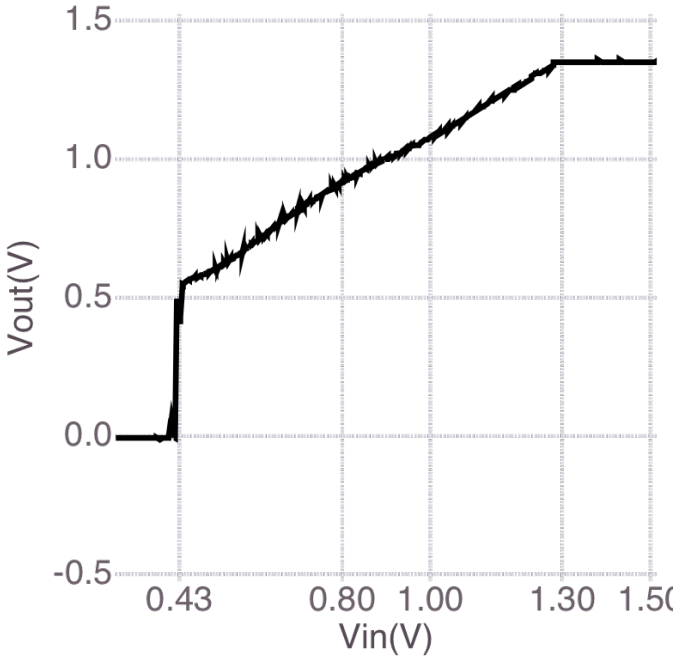


Figure 1.17: The input-output response of the second stage circuit.

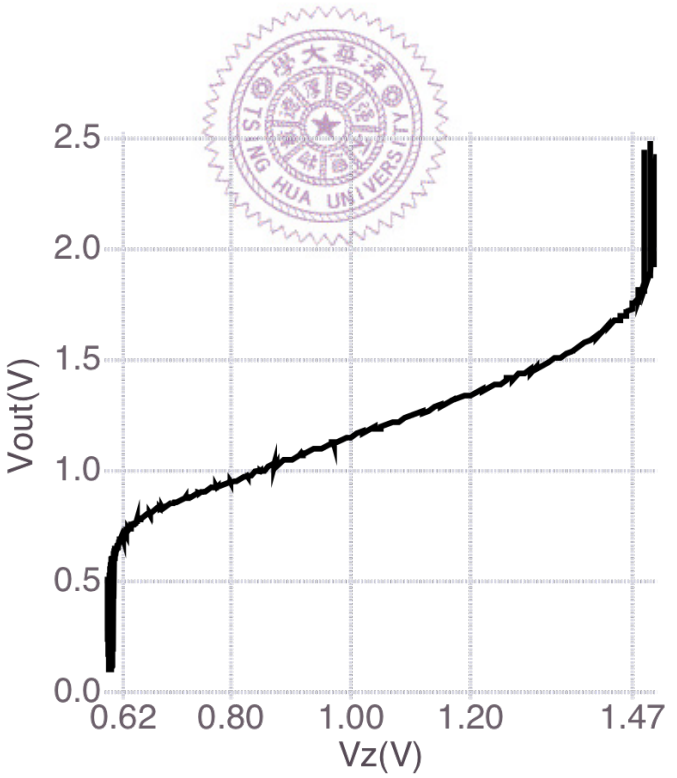
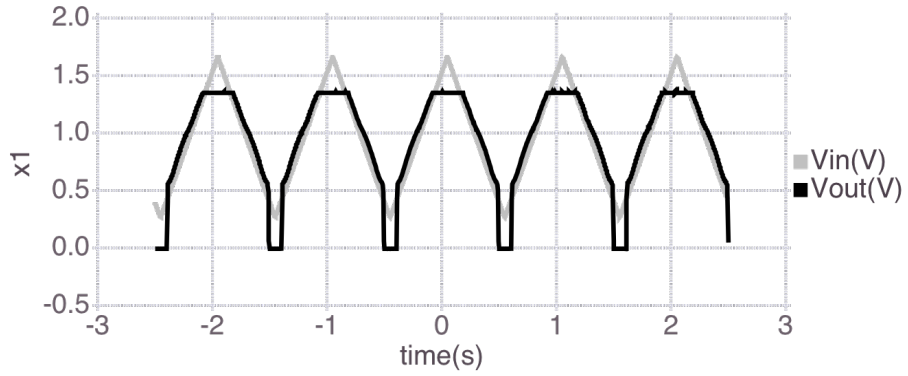
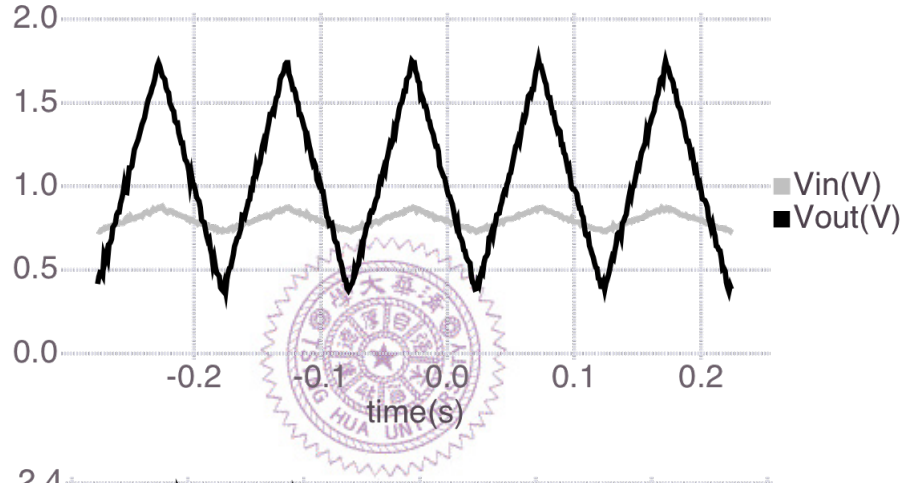


Figure 1.18: The input-output response of the second stage circuit. The input is Vz, which is decide the output offset of the circuit.

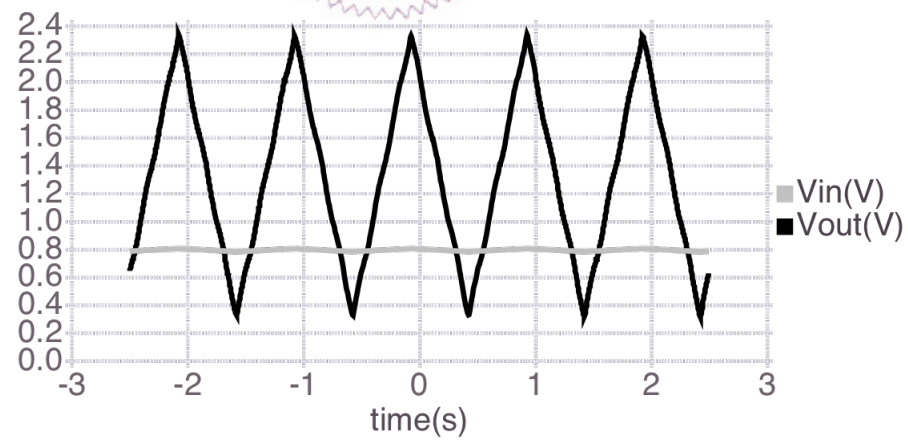
Fig.1.19) (a), (b) and (c) are the results of the second stage circuit with amplification rate of 1, 10 and 100 respectively. The exact gain values are summarized in the end of the section (Table.1.1).



(a)



(b)



(c)

Figure 1.19

Designed Amplification Rate	100	10	1
Measured Amplification Rate	93.3	9.2	1
Error Rate	7.7 %	8 %	0

Table 1.1

1.2.2 Transient Measurement Mode

The TIA from the fronted circuit and the second stage circuit compose the circuit of Transient Measurement Mode. This section presents the important properties of the circuit (gain, noise and bandwidth).

1.2.2.1 Bandwidth and Gain

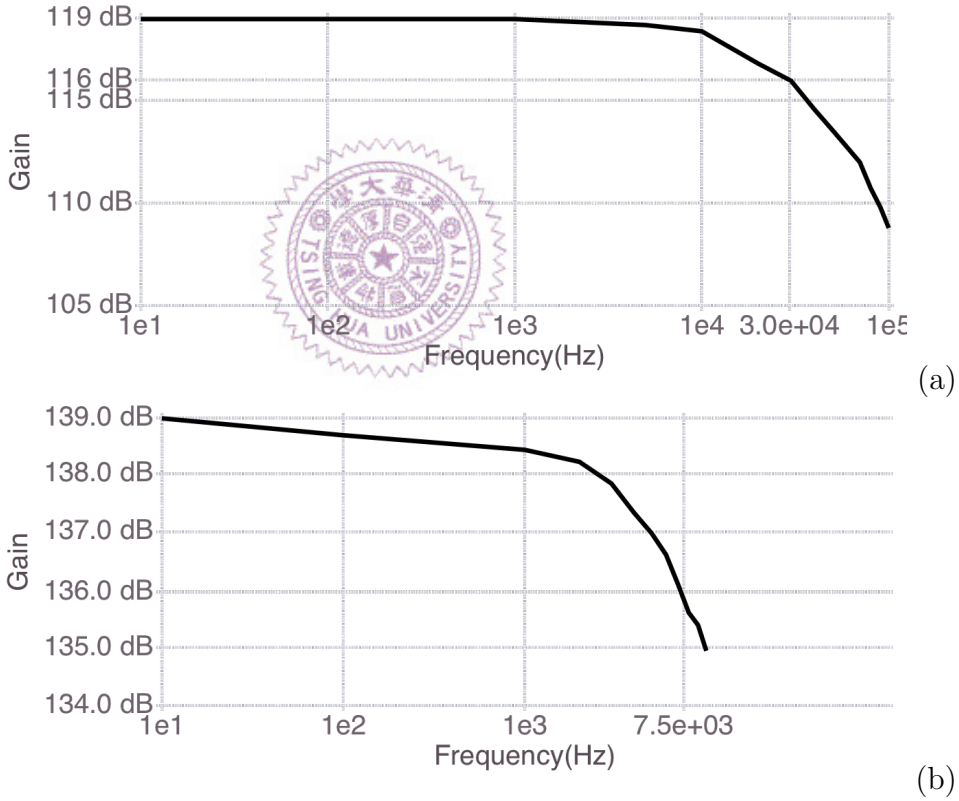


Figure 1.20

The gain is the input current to output voltage ratio. Because the noise oscillation problem may disturb the bandwidth measurement, we did not measure the circuit with A_{amp} of 1. The circuit with A_{amp} of 10 has gain of $891k$ and bandwidth of

$30k$Hz. The circuit with A_{amp} of 100 has gain of $8.9M$ and bandwidth of $7.5k$Hz.

1.2.2.2 Input Referred Noise

The spectrum analyzer are used to measure the noise. We measure the power spectral density (PSD) of noise at the output of the circuit and refer it to the input to show the equivalent input current noise. As illustrate in Fig.1.21, the primary type of noise are the low frequency noise, especially the 60Hz environmental noise. The environmental noise may be lowered by adopting better method of experiment or equipment. Overall, the amount of noise is tolerable. The spec. from chapter 3 allows for a maximal input current noise of $2nA$.

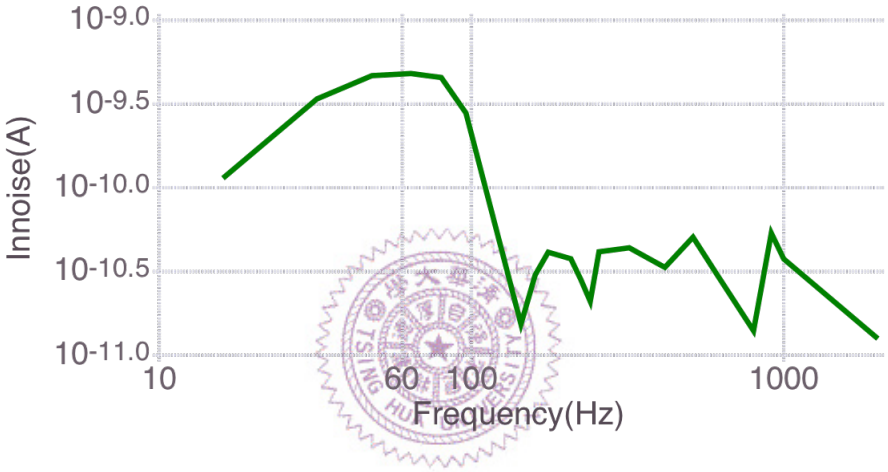


Figure 1.21

1.2.2.3 Modulating biomolecule signals from the source terminal

The second usage of the Transient Measurement mode circuit is to apply a sinusoidal signal at the source of nanowire. In Fig.**??**, we injected a 500Hz sinusoidal signal with amplitude of $0.5V$ into the source of nanowire and measured the output. The nanowire was put under two solutions with different pH values in (a) and (b). After dividing the amplitude of the output signal by the transimpedance gain of the circuit (891k), we learned that the g_m of nanowire under these two pH solutions are 1μ and 1.8μ.

This method aims to modulate the biomolecule signal into higher frequency to avoid the flicker noise and other kinds of low frequency noise. However, from the

result blow, we observe that the output contains large amount of high frequency noise. We believe the noise comes through the gate of nanowire which is covered by the testing solution. In the future, a bandpass filter with adjustable center frequency should be added into the circuit.

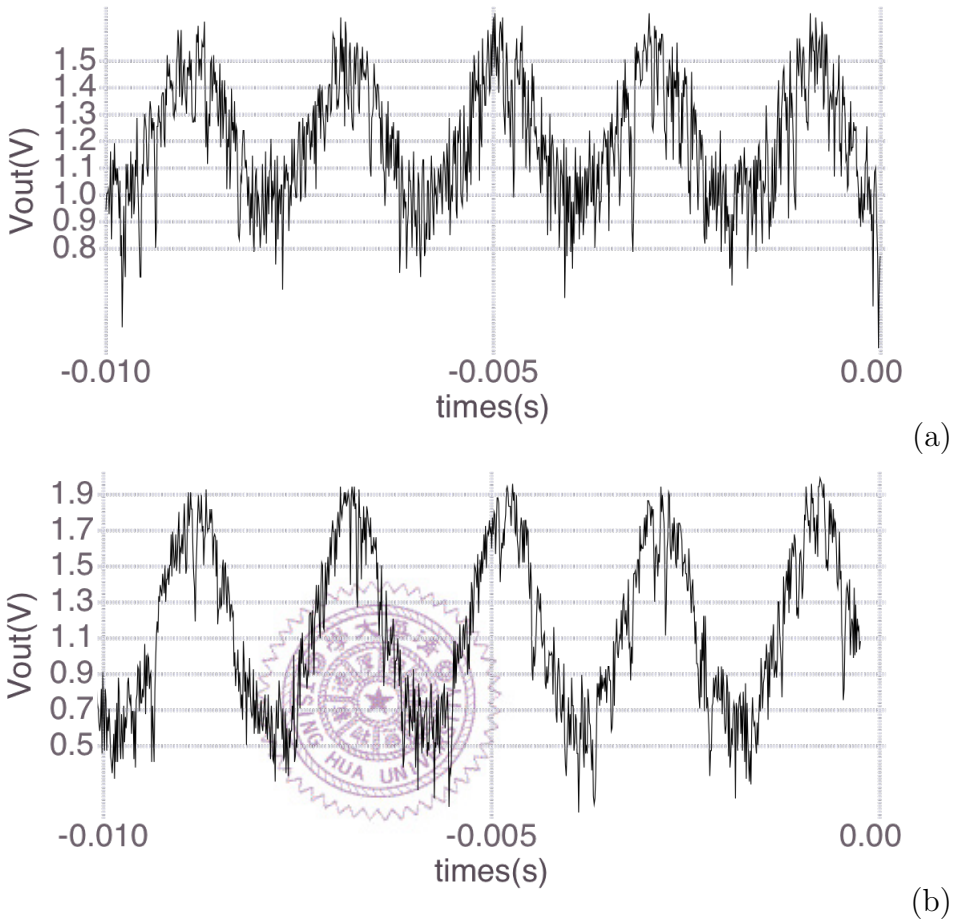


Figure 1.22

1.2.2.4 Summary of Transient Measurement mode

The table that compares the chip properties and the specification for transient measurement mode is given below (Table.1.2). Although there is the noise oscillation problem, the overall performance of the circuit is as expected.

	Design Spec.	Chip Properties
ΔI_D	$\pm 2.8\mu A$	$5.3\mu A$--$15\mu A$
Input Referred Current Noise	$< 2nA$	$< 0.5nA$
Transimpedance Gain (max)	$5M(\frac{V}{A})$	$8.9M(\frac{V}{A})$
Bandwidth	$> 1k$ (Hz)	$7.5kHz$

Table 1.2: The comparison between the chip properties and the specification for transient measurement mode from chapter 3.

1.3 Dealing with the Device Variability Problem

This section presents the measurement with the proposed variability-resisting method. As illustrated in Fig.1.23, the device variability problem happens on two nanowire devices (nw1-2, nw2-1). The Fig.1.23(a) shows the I_D-V_G curves of two devices are different.

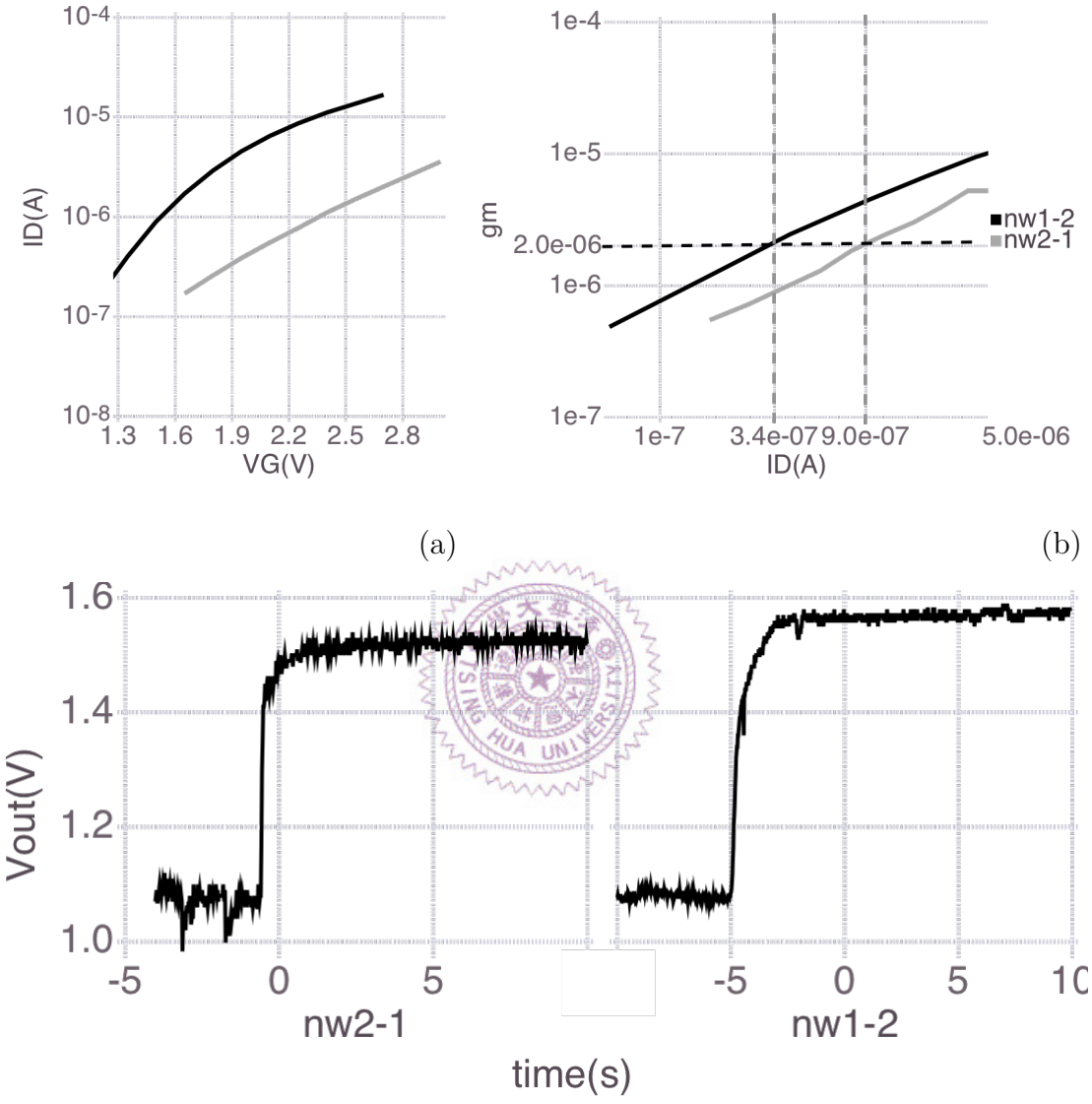

10-4
10-5
10-6
10-7
10-8
ID(A)
1.3 1.6 1.9 2.2 2.5 2.8
VG(V)
(a)
1e-4
1e-5
2.0e-06
1e-6
1e-7
gm
nw1-2
nw2-1
1e-7 3.4e-07 9.0e-07 5.0e-06
ID(A)
(b)
1.6
1.4
1.2
1.0
Vout(V)
-5 0 5
nw2-1
-5 0 5 10
nw1-2
time(s)
(c)
(d)

Figure 1.23

Bibliography

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