

國立清華大學

碩士論文

積體化電路設計之矽基體奈米線

An Integrated Circuit Design  
for Silicon-Nanowire



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# Abstract

Poly-silicon nanowire (SiNW) is a well-studied and interesting one-dimensional nanostructure. Since it was introduced to the biosensor field in 2001, it has become a promising candidate for ultra-sensitive, real-time and label-free sensor device. Nevertheless, many physical and chemical challenges constrain nanowire from being robust and practical. Nowadays, many studies adopt the integrated-circuit techniques to solve the problems. Circuits with different design concepts and purposes are proposed to meet practical needs.

In this thesis, based on the nanowire designed by Prof.Yang (National Chiao Tong University), we design our own read-out circuit. This research first analyzes biological experiments results (From Prof.Yang) and the electrical characteristics of the nanowires. The circuit specification and design are then based on these data analysis.

The circuit is capable of performing both DC-sweep ( $I_D-V_G$  sweep) and transient measurement. Moreover, we proposed a measurement method combining of these two functions. We believe this method mitigates the device variability induced by the fabrication process. Currently, most operations in this method are manual. We hope to make them automatic in the future by inducing digital circuits and constructing a system-level structure.

## 中 文 摘 要

矽基體奈米線（以下簡稱奈米線）乃一有趣並經過充分研究的一維奈米結構物。自從於 2001 年該元件被引入生物量測領域，奈米線就被賦予高度期望，能成為具有高靈敏度、即時性和不需生物標記等優勢的生物分子感測元件。雖然如此，目前仍有有物性和化性上的因素，限制了奈米線的良率和實用性。如今，許多研究採用了積體電路的技術，設計出在概念上和目的上不同的電路，來解決奈米線所遇到的問題和應付特定的需求。

我們使用由交大楊裕雄老師的奈米線元件和一部分量測資料，設計出一套元件訊號讀取電路。本篇研究首先進行生物實驗和電性量測的數據分析，接著根據分析結果來訂出電路的規格和進行電路設計。

我們的電路可以進行直流掃描量測 (DC-sweep) 和暫態量測 (Transient measurement)。並且，藉由結合此二量測，我們提出一套元件量測方式。這個量測方式被認為具有減輕因製程變異性而導致的元件差異問題 (Device Variability) 的能力。目前，該量測方式多採用手動操作，我們希望日後能引入數位電路於系統性架構，使量測能夠自動化。

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# Chapter 1

## Introduction

### 1.1 Motivation

Poly-silicon nanowire(SiNW) is a well-studied and promising one-dimensional nanosstructure. It was first introduced to the biosensor field in 2001[1] and has become a potential candidate for various features such as high surface-to-volume ratio, ultra sensitivity, label-free electrical detection and real-time measurement.

Although there have been substantial advances on nanowire structure design [2], the work on the system-level engineering is still insufficient. Systems designed for a specific purpose can help the device to meet practical needs such as noise reduction, real-time measurement, and analog-to-digital conversion. Moreover, there are still several challenges that may be overcome through a better signal acquisition system [2].

One of the challenges is that the mass production of robust nanowire device is still improbable. Device variability may be the main reason among others. This problem also happens to the measurement of our nanowire. The nanowire we use is made by Professor Yang's team (National Chiao Tong University). According to them, the nanowire uses thick gate dielectric and has non-regular cross-sectional shape, which result in the problem of fabrication uncertainty [3].

## 1.2 Design Overview

In this project, we design a nanowire read-out circuit with two modes: DC-sweep mode and Transient Measurement mode. In DC-sweep mode, one can use the circuit to perform a DC sweep of drain-to-source current ( $I_D$ ) to show how the gate voltage ( $V_G$ ) changes, or gives nanowire a constant  $I_D$  and measures the  $V_G$  response to different solution concentration. In Transient Measurement mode, the circuit detects and amplifies the variance of  $I_D$  with constant bias voltages applied ( $V_D$ ,  $V_G$ ,  $V_S$ ). We also combine two modes to implement our proposal: the variability-resisting method. This method of measurement may mitigate the device variability problem.

### Dealing with the Device Variability Problem: the Variability-resisting Method

The variability-resisting method is based on two assumptions:

1. The transconductance ( $g_m = \frac{\partial I_D}{\partial V_{GS}}$ ) of nanowire in weak inversion is linearly dependent on  $I_D$  and independent of  $V_{GS}$ .
2. The change of biomolecule concentrations can induce potential change on the surface of the gate of a nanowire.

(Since the source of nanowire is always grounded in this method, from now on  $V_{GS}$  is simplified as  $V_G$ .) The first assumption implies one can control the nanowire transconductance by its  $I_D$ . The second assumption means that as long as different nanowire elements have the same transconductance, the  $I_D$  variance induced by a concentration difference should be same.

The method works as follows:

**Initial stage** At the beginning of each measurement event, we perform a DC sweep with DC-sweep mode. By analyzing the sweep results with numerical method, we keep all nanowire devices under a selected transconductance by controlling their  $I_D$  and corresponding  $V_G$ .

**Measurement stage** We bias the circuit in Transient Measurement mode at this stage. Since the transconductance of all devices are same, they should behave uniformly based on assumption 2. At the end of the stage, we return to DC-sweep mode to reset  $I_D$  of the elements. The circuit adjusts their  $V_G$  to do so.

At the beginning of each measurement stage, a device always has the same  $I_D$  but different  $V_G$ . Based on assumption 1, its transconductance is kept constant.

Other details are reviewed in chapter 5. Currently, most operations are manual. We hope to make them automatic in the future, which may require digital circuits.

## 1.3 Design Flow and Chapter Layout

In this thesis, there are six chapters sorted according to the design flow.

Chapter 2 reviews the basic theories and the literature that are related to our work.

Chapter 3 gives a brief description of nanowire structure. It is then followed by two sections about some measurement and data analysis. The data of the first one is from the biological experiments while the second one is from the electrical measurement. We use the analysis results to design the read-out circuit.

Chapter 4 is an “accessory”. This chapter contains the discrete circuit which was designed for ion-sensitive field-effect transistor (ISFET) [4]. It is constructed and some electrical measurements are performed. The purpose of this process is to practice the constant-current constant-voltage method. The outcomes of this chapter underpin our integrated circuit design.

Chapter 5 talks about the schematic, design process and the simulation results of the read-out circuit.

Chapter 6 presents the measurement results of our integrated circuit and the conclusion of this project.

# Chapter 2

## Literature Review & Theory Description

As previously mentioned in the introduction section, the read-out circuit has two operation modes. DC-sweep mode controls the drain current ( $I_D$ ) of nanowire while Transient Measurement mode is for current variance measurement. Each of them refers to different sources. Section 2.1 talks about the reason why we perform  $I_D-V_G$  sweep. It is then followed by the literature review related to the circuit design of DC-sweep mode. The literature related to Transient Measurement mode circuit design is in section 2.2. The last section discusses the two assumptions mentioned in section 1.2.

### 2.1 DC Sweep: $I_D-V_G$ Curves

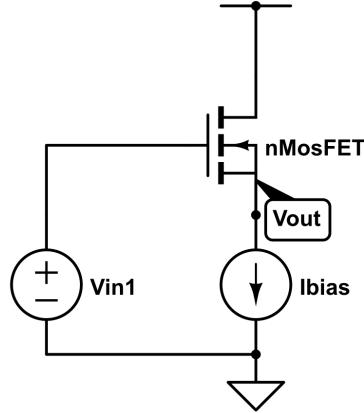
This section reviews the knowledge and an article that is related to DC-sweep mode.

#### 2.1.1 $I_D-V_G$ and Transconductance

A common method for examining nanowire electrical properties is to perform DC sweep. Among all kinds of sweep method, we choose the  $I_D-V_G$  in respect of the physical characteristic. In the n-type transistor, the binding of negatively charged biomolecules induces surface-near silicon ions discharged and thus increases the threshold voltage. It is straightforward to think of these binding molecules as a

voltage signal input to the gate with its value depends on the concentration. And this voltage signal effects nanowire in the same way  $V_G$  does. So by plotting  $I_D$ - $V_G$  curves, we can have a thumbnail of how concentration affects the  $I_D$ .

### 2.1.2 The Source Follower Structure



**Figure 2.1:** Sorce Follower

As one of the basic single stage amplifier, source follower (common drain) are employed to transfer voltage signal from gate to source while keeping  $I_D$  constant. The transfer function can be derived as:

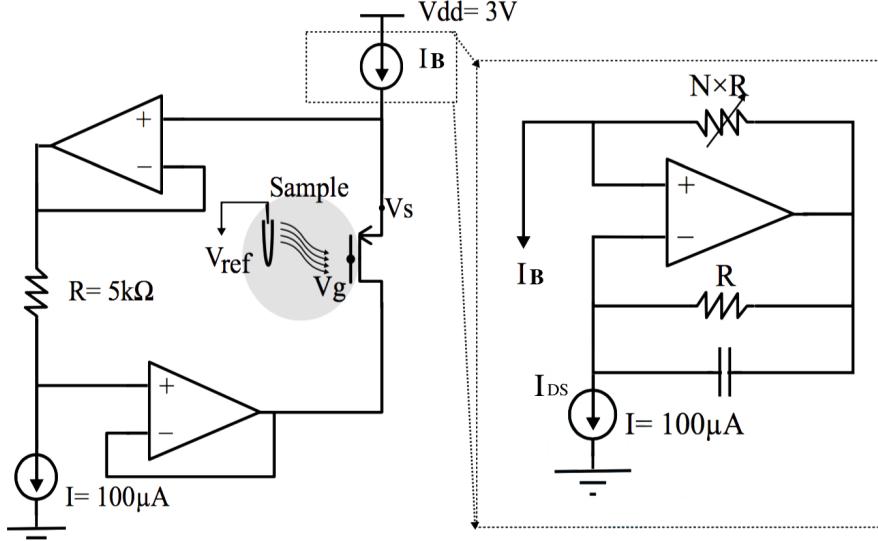
$$\frac{V_{out}}{V_{in}} = \frac{r_{ds}g_m}{1 + r_{ds}g_m} \quad (2.1)$$

$$\approx 1 \quad \text{for} \quad r_{ds}g_m \gg 1 \quad (2.2)$$

$g_m$  is the transconductance ( $\frac{\partial I_D}{\partial V_{GS}}$ ) and  $r_{ds}$  is the drain-to-source resistance. Although we have not seen the structure being applied to the nanowire, there have been several applications in the read-out circuits of ISFET (Ion-sensitive Field-effect Transistor)[4, 5] for a while.

The read-out circuit in [4] employs ISFET as a biological transducer that converts detected bio-signals into electrical signals, which resembles our nanowire biosensor. It adopts the source follower structure as its analog front-end. The potential change induced by the biomolecules at the gate of ISFET is converted to the source. This structure requires a biasing current which needs to be stable, noiseless or wide-range on demand. Since the biasing current is usually under micro-scale or even nano-scale,

it is impractical to use an external current source. The article [4] uses two resistors and an op-amp to design a current scale down circuit. As in Fig.2.2, bias current decreases in proportional to the resistance ratio ( $N$ ) as the current source circuit  $I_B$ .



**Figure 2.2:** ISFET readout circuit in [4]

The circuit in Fig.2.2 also removes the short channel effect by keeping  $V_{DS}$  at a constant value (0.5v). It adopts two op-amp based unit gain buffer to force the voltage at drain follows the source.

Attention should be paid to the impedance matching between the device-under-test (DUT) and the current source circuit. The output impedance of current source should be much larger than the input impedance of the DUT. By using nanowire as the DUT, the input impedance of it is:

$$\frac{r_{ds}}{1 + g_m r_{ds}} \quad (2.3)$$

This equation can be simplified as:

$$\frac{1}{g_m} \quad \text{for } g_m r_{ds} \gg 1 \quad (2.4)$$

The output impedance of the current source  $I_B$  is:

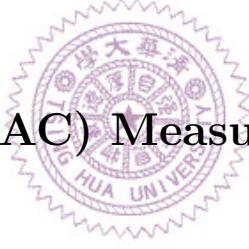
$$N \times Z_{DS} \quad (2.5)$$

$Z_{DS}$  is the impedance of the current source  $I_{DS}$  in Fig.2.2. In the integrated circuit,  $Z_{DS}$  is non-ideal but usually close to the  $r_{ds}$  of a single MOSFET.

As mentioned, Eq.(2.5) should be far larger than Eq.(2.4). However,  $g_m$  is proportional to  $I_B$ , which means Eq.(2.4) is inversely proportional to N. When the biasing current decreases, the output impedance of  $I_B$  decreases while the input impedance at the source of ISFET increases. This relationship determines the limit for  $I_B$ . We observed this boundary when we constructed this circuit with discrete elements. These will be presented and discussed in chapter 4.

The source follower structure provides a direct signal transition method. It is a good candidate for the read-out circuit with the aim of detecting transconductance or threshold voltage variance. Nevertheless, post-processing such as amplification and filtering is necessary. The experiment results in [4] are untreated. Significant signal attenuation exists, which is mainly caused by low-frequency noise and ISFET drift [6]. The drift problem is dealt with by signal processing techniques while noise problem is left untreated.

## 2.2 Small Signal (AC) Measurement Method Review

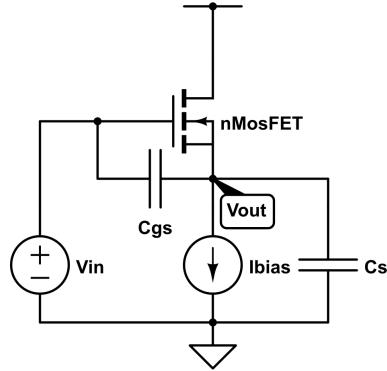


The previous section mentioned that the source follower exhibits compelling advantages as a signal processing structure of nano-device. However, the structure faces obstacles when being applied to the small signal detection. Parasitic capacitors and resistors can influence the results.

As the parasitic elements are included in Fig.2.3, the transfer function Eq.(2.2) is modified as:

$$\frac{V_{out}}{V_{in}} = \frac{r_{ds}(sC_{gs} + gm)}{1 + r_{ds}(gm + s(C_{gs} + C_s))} \quad (2.6)$$

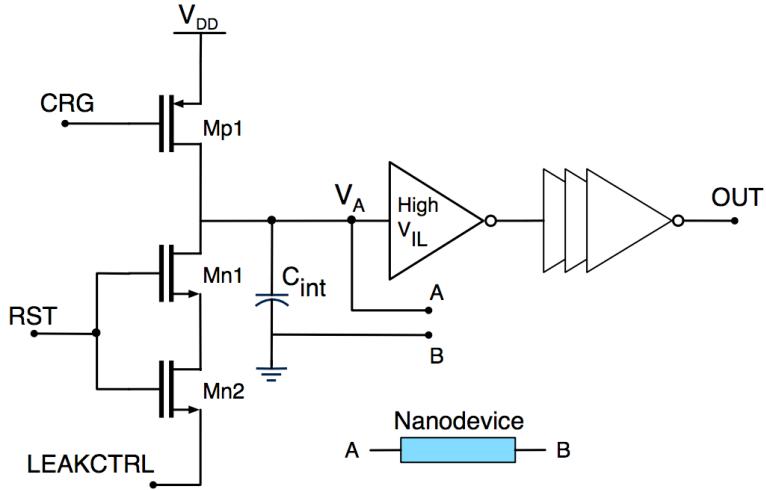
The equation can be similar to Eq.(2.2) which roughly equals to 1 as long as  $C_s$  is far smaller than  $C_{gs}$ . Unfortunately,  $C_s$  can be close to or greater than  $C_{gs}$  since the output of the source follower is connected to a next stage input or a pad. In that case, the signal may be attenuated.



**Figure 2.3:** Sorce Follower with parasitic capacitance

We want to build another circuit structure that can not only perform AC signal measurement but also disregard parasitic capacitance. We started by reviewing the works trying to measure the parasitic capacitance. Below, the works from two teams aim to measure the drain-to-source resistance ( $R_{NW}$ ) and the drain-to-source capacitance ( $C_{NW}$ ). The review focuses on the function and design theory of their read-out circuits.

### 2.2.1 RC Time Delay Measuring



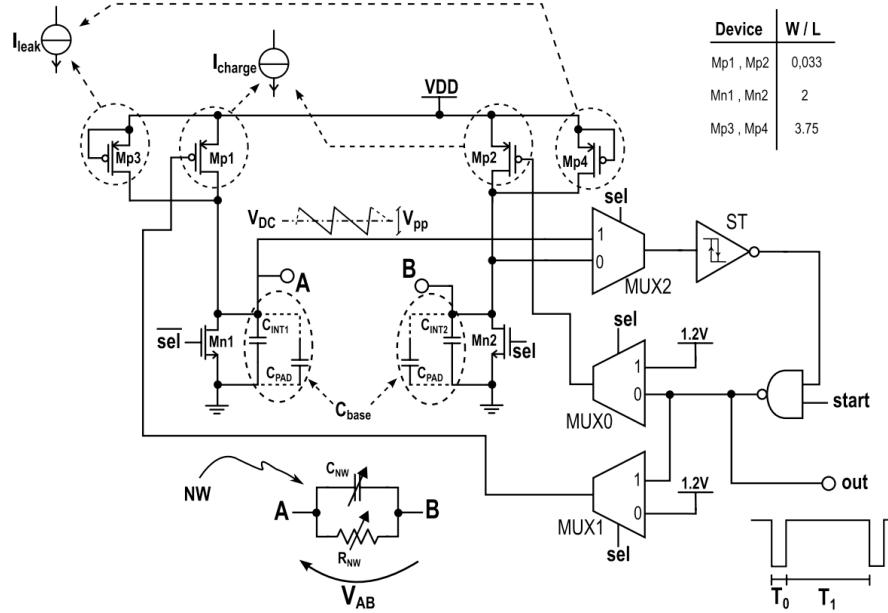
**Figure 2.4:** (a) Schematic of [7].

The measurement system for ZnO-nanowire based sensor array from [7] applies the Time-over-Threshold technique to its read-out circuit (Fig.2.4). The circuit alternatively charges an on-chip capacitor ( $C_{int}$ ) with a constant current and discharges

it through the nano-material resistance (nanowire). An inverter with its output switches from on to off when the capacitor is charged to its input threshold voltage, and vice versa. This behavior converts information of nanowire such as capacitance and resistance into time information.

The work presented in [7] does not have enough explanation of how they interpret the capacitance and resistance information. It merely mentioned that a microcontroller is responsible for the calculation. Besides, the work lacks simulation and experiment of measuring complex devices. Most of the results are the measurement of a concrete resistor as the substitute for nanowire, and  $C_{NW}$  is regarded as  $0pF$ . The only nanowire experiment does not have good performance. It seems that the design may only be applied to a device with pure resistance or pure capacitance.

The recent publican [8] by the team is more elaborate and contains the measurement of complex devices (A device composed of a discrete resistor and a discrete capacitor).



**Figure 2.5:** Schematic of [8].

In Fig.2.5, nanowire appends between point A and B. The charging current can be applied from Mp1 or Mp2, which is determined by the “sel” signal with the aid from MUXs. Below, it is assumed that sel = 1 and point B is virtual ground. (When the sel = 0, the circuit measures the device with a reversed biasing current.) The circuit

design concept is the same as [7]. The current charge both  $C_{int}$  and  $C_{NW}$ . When the voltage at A exceed the threshold voltage, the output switches off and causes Mp1 to turn off. (It is notable that the inverter at the output stage in [7] is replaces by a Schmitt trigger in [8]) Then the capacitor discharges through nanowire ( $r_{ds}$ ).

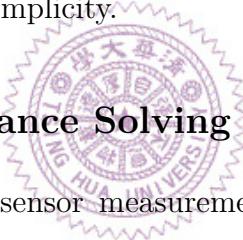
The bottom-right plot in Fig.2.5 defines  $T_0$  as the charging time and  $T_1$  as the discharging time. The calculation of the  $R_{NW}$  and  $C_{NW}$  can be simplified as:

$$C_{NW} = T_0 - C_{base} \quad (2.7)$$

$$R_{NW} = \frac{T_1 R_{par}}{(C_{NW} + C_{base}) R_{par} - T_1} \quad (2.8)$$

$$\text{where } R_{NW} || R_{par} = \frac{T_1}{C_{NW} + C_{base}} \quad (2.9)$$

$C_{base}$  are the  $C_{int}$  plus parasitic capacitance and  $R_{par}$  the parasitic resistance. These parasitic elements come from the transistor in the integrated circuit block such as MUX and Mp. It is notable that we do not consider the hysteresis of the Schmitt trigger here owing to simplicity.



## 2.2.2 Complex Impedance Solving

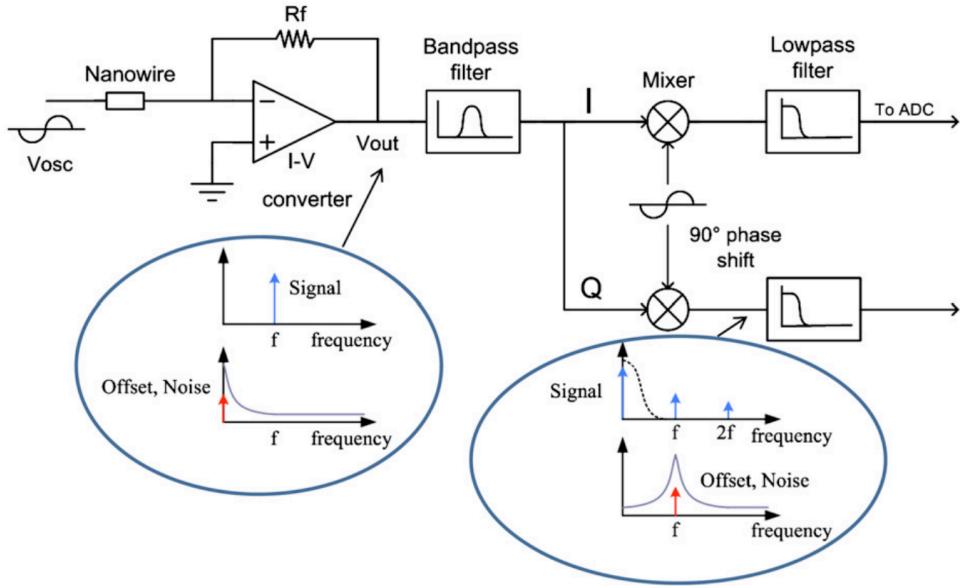
The nanowire-based hydrogen sensor measurement system in [9] adopts another method. It uses a lock-in amplifier to realize both resistive and capacitive impedance measurement.

As the previous method, it treats nanowire as a device with complex impedance. The nanowire is modeled as a resistor and a capacitor in parallel connection. The system applies a sinusoidal voltage signal to one end of the device. Another end of the device is virtually grounded by a transimpedance amplifier (TIA). The TIA then converts the current variance into a voltage output which depends on the complex impedance of the nanowire. The resistance is in the real part while the capacitance is in the virtual part.

$$V_{out} = I_{NW} R_{TIA} \quad (2.10)$$

$$I_{NW} = V_{in} \left( \frac{1}{R_{NW}} + j2\pi f C_{NW} \right) \quad (2.11)$$

$f$  is the frequency of input signal.



**Figure 2.6:** Block diagram of the lock-in amplifier in [9]

The output of TIA is followed by a controllable bandpass filter (BP). The BP removes high-order harmonic interferences. Then the signal is demodulated. The resistive and capacitive impedance values are resolved through two channels: I and Q with their phase different by 90 degrees. A mixer which is a linear multiplier performs the demodulation. With a radio frequency (RF) input and a local oscillator (LO) input, it produces an output signal that consists of signals with frequencies  $f_{RF} + f_{LO}$  and  $f_{RF} - f_{LO}$ .

### 2.2.3 Comparison and Conclusion

We compare the Method 1 (Sec.2.2.1) and Method 2 (Sec.2.2.2) here. Both of them focus on detecting the  $R_{NW}$  difference. According to the comparison table below (2.1), we can see the resistor measurement range of Method 1 is different from Method 2 by a large extent. It is not appropriate to make a comparison directly. These ranges are conformed to a detecting range for the current variance, which is also more helpful for our circuit design.

The resistance measuring range of Method 1 is  $1M\Omega \sim 1G\Omega$ . Since the circuit applies an input ac signal with amplitude of  $120mV$  to the nanowire device, the equivalent current variance is  $120\mu A \sim 0.12nA$ .

	[8]	[9]
R meas range	1M - 1G	10 - 40k
R meas error	< 2.5%	< 2%
C meas range	100fF - 1uF	0.5 - 1.8nF
C meas error	< 3%	< 3%
Detection of Input Current Varinace	$120\mu A$ - $0.12nA$	$3\mu A$ - $60nA$
SNR	> 45dB	-
Input referred noise	-	190 nV/sqrt(Hz) @ 5 kHz
CMOS Technology	0.13um	0.18um
Power consumption	14.82uW	2mW

**Table 2.1:** Specification Summary

As for Method 2, the measuring range relates to the noise. A  $3mV$  output referred noise limits the detecting range. According to the article, this noise value is equivalent to a 2% resistance resolution. Therefore, the output voltage range should be  $3mV \sim 0.15V$ . Moreover, the gain of the post-stage (BP and last-stage low pass filter) is 5 and the R<sub>f</sub> in the TIA is 10k. Hence the current variance that circuit can detect should be  $60nA \sim 3\mu A$ .

The relatively narrow current detection range of Method 2 should be because of the TIA block it adopts. Our method adopts this TIA block and will discuss this problem in Section 5.1.4.1.

Method 2 performs well when it comes to noise suppression. In fact, the circuit in Method 1 does not provide noise reduction ability. The particular structure it uses (The article [7] mentioned it as Micro-for-Nano (M4N) approach [10].) is the one responsible for that.

Method 1 has lower power consumption. However, it does not include the power of microcontroller and may be underestimated.

Overall, Method 1 has the advantage in detecting range and accuracy while Method 2 has better noise suppression.

In our project, capacitance measurement is not our object. But we still need to consider the parasitic capacitor effect in our circuit design. Method 1 converts the

resistance information into time (frequency) information. If one wants to avoid the effect of the parasitic capacitor, he should apply a  $C_{int}$  that is much larger than  $C_{NW}$ . However, it is not practical in integrated design because the chip size is limited.

Method 2 uses a TIA to measure resistance and capacitance together first and then resolves the complex value. We can write the complex impedance value as:

$$\frac{R_{NW}}{1 + i2\pi f R_{NW} C_{NW}} \quad (2.12)$$

In Eq.(2.12),  $i$  is the imaginary unit and  $f$  is the signal frequency. The equation can be simplified as  $R_{NW}$  when  $i2\pi f R_{NW} C_{NW} < 0.1$ . The simplification can be applied when the signal frequency or  $C_{NW} R_{NW}$  is small enough.

Since our goal is to ignore the capacitance and merely detect the resistance (or transconductance), Method 2 is more suitable for us. Because it is easier to separate capacitive and resistive measurement by Method 2 than by Method 1.

## 2.3 Two assumption for Dealing with Device Variability Problem



In chapter 1, to deal with device variability problem, we assume that:

1. The transconductance ( $g_m = \frac{\partial I_D}{\partial V_G}$ ) of nanowire in weak inversion is linearly dependent on  $I_D$  and independent of  $V_G$ .
2. The change of the biomolecule concentration can induce potential change on the surface of the gate of a nanowire..

We discuss them in this section.

### 2.3.1 Transconductance and $I_D$

With the MOSFET model of weak and strong inversion, we have the  $I_D$  equations of MOSFET :

$$\text{weak inversion: } I_D = I_0 e^{\kappa V_{GS}/\phi_t} (1 - e^{-V_{DS}/\phi_t}) \quad (2.13)$$

$$= I_0 e^{\kappa V_{GS}/\phi_t} \quad \text{where } V_{DS} > 4\phi_t \quad (2.14)$$

$$\begin{aligned} \text{strong inversion: } I_D &= \mu C_{ox} \frac{W}{L} ((V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2}) \quad (2.15) \\ &= \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2 \quad \text{where } V_{DS} > V_{GS} - V_{th} \end{aligned}$$

$$(2.16)$$

$V_{GS}$  is the gate-to-source voltage ( $V_{GS} = V_G - V_S$ ). It will be written as  $V_G$  in the following paragraphs since source is considered to be grounded.  $C_{ox}$  is the oxide capacitance and  $\mu$  is the electron mobility. Both of them depends on doping concentration.  $W$  and  $L$  are the width and length of the transistor.  $\phi_t$  is the thermal voltage depending on temperature. The  $\kappa$  is the gate coupling coefficient. To be noted that we ignore the short channel effect, which does not effect our discussion since  $V_{DS}$  is always kept constant.

We then derive  $g_m$ :

$$\text{weak inversion: } g_m = \frac{\kappa I_D}{\phi_t} \quad (2.17)$$

$$\text{strong inversion: } g_m = \sqrt{2\mu C_{ox} \left(\frac{W}{L}\right) I_D} \quad (2.18)$$

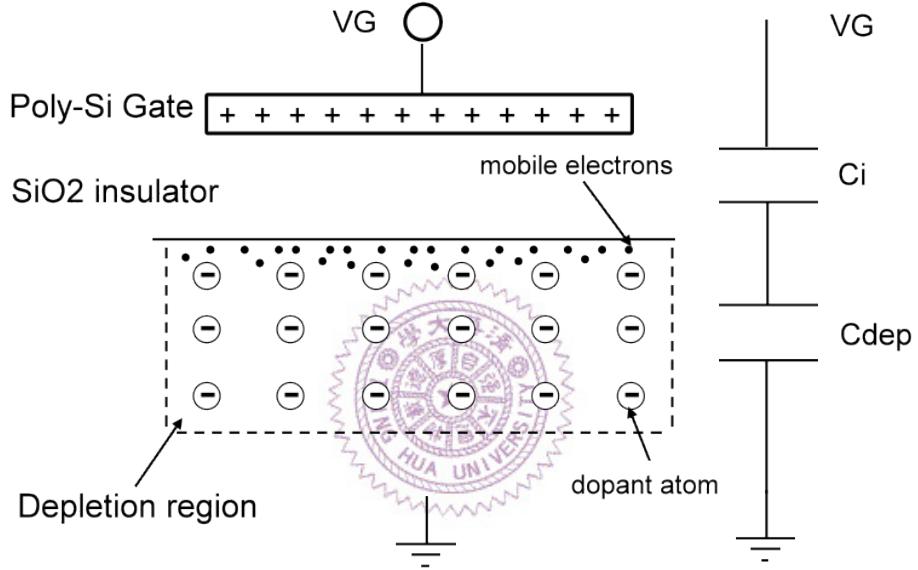
The Eq.(2.17) shows that the  $g_m$  in weak inversion is affected by the gate coupling effect. This effect is illustrated in Fig.2.7. The  $\kappa$  is actually the ratio of voltage divider:

$$\kappa = \frac{C_{ox}}{C_{ox} + C_{dep}} \quad (2.19)$$

The fact that  $C_{dep}$  varies with  $V_G$  makes  $\kappa$  a non-linear parameter. Its value ranges from 0.4 to 0.9. The structure of nanowire is different from MOSFET and is illustrated in Fig.2.8 The SiO<sub>2</sub> insulator in MOSFET is replaced by the solvent

and the  $C_{ox}$  becomes  $C_{sol}$ . According to the famous Gouy-Chapman model, the potential difference in the solution affect the double layer capacitance in solution [11]. Thus, it is still true that  $V_G$  affect  $gm$ . Nevertheless, it is convinced that the  $\kappa$  value is very close to 1 because  $C_{sol}$  is much greater than  $C_{dep}$ . This will be discussed later.

As for the strong inversion,  $g_m$  linearly depends on  $\sqrt{I_D}$  and independent of  $V_G$ . However, in nanowire, the  $C_{ox}$  is replaced by  $C_{sol}$  and is affected by  $V_G$  and the solvent concentration. Therefore, the assumption 1 cannot be applied to nanowire in strong inversion region.

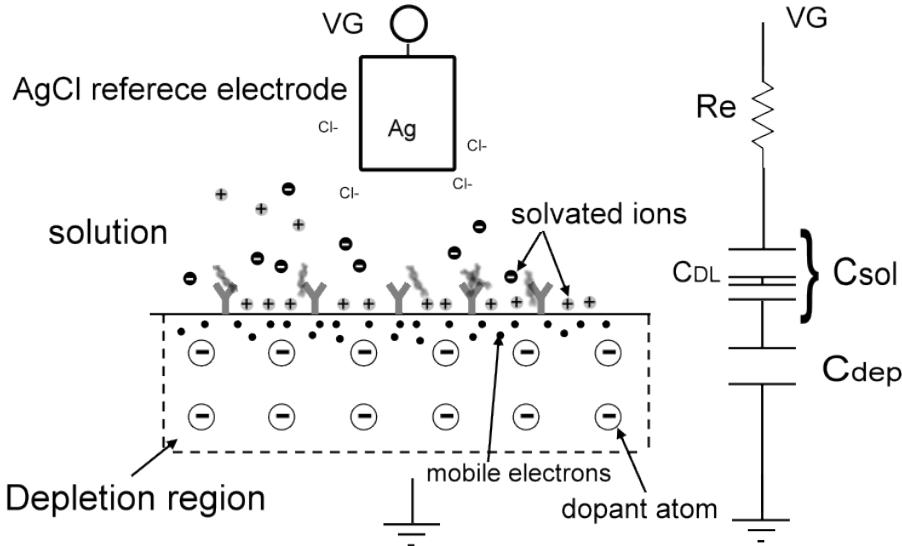


**Figure 2.7:** The gate coupling effect in MOSFET [12].

### Estimation of $C_{sol}$

$C_{sol}$  can be estimated by applying the famous Gouy-Chapman-Stern model [13]. The model explains the double-layer capacitance ( $C_{DL}$ ), which is the structure appears on the contact surface between liquid and metal or solid particle. The capacitance is considered to be two capacitors in series:

$$\frac{1}{C_{DL}} = \frac{1}{C_{stern}} + \frac{1}{C_D} \quad (2.20)$$



**Figure 2.8:** The gate coupling effect in nanowire.

$C_{stern}$  represents the capacitor in the stern layer and  $C_D$  represents the capacitor in diffusion layer. For DNA solution and PBS as buffer, the relative permittivity is 8 [14] and debye length is about  $0.7\text{nm}$ .  $C_{stern}$  is therefore roughly  $97\mu/\text{cm}^2$ . As for  $C_D$ , the value is hard to know since it relates to ion concentration and fluid potential. However, the model implies that  $C_{DL}$  is mostly dominated by  $C_{stern}$ . Only if the solution contains scarce solvent,  $C_D$  should be taken into consideration. It is clearly not our case because the PBS buffer we use has high ion concentration.

### 2.3.2 A Simple Model for Concentration Effect

In [15], the team plots the  $I_D-V_G$  curves and study how the curves change with the concentration of biomolecules. We observed that in the plot (Fig.2.9) with a log scale for the y-axis, curves with different concentrations exhibit the same rising trend when  $I_D$  is low ( $< 100\text{nA}$ ). Each curve seems to be different from each other by a constant shift. We found that this concentration effect can be explained by applying the weak inversion current equation of MOSFET.

$$I_{D1} = I_0 e^{\kappa(V_G)/\phi_t} \quad (2.21)$$

$$I_{D2} = I_0 e^{\kappa(V_G + \Delta v)/\phi_t} \quad (2.22)$$

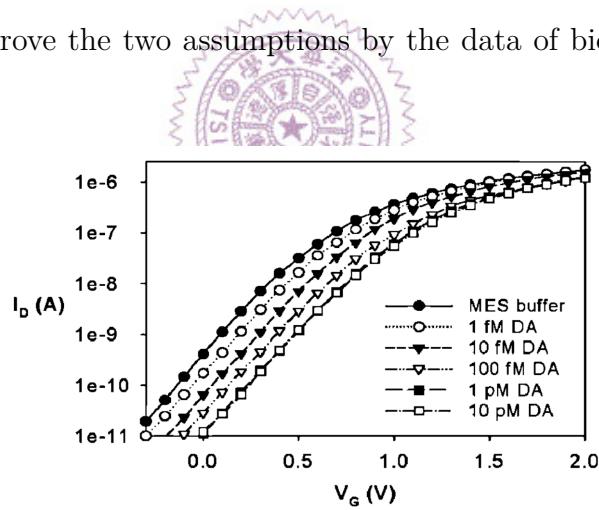
$$\rightarrow I_{D2} = f(\Delta v) \times I_{D1} \quad \text{where} \quad f(\Delta v) = e^{\Delta v/\phi_t} \quad (2.23)$$

The  $I_{D1}$  and  $I_{D2}$  are the current of two nanowire devices immersed in solutions with different concentrations. The  $(\Delta v)$  is a concentration related variable we create. The Eq.(2.23) implies that when nanowire is in weak inversion region, its  $\log I_D$  difference is independent of  $V_G$ .

$$\log I_{D2} - \log I_{D1} = \log \frac{I_{D2}}{I_{D1}} = \log f(\Delta v) = \Delta v/\phi_t \quad (2.24)$$

As for the strong inversion region corresponding to the large current segments in Fig.2.9, the difference among the curves diminish as  $V_G$  increases. This is reasonable when  $V_G$  is far larger than  $\Delta v$  and the concentration effect becomes ignorable.

We will further prove the two assumptions by the data of biology experiment in section 3.2.2.

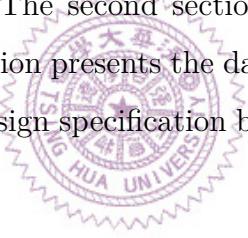


**Figure 2.9:** Concentration-dependent electric response ( $I_D - V_G$ ) of biotin-modified poly-Si NWFET following biotin–streptavidin interaction.[15]

# Chapter 3

## Nanowire Structure and Measurement

In this chapter, we present the experiment data and some analysis which are the foundation of our circuit design. The first section describes briefly the silicon nanowire in our experiments. The second section analyzes the data of the biology experiments. The third section presents the data of the electrical measurement. The last section provides the design specification based on the information given by the previous sections.

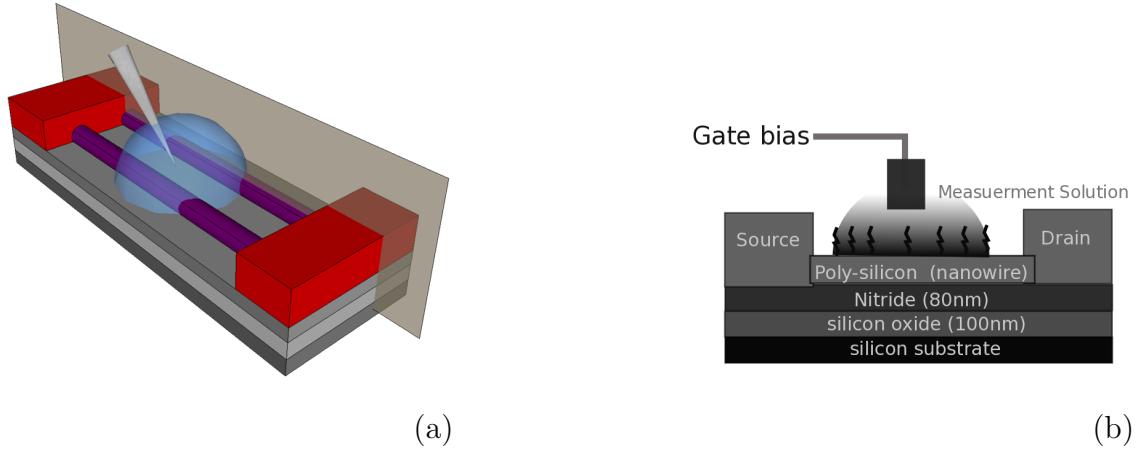


### 3.1 Brief Description of Nanowire

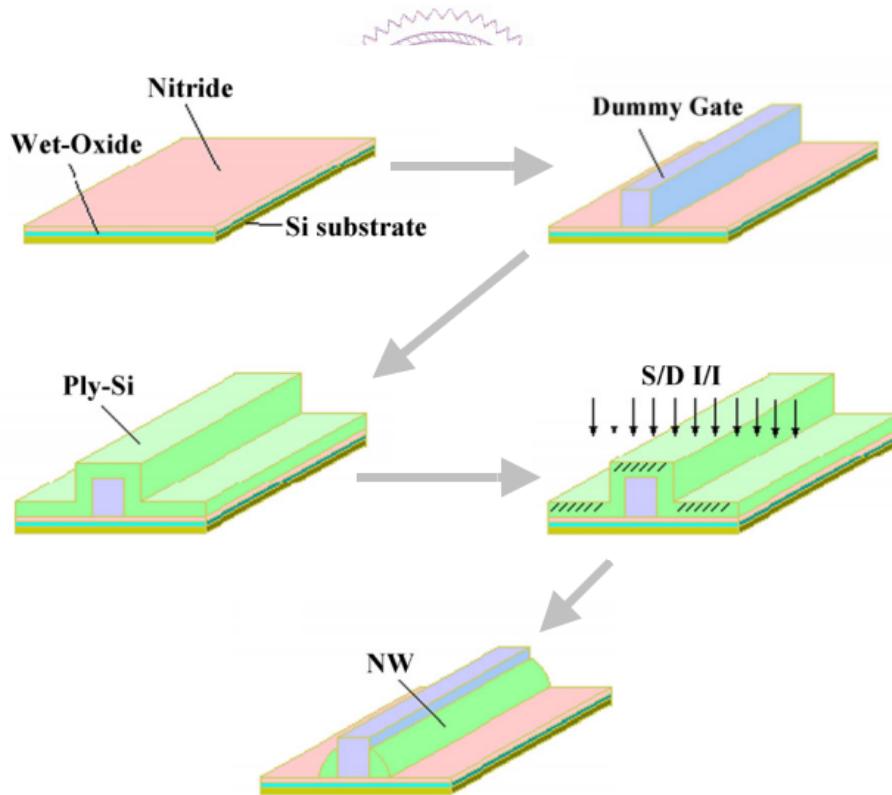
#### 3.1.1 The Fabrication Process and Structure of Nanowire

The nanowire we use is made by Prof.Yang's team (National Chiao Tong University)[16]. Fig.3.1 is the cross-sectional view of the nanowire structure. The poly-SiNW FET has two to ten poly-silicon channels. Each channel is 80nm in width and 2 $\mu$ m in length. The fabrication process is based on the poly-silicon sidewall spacer technique (Fig.??). The bottom of nanowire is a p-type Si serving as back-gate and starting material. It is covered by the oxide layer and a nitride layer. The nitride is to prevent the current from leaking into the back-gate. After three layers were formed, TEOS-dummy gate was placed. Then a 100nm a-Si is deposited on the device. The annealing step is performed. This step causes the a-Si to turn into poly-Si

and the S/D doping. Finally, with the Reactive-Ion Etching (RIE), the nanowire is formed. Through several post-process steps, the poly-Si of nanowire captures the DNA probe and serves as the sensing site for DNA molecules.[16, 3]



**Figure 3.1:** Nanowire Structure. **(a)** A nanowire device with two poly-silicon channels. **(b)** The sectional view of the cutting plane in (a).



**Figure 3.2:** The fabrication process of the nanowire. This figure is plotted by Prof.Yang's team [15].

### 3.1.2 The Two Gates of nanowire and the Working Concept

There are two gates in our nanowire (Fig.3.3). The back-gate which has been mentioned in the last paragraph is the silicon substrate at the bottom. The other one is the floating-gate which locates at the nanowire surface. The gate bias voltage is provided from an AgCl reference electrode immersed in the DNA solution.

Both of the gates send a positive electrical field to the nanowire. This field stimulates the silicon atoms in nanowire and increases the free electrons. In other words, when the gate bias rises, the current flowing thorough nanowire ( $I_D$ ) increases. Since the DNA molecule is negative charged, the higher the DNA concentration is, the larger the  $I_D$  is.

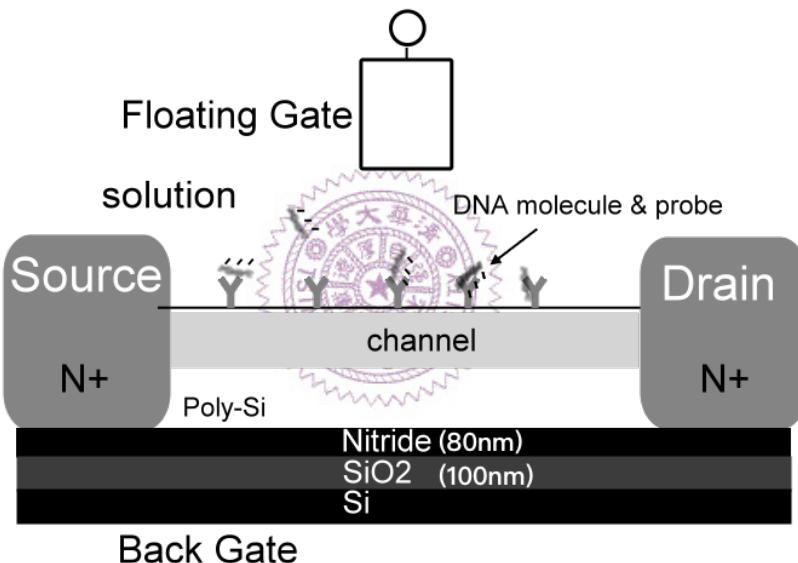
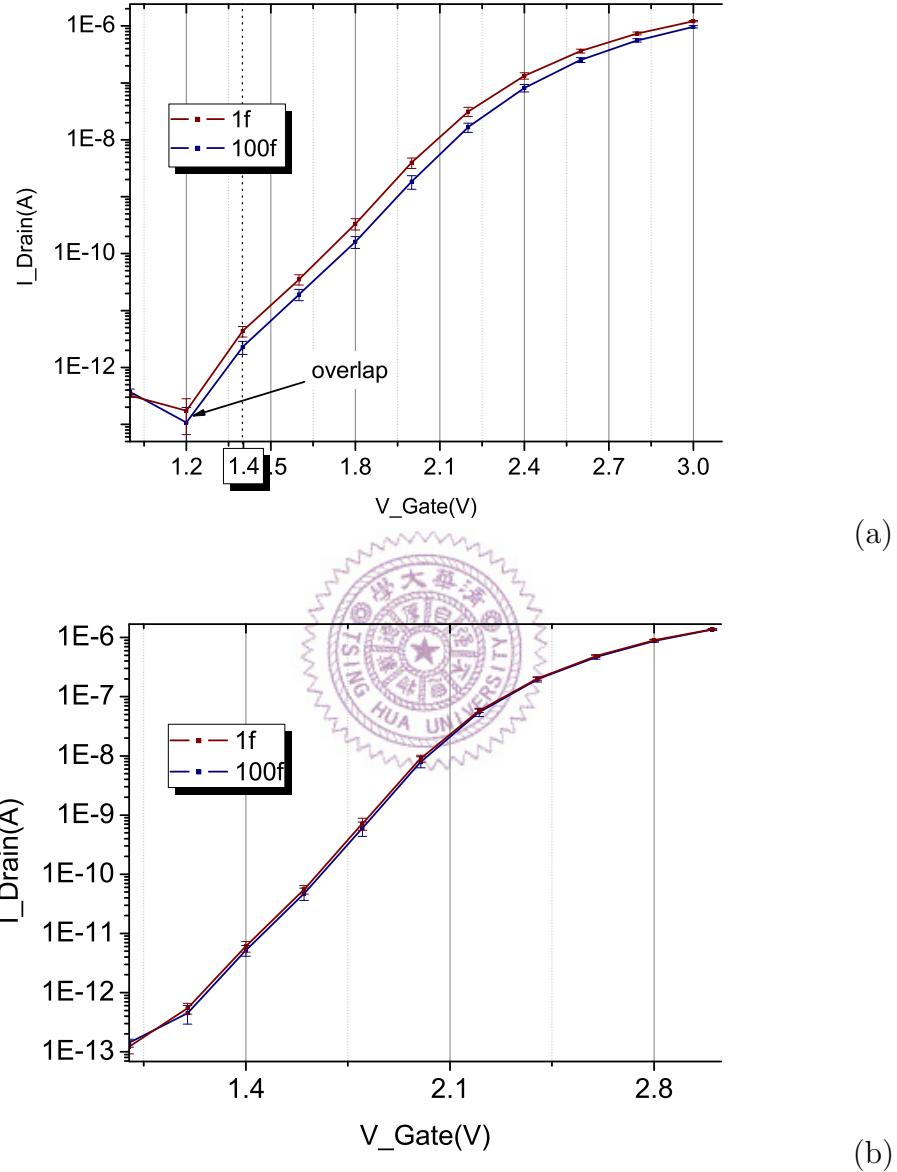


Figure 3.3

## 3.2 Biology Experiment

The biology experiment data are provided by Prof.Yang's team. These data are the Id-Vg measurement of the same biomolecule placed under different circumstances or with different nanowire devices. With each measurement repeated for three times, we find the mean and standard deviation (SD) of them and consider the SD value

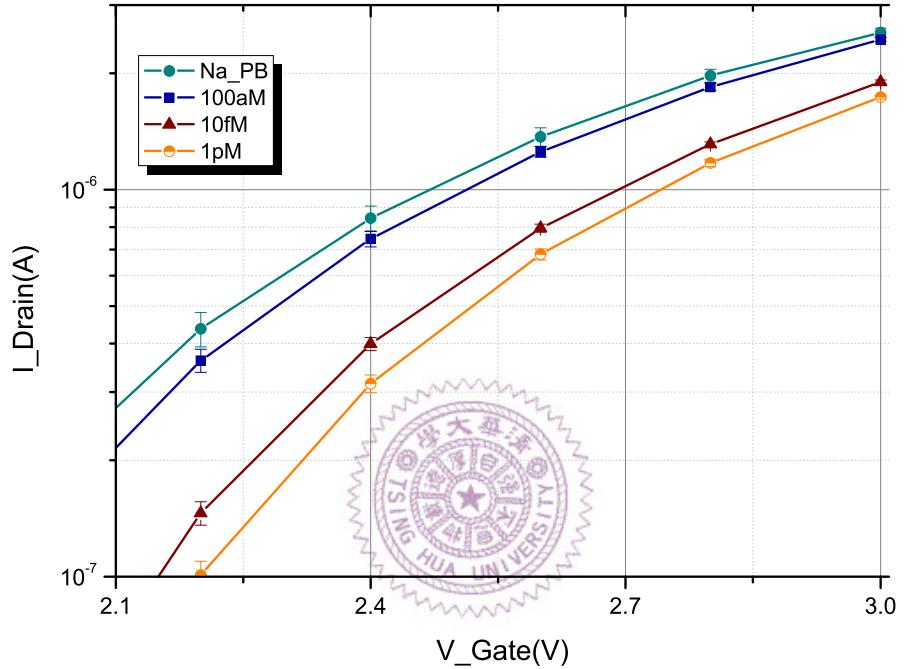
as the intrinsic noise of nanowire. We want to ensure that such noise should not be greater than the signal. To be more specific, we examine whether the Id-Vg curves of different concentrations overlap with others or not. An example is presented below:



**Figure 3.4:** Concentration-dependent  $I_D$ - $V_G$  curves of two equivalent nanowire devices. In (a), the measurement result of 1fM and 100fM biomolecule solution is distinguishable. There is no overlap between two curves. This is not true in (b).

Fig.3.4 are concentration-dependent measurements (1 femto mole(fM) and 100fM biomolecule solution) obtained with two devices ((a) and (b)). The two curves in (a)

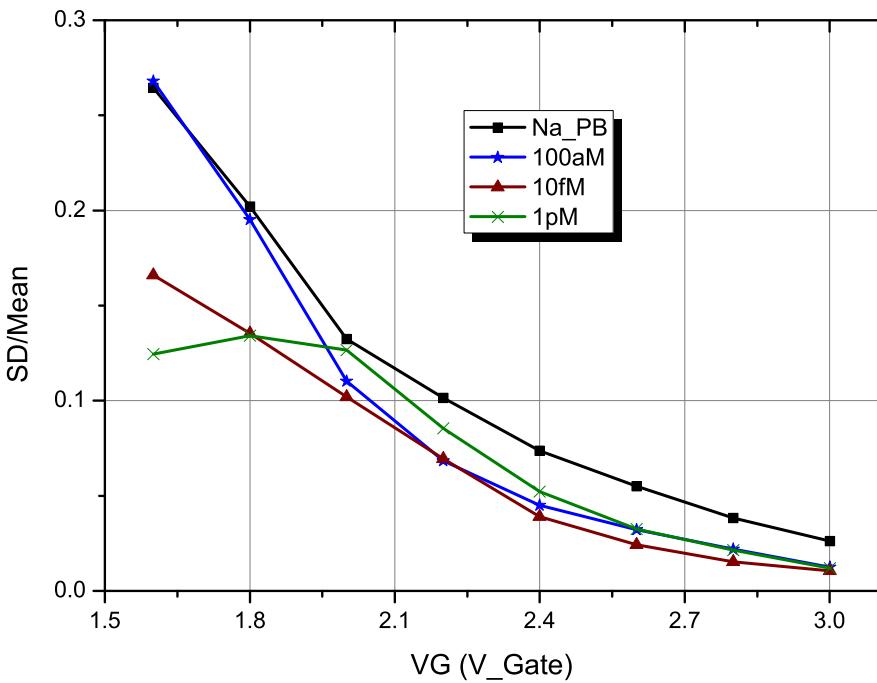
are distinguishable from each other after gate voltage is above 1.4v. They are not distinguishable in (b) since they overlap with each other. We thus assert that the device of (b) can not detect the concentration difference between 1fM and 100fM. The noise is stronger than the signal (The signal means difference in  $I_D$  caused by the concentration difference). The device of (a) can do so if it is biased at a gate voltage larger than 1.4v or a drain current larger than 1E-11.



**Figure 3.5:** Concentration-dependent  $I_D$ - $V_G$  curves with concentration of Na\_PB(Buffer solution only), 100aM, 10pM, 1pM. Since the biomolecule is negative-charged, the lower the concentration is, the higher the curve is. To be noticed, the 10fM curve is closer to the curve of 1pM than 100aM.

In Fig.3.5,  $I_D$  increases with the biomolecule concentration. One can find that there is only a small separation between the curve for PBS buffer and the solution containing 100aM of biomolecules. Hence 100aM should be the limit of detection.

It is worth noting that there is more significant difference between the curves for 100aM and 10fM than that between 10fM and 1pM. Besides, Fig.3.6 shows that the normalized variation:  $SD/Mean$  has not much to do with concentration. Hence,



**Figure 3.6:** The normalized variation of Fig.3.5. The normalized variation is obtained by dividing SD by Mean.

the analysis indicates that the “resolution” for detecting concentration ranging from 100aM to 10fM may be better than the that ranging from 10fM to 1pM.

### 3.2.1 Appropriate operation region

In [3], the team found that the current change ( $I_D$ ) induced by biomolecules was dependent on the applied gate voltage ( $V_G$ ). A device with a larger  $I_D$  change means that the device is more sensitive to the concentration difference. Thus, the team tried to find a biasing gate voltage which concentration difference can induce more  $I_D$  change.

We also want to operate the nanowire under the condition that the device has higher sensitivity. Differently, we suppose that one should find the appropriate operation region instead of a bias range for  $V_G$ . We also take noise into consideration. The comprehensive method we proposed below proves that the nanowire should be operated in the weak inversion region adjacent to the transition region.

Our method is that we choose the operation region with more “noise tolerance”. The noise tolerance is defined as below:

$$\text{For } I_{D1} > I_{D2} \quad (3.1)$$

$$\text{Noise Tolerance} = \frac{\text{Noise Margin}}{I_{D2}} \quad (3.2)$$

$$\text{Noise Margin} = (I_{D1} - S_{D1}) - (I_{D2} + S_{D2}) \quad (3.3)$$

$I_D$  and  $SD$  are the mean and standard deviation of several  $I_D$ - $V_G$  curves obtained in a same experimental condition. The larger the noise tolerance implies there is more space between two curves. And more space implies the less chance of overlapping that may happen between two concentration curves.

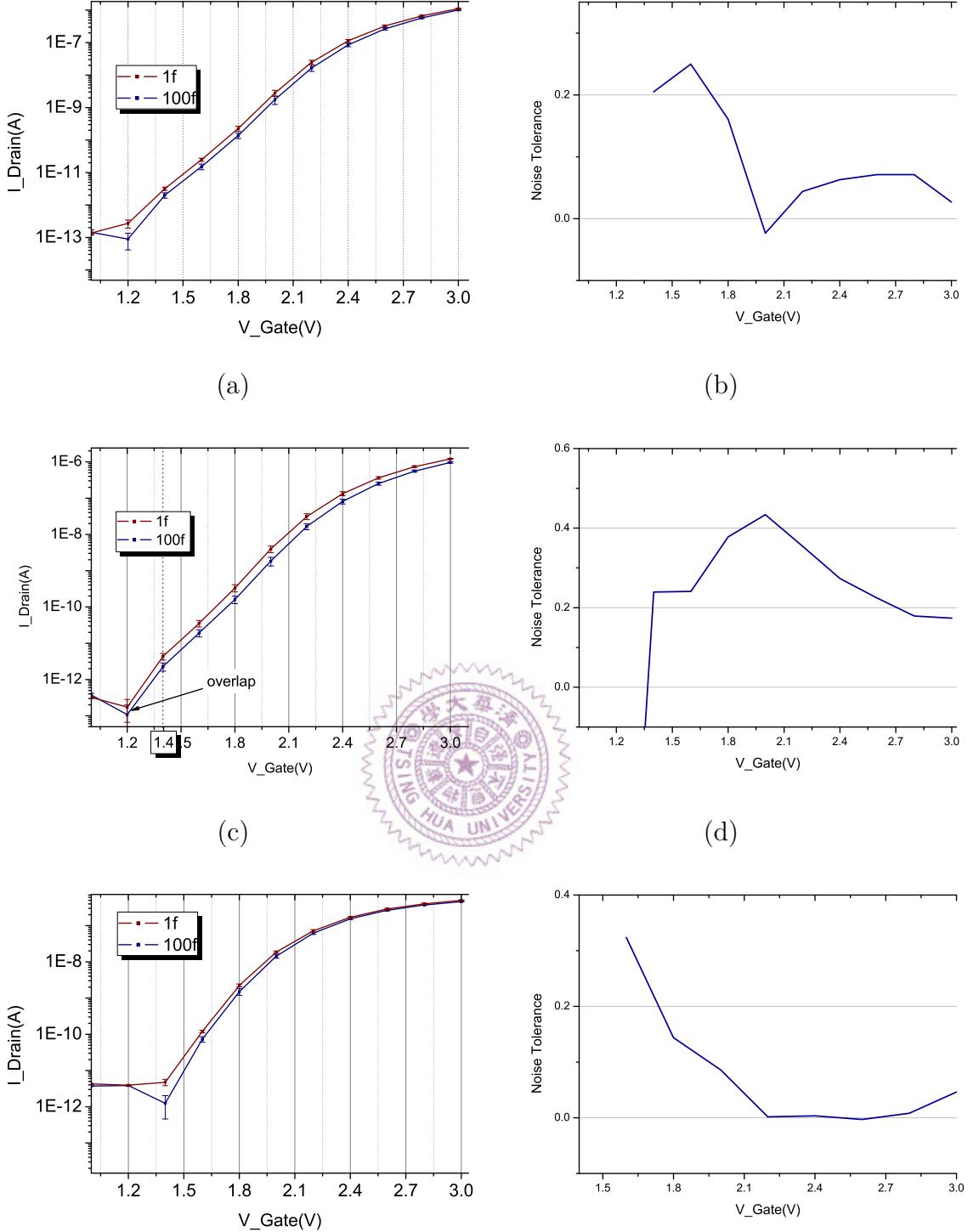
We present analysis results from three nanowire devices in Fig.3.7. Figure (a), (c), (e) are the  $I_D$ - $V_G$  curves of three devices and Fig.3.7(b), (d), (f) are the noise tolerance respectively. One can observe in (b) and (d) that there is first a rising trend then followed by a drop as gate voltage decreases. The drop does not exist in (f) may because the measurement failed before the drop appears (The failure is because the  $I_D$  is too small to be detected.). But one can still observe the rising trend. The highest points of (b) and (d) locate in the weak inversion region and is adjacent to the transition region (The region between strong inversion and weak inversion region). We therefore suggest that it is where nanowire should have better sensitivity.

### 3.2.2 $g_m$ - $I_D$ Plot

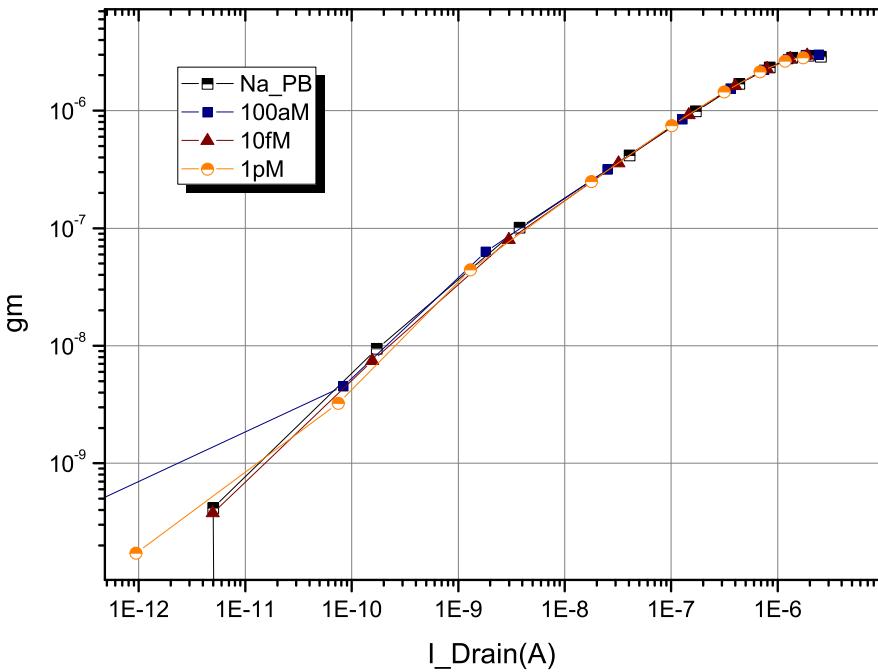
We plot the  $g_m$ - $I_D$  curves for the data in Fig.3.5. The result in Fig.3.8 clearly proves our two assumptions for dealing with the device variability problem, which we have discussed in section.2.3.

In Fig.3.8, the  $g_m$  of nanowire is almost independent of concentration and merely depends on  $I_D$  when  $I_D$  ranges from 0.1nA to 1 $\mu$ A. In fact, the curves start splitting after  $I_D > 1\mu$ A. It means the device is no longer in weak inversion region but enters strong inversion region.

With the data from Fig.3.5, we may find the equivalent voltage change induced by the concentration difference based on the assumption 2 (section.2.3). The values



**Figure 3.7:** (a), (c), (e)  $I_D$ - $V_G$  curves for three nanowire devices placed under solution with DNA concentration of 1f and 100f. (b), (d), (f) are the noise tolerance of the three devices respectively.



**Figure 3.8:** The  $g_m$ - $I_D$  curve obtained by the  $I_D$ - $V_G$  curve in Fig.3.5. The curves start splitting after  $I_D > 1\mu\text{A}$  where the device may enter into strong inversion region.

is changeable, which may depend on the gate-coupling coefficient (Eq.2.13).

Concentration Difference	Na_PB - 100aM	100aM - 10fM	10fM - 1pM
Equivalent voltage value	$30mV - 40mV$	$200mV - 280mV$	$38mV - 60mV$

**Table 3.1:** The equivalent voltage value generated by the concentration difference. They are obtained by the data from Fig.3.8. The  $I_D$  difference of different concentration is divided by their  $g_m$  ( $\Delta I_D = g_m \Delta V_G$ ).

### 3.3 Electrical Measurements

This section presents the data analysis results. The data are obtained from our measurements with the source meter (Keithley 2602). To exclude the effect of ions, we placed nanowire devices in the distilled deionized water instead of biomolecule

solution. And there is no DNA probe on the surfaces of poly-silicon channel.

### 3.3.1 Floating-gate and Back-gate

Our nanowire has two gates available: floating-gate (liquid gate) and back-gate. We choose floating-gate as the operation gate mainly because the floating-gate can induce a larger drain current. In other words, it has higher transconductance (Fig.3.9). In our circuit design, nanowire is placed in a feedback loop where its transconductance is proportional to the loop gain (chapter 5).

There are some advantages of back-gate. One of them is the ability to lower the  $1/f$  noise [17, 18]. But this only holds for a very high gate voltage, which is not practical in the integrated circuit design.

### 3.3.2 Transconductance

The most crucial parameter for our circuit design is the transconductance ( $g_m$ ). It is acquired by calculating the partial derivative of  $I_D$  with respect to  $V_G$ . Since in section.2.3.1 we proved that  $g_m$  is dependent on  $I_D$ , we plot the  $g_m$ - $I_D$  curve to reveal their relation (Fig.3.10(b)).

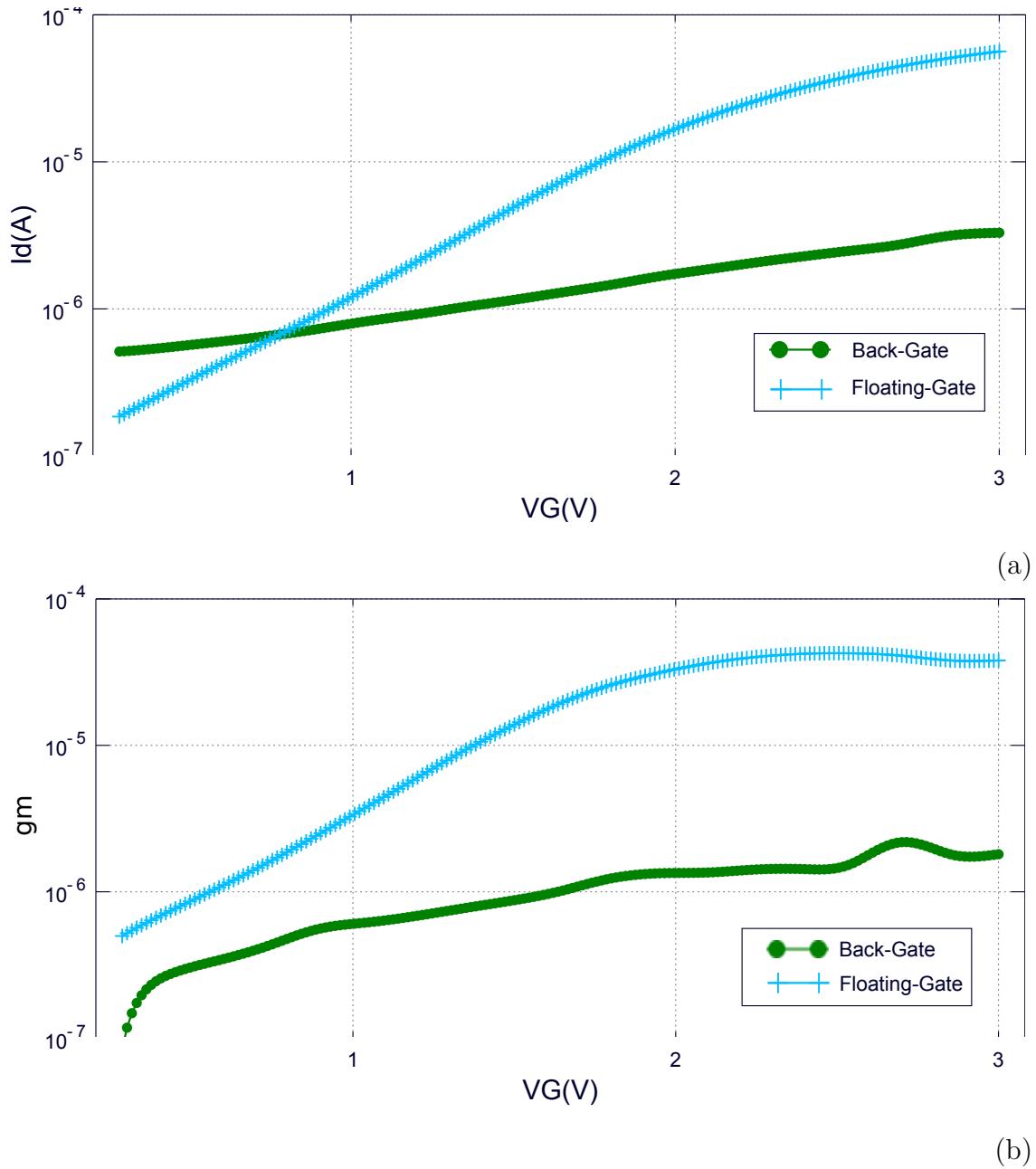
The  $g_m$ - $I_D$  plot indicates that there is a “linear region” where  $g_m$  is proportional to  $I_D$ . This corresponds to our derivation in Eq.(2.17). It can be recognized that our nanowire device is operated in weak inversion region when  $I_D$  is less than  $10\mu A$ . Therefore, by the section.3.2.1, we decide the  $I_D$  of our nanowire should be operated below  $10\mu A$ .

We also proved that the transconductance under this region is unaffected by  $V_{DS}$ .

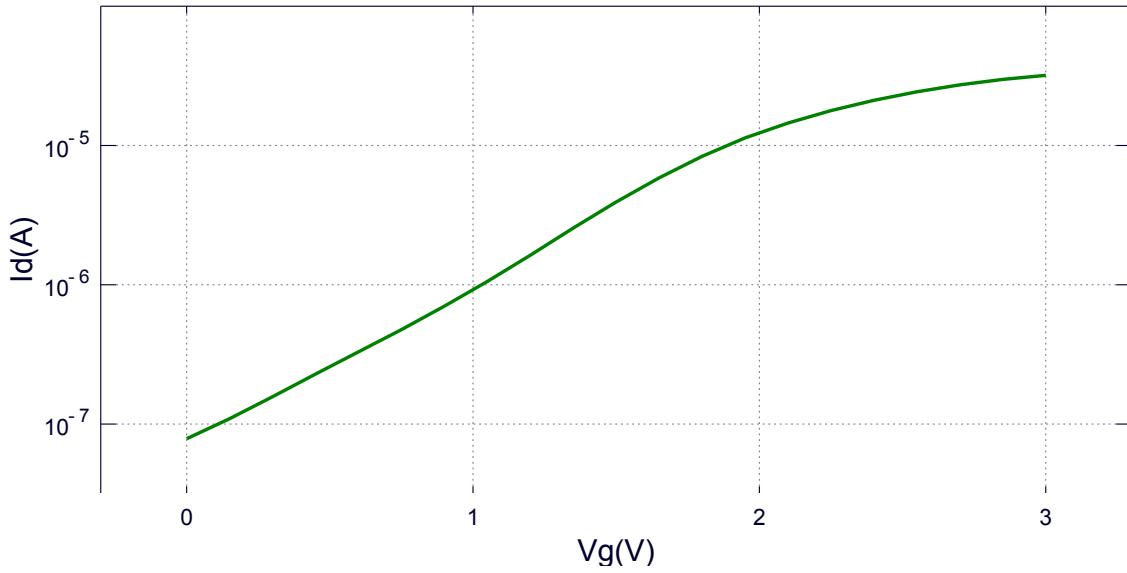
### 3.3.3 Drain-to-source impedance ( $r_{ds}$ )

In our circuit design,  $V_{DS}$  is kept constant. According to the measurement data from Fig.3.11,  $V_{DS}$  of  $0.7V$  is enough to keep nanowire in saturation region for  $V_G$  ranging from  $0v$  to  $3v$ .

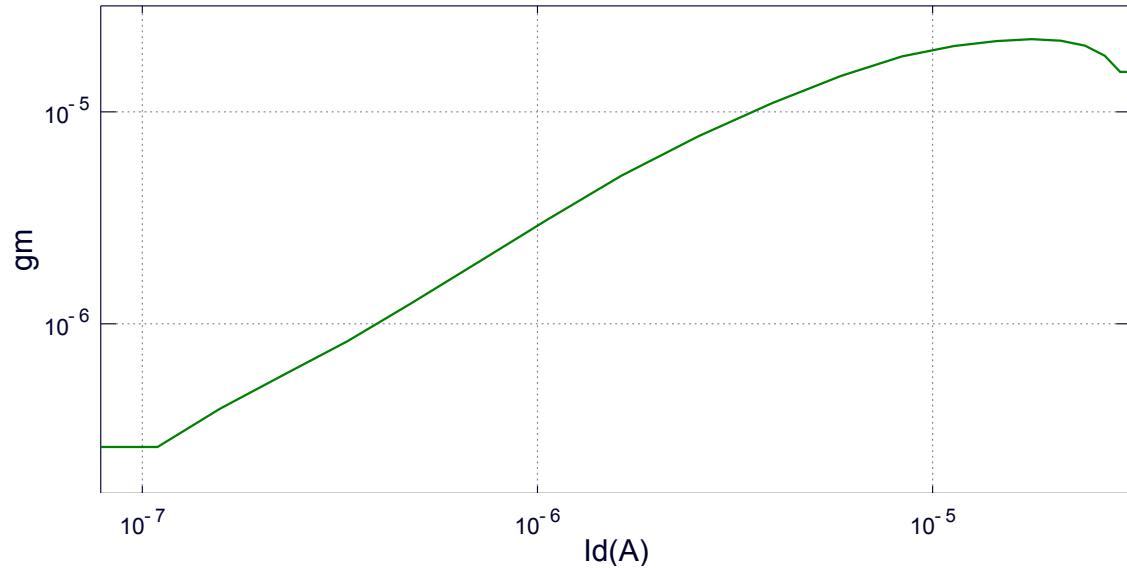
We concern about how  $I_D$  effect  $r_{ds}$ . The way we obtained  $r_{ds}$  is as follows:



**Figure 3.9:** Comparison between the DC sweep of voltage on the floating gate and back-gate. (a)  $I_D$ . (b) Transconductance ( $g_m$ ). The  $I_D$  and  $g_m$  of the floating gate are larger than the back-gate.

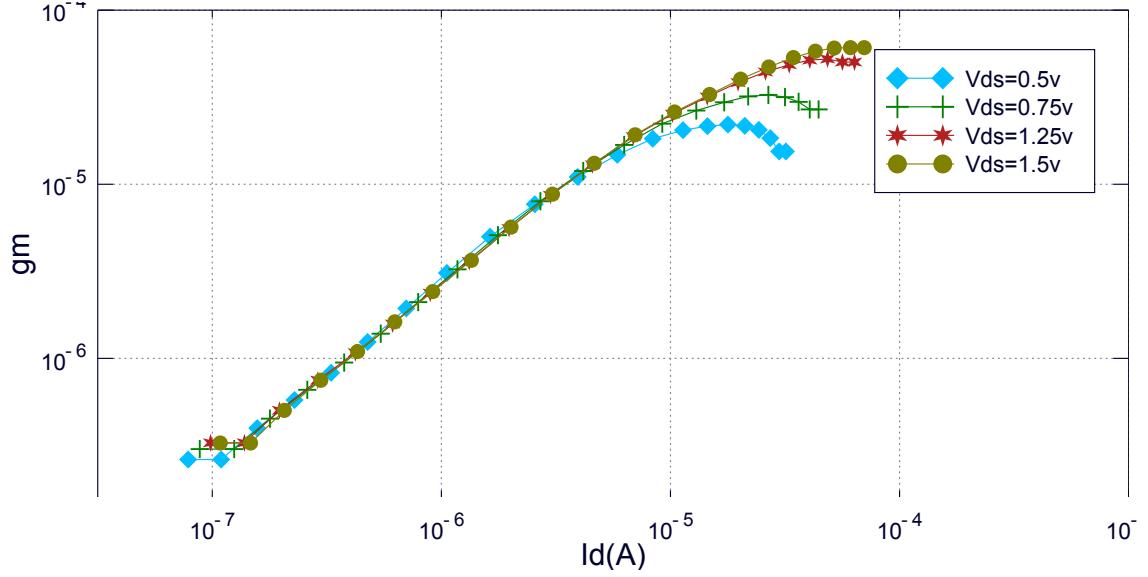


(a)



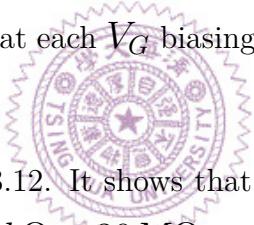
(b)

**Figure 3.10:** Electrical response of a nanowire device. **(a)** Sweep  $V_G$  and measure the  $I_D$  changes. By finding  $g_m(\frac{\partial I_D}{\partial V_G})$ , **(b)** the  $g_m$ - $I_D$  curve is plotted.



**Figure 3.11:**  $gm$ - $I_D$  curves with  $V_{DS}$  variance

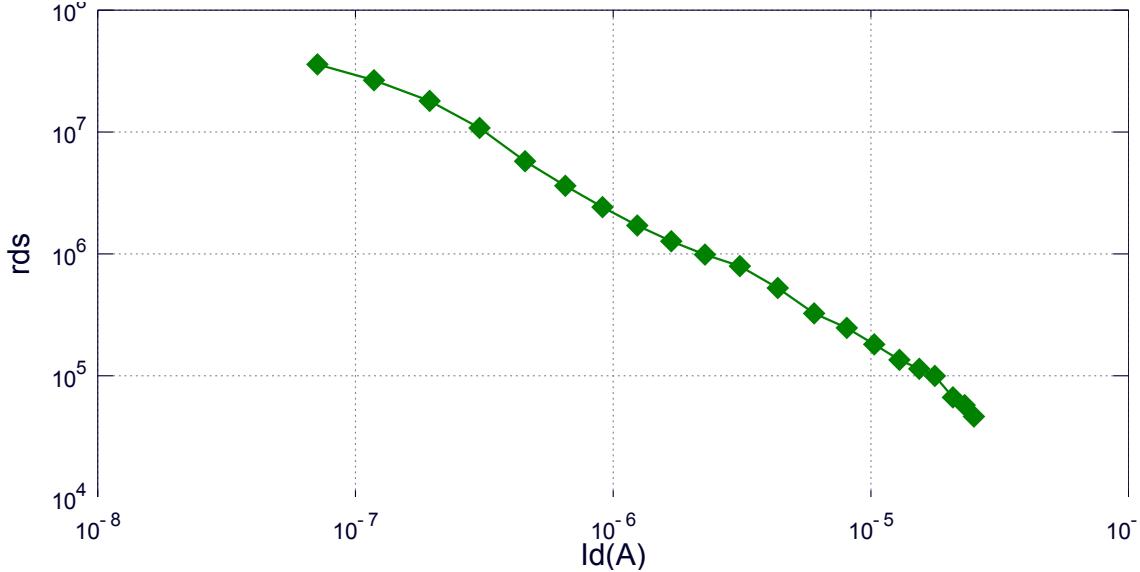
1. Perform  $I_D$ - $V_G$  sweep with two different  $V_D$ . We picked  $V_D$  values of 0.75V and 1V.
2. Find the difference of  $I_D$  at each  $V_G$  biasing point and divide it by the difference of  $V_D$ .



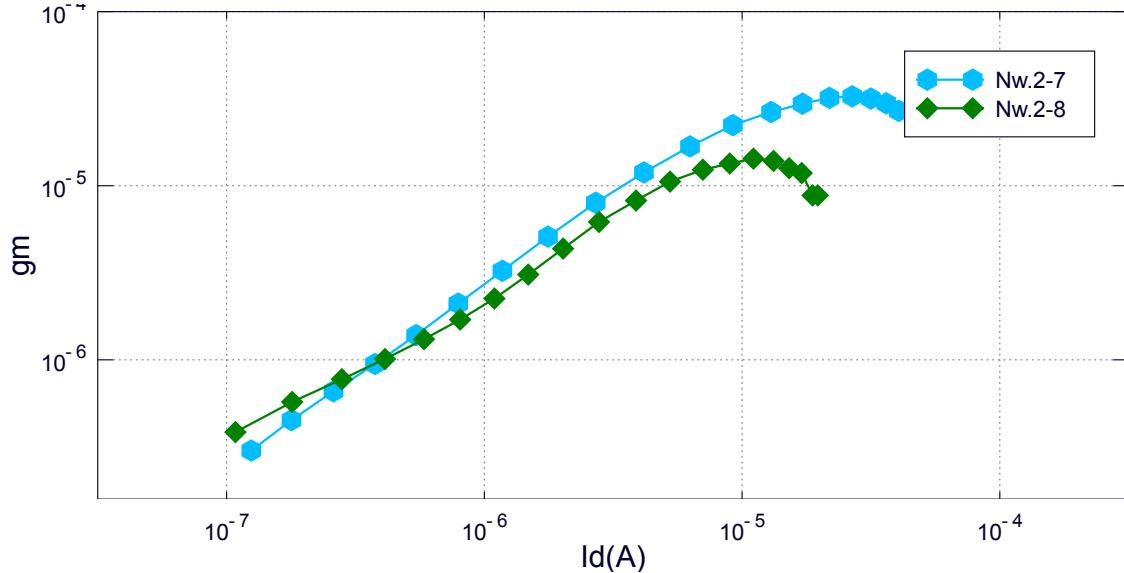
The result is presented in Fig.3.12. It shows that the  $r_{ds}$  is inversely proportional to  $I_D$ . Its value ranges from  $40k\Omega$  to  $30M\Omega$ . This result becomes useful when we perform the analysis of impedance matching in chapter 5.

### 3.3.4 Device variability Problem exists

We measured two nanowire devices which lie on the same wafer and are immersed with the same testing PBS solution. Below, the  $g_m$ - $I_D$  plot (Fig.3.13) shows that even the environment is same, two devices exhibit different electrical responses. This problem causes issues such as non-uniform specification for measurement or bad quality assurance in a mass production. We try to diminish it by performing the variability-resisting measurement, which have been mentioned in chapter 1.



**Figure 3.12:**  $I_D$ - $r_{ds}$  plot



**Figure 3.13:** Device variability problem cause nanowire devices with same environment can exhibit different electrical responses.

### 3.4 Conclusion and Design Specification

Table.3.2 summarizes the electrical characteristics of our nanowire.

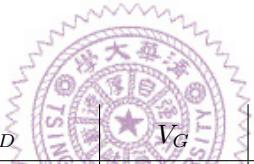
We hence decide the design specification for DC-sweep mode as Table.3.3.

As for Transient Measurement mode, section.3.2.1 suggests that the device should be operated in the weak inversion region adjacent to the strong inversion region. And Table.3.1 indicates that the voltage change ( $\Delta V_G$ ) induced by concentration

difference ranges from  $20mV$  to  $280mV$ . These factors give result to the table of device characteristics for transient measurement (Table.3.4).

The design specification for Transient Measurement mode is presented in Table.3.5.  $\Delta I_D$  is the multiplication of  $\Delta V_G$  and  $g_m$  from Table.3.4. The limitation of input referred noise (referred to the gate) is 10% of the minimal  $\Delta V_G$  ( $20mV \times 10\% = 2mV$ ) or 10% of the minimal  $\Delta I_D$  ( $1\mu A \times 20mV \times 10\% = 2nA$ )

. The transimpedance (input current to output voltage) is  $5M\Omega$ . This is because the minimal  $\Delta I_D$  is  $20nA$  and a transimpedance of  $5M\Omega$  allows the output voltage to be larger than  $0.1V$ . The bandwidth is  $1k$  Hz. The input signal  $\Delta I_D$  is a very slow signal with the speed less than  $10$  Hz. However, we implement a modulation method in chapter 5, which resembles the method adopted by [9]. The input signal is modulated to a higher frequency to avoid the low frequency noise. Thus, we determined that the bandwidth of the circuit should be at least  $1k$  Hz.



Operation Region	$I_D$	$V_G$	$g_m$	$r_{ds}$
Cut off	$< 100nA$	$< 0V$	-	-
weak inversion	$100nA - 10\mu A$	$0V - 2.5V$	$200n - 20\mu$	$50M\Omega - 200k\Omega$
strong inversion	$> 1\mu A$	$> 2.2V$	$20\mu - 30\mu$	$< 200k\Omega$

**Table 3.2:** Electrical characteristics. There are overlaps due to the device variability

$I_D$	$g_m$	$V_G$
$100nA - 30\mu A$	$200n - 20\mu$	$0.5V - 3V$

**Table 3.3:** Specification for DC-sweep mode

$I_D$	$g_m$	$\Delta V_G$
$600nA - 10\mu A$	$1\mu - 20\mu$	$20mV - 280mV$

**Table 3.4:** The summation of the nanowire characteristics when applied with Transient Measurement mode circuit

$\Delta I_D$	Input Referred Noise (referred to $V_G$ )	Input Referred Noise (referred to $I_D$ )	Transimpedance Gain (max)	Bandwidth
$20nA - 2.8\mu A$	$< 2mV$	$< 2nA$	$5E6(\frac{V}{A})$	$> 1k$ (Hz)

**Table 3.5:** Specification for Transient Measurement mode circuit

# Chapter 4

## Discrete Circuitry Design

This chapter contains the discrete circuit which has been briefly reviewed in section 2.1.2. We built this circuit to apply the constant-current constant-voltage ( $V_{DS}$ ) method to our nanowire device.

### 4.1 Transforming the design from p-type measuring into n-type measuring

In [4], the circuit is for p-type ISFET device (Fig.4.1). Our nanowire device is n-type. Hence we transformed the circuit into the one in Fig.4.2.

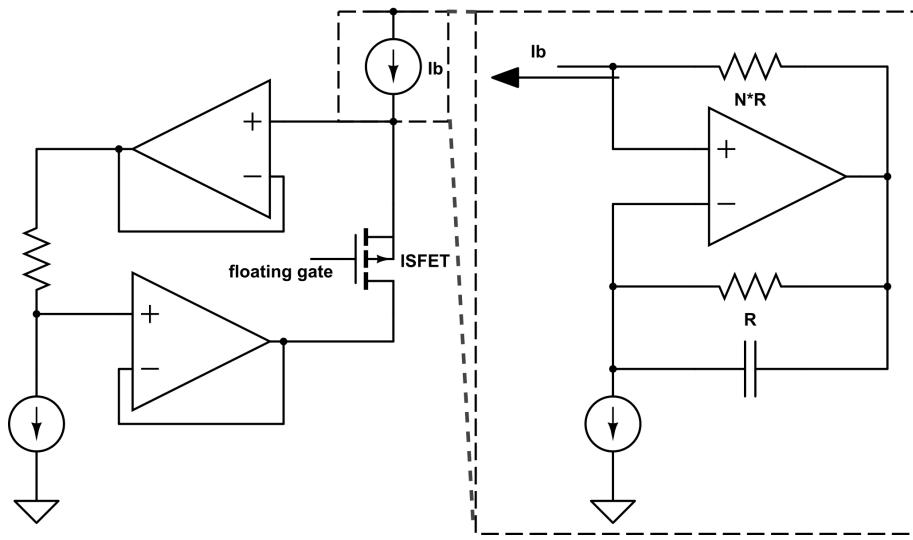
### 4.2 Circuit Description

The circuit is divided into two sections: the constant-voltage circuit and the constant-current source ( $I_b$ ).

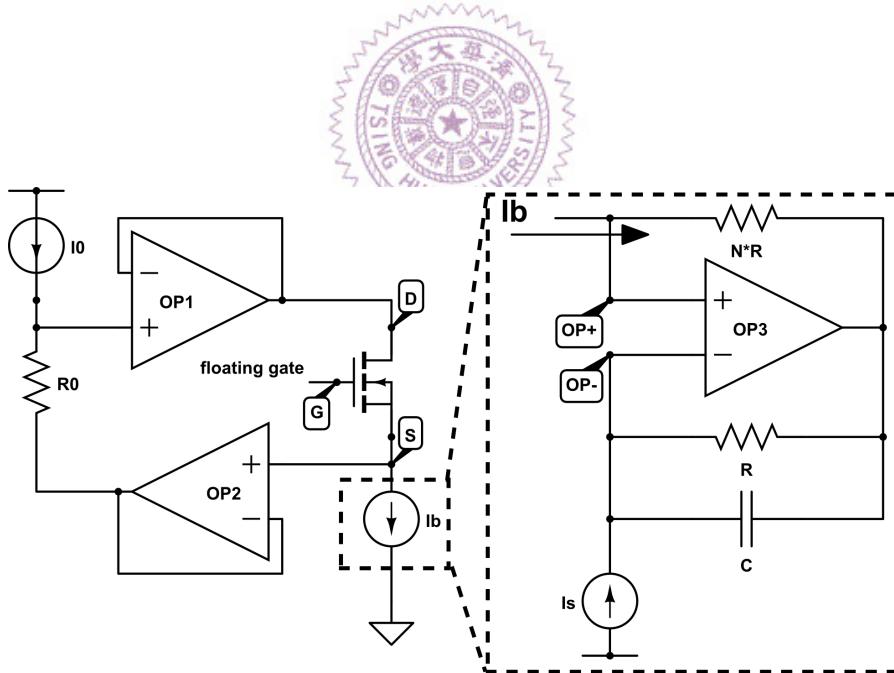
#### The constant-voltage circuit

The constant-voltage circuit section has a source follower structure. The input of the circuit is at the floating gate ( $G$ ) of the device under test (DUT), where the output is at its source ( $S$ ).

The  $I_D$  of DUT is controlled by  $I_b$ . Because the leakage current flowing into the negative input of OP2 is less than 0.1nA, the  $I_D$  of the transistor should always be



**Figure 4.1:** The schematic of read-out circuit from [4]. The ISFET is a p-type device. It is controlled by the current source  $I_b$  whose sub-circuit is shown at right.



**Figure 4.2:** Our circuit schematic transformed from Fig. 4.1. The device under test (DUT) is a n-type device. It is controlled by the current source  $I_b$  whose sub-circuit is shown at right.

same as the current provided by Ib.

The  $V_{DS}$  of DUT is always equal to the potential difference ( $I_0 \times R_0$ ) across the resistor  $R_0$ . This is achieved by two OP-based, unity-gain buffer. They connected serially with  $R_b$  and cause the voltage at the drain ( $D$ ) to follow the voltage at the source ( $S$ ).

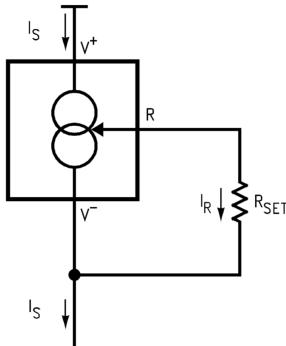
### The constant-current source (Ib)

The Ib circuit is in fact a current scaling down circuit. By concerning the OP as ideal, the node  $OP+$  has the same voltage as  $OP-$ . This equalizes the potential difference between two resistors whose resistance are different by  $N$ -fold. As a result, the currents  $I_b$  and  $I_s$  are also different by  $N$ -fold.  $I_b = I_s/N$ .

The capacitor is for filtering. It filters the high frequency noise out to create a stable output current.

### 4.3 Discrete Element

We use tlc2264 made by Texas Instrument (TI) as our OP. This OP requires a supply voltage of  $\pm 5v$  and can perform rail-to-rail output operation. Its open-loop gain (Large-signal differential voltage amplification rate) is 170 for the output load greater than 50k.



**Figure 4.3:** LM334: The discrete element we use for current source  $I_s$ . It has three terminals:  $R$ ,  $V_+$ ,  $V_-$ . The output current ( $I_s$ ) flows from  $V_+$  to  $V_-$ . The resistor  $R_{SET}$  connected to  $V_-$  and  $R$  is for adjusting the output current.

For the current source  $I_s$  and  $I_0$ , we use lm334 (Fig.4.3) made by National Semiconductor. It is a 3-terminal adjustable current sources with a wide dynamic cross voltage range of 1v to 40v (the cross voltage  $V_+ - V_-$  in Fig.4.3), and current accuracy of  $\pm 3\%$ . In our experiment, the current  $I_s$  is fixed at  $1\mu A$  with an output impedance of  $1.2G\Omega$ .

## 4.4 Circuit Performance and Conclusion

We examined the performance of our circuit by plotting its  $I_D$ - $V_G$  curve. The  $I_0$ ,  $R_0$  and  $V_G$  were kept constant. We swept  $I_D$  by changing the  $N$  value with a variable resistor.  $N$  ranges from 1 to 1000. And  $I_b$  should range from  $1\mu A$  to  $1nA$ .

We measured the output voltage at  $S$  and subtracted this value from  $V_G$  to get the corresponding  $V_{GS}$ . These two values gave the  $I_D$ - $V_{GS}$  curve in Fig.4.4. We compare this curve with the curve obtained by directly sweeping  $V_G$  and measuring  $I_D$  with Source Meter (Keithley 2602).

The result shows that when  $I_D$  is larger than  $10nA$ , the circuit is functional. Two curves are same as each other.

The circuit fails when  $I_D$  is smaller than  $10nA$ . This is related to the impedance matching between the constant-voltage circuit and the Ib circuit, which we have discussed in section.2.1.2.

The output impedance of the Ib circuit is:

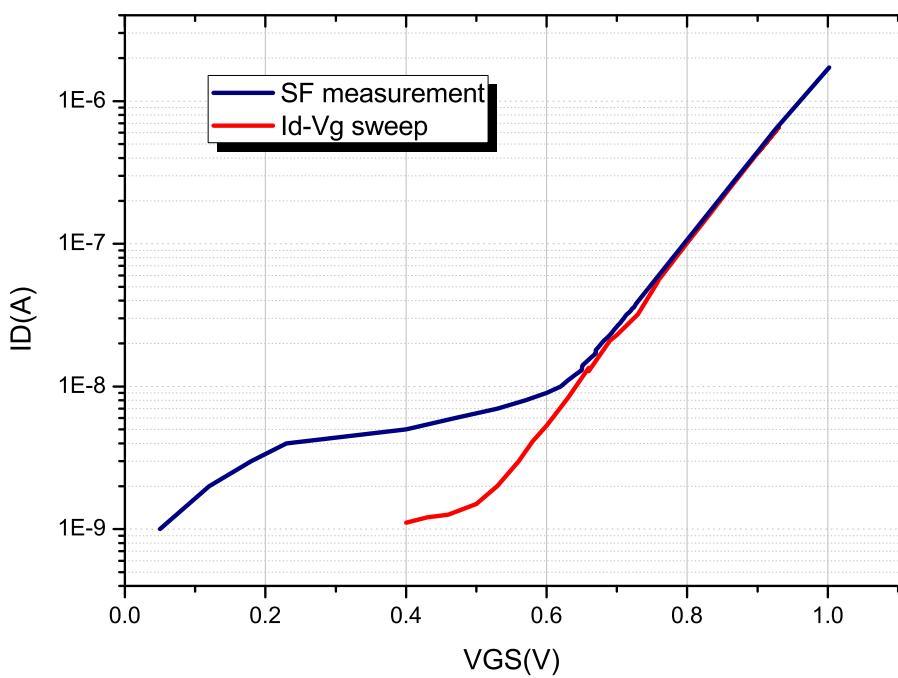
$$N \times R_s \quad (4.1)$$

$R_s$  is the output impedance of the current source  $I_s$  which equals to  $1.2G\Omega$ . And the current input impedance at the  $S$  of the constant-voltage circuit is:

$$\frac{1}{g_m} \quad (4.2)$$

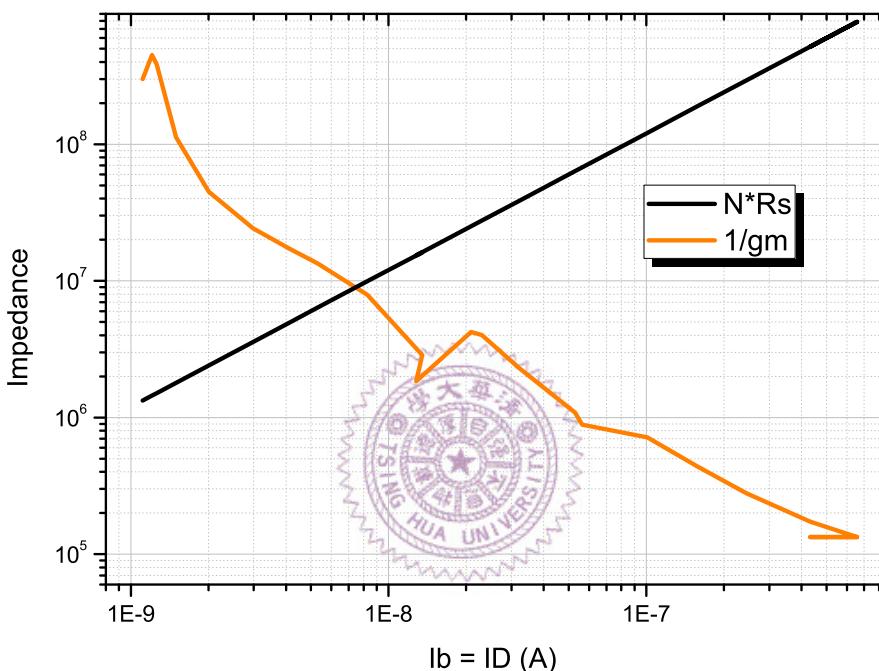
We plot the  $I_b$ -Impedance relationship in Fig.4.5.

It shows that the output impedance of Ib is close to the input impedance of transistor when current is  $10nA$  ( $N = 100$ ). The impedance is unmatched.



**Figure 4.4:** The measurement result (“SF measurement”) compares with the direct  $I_D$ - $V_G$  sweep (“Id-Vg sweep”).

Overall, the constant-current constant-voltage method is feasible. What one needs to notice when applying this method is the impedance matching. In the source follower structure, its current input impedance varies with the bias current. It affects the dynamic range and needs more design concern.



**Figure 4.5:** Input impedance of transistor (“ $1/gm$ ”) and output impedance of  $I_b$  circuit (“ $N * R_s$ ”). The former is found by the derivative of  $I_D$  of  $V_{Gs}$ . The latter is obtained by Eq.4.1.

# Chapter 5

## Integrated Circuitry Design

This chapter presents the design of the read-out circuit and the post-simulation results.

### 5.1 Fronted Circuit Design

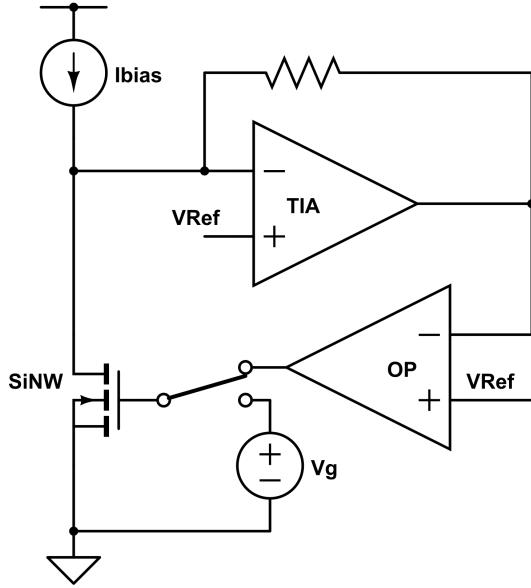
The review of the source follower in section.2.1.2 suggests the constant current method for the circuit of DC-sweep mode. The data analysis from chapter 3 supports it by the linear relation between  $I_D$  and  $g_m$ . However, section.2.2 shows that source follower is not suitable for transient measurement. It alternatively recommends the circuit in Fig.2.6 which measures the transient current signal and converts it into a voltage output.

The fronted circuit combined these two methods into one circuit structure with two modes available: DC-sweep mode and Transient Measurement mode.

#### 5.1.1 The Circuit of DC-sweep mode

Fig.5.1 is the fronted circuit operated in DC-sweep mode. The switch turns the circuit into DC-sweep mode by connecting the output of OP with the gate of nanowire.

As in the source follower, our circuit contains a biasing current source (Ibias) for controlling the  $I_D$ . The difference is that the Ibias inputs the current into drain instead of source. In addition, we employs the transimpedance amplifier (TIA) from section.2.2 ([9]). Its output is connected to an OP amplifier to form a negative



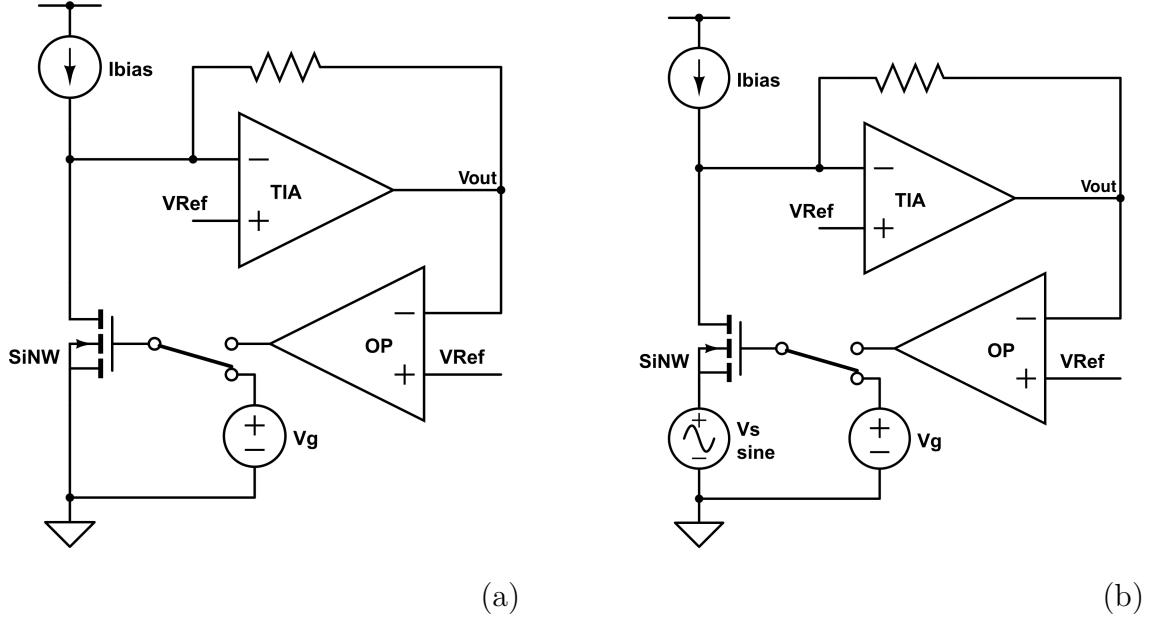
**Figure 5.1:** The fronted circuit operated in DC-sweep mode.

feedback loop. When  $I_D$  is less than Ibias, the output voltage of TIA falls and the gate voltage  $V_G$  rises to increase  $I_D$ . On the contrary, output voltage of TIA rises and the gate voltage ( $V_G$ ) drops if Ibias is smaller than  $I_D$ . Finally, the feedback mechanism forces  $I_D$  to be the same as Ibias by adjusting  $V_G$  automatically.

### 5.1.2 The Circuit and Usage of Transient Measurement mode

In Fig.5.2(a), the switch turns to a simple voltage source ( $V_g$ ) that provides a constant gate voltage. The feedback OP is nonfunctional in this mode. When performing measurement, we directly find how the output voltage ( $V_{out}$ ) changes with the biomolecule concentration. This output voltage will be sent into a second stage circuit for further amplification.

**Another Usage of Transient Measurement mode** There is another method to perform measurement with Transient Measurement mode, which resembles the measurement in [9]. This method measures the  $g_m$  of the nanowire. As shown in Fig.5.2(b), a sinusoidal signal with an amplitude of  $v_s$  is sent to the source of the nanowire. The output response ( $V_{out}$ ) is a sinusoidal signal at the same frequency with an amplitude equaling to  $v_s g_m \times R_{TIA}$ . The values of Ibias and Vg can be



**Figure 5.2:** Two usage ((a), (b)) of the fronted circuit operated in Transient Measurement mode.

arbitrary. But one need to be aware that their values should not cause the output of TIA or the second-stage circuit to saturate.

### 5.1.3 The Variability-resisting method

As mentioned in chapter 1, we combine DC-sweep mode and Transient Measurement mode to implement the variability-resisting measurement method.

**Method Procedure** Assuming there are two nanowire devices and the device variability problem exists between them. Initially, we use these element to perform the  $I_D-V_G$  sweep in DC-sweep mode. We use the  $I_D-V_G$  curve to find the  $g_m$  of each device. ( $g_m = \frac{\partial I_D}{\partial V_G}$ ) When we turns to Transient Measurement mode, we bias these two devices under the same  $g_m$  by setting Ibias and Vg correspondingly. After the buffer solutions, the same voltage difference at the output ( $V_{out}$ ) should be detected because the two devices have the same  $g_m$ . Before a new solution is added, we return to DC-sweep mode again. This is for finding the new biasing  $V_G$  to reset their  $I_D$  to be the same as Ibias. This implies that every time when we enter Transient Measurement mode, the devices always have the same  $I_D$  and  $g_m$ .

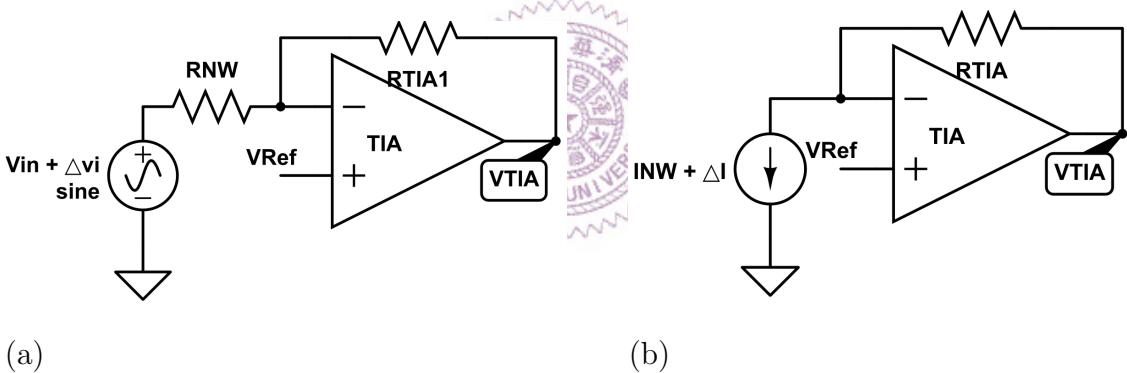
as those in the beginning of experiments.

### 5.1.4 Design Description

In this section, we first talk about TIA block and focus on how we improve the detecting limits of this block. It is followed by the design of the TIA circuit. Then we analyze the feedback mechanism of DC-sweep mode and the input impedance of the circuit. After that, we discuss the stability issue. Finally, we show the design of the feedback OP block.

#### 5.1.4.1 Strategies for lowering current detecting limits

The TIA subcircuit in section.2.2.3 is shown as Fig.5.3(a), we mentioned that the detecting range of  $R_{NW}$  is limited by  $I_{NW}$  provided by TIA. We now discuss the causes of the upper and lower limits, and show the strategies we use to improve them.



**Figure 5.3:** (a) The transimpedance block (TIA) of the read-out circuit from [9]. The circuit input a voltage signal into resistive nanowire element  $R_{NW}$ . To compare it with our circuit (Fig.5.4), we transform the voltage input into an equivalent current input in (b). The  $I_{NW} = (V_{Ref} - V_{in})/R_{NW}$  and  $\Delta i = \Delta vi/R_{NW}$

**Lower Limit:** In Fig.5.3(b), the TIA output voltage is:

$$V_{TIA} = V_{Ref} + I_{NW}R_{TIA} + \Delta iR_{TIA} \quad (5.1)$$

Two reasons relate to a large offset current  $I_{NW}$ . One is that the output current provided by TIA is restricted by design. The other is that the restriction of the

current flowing through the resistor  $R_{TIA}$ :

$$\frac{V_{Ref} - VSS}{R_{TIA}} < I_{NW} < \frac{VDD - V_{Ref}}{R_{TIA}} \quad (5.2)$$

Both reasons lead to the output saturation of TIA.

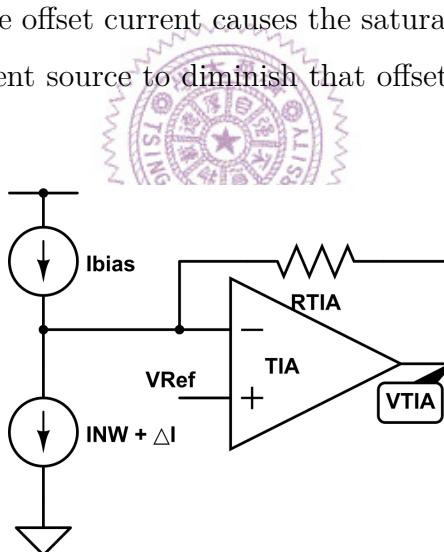
A naive way to handle the first one is to increase the maximal output current that TIA can provide. The disadvantage of this method is the increase in power consumption and chip area. As for the second one, using smaller  $R_{TIA}$  can release the restriction on  $I_{NW}$ . Unfortunately, this is not preferred because it reduces the current-to-voltage gain of TIA.

Our strategy for decreasing the lower limit is to utilize the biasing current source ( $I_{bias}$ ) of nanowire. As shown in Fig.5.4, Eq.(5.1) is transformed into:

$$V_{TIA} = V_{Ref} + (I_{NW} - I_{bias})R_{TIA} + \Delta i R_{TIA} \quad (5.3)$$

Now we can diminish the large  $I_{NW}$  by  $I_{bias}$ .

In conclusion, the large offset current causes the saturation of the output of TIA. We use the biasing current source to diminish that offset current, so as to increase the detection range.



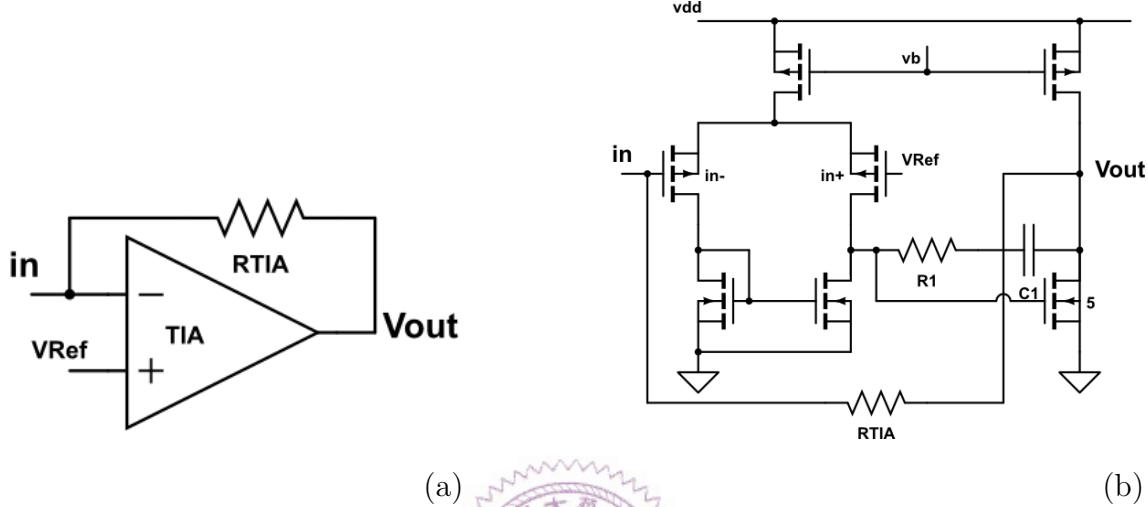
**Figure 5.4**

**Upper Limit:** The upper limit depends on the output resolution. When the input current signal  $\Delta I$  in Fig.5.4 is too small, the output response may be defeated by the noise. This may be solved by increasing the SNR through a larger  $R_{TIA}$ . However, the chip area constrains the size of resistors. In our circuit design, it is hard to make a wide linear range resistor with resistance value out of  $100k\Omega$ . Furthermore, even

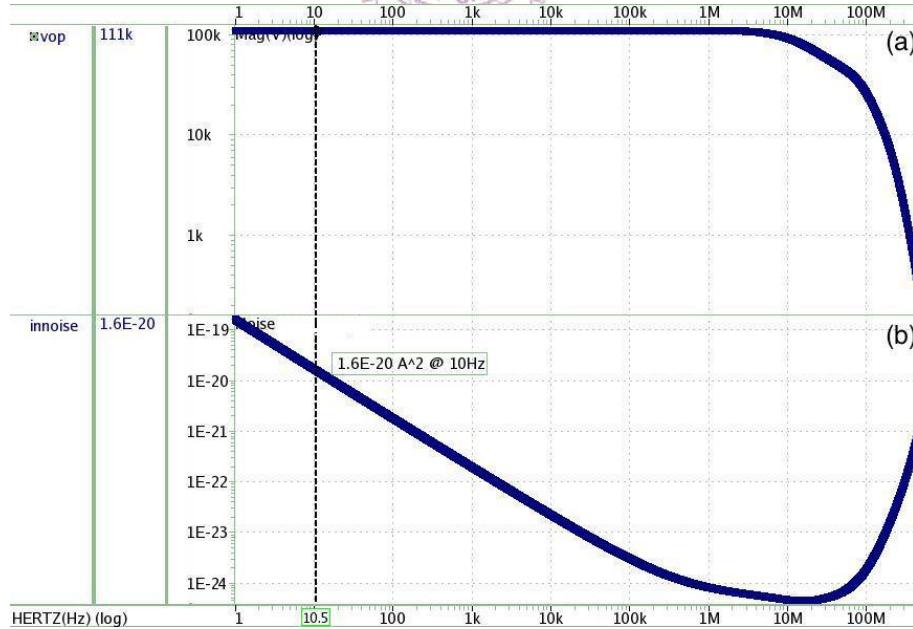
if the resistor can be greater, one needs to concern for the noise brought by the large resistance.

Our strategy is to reduce the noise of TIA by designing its input MOSFETs with a large area. We also amplify the output signal through the second-stage circuit.

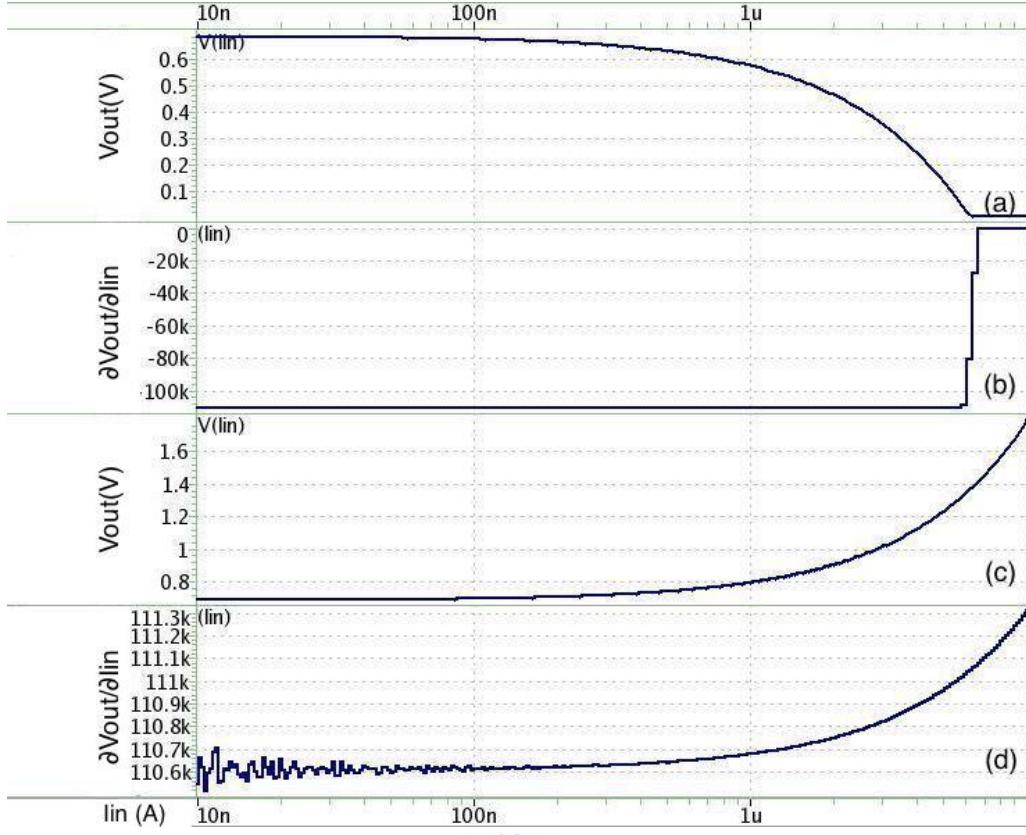
#### 5.1.4.2 TIA (Transimpedance Amplifier) Design



**Figure 5.5:** (a) The transimpedance block and the (b) schematic



**Figure 5.6:** The ac simulation results of TIA. The x-axis is the input signal frequency. (a) is the  $V_{out}$  and (b) is the input-referred noise ( $A2$ ).



**Figure 5.7:** The dc simulation results of TIA. The x-axis represents positive/negative input current (log scale). (a) is the  $V_{out}$  responding to the positive input current while (c) is to the negative input current. (b) and (d) are the derivative of  $V_{out}$  of input current ( $\frac{\partial V_{out}}{\partial I_{in}}$ ) from (a) and (c) respectively.

Fig.5.5 shows the Transimpedance Amplifier circuit. We implement the operational amplifier in TIA with the two-stage, differential-pair structure. This simple structure has merits such as large output current and wide output voltage range.

Fig.5.6 and Fig.5.7 are the ac and dc post-simulation of TIA. Fig.5.6(a) indicates that the bandwidth is  $7MHz$ . Fig.5.6(b) is the input referred noise. Fig.5.7 shows that TIA has a constant transimpedance of  $100k\Omega$  when the input current range is  $6\mu A \sim -10\mu A$ . In Table.5.1, these three parameters are compared with the specification given by Table.3.5. Other results such as biasing current, spec. of OP ... etc. are also provided in it.

VDD	3.3V	
Biasing Current	$35\mu A$	
Transimpedance	$100k(\frac{V}{I})$	
Closed loop		
	Post-simulation	Spec. from Table.3.5
Input Current range	from $6\mu A$ to $-10\mu A$	$\pm 20nA - 2.8\mu A$
Output Voltage range	$0.1V - 2.8V$	-
Bandwidth	7M Hz	1k Hz
Input referred noise (@10Hz)	$0.13nA$	$< 2nA$
Open loop		
Output dynamic range	$0.1V - 3.1V$	
Phase Margin	103 (degree)	
PSRR	$60dB$	
CMRR	$123dB$	
ICMR	$0.1V - 2.6V$	

**Table 5.1:** Post-simulation result of TIA

#### 5.1.4.3 Feedback Mechanism

DC-sweep mode circuit forms a negative feedback loop. Fig.5.8 is the block diagram of the circuit.

From the block diagram, we can compute the loop gain ( $LG$ ) and the transfer function ( $TF$ ):

$$R_A = R_{TIA} \times A_{OP} \quad (5.4)$$

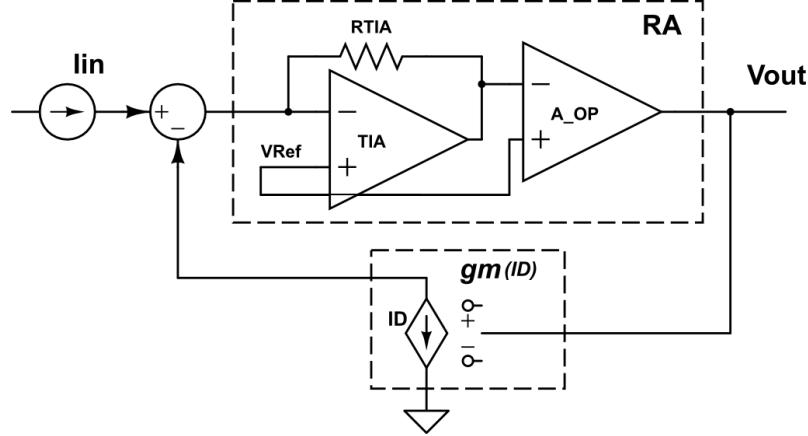
$$LG = R_A \times g_m \quad (5.5)$$

$$TF = \frac{V_{out}}{I_{in}} = \frac{R_A}{1 + LG} \quad (5.6)$$

$$\approx \frac{1}{g_m} \quad \text{If } LG \geq 100 \quad (5.7)$$

The transfer function suggests that if we want to obtain an  $I_D$ - $V_G$  sweeping curve with an error less than %1, our loop gain should be greater than 100. According to

chapter 3, the specification for  $g_m$  detection ranges from  $200n$  to  $20\mu$ . This implies that  $A_{OP}$  should be at least greater than 5k. We will show in the next section that the  $A_{OP}$  in the post-simulation is 10k.

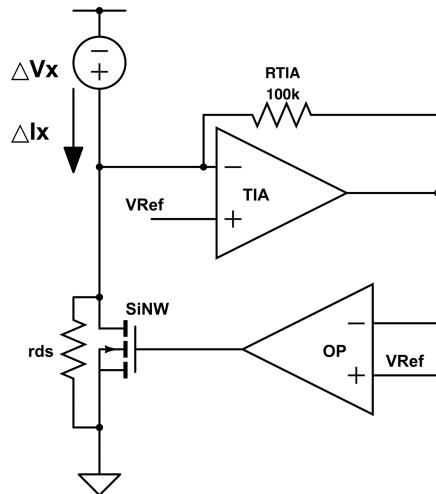


**Figure 5.8:** Block diagram of DC-sweep mode. The  $I_{in}$  refers to the Ibias and  $V_{out}$  refers to the output voltage of OP, which is also the gate voltage of nanowire (Fig.5.1). The  $gm(I_D)$  is the transconductance of nanowire whose values depends on  $I_D$ .



#### 5.1.4.4 Input Impedance (DC-sweep mode)

In chapter 4, we have discussed the impedance matching between the current source and the nanowire device. Here we compute the input impedance of the circuit.



**Figure 5.9**

In Fig.5.9, we apply an input voltage  $\Delta v_x$  and find the  $\Delta i_x$ . The input impedance of the circuit is  $\Delta v_x / \Delta i_x$ .

$$\Delta I_x = \frac{\Delta V_x}{r_{ds}} + I_{SiNW} \quad (5.8)$$

$$I_{SiNW} = \frac{\Delta V_x}{r_{ds}} LG \quad (5.9)$$

$$\rightarrow \Delta I_x = \frac{\Delta V_x}{r_{ds}} + \frac{\Delta V_x}{r_{ds}} LG \quad (5.10)$$

$$\rightarrow \frac{\Delta V_x}{\Delta I_x} = \frac{r_{ds}}{1 + LG} \quad (5.11)$$

$$\text{where } LG = R_{TIA} A_{OP} g_m \quad (5.12)$$

The  $A_{OP}$  is the gain of the feedback OP. The  $r_{ds}$  is the drain-to-source resistance of nanowire, which is larger than  $100k\Omega$ .

The LG is greater than 5k from the last section. By the section.3.3.3, the  $r_{ds}$  ranges from  $40k\Omega$  to  $30M\Omega$ . Thus, the maximal input impedance of the feedback circuit is  $6k\Omega$ . In our design, the Ibias is a simple pmos. Its output impedance ranges from  $1M\Omega$  to  $1G\Omega$ , which is much larger than the input impedance of the feedback circuit. Therefore, the impedance matching is fine.

#### 5.1.4.5 Stability and Feedback OP Design

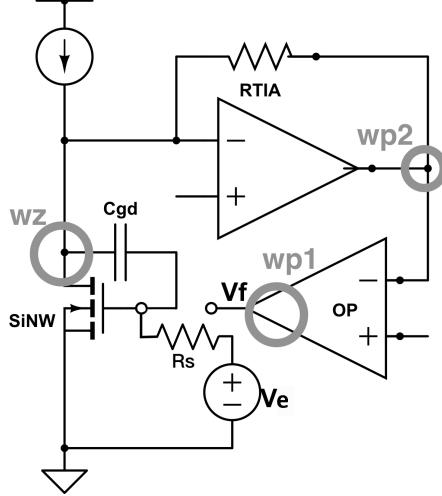
To decide the structure of the feedback OP, we must discuss the stability of the feedback loop in DC-sweep mode. The OP plays a crucial role in the stability issue because it not only decides the loop gain but also contains the dominant pole at its output.

In Fig.5.10, we mark the dominant pole ( $w_{p1}$ ), second order dominant pole ( $w_{p2}$ ) and the zero ( $w_z$ ). We can write the loop gain as:

$$\frac{v_f}{v_g} = R_{TIA} \times A_{OP} \times g_m \frac{1 - s/w_z}{(1 + s/w_{p1})(1 + s/w_{p2})} \quad (5.13)$$

$$w_z = \frac{g_m}{C_{gd}} \quad (5.14)$$

The parasitic capacitance  $C_{gd}$ , at the conservative estimate, has a maximal value of  $1pF$  (The estimation is based on the fabrication information in [15] and [3]).



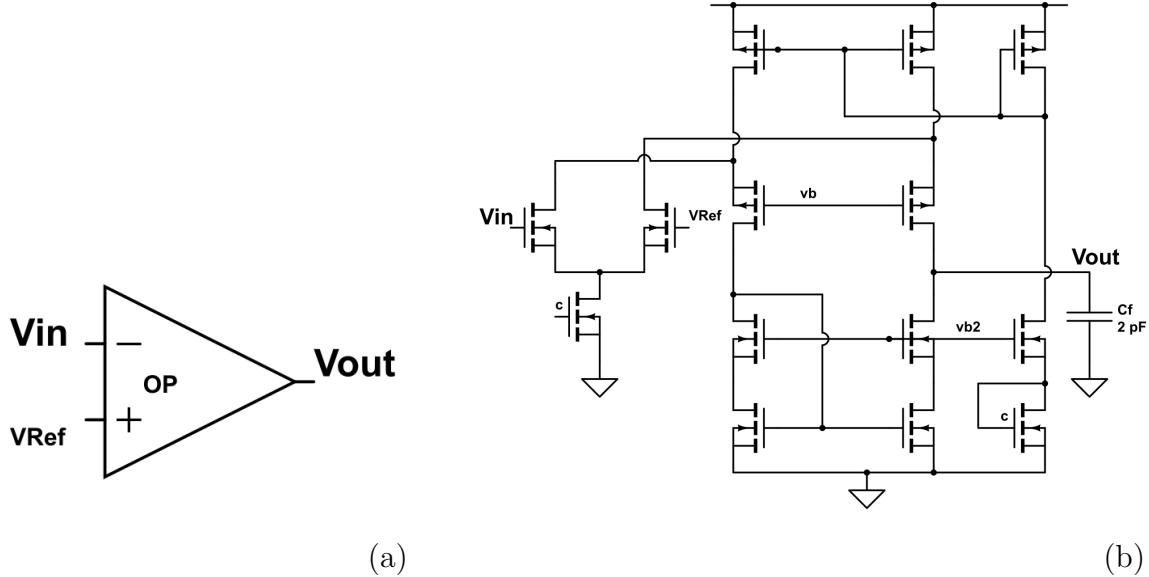
**Figure 5.10:** The illustration of the loop gain test with several poles and zero marked.

Because the lower bound of  $g_m$  in our design specification (Table.3.3) is  $200n$ , the  $w_z$  can be as small as  $20k(\text{rad/s})$ . To force the total loop gain to drop to 1 before  $s > 2k(\text{rad/s})$ , we have to reduce the first dominant pole frequency.

We choose  $w_{p1}$  as the first dominant pole. From section.5.1.4.3, we learned that the  $A_{OP}$  should be larger than  $5k$ . Thus, we choose a folded cascode structure which provides high output impedance and gain.

To be noted that the resistor  $R_s$  introduces another pole. The value of  $R_s$  is equivalent to the output impedance of the feedback OP. This pole can be dominant if its value is larger than  $100M\Omega$ . This may happen because the folded cascode structure has larger output impedance. Therefore, in the chip measurement (chapter 6), we add an external unit-gain buffer to the output of OP. This buffer reduces the  $R_s$  to about  $100\Omega$ .

We designed a folded cascode OP with a gain of  $10k$  ( $80\text{dB}$ ) and bandwidth less than  $3\text{Hz}$  (Fig.5.11, Table.5.2). A higher gain reduces the effect of fabrication variation (30% deviation of the impedance of the  $R_{TIA}$  in TIA block). The low bandwidth is owing to the large capacitance ( $C_f$ ) appended to the output. This capacitance results in a lower slew rate, which is fine because the circuit is for DC signal and there is no need for high speed operation.



**Figure 5.11:** (a)The feedback OP block and its (b) schematic

VDD	3.3V
Ibias	$35\mu A$
BandWidth	2 Hz
Max Gain	81dB
Output Dynamic Range	0.45V - 3V
PSRR	41(dB)
CMRR	126(dB)
ICMR	0.32V - 3.1V

**Table 5.2:** Post-simulation result of feedback OP

## 5.1.5 The Post-simulation Result of DC-sweep mode circuit

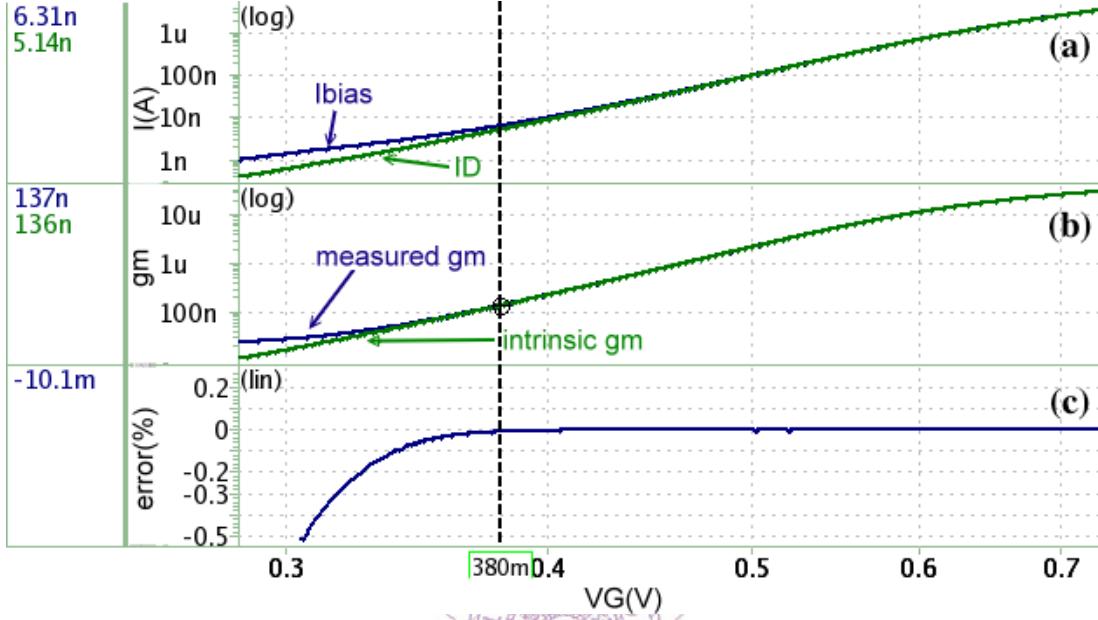
### 5.1.5.1 DC Current (Ibias) Sweep

In Fig.5.1, Ibias is swept and the output voltage of the feedback OP ( $V_G$ ) is measured. We also measured the  $I_D$  of the transistor. (Because we don't have nanowire model, we performed the simulation by using an alternative mosfet.) In Fig.5.12(a), the curve of  $I_{bias}$ - $V_G$  is compared with the curve of  $I_D$ - $V_G$ . Based on Eq.(5.7),  $\frac{\partial I_{bias}}{\partial V_G}$  is approximately equal to  $g_m$ . This is verified in Fig.5.12(b) where two  $g_m$ : the measured  $g_m$  ( $\frac{\partial I_{bias}}{\partial V_G}$ ) and the intrinsic  $g_m$  ( $\frac{\partial I_D}{\partial V_G}$ ) are plotted together. We

defined the difference between two  $g_m$  as error rate. That is:

$$error = \left| 1 - \frac{\text{measured } g_m}{\text{intrinsic } g_m} \right| (\%) \quad (5.15)$$

The error rate is showed in Fig.5.12(c) It is pointed out by the cursor that after the intrinsic  $g_m$  is less than  $130n$ , the error is over 1%.



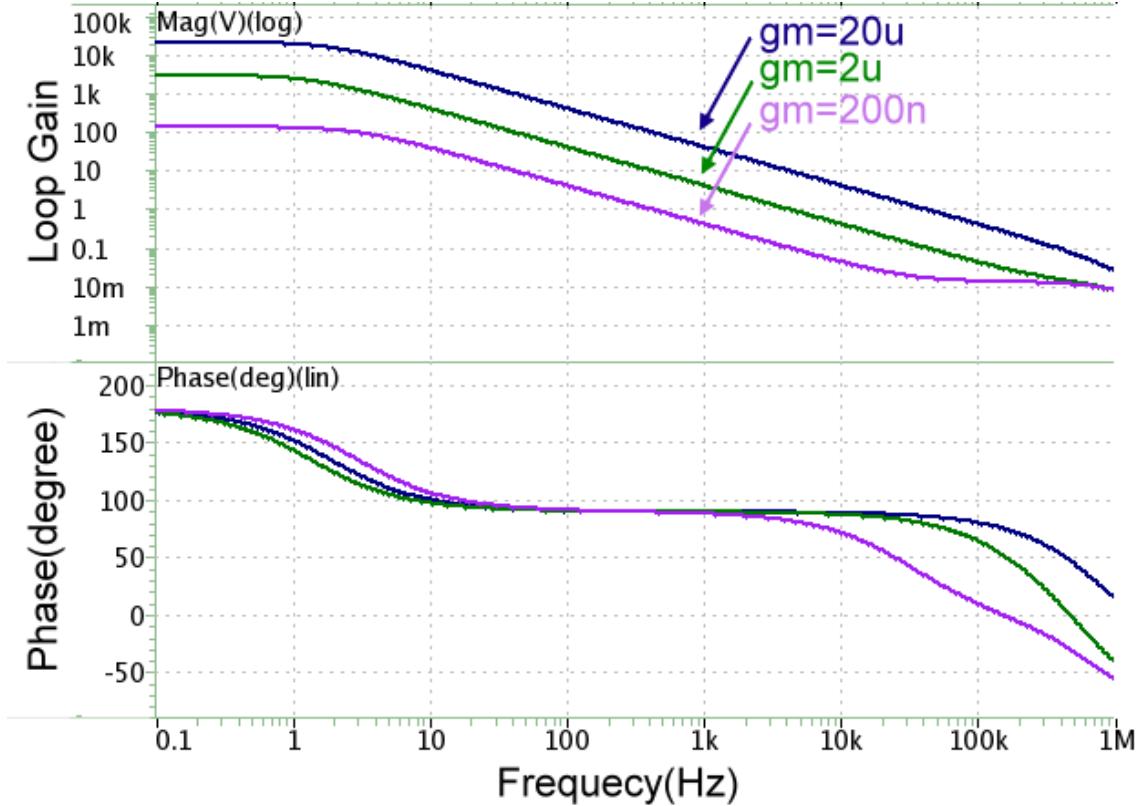
**Figure 5.12:** Post-simulation result of the dc sweep of Ibias in Fig.5.1. (a) is the  $I_D$ - $V_G$  curves of  $I_D$  and  $I_{bias}$ . (b) is the  $gm$ - $V_G$  curves of intrinsic  $g_m$  and measured  $g_m$ . (c) is the ratio of the difference between two  $g_m$  (error).

### 5.1.5.2 Bode Plot of Loop Gain and Phase

The simulation here is according to the stability section (section.5.1.4.5). We present the Bode plot of the loop gain and the phase (Fig.5.13). The summary table is also given (Table.5.3). We adjusted the transistor to the specific  $g_m$  values by selecting Ibias and corresponding  $V_G$ . We also appended a  $1pF$  capacitor to model the  $C_{gd}$ .

### 5.1.5.3 Summary

Table.5.4 compares the design specification and the simulation result. It is notable that in fact the upper limits of  $g_m$  is depends on two factors. One is the gate voltage. Table.5.2 shows that the maximal gate voltage that the Feedback OP can provides

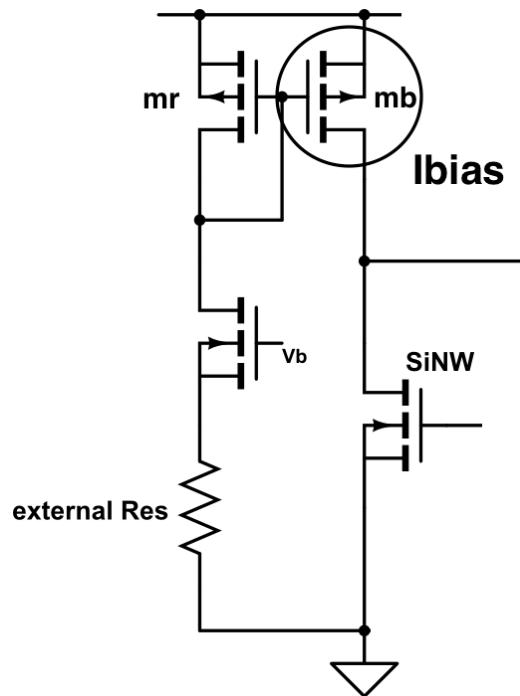


**Figure 5.13:** Results of the ac simulation of the loop gain and phase (Bode plot) with different  $g_m$  value ( $200n$ ,  $2\mu$ ,  $20\mu$ ). These  $g_m$  value is selected according to DC-sweep mode specification we set in chapter 3 (section.3.4).

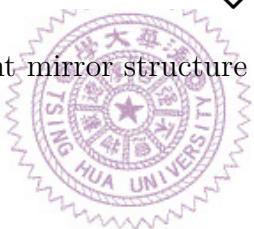
$g_m$	$20\mu$	$2\mu$	$200n$
Loop Gain	20k	2k	200
Phase Margin	80(deg)	78(deg)	81 (deg)

**Table 5.3:** The phase margin and loop gain of the fronted circuit

is  $3V$ . The other is the current  $I_{bias}$ .  $I_{bias}$  is generated by a simple pmos whose current is decided by an external resistor (Fig.5.14). The size ratio between pmos mr and mb is  $1 : 10$ . This current mirror structure has a maximal output current of  $70\mu A$ . In Table.5.4, the upper limits of  $g_m$  is  $50\mu$ . According to our electrical measurement, this is the maximal  $g_m$  value that our nanowire can have when  $V_G$  is  $3V$ .



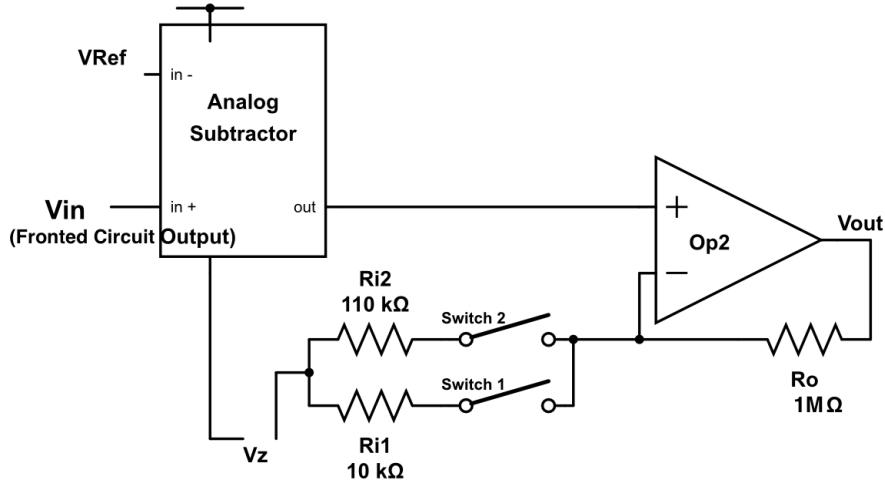
**Figure 5.14:** The current mirror structure of the current source Ibias.



	Design Spec.	Simulation result
$I_D$	$100nA - 30\mu A$	$20nA - 70\mu A$
$g_m$	$200n - 20\mu$	$130n - 50\mu$
$V_G$	$0.5V - 3V$	$0.45V - 3V$

**Table 5.4:** The comparison between the design specification and simulation result of DC-sweep mode circuit.

## 5.2 The Second Stage Circuit



**Figure 5.15:** Block diagram of the second stage circuit

We discuss the second stage circuit in this section. The second stage circuit is only used for the transient measurement mode.

Fig.5.15 shows the block diagram of the second stage circuit. The analog subtractor shifts the voltage of  $V_{in}$  from  $V_{Ref}$  to  $V_z$ . It is followed by a resistor-based non-inverting amplifier composed of a two-stage differential operational amplifier, two switches and three resistors. The switches select the amplification rate among 100, 10 and 1 (Table.5.5).

### 5.2.1 The Analog Subtractor

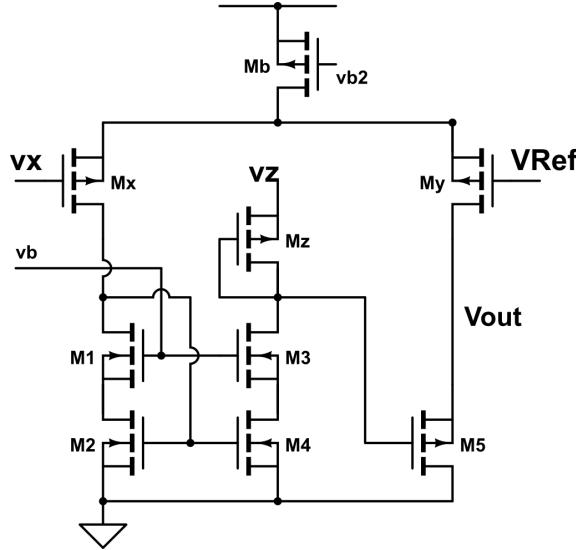
Fig.5.16 shows the schematic of the analog subtractor [19]. The output voltage equals to:

$$V_x - V_{Ref} + V_z \quad (5.16)$$

If a voltage signal  $\Delta v$  sent to  $v_x$ , it induces a current change ( $\Delta i_d$ ) in  $M_x$ . This current is mirrored to the diode-connected  $M_z$  by the cascode current mirror formed

switch 1   switch 2	on on	on off	off off
amplification rate	100	10	1

**Table 5.5:** Switches 1 and 2 select the amplification rate among 100, 10 and 1.



**Figure 5.16:** Block diagram of the second stage circuit.

by  $M1 \sim M4$ .  $\Delta i_d$  changes the gate voltage of  $Mz$ , and this voltage is buffered to the output by the source follower  $M5$ .

$$\Delta v_{out} = \Delta v_x \frac{gm_x}{gm_z} - V_{Ref} \frac{gm_y}{gm_5} + V_z \quad (5.17)$$

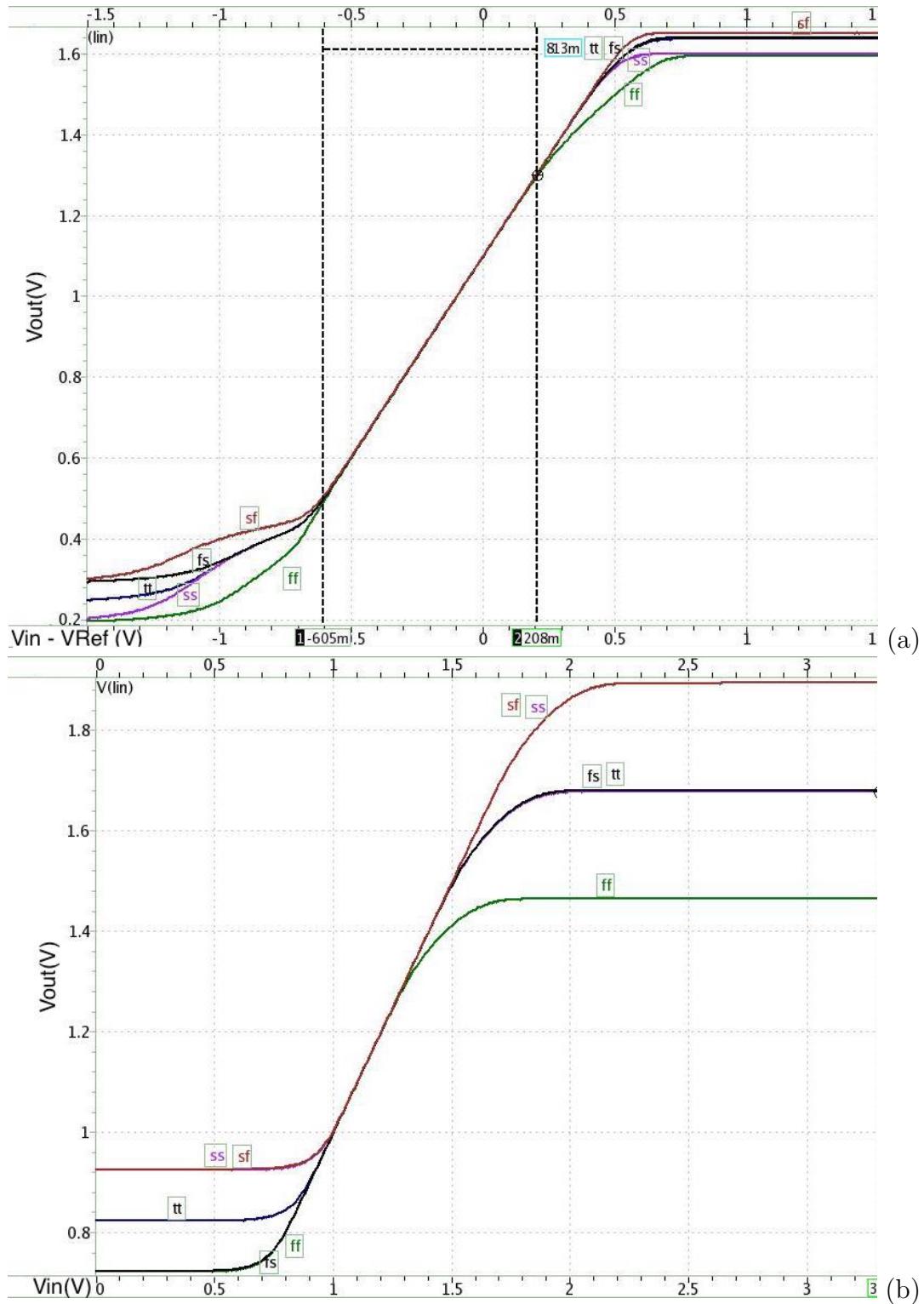
$$\Delta v_{out} = \Delta v_x - V_{Ref} \quad \text{For } gm_x = gm_z; gm_y = gm_5 \quad (5.18)$$

One reason for employing this block is that the  $V_{Ref}$  is an internal voltage reference which may drift with the process variation. We prefer the output offset voltage of the circuit to be constant and controllable. Therefore, we shift it to  $V_z$  controlled by an external voltage source. Another reason is to increase the output dynamic range of the next-stage amplifier. This reason will be much clearer when we start discussing the amplifier circuit in the next section.

The DC sweep is performed on input ( $V_X$ ) and  $V_z$  at five corners to show the linear region of the circuit (Fig.5.17, Table.5.6). The circuit has an input dynamic range of  $0.77V$  ( $-0.57V \sim +0.2V$ ) while the dynamic range for  $V_z$  is  $0.38V$ .

### 5.2.2 Non-inverting Resistor-based Amplifier

In Fig.5.16, the Op2 along with the resistors ( $R_o$ ,  $R_{i1}$ ,  $R_{i2}$ ) and the switches (Switch1, Switch2) compose our non-inverting resistor-based Amplifier. We adopt



**Figure 5.17:** DC response of the output of our analog subtractor. (a) The x-axis is the difference between positive input and negative input ( $V_x - V_{Ref}$ ). (b) The x-axis is the voltage of  $V_z$

VDD	3.3V	
Ibias	$40\mu A$	
Output voltage dynamic range	0.2V-2.5V	
Input voltage type	$V_x$	$V_z$
Input Dynamic Range	from $V_{Ref} - 0.57V$ to $V_{Ref} + 0.2V$	from 1V to 1.38V
Bandwidth	$675kHz$	irrelevant
SNR (@10Hz)	$8.3e10$	$8.4e10$

**Table 5.6:** The summary table of the analog subtracter circuit.

this simple structure to amplify the output signal of the subtractor. When the subtractor sends a small signal  $\Delta v$  into Vin, the output voltage ( $v_{out}$ ) is:

$$v_{out} = (\Delta v - v_f) \times A_{Op2} \quad (5.19)$$

$$v_f = v_{out} \frac{R_i}{R_o + R_i} \quad (5.20)$$

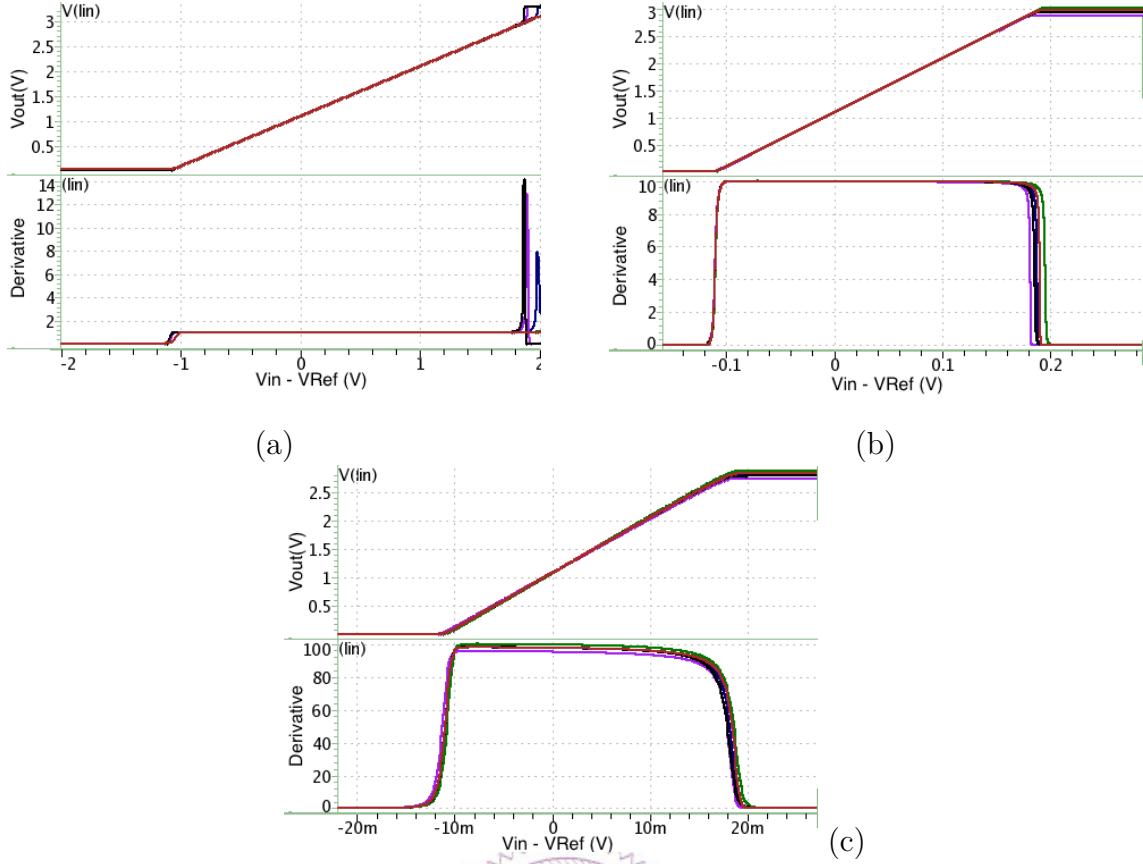
$$\frac{v_{out}}{\Delta v} = \frac{A_{Op2}}{1 + A_{Op2} \frac{R_i}{R_i + R_o}} \quad (5.21)$$

$$\approx \frac{R_i + R_o}{R_i} \quad \text{For } \frac{R_i A_{Op2}}{R_i + R_o} > 10 \quad (5.22)$$

The  $R_i$  can be  $110k\Omega$  or  $9.2k\Omega$  ( $10k\Omega || 110k\Omega$ ). When two switches is off, the circuit acts like an unit-gain buffer. Eq.(5.22) suggests that  $A_{Op2}$  should be larger than 1000 (60dB). Thus, the Op2 in Fig.5.15 adopts the structure of a two-stage amplifier (same with the operational amplifier in TIA block) due to its high gain and wide output dynamic range.

Amplification Rate	100	10	1
Error	< 7%	< 0.7%	< 0.02%
Bandwidth	$10.1k Hz$	$24k Hz$	$220k Hz$
Phase Margin	110 degree	110 degree	84 degree
Input Dynamic Range	from $-9mV$ to $17mV$	from $-0.11V$ to $0.14V$	from $-1.06$ to $1.9V$
Output Dynamic Range	0.1V - 3V		

**Table 5.7:** The summary table of simulation results.



**Figure 5.18:** Five corners output DC response ( $v_{out}$ ) and derivative ( $dv_{out}/dvin$ ) when being operated under the amplification rate of (a)1, (b)10, (c)100.

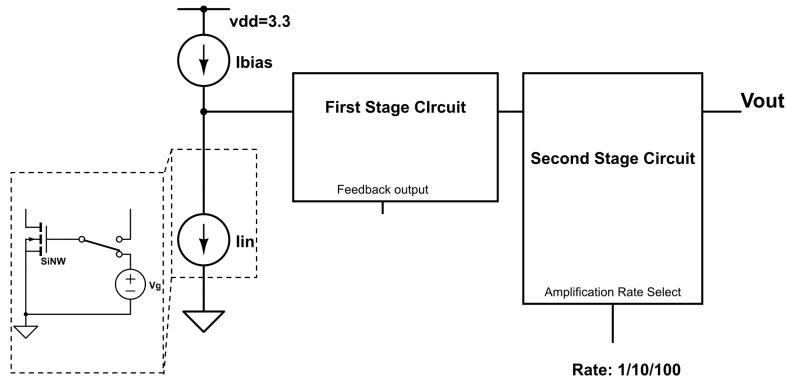
One thing to note is that the derivation above views the  $V_z$  as the virtual ground.  $V_z$  is both the input and output offset voltage of the amplifier. It is usually applied with  $1.1V$ . As mentioned in the subtractor section (Section 5.2.1), the subtractor increases the output dynamic range of the amplifier stage. If the subtractor is removed, the output offset voltage of this stage would be  $V_{Ref}$ , which is much lower ( $\sim 0.8V$ ), and is changeable due to the process variation.

Fig.5.18 presents the five corners post-simulation results of the amplifier and Table 5.7 is the summary table. We swept the input and measured the output under three amplification gain.

## 5.3 Post-simulation Result of Transient Measurement mode

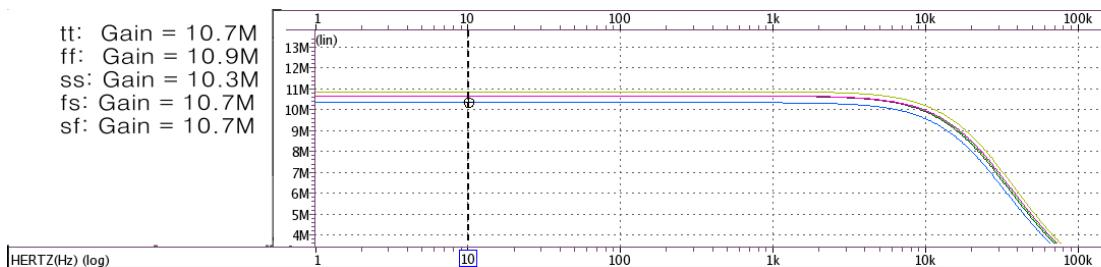
As mentioned in section 5.1.2, there are two usage of Transient Measurement mode (Fig.5.2). There simulation results are presented separately below.

### 5.3.1 Detecting signals of biomolecules at the gate

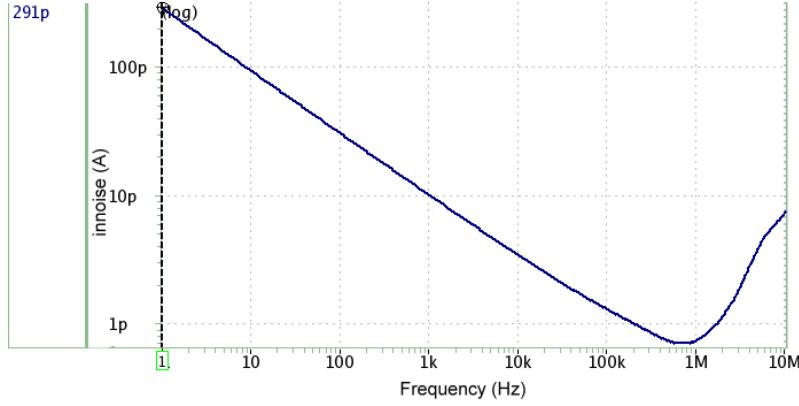


**Figure 5.19:** The block diagram of the Transient Measurement circuit. We simulate it by sending ac signal through the voltage source  $V_g$ .

The first usage is to detect the output response of input voltage signal at gate. The voltage signal is caused by the biomolecule concentration. This measurement is usually preceded by DC-sweep mode, which initializes the  $I_D$  with the value of Ibias and set  $g_m$  to a corresponding value. Therefore, we replaced the transistor by a current signal  $I_{in}$  as in Fig.5.19. The ac signal is applied from  $I_{in}$  to perform the ac analysis.



**Figure 5.20:** The gain of  $\frac{V_{out}}{I_{in}}$  when the voltage gain of the second stage is 100.



**Figure 5.21:** The input referred noise when the amplification rate of the second stage is 100.

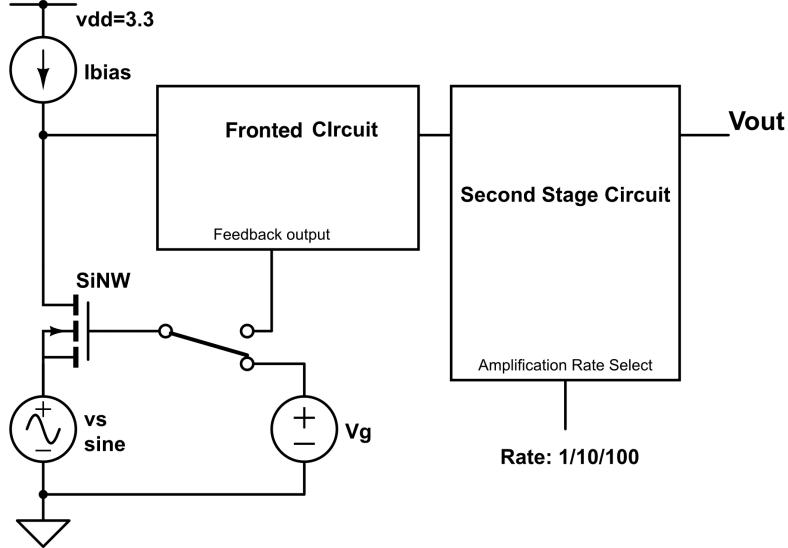
Fig.5.20 presents the maximal gain that the circuit provides at five corners. Fig.5.21 shows the input referred noise. The design specification requires the gain to be greater than  $5M$  and the voltage noise referred to the gate of nanowire to be smaller than  $2mV$ . The summary table (Table.5.8) computed the noise result by considering the  $g_m$  as  $1\mu$ , which is the minimum  $g_m$  that may exist in our measurement.

	Design Spec. (Table.3.5)	Simulation Result
$I_D$ Range	600nA - $10\mu A$	
$gm$ Range	$1\mu$ - $20\mu$	
$\Delta V_G$	$20mV$ - $280mV$	
Dynamic Input Current Range	$\pm 2.8\mu A$	$6\mu A$ - $10\mu A$
Maximal Amplification Rate ( $\frac{V}{A}$ )	$5M$	$10.3M$
Bandwidth	$> 1kHz$	$10.1kHz$
Input Referred Noise ( $V_G$ )	$< 2mV$	$= \frac{0.291n}{1\mu} = 0.29mV @1Hz$

**Table 5.8:** The summary table. The first three rows are the nanowire characteristics when applied with Transient Measurement mode. Others are the simulation results comparing with the design specification.

To be noted that in the simulation of Fig.5.21, Ibias provides  $10\mu A$  which is the largest biasing current in transient measurement mode (Table.3.4). This should be when the circuit has largest noise.

### 5.3.2 Modulating biomolecule signals from the source terminal



**Figure 5.22:** The block diagram of Transient Measurement circuit. We simulate it by sending ac signal to the source of the nanowire.

The second usage of Transient Measurement mode is to apply a sinusoidal signal at the source of nanowire.  $V_g$  and  $I_{bias}$  are kept constant during the measurement. The output voltage is measured and used for computing the  $g_m$  of the element.

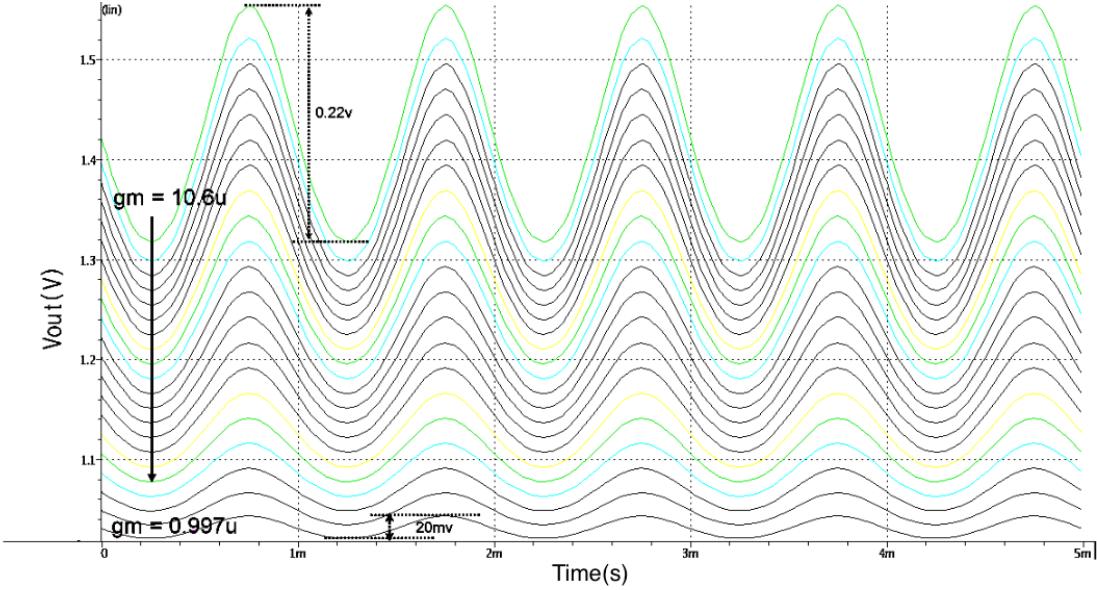
$$g_m = \frac{V_{out}}{v_s \times R_{TIA} \times A_{second}} \quad (5.23)$$

$v_s$  is the amplitude of the input sinusoidal signal.  $A_{second}$  is the voltage gain of the second stage circuit and  $R_{TIA}$  is the transimpedance of TIA in the fronted circuit.

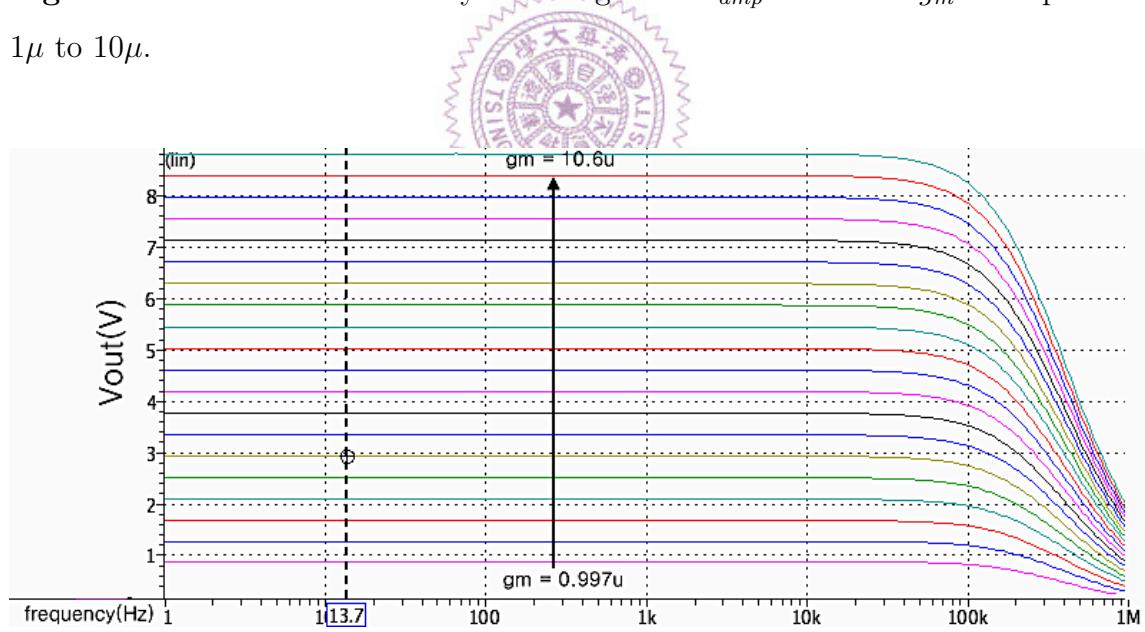
One thing to be noted is the offset voltage of the output. The biomolecule concentration difference changes the  $I_D$  of nanowire. This  $I_D$  difference not only results in the change of  $g_m$  but also alters the offset current flowing through  $R_{TIA}$ . This current is also amplified and may cause too much current flowing into the circuit. The solution is to utilize  $I_{bias}$  to cancel the offset current.

Two simulation results presented below are the transient responses of the output voltage when  $A_{amp}$  is 10 (Fig.5.23) and 100(Fig.5.25).  $g_m$  of the transistor is swept in the same time. According to the specification given in chapter 3 (Table.3.5),  $g_m$  ranges from  $1\mu$  to  $10\mu$  in transient measurement. The input sinusoidal signal has a

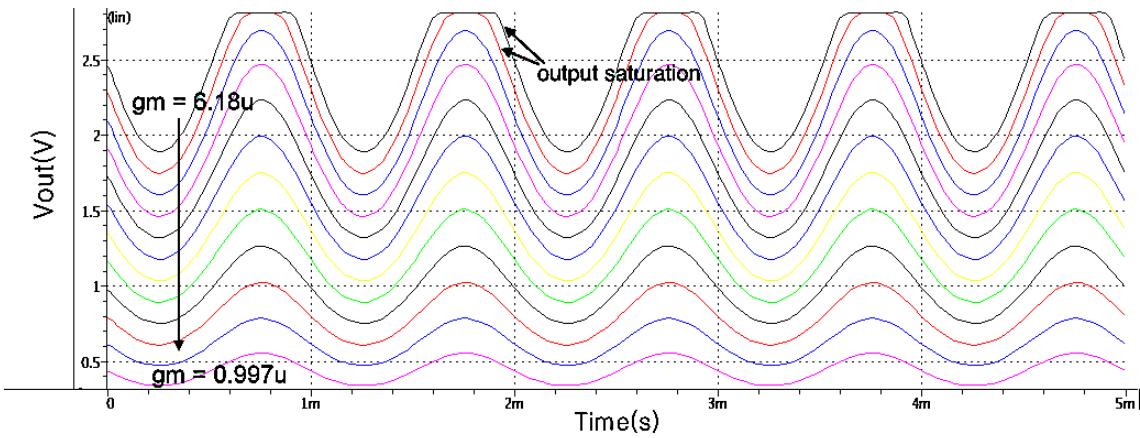
frequency of  $1\text{kHz}$  and an amplitude of  $20mV$ . Their corresponding ac sweeps are presented in Fig.5.24 and Fig.5.26. These results show that the circuit bandwidth is about  $10\text{kHz}$ , which is caused by the last amplifier block.



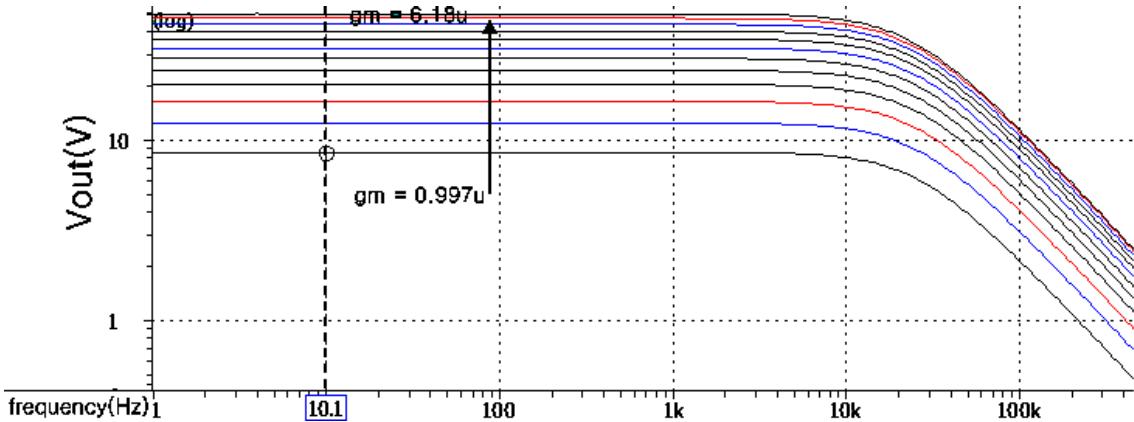
**Figure 5.23:** The transient analysis. The gain of  $A_{amp}$  is 10. The  $g_m$  is swept from  $1\mu$  to  $10\mu$ .



**Figure 5.24:** The ac analysis of the transient simulation result in Fig.5.23.



**Figure 5.25:** The transient analysis. The gain of  $A_{amp}$  is 100. The  $g_m$  is swept from  $1\mu$  to  $6\mu$ . There are two curves have the output saturation problem. This is because of the offset current flowing through  $R_{TIA}$ . It can be solved by increasing the current provided by Ibias.



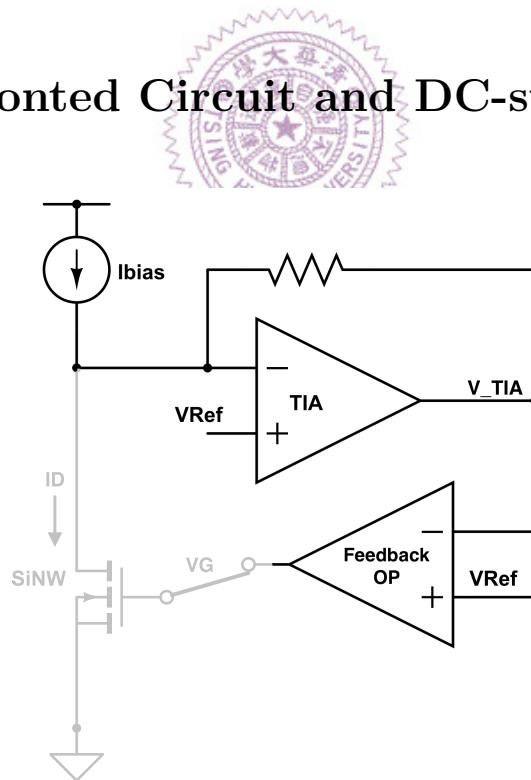
**Figure 5.26:** The ac analysis of the transient simulation result in Fig.5.25.

# Chapter 6

## Circuit Results Discussion and Summary

This chapter presents the results of our read-out circuit and the summary of this thesis.

### 6.1 The Fronted Circuit and DC-sweep mode

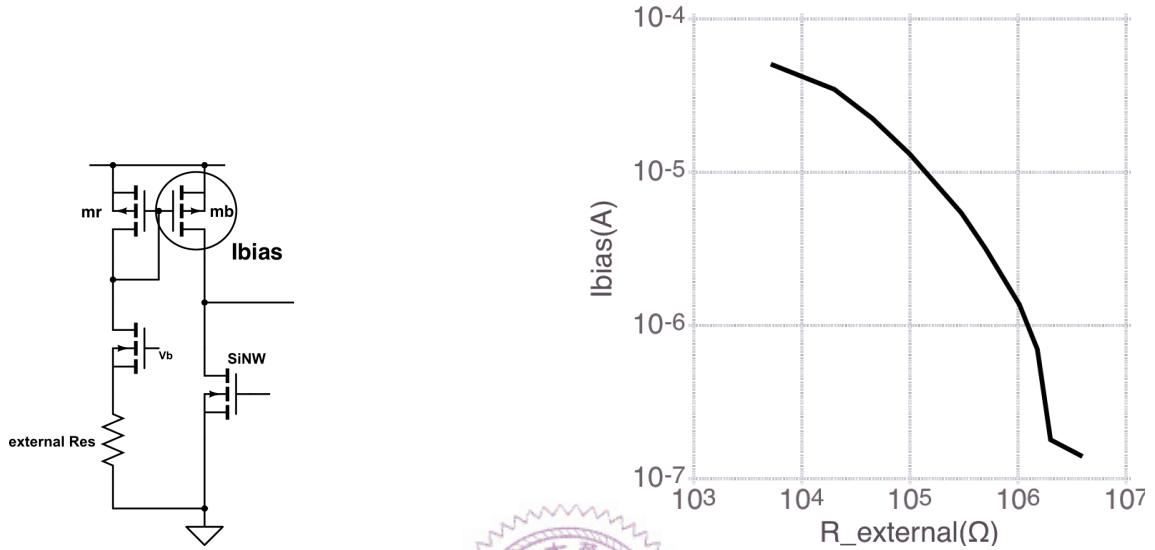


**Figure 6.1:** The fronted circuit

As in Fig.6.1(a), the fronted circuit includes a biasing current source ( $I_{bias}$ ), tran-

simpedance amplifier (TIA) and an operational amplifier (OP). These three circuit blocks combined with the nanowire device (SiNW) form a feedback structure, which is DC-sweep mode of our circuit.

### 6.1.1 The Output Current Range of Ibias Circuit



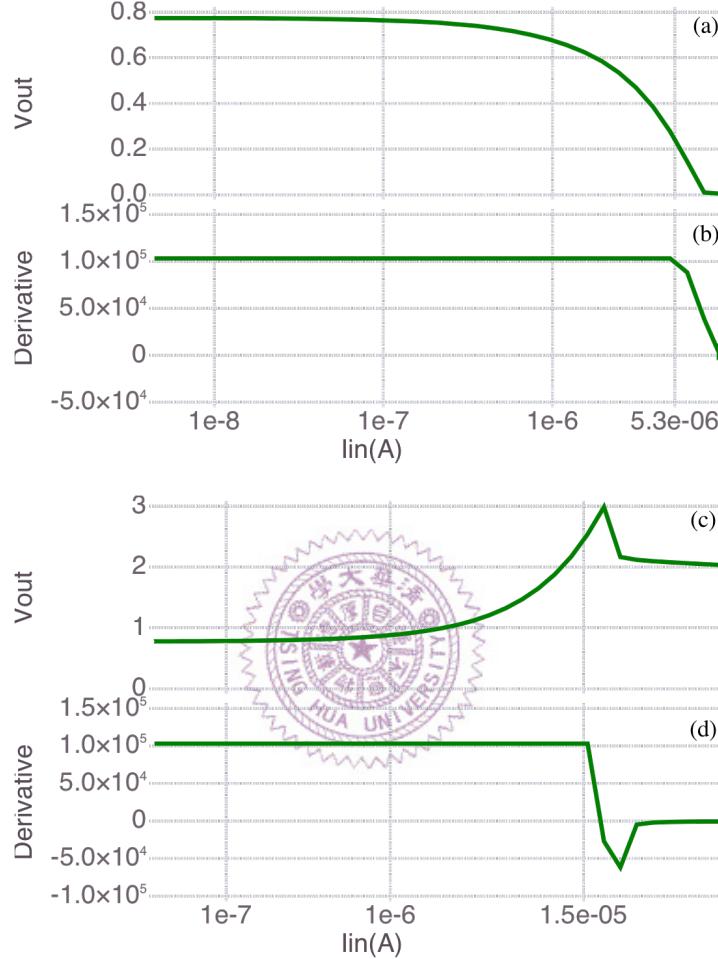
**Figure 6.2:** (a) The Ibias circuit. (b) The relation between biasing current ( $I_{bias}$ ) and resistance of the external resistor.

The Fig.6.2(a) is the schematic of the Ibias circuit. The relation between the resistance of the external resistor and the biasing current is shown in Fig.6.2(b). The Ibias circuit is able to provide a biasing current from  $100nA$  to  $50\mu A$  stably. It should be noted that this biasing current range binds the operational range of DC-sweep mode circuit.

### 6.1.2 The Chip Measurement Results of TIA

The Fig.6.3(a) and (c) show that the dynamic input current range of TIA is  $+5.3\mu A \sim -15\mu A$ . The Fig.6.3(b) and (d) are the respective derivative ( $\frac{\partial V_{out}}{\partial I_{in}}$ ). As illustrated in these figures, the transimpedance of TIA is  $103k$ . It is notable that not all TIA on the chips have the same transimpedance. This is because the transimpedance value depends on the resistance of the resistor in TIA (Fig.6.1). This resistor is made of N-well, which should have the largest resistance-to-surface ratio among

other kinds of resistor. But since the doping concentration may vary with the fabrication process, such kind of resistor has a larger resistance variance (% 30). We have performed necessary simulations before tap out. It is assured that the variance does not disturb the important properties of whole read-out circuit such as stability and noise ratio.

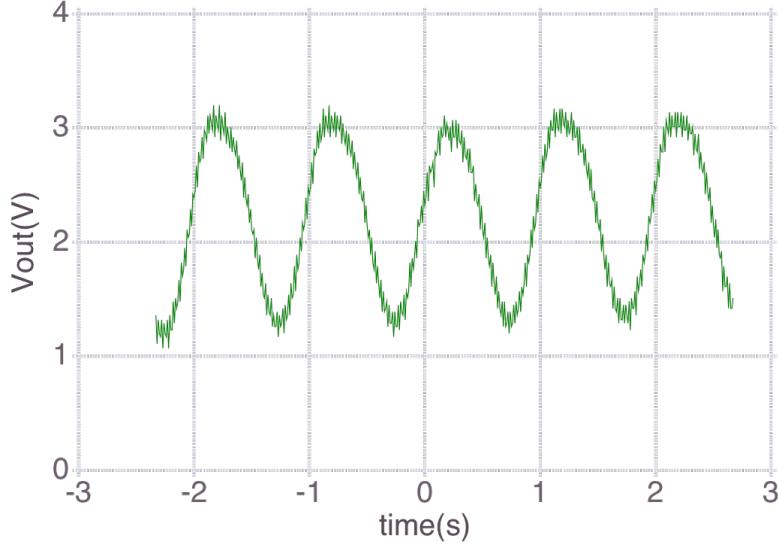


**Figure 6.3:** The dc simulation results of TIA. The x-axis represents positive/negative input current (log scale). (a) is the  $V_{out}$  responding to the positive input current while (c) is to the negative input current. (b) and (d) are the partial derivative of  $V_{out}$  with respect to input current ( $\frac{\partial V_{out}}{\partial I_{in}}$ ) from (a) and (c) respectively.

### 6.1.3 The Chip Measurement Results of the Feedback OP

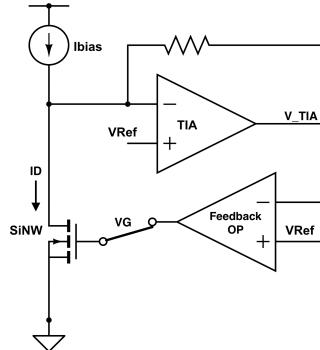
A sinusoidal signal is sent to the negative input of OP and the output signal is measured in Fig.6.4. It shows that the gain of the feedback OP is only about  $1k$ .

However, the gain of OP was designed to be more than  $5k$ . We will discuss this problem in the following section.



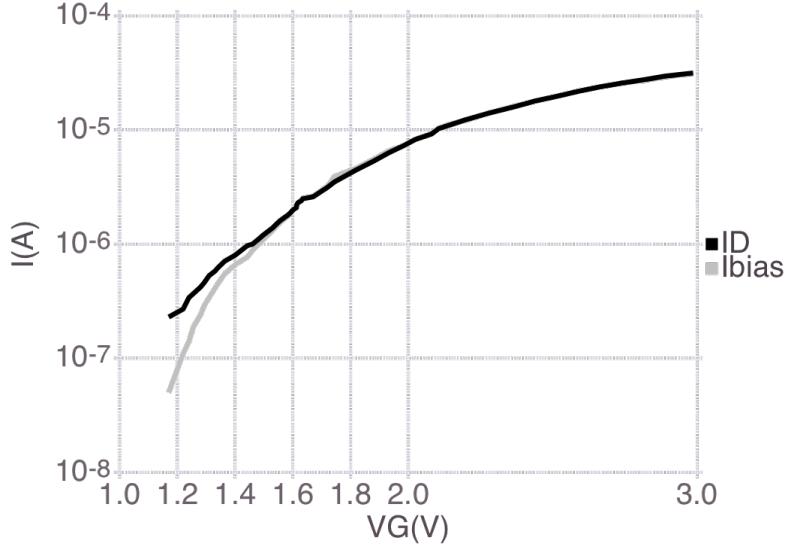
**Figure 6.4:** The output voltage of the feedback OP when the negative input is applied with a sinusoidal signal. This input sinusoidal signal has frequency of 1Hz and amplitude of 2mV. The positive input of OP is biased with a constant voltage generated by the chip (VRef in Fig.6.5). The output signal has amplitude around 2V, which means that the gain of OP is about 1k.

#### 6.1.4 Measurement with DC-sweep Mode Circuit and the Low-current Defect Problem



**Figure 6.5:** DC-sweep mode circuit

With DC-sweep mode (Fig.6.5), Ibias is swept and  $V_G$  and  $I_D$  are measured to



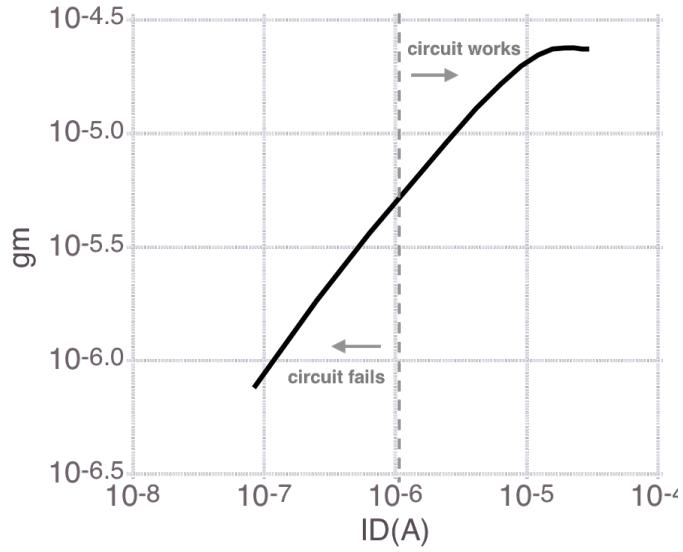
**Figure 6.6:** The measurement result of DC-sweep mode circuit.  $I_{bias}$  is the biasing current.  $I_D$  is the current flowing through the nanowire device. One can observe a separation between two curves in low current section ( $< 1\mu A$ ).

obtain the  $I_D-V_G$  and  $I_{bias}-V_G$  curves (Fig.6.6). The chip works well when  $I_{bias}$  is larger than  $1\mu A$ . The overlap between two curves implies that  $I_D$  follows  $I_{bias}$  and  $V_G$  consequently alters owing to the feedback mechanism.

When current becomes low, the circuit fails to prompt nanowire to follow the biasing current. This phenomenon could be reasonable because lower  $I_D$  implies lower  $g_m$  and the feedback ability of the circuit may be not strong enough to push the gate of nanowire. However, we expected this happens for  $g_m$  below  $200n$ . The Fig.6.7 indicates that the this happens when  $g_m$  is less than  $5\mu$  instead. We call this problem as low-current defect problem.

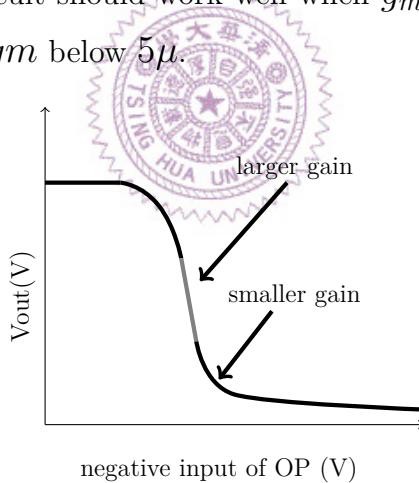
### Insufficient Gain

We first suspected that it is caused by the insufficient gain of the feedback OP. According to the last section (Section.6.1.3), the gain is about  $1k$ . The discussion in Section.5.1.4.3 suggests that the feedback mechanism depends on the loop gain. The loop gain should be larger than 100 for DC-sweep mode being functional. Based on Eq.(5.4) and Eq.(5.5), if  $A_{OP}$  is  $1k$ , the loop gain drops below 100 when  $g_m$  is less than  $1\mu$ . In other words, even though the gain of OP is 5 fold smaller than the



**Figure 6.7:** The  $g_m$ - $I_D$  curve. It is obtained from the  $I_D$ - $V_G$  curve in Fig.6.6. “Circuit fails” means the two curves in Fig.6.6 are separated where “circuit works” means they are overlapped.

gain we designed, the circuit should work well when  $g_m$  is larger than  $1\mu$ . But in fact, the circuit fails for  $gm$  below  $5\mu$ .



**Figure 6.8:** The illustration of the input-output response of the feedback OP.

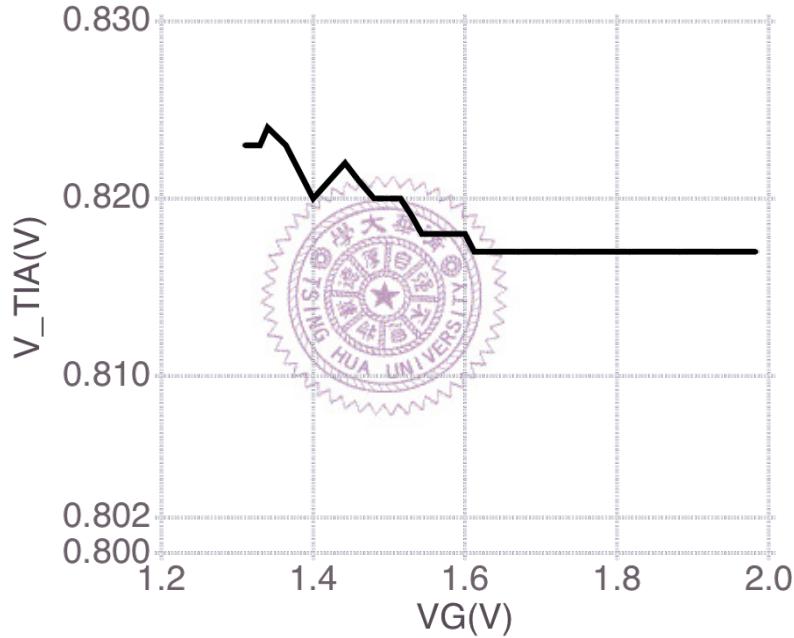
### Input Offset Voltage

Another reason may be responsible for the low-current defect is the offset voltage at the input of the feedback OP.

The output voltage of TIA ( $V_{TIA}$ ) of the DC-sweep experiment in Fig.6.6 is examined and shown in Fig.6.9. Ideally, when feedback mechanism works well,

$V_{TIA}$  should be equal to  $V_{Ref}$  (Fig.6.5). However, the value of  $V_{Ref}$  is  $0.802V$ , which is smaller than  $V_{TIA}$ . (This  $V_{Ref}$  is connected to a constant voltage point inside the chip. its value is known indirectly by measuring the drain voltage of nanowire since the drain of nanowire is kept to be same as  $V_{Ref}$  by TIA.) When the circuit works well,  $V_{TIA}$  and  $V_{Ref}$  is still different by  $15mV$ . This voltage difference can result in a  $150nA$  offset current flowing through TIA and into the nanowire device. This offset current becomes remarkable when the  $I_{bias}$  becomes small.

We suggest the reason that  $V_{TIA}$  is large than  $V_{Ref}$  is due to the offset voltage appearing at the input of the feedback OP. This speculation is reasonable with respect to the layout, which will be discussed in the next section.

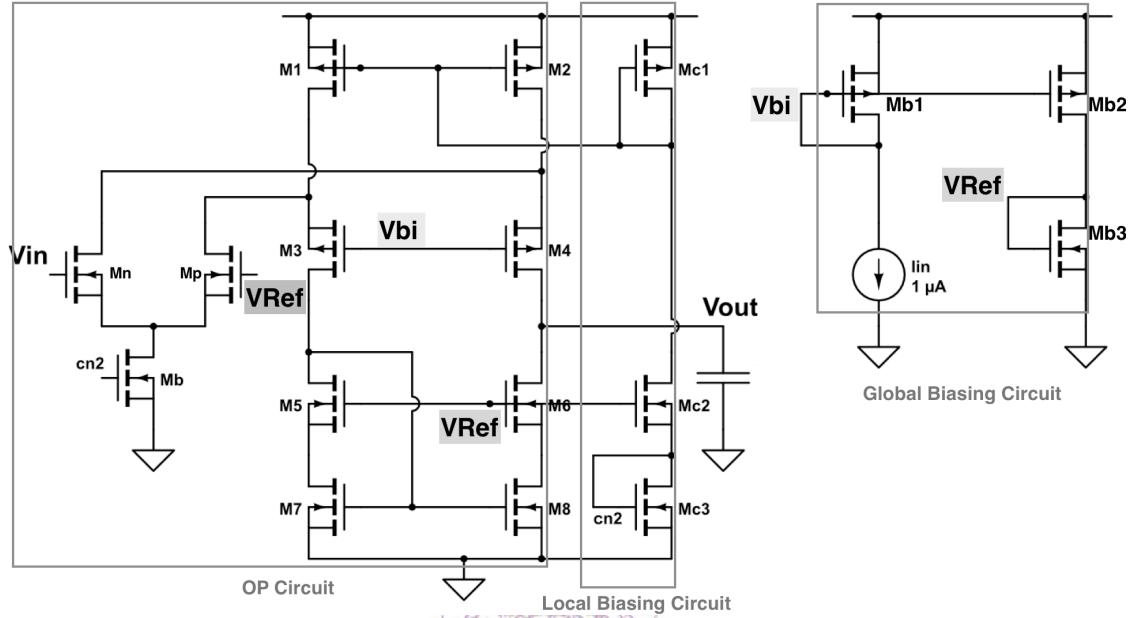


**Figure 6.9:** The  $V_{TIA}$ . The x-axis is the corresponding gate voltage. With the information from Fig.6.6, we found that the  $V_{TIA}$  is not equal to  $V_{Ref}$  no matter feedback mechanism works well or not.

Overall, the insufficient gain and the input offset may be the main reasons of the low-current defect. Both of them relate to the feedback OP. We then discuss these two reasons from the perspective of layout in the following section.

### 6.1.5 The Layout Problems of OP

The last section mentioned that the gain of OP is lower than we expected and there may exist an input offset voltage. In this section, we will deduce that several layout flaws may be responsible for these two problems.

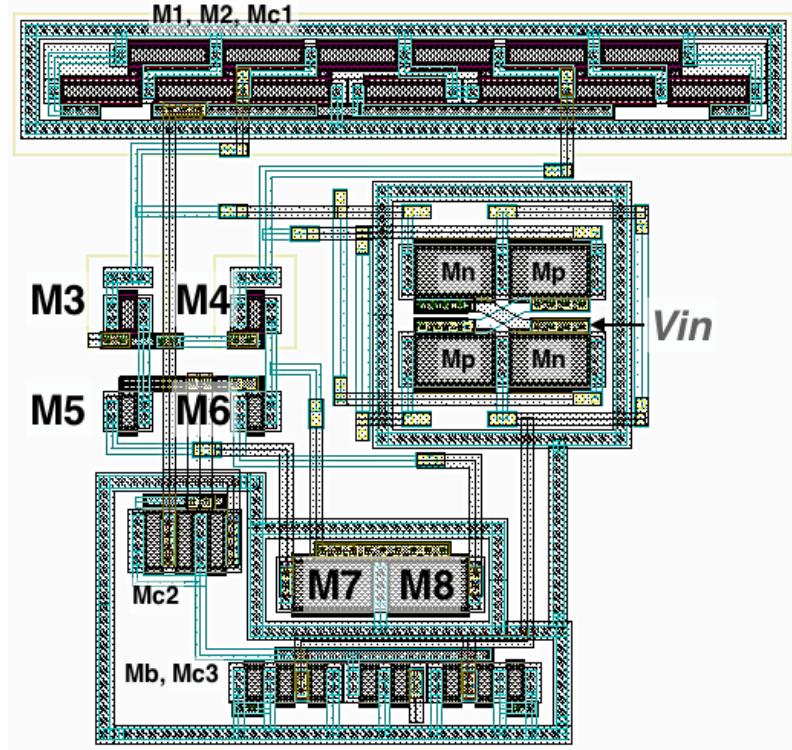


**Figure 6.10:** The left section is the schematic of the feedback OP including the local biasing circuit and OP circuit. The right section is the global biasing circuit for generating two global biasing voltages:  $V_{bi}$ ,  $V_{Ref}$ . The  $I_{in}$  is an external current source.

#### 6.1.5.1 The Possible Reasons for Insufficient Gain

The schematic presented in Fig.6.10 contains two sections. The left section is the body of the feedback OP and the local biasing circuit while the right one is a global biasing circuit. The global biasing circuit generated  $V_{bi}$  and  $V_{Ref}$ , which bias two pmos (M3, M4) and two nmos (M5, M6) respectively.

One layout flaw is that the  $M3 \sim M6$  are all single transistor. They are placed alone on the chip (Fig.6.11) without any protection. In consequence their size and doping concentration are more vulnerable to the process variation than other transistors. Another layout flaw is that the global biasing circuit is placed far from the



**Figure 6.11:** The layout of the feedback OP including the local biasing circuit.

OP circuit. The extent of the process variation from which the OP circuit and global biasing circuit suffer may be different.

Take an example, when process variation happens in global biasing circuit,  $V_{bi}$  and  $V_{Ref}$  change respectively. Ideally, the effect of these two changes on the gain of OP are countervailing. But this may not be true if M4 and M6 suffer another process variation. The changes on  $V_{bi}$  and  $V_{Ref}$  may affect M4 and M6 in different extent. Moreover, the high output impedance of OP amplifies this difference and as a result of the gain distortion.

#### 6.1.5.2 The Possible Reasons for Input Offset

The input offset can be related to the size mismatch between M7 and M8 (Fig.6.11). The transistors were designed to be same. But there is no dummy gate or matching technique applied to the transistors. Therefore, the size mismatch may prone to happen on M7 and M8. In our case, the offset voltage is negative ( $V_{\text{negative input}} > V_{\text{positive input}}$ ). If the size mismatch is responsible for it, the size of M8 should be relatively smaller than M7.

### 6.1.5.3 Improvement Methodology

Although all problems mentioned above relate to the layout, we do not think that simply revising the layout is a reliable solution. The feedback OP is an open-loop circuit with high output impedance. Its characteristics (such as gain and bandwidth) are hard to be controlled accurately considering the process variations. A better solution is to replace it with other amplifier. Since this OP serves as a high-gain and low bandwidth block, it can be substituted with a close-loop amplifier and low pass filter.

### 6.1.5.4 Summary of DC-sweep mode

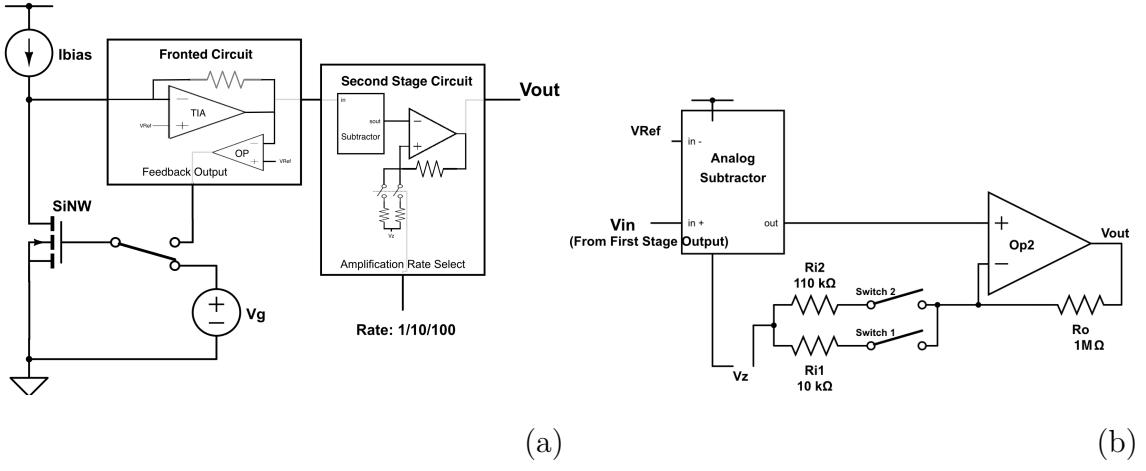
The table that compares the chip properties and the specification for DC-sweep mode is given below (Table.6.1). The chip does not meet the specification due to the low-current defect problem.

	Design Spec.	Chip Properties
$I_D$	$100nA - 30\mu A$	$1\mu A - 50\mu A$
$g_m$	$200mA - 20\mu A$	$3\mu - 20\mu A$
$V_G$	$0.5V - 3V$	$0.45V - 3V$

**Table 6.1:** The comparison between the chip properties and the specification for DC-sweep mode from chapter 3.

## 6.2 The Second Stage Circuit and Transient Measurement Mode

As in Fig.6.12, Transient Measurement mode includes the second stage circuit and the Ibias and TIA from the fronted circuit. An analog subtractor and a resistor-based amplifier are included in the second stage circuit. The input signal can be sent from the gate or the source of nanowire (SiNW).



**Figure 6.12:** (a) The block diagram of Transient Measurement circuit. (b) The schematic of the second stage circuit.

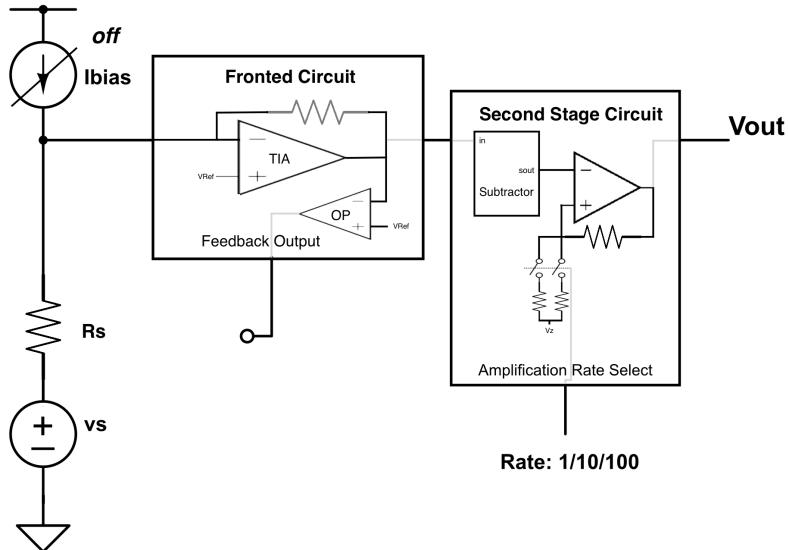
### 6.2.1 The Second Stage Circuit

This section presents the important properties of the second stage circuit. To be notable that the performance of the subtractor and amplifier cannot be measured independently because there is no external pad connected to the output of the subtractor. Besides, second stage input is always connected with the output of TIA. Due to the low output impedance of the TIA, it is hard to send input signal into the second stage circuit directly. Fig.6.13 is the alternative approach. The resistor  $R_s$  and the TIA compose a voltage amplifier. The input signal, which is usually triangular or sinusoidal, is injected through the  $R_s$ . It is then modulated in proportional to the ratio of  $R_s$  and TIA before being sent into the second stage circuit.

$$\text{Input of the } 2^{\text{nd}} \text{ stage circuit} = V_s \times \frac{\text{transimpedance of TIA}}{R_s} \quad (6.1)$$

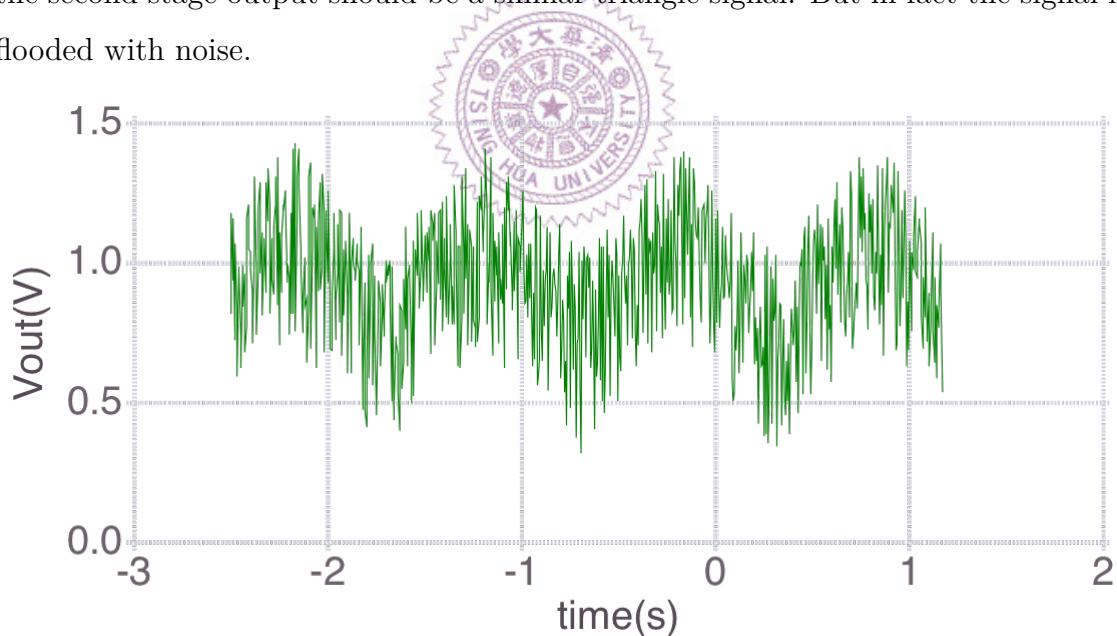
#### 6.2.1.1 The Oscillation Problem in Amplifier with Amplification Rate of 1

The amplifier in the second stage circuit has three amplification rate ( $A_{amp}$ ): 1, 10 and 100. The amplifier works well as the  $A_{amp}$  is 10 and 100. However, when



**Figure 6.13:** The second stage circuit measurement approach.

$A_{amp}$  is 1, the output signal is flooded with a set of high frequency signal (Mainly 180kHz in oscillosopce). In Fig.6.14, the input is a 1Hz triangle signal. Ideally, the second stage output should be a similar triangle signal. But in fact the signal is flooded with noise.



**Figure 6.14:** The noise ocsillation problem

We suggest that the oscillation of high frequency signal should be the main cause of the problem. When designing the amplifier, we did not consider the parasitic capacitance brought by the switches and the pad (with ESD circuit) at the output.

The simulation below proves our suggestion. The parasitic capacitance is modeled by a  $5pF$  capacitor. Fig.6.15(a) and (b) are the phase margin test of the amplifier before and after the capacitor is loaded on the output. The figures indicate that the second dominant pole locates at the output and the parasitic capacitors push it to the left. The phase margin is decreased subsequently. When the modeled capacitor is increased to  $25pF$ , the phase drops to -180 degree at  $180kHz$ , which is roughly same with the frequency of the oscillation signal.

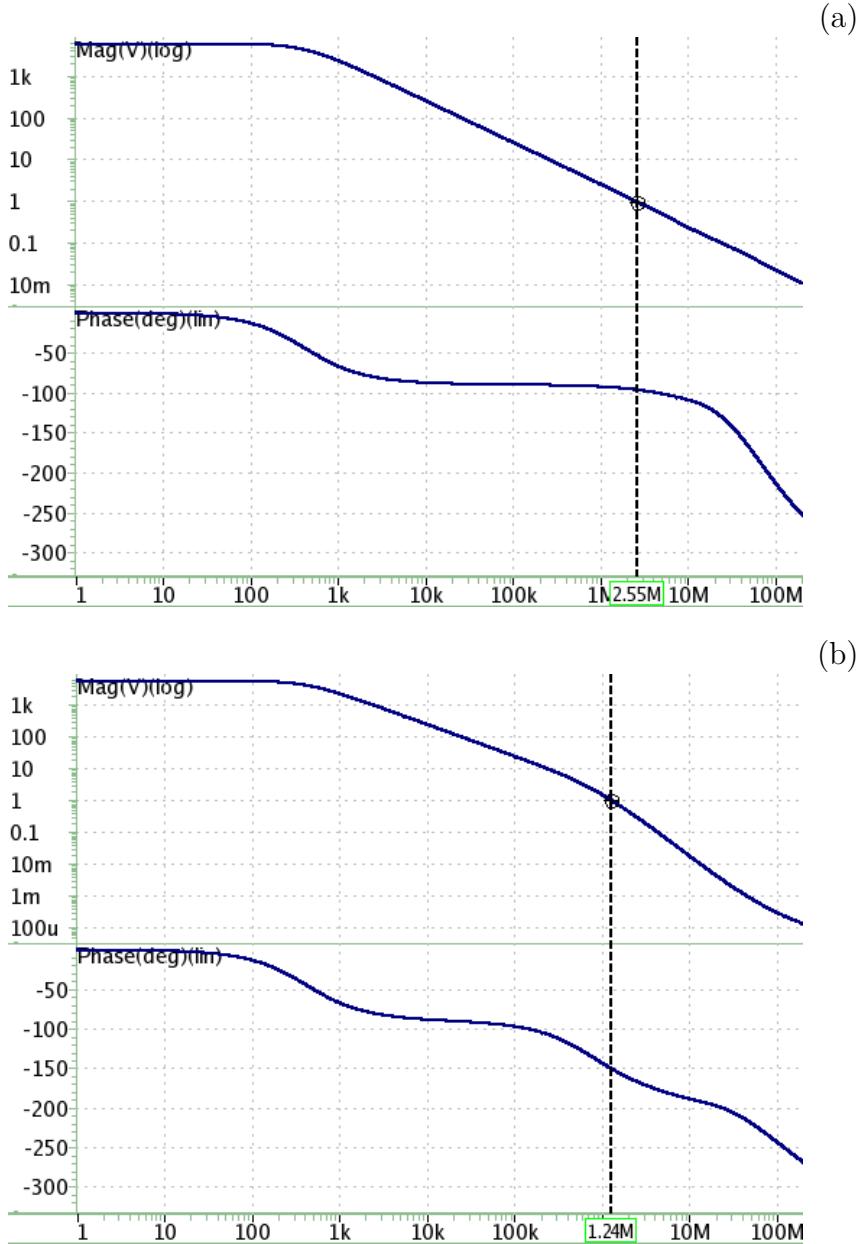
The reason that the oscillation problem only happens when  $A_{amp}$  is 1 is because of the feedback mechanism. When  $A_{amp}$  is 1, the structure is similar to an unit-gain buffer (Fig.6.12(b)). In Fig.6.16, (a) is the feedback network of this structure while (c) is of the amplifier with  $A_{amp}$  is 10 and 100. To compute the loop gain, the structure is broken at the negative input and a tested signal is injected ( $Vt$ ) as illustrated in Fig.6.16 (b), (d). The loop gain ( $\frac{V_f}{Vt}$ ) of the two structure is derived as:

$$\text{when } A_{amp} = 1: \quad \frac{V_f}{Vt} = A_{op} \quad (6.2)$$

$$\text{when } A_{amp} = 10 \text{ or } 100: \quad \frac{V_f}{Vt} = A_{op} \times \frac{R_i}{R_i + R_o} \quad (6.3)$$

$A_{op}$  is the gain of the OP in the amplifier. ( $A_{op}$  is similar in two cases even if the loading effect is taken into consideration because  $R_O \gg R_i$ .) Since the  $R_O$  is at least larger than  $R_i$  by 10-fold, two loop gains are different by 10-fold as well. The smaller loop gain increases the phase margin of amplifier by about 45 degree and diminish the oscillation (Fig.6.17).

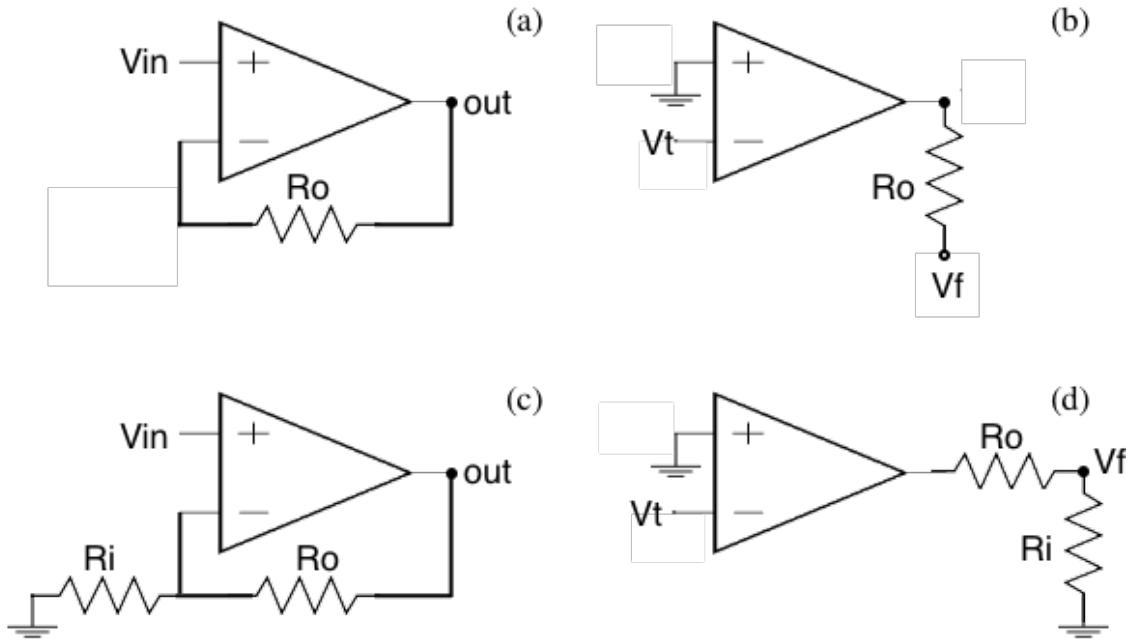
We tried to dealt with the oscillation problem by the signal average technique. The output signal is averaged out to remove the noise component. However, the average of the signal may lie on the wrong offset. Therefore, the amplifier with  $A_{amp} = 1$  is used only when the signal trend is of interest (such as the dynamic input range in Section.6.2.1.2). When the output signal is large and the amplification is not necessary, we simply measure the output of TIA.



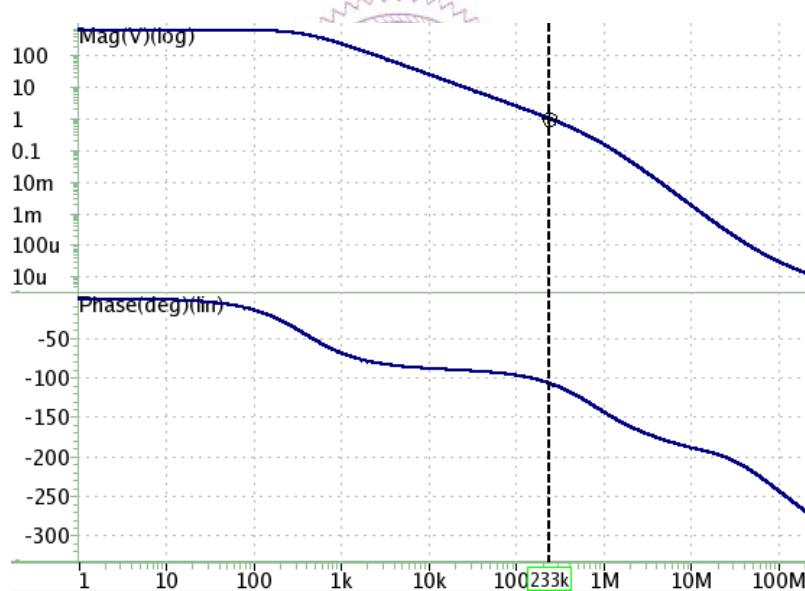
**Figure 6.15:** The post-simulation of the phase margin test of the amplifier when amplification rate is 1. **(a)** Without the parasitic capacitor, the phase margin is 108 degree. **(b)** With the parasitic capacitor (modeled by a  $5\text{pF}$  capacitor), the phase margin becomes 30 degree.

#### 6.2.1.2 Dynamic Input Range

Fig.6.18 is the input-output response of the second stage circuit ( $A_{amp} = 1$ ). It is used for finding the dynamic input range of the circuit. The linear region locates at  $V_{in} = 0.43V \sim 1.32V$ . According to chapter 5, this range is determined by the



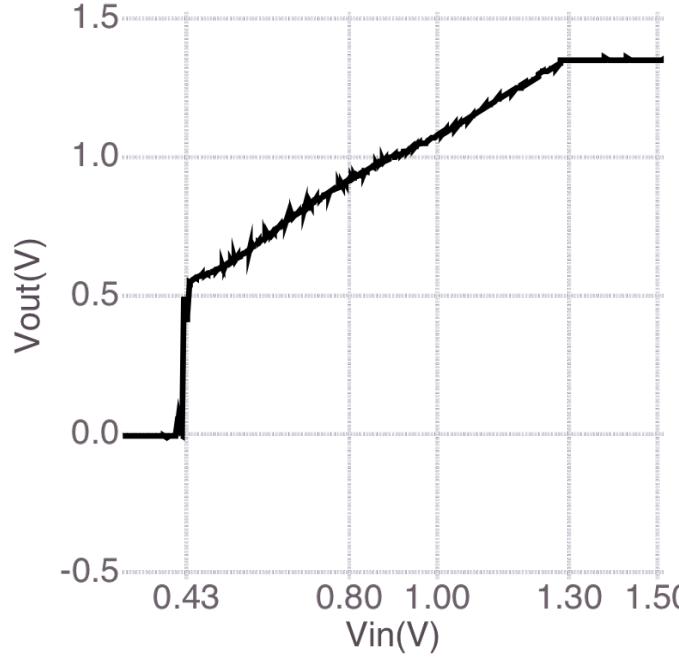
**Figure 6.16:** The feedback network and loop gain computation structure of the amplifier with (a), (b)  $A_{amp} = 1$  and (c), (d)  $A_{amp} = 10$  or 100.



**Figure 6.17:** The post-simulation of the phase margin test of the amplifier when amplification rate is 10. With the parasitic capacitor loaded on the output(modeled by a  $5\text{pF}$  capacitor), the phase margin is 73 degree

subtractor block.

Another input of the circuit is the  $V_z$  (Fig.6.12(b)). This voltage is for shifting



**Figure 6.18:** The input-output response of the second stage circuit ( $A_{amp} = 1$ ).

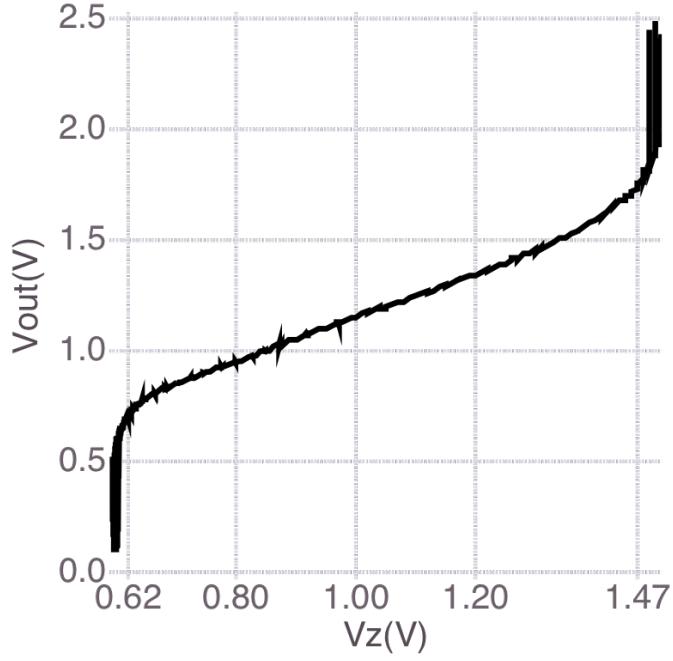
Designed Amplification Rate	100	10	1
Measured Amplification Rate	93.3	9.2	1
Error Rate	7.7 %	8 %	0

**Table 6.2:** Comparison between the designed and measured gain of the second stage circuit.

the offset voltage. Its dynamic input range is measured and presented in Fig.6.19, which ranges from  $0.62V$  to  $1.47V$ . To be notable that ideally the input  $V_z$  should be equal to the output. But in fact an offset voltage of  $0.15V$  occurs in Fig.6.12 due to the oscillation problem mentioned in the last section. This offset does not exist when the  $A_{amp}$  is 10 and 100.

### 6.2.1.3 The Circuit Gain

A triangle wave is sent to the end of  $R_s$  (Fig.6.13) and the input and output of the second stage circuit are recorded by an oscillation scope. Fig.6.20) (a), (b) and (c) are the time domain results when the  $A_{amp}$  is 1, 10 and 100 respectively. The exact gain values are summarized in the Table.6.2.



**Figure 6.19:** The input-output response of the second stage circuit. The input is  $V_z$ , which decides the output offset of the circuit.

## 6.2.2 Transient Measurement Mode

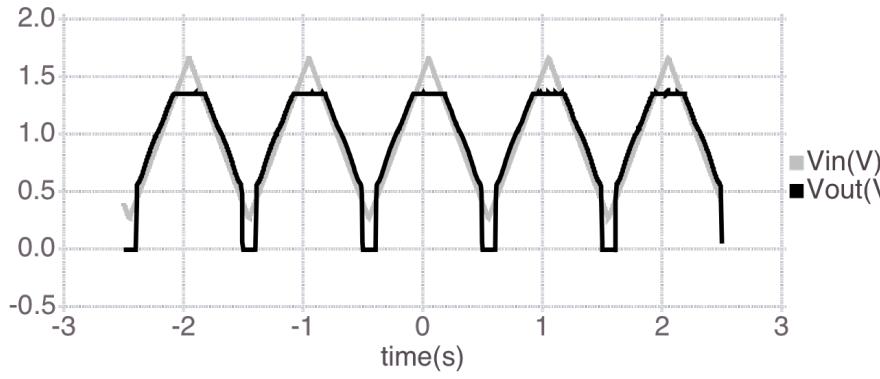
The second stage circuit and the TIA from the fronted circuit compose the circuit of Transient Measurement Mode. This section presents some of its important properties (gain, noise and bandwidth).

### 6.2.2.1 Bandwidth and Gain

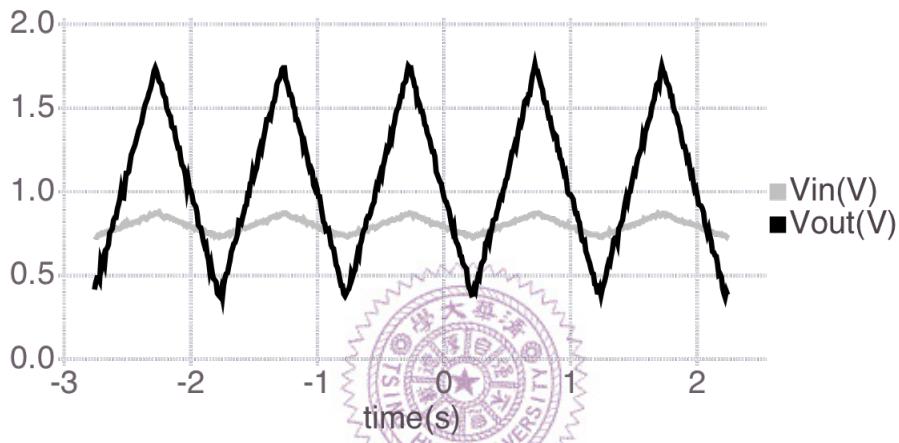
The gain is the input current to output voltage ratio. Because the oscillation problem may disturb the bandwidth measurement, we did not measure the circuit with  $A_{amp}$  of 1. The circuit with  $A_{amp}$  of 10 has gain of  $891k$  and -3dB bandwidth of  $30kHz$ . The circuit with  $A_{amp}$  of 100 has gain of  $8.9M$  and -3dB bandwidth of  $7.5kHz$ .

### 6.2.2.2 Input Referred Noise

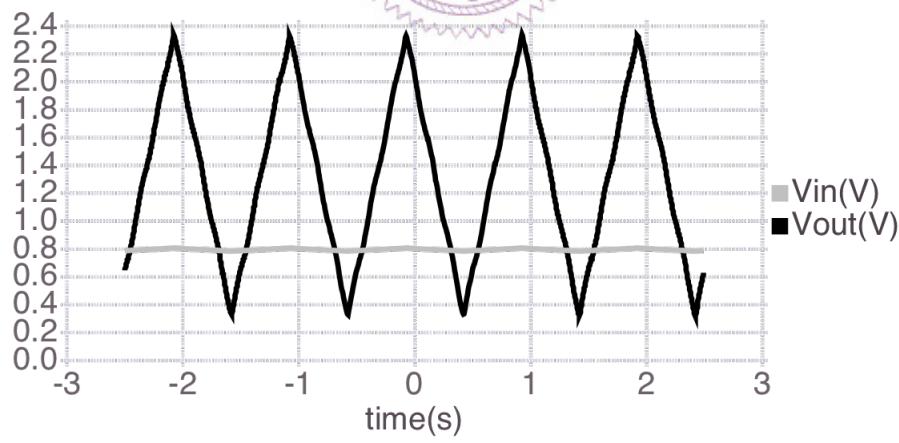
The spectrum analyzer are used to measure the noise. The power spectral density (PSD) of noise at the output of the circuit is measured and is referred to the input to show the equivalent input current noise (Fig.6.22). While measurement is performing, Ibias provides  $10\mu A$ , which is same to the condition of the post-simulation



(a)

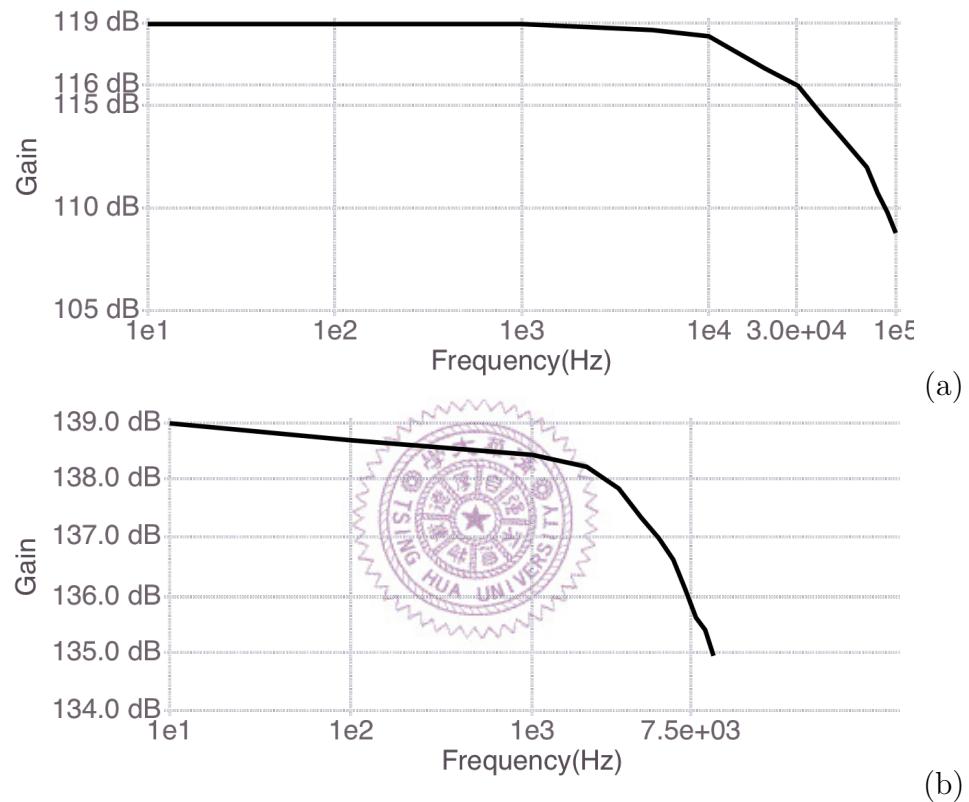


(b)



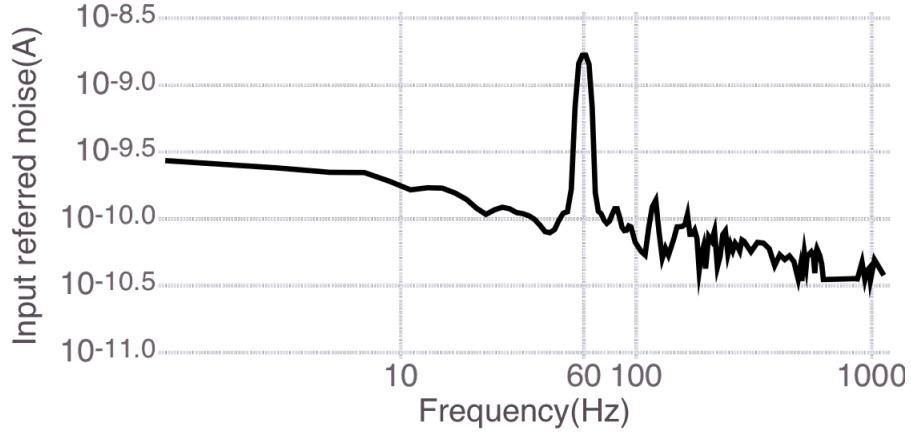
(c)

**Figure 6.20:** The input output signal of the second stage circuit in time domain when  $A_{amp}$  is (a) 1, (b) 10 and (c) 100.



**Figure 6.21:** The gain and bandwidth of Transient Measurement circuit. The  $A_{amp}$  is 10 in (a) and 100 in (b).

measurement (Fig.5.21). The primary type of noise are the low frequency noise (flicker noise). Other types of noise such as 60Hz come from the environment and working machines. They may be lowered by adopting better method of experiment or equipments. Overall, the amount of noise is tolerable. The input current noise is  $0.3nA$  at 1 Hz. The spec. from chapter 3 allows for a maximal input current noise of  $2nA$ .

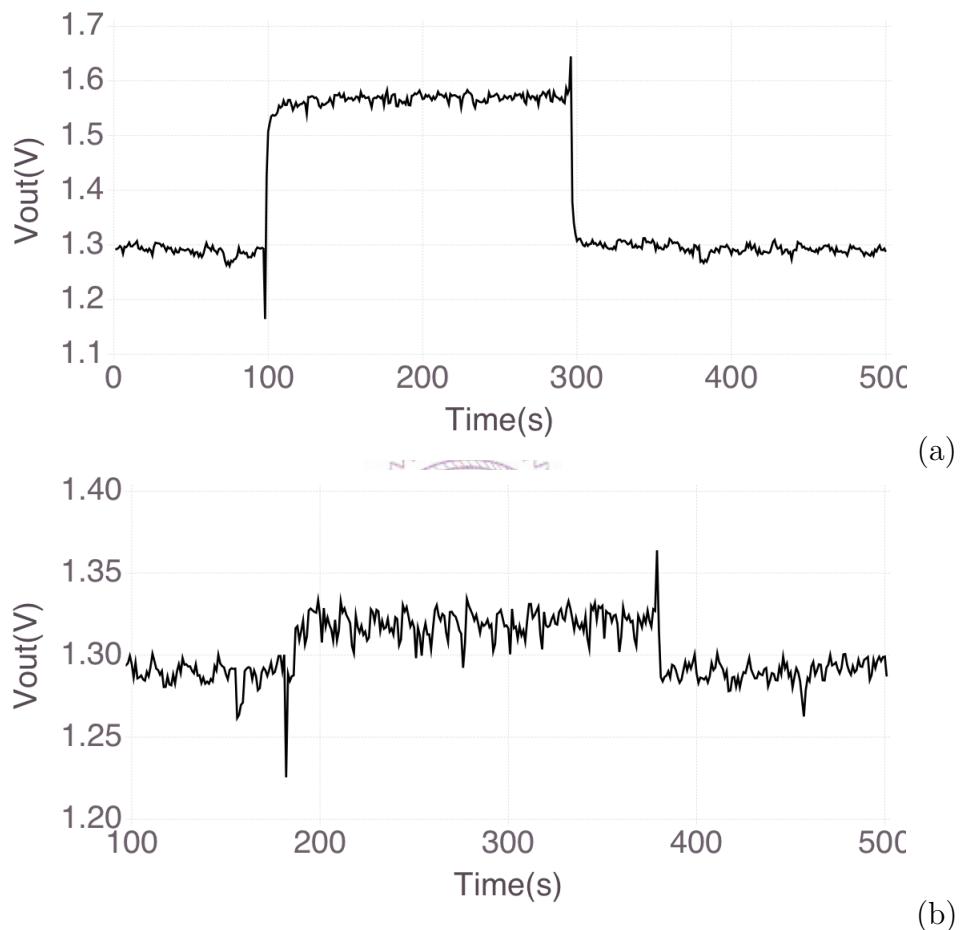


**Figure 6.22:** Input referred noise of Transient Measurement circuit.

### 6.2.2.3 The Detection Range

The spec. of our design demand a detection range for input current of  $\pm 20nA \sim \pm 2.8\mu A$ . The upper bound of the current detection is decided by the TIA circuit, which is  $5.3\mu A$  and  $15\mu A$ . The lower bound mainly relates to the noise. We find the lower bound by sending a pulse input to the gate of nanowire. This input voltage induced a current variance ( $\Delta I_D$ ) and resulted in a pulse signal at output. We then used oscilloscope to see how low the  $\Delta I_D$  can be when it is still possible to detect it through the output.

The Fig.6.23(a) and (b) are the output signals when the amplitude of input pulse signals are  $150mV$  and  $20mV$  respectively. The current variance induced in two cases are  $28nA$  and  $2.8nA$ . The high and low value can be barely distinguished in 6.23(b). Therefore, we say the lower bound of our circuit is  $\pm 2.8nA$ . (The positive input and negative) This matches the noise measurement in the last section. The noise is  $0.3nA$  and the detecting range is ten-fold larger than that value.



**Figure 6.23**

#### 6.2.2.4 Modulating biomolecule signals from the source terminal

The second usage of Transient Measurement mode is to apply a sinusoidal signal at the source of nanowire. In Fig.6.24, is obtained by this measurement method. The input is a sinusoidal signal with frequency of 500Hz and the amplitude of 0.5V. The nanowire was put under two solutions with different pH values in (a) and (b). After dividing the amplitude of the output signal by the transimpedance gain of the circuit (891k), we learned that the  $g_m$  of nanowire under these two pH solutions are  $1\mu$  and  $1.8\mu$ .

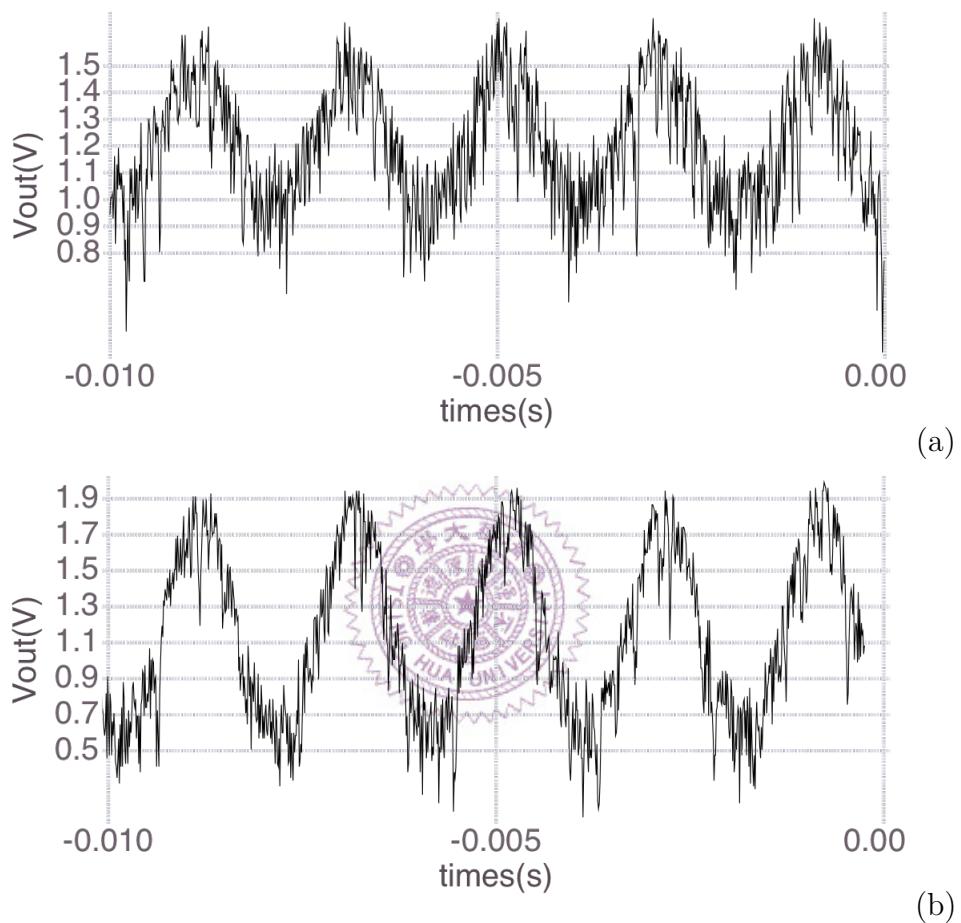
This method aims to modulate the biomolecule signal into higher frequency to avoid the flicker noise and other kinds of low frequency noise. However, from the result below, it can be observed that the output contains large amount of high frequency noise. We believe the noise comes from the testing solution and through the gate of nanowire. In the future, a bandpass filter with adjustable center frequency should be added to the circuit to filter the signal of the unwanted frequency.

#### 6.2.2.5 Summary of Transient Measurement mode

The Table.6.3 compares the chip properties and the specification for transient measurement mode. Although there is the oscillation problem, the performance of the circuit is fine.

	Design Spec.	Chip Properties
IBias Current ( $I_D$ )	$600nA - 5\mu A$	$100nA - 50\mu A$
Dynamic Input Current Range( $\Delta I_D$ )	$\pm 20nA - \pm 2.8\mu A$	$2.8nA \sim 5.3\mu A$ $-15\mu A \sim -2.8nA$
Input Referred Noise (A)	$< 2nA$	$< 0.3nA @ 1Hz$
Transimpedance Gain (max)	$5M(\frac{V}{A})$	$8.9M(\frac{V}{A})$
Bandwidth	$> 1k$ (Hz)	$7.5kHz$

**Table 6.3:** The comparison between the chip properties and the specification for Transient Measurement mode from chapter 3.



**Figure 6.24:** The output signal of the measurement using source of nanowire as input. The  $gm$  of nanowire in two figures are different by using testing solution with different pH values. The  $gm$  of nanowire is  $1\mu$  in (a) and  $1.8\mu$  in (b).

## 6.3 Dealing with the Device Variability Problem

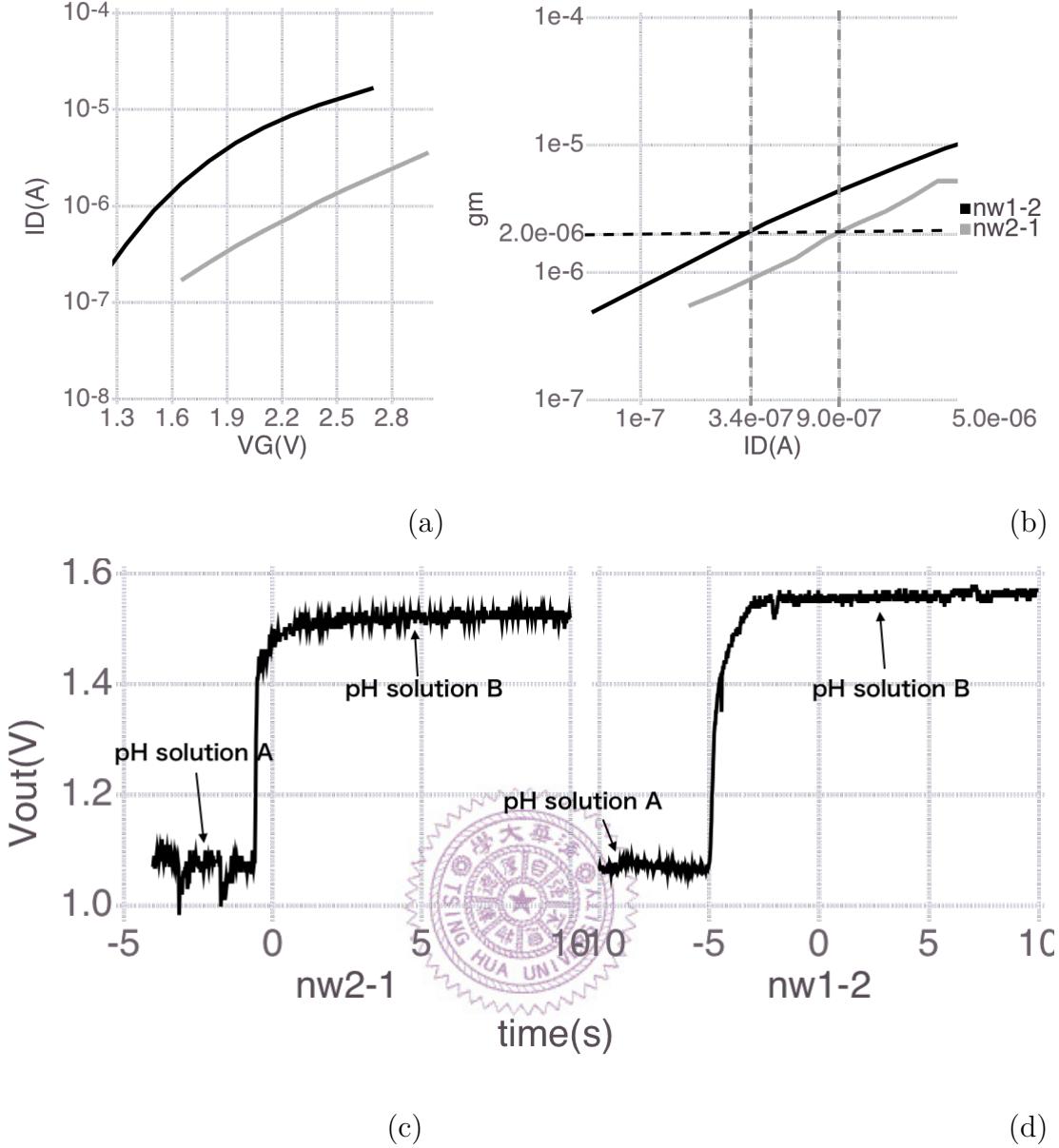
This section presents the measurement with the proposed variability-resisting method.

Two nanowire devices (nw1-2, nw2-1) lying on the same substrate are under test. The  $I_D-V_G$  curves of two devices are obtained and substantiate that they have device variability problem (Fig.6.25(a)). These curves are then transformed into  $gm$ - $I_d$  curves (Fig.6.25(b)). Based on the conclusion of appropriate operation region (Section.3.2.1), the  $gm$  of  $2\mu$  is selected. The certain  $I_D$  under which devices are biased are therefore determined. As illustrated in Fig.6.25(b), nw1-2 is biased under  $340nA$  and nw2-1 is biased under  $900nA$ . The devices are connected with the circuit in Transient Measurement mode, where the bias current and gate voltage are set. Finally, the output response of two devices are presented in Fig.6.25(c) and (d). Two solutions with different pH values is used in substitution for the DNA solution. The pH value of solution A is lower than solution B. The lower pH value means the solution is more positive. Thus, solution B increase  $I_D$  and increases output voltage.

Two devices have similar output response, which suggest our method is functional. But still the responses are not exactly same. The voltage difference appears in the are different by 8% ( $\frac{(|\Delta V_1 - \Delta V_2|)}{\Delta V_1}$ ). We can blame the inaccurate biasing current because DC-sweep mode circuit fails in low current and the  $V_G$  is manually adjusted to make the  $I_D$  follows the biasing current. Still there may be other reasons.

Although we keep the devices under a same  $gm$ , the output signals can diverge if they receive incomparable input. The input of the experiment above is the equivalent voltage change induced by the concentration (pH value) difference ( $\Delta V$ ). Its value may be different because of two reasons. One is that the thickness of the each nanowire may not be same. There may be corrosion of the nanowire surface since the devices we use have been produced for more than 2 years and have bedd used repeatedly. The other is the gate coupling effect. The effect caused by the double layer capacitance varies with the gate voltage, which we have mentioned in Section.2.3.

The first reason can be solved by producing a new device. The second reason need the improvement on circuit structure. This reminds us one of the advantages



**Figure 6.25:** The variability-resisting method.

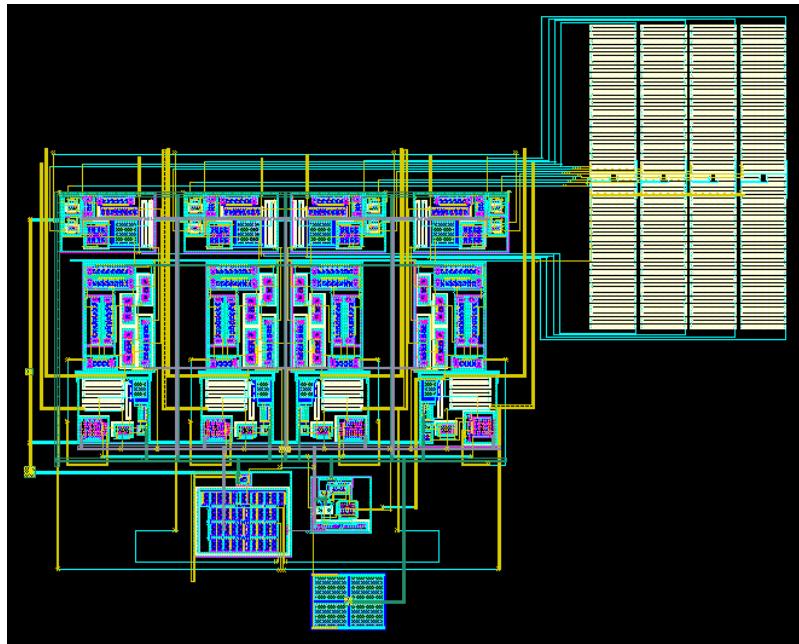
of source follower structure (Section 2.1.2). The structure keeps  $V_G$  constant and adjusts the source voltage of nanowire instead. But changing source voltage will as well change the drain-to-source voltage ( $V_{DS}$ ) of nanowire, which brings about the short channel effect. Therefore, in the future, if our circuit adopts the concept of source follower, the additional feedback network that keeps  $V_{DS}$  constant is required.

Overall, although our method does not entirely remove the device variability problem, it mitigates the problem. Furthermore, the improvement method is proposed and the progress can be looked forward.

# Chapter 7

## Conclusion and Future Work

### 7.1 Conclusion



**Figure 7.1:** The layout of the Readout circuit

Fig.7.1 is the chip layout of the circuit. It contains four unit of the read-out circuits and is able to measure four nanowire devices at the same time.

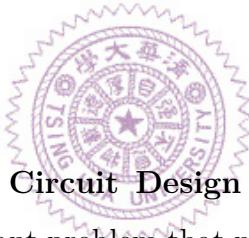
In this project, a circuit with two mode: DC-sweep mode and Transient Measurement mode is designed. The first mode is to perform  $I_D-V_G$  sweep while the second mode is to perform transient measurement. By combining two mode, the circuit perform measurement by the variability-resisting method we proposed in this

project. This method mitigate the device variability problem and can be further improve in the future. In Table.7.1, our circuit is compared with the methods that were reviewed in chapter 2 [8], [9]. Our circuit has wider  $\Delta I$  detection range and lower power consumption when comparing with the similar work [9]. The work in [8] has better performance over all. Still our circuit deals with the device variability problem, which does not be mentioned in both works.

	[8]	[9]	This work
$\Delta I$	$120\mu A \sim 0.12nA$	$3\mu A \sim 60nA$	$3nA \sim 5.3\mu A$ $-15\mu A \sim -3nA$
Power consumption	14.82uW	2mW	1.48mW
CMOS Technology	0.13um	0.18um	0.35um
Device Variability	No Discussion	No Discussion	Variability-resisting method

**Table 7.1:** Specification Summary

## 7.2 Future Work



**7.2.0.0.1 Problems in the Circuit Design** The low current defect in DC-sweep mode is the most important problem that must be solved. The solution for it is to replace the feedback OP with other closed-loop amplifier. Another problem is the oscillation problem that happens when the  $A_{amp}$  of the amplifier in the second-stage circuit is 1. This problem can be solved simply by fixing the insufficient phase margin.

**7.2.0.0.2 Introduce Filter and Better Experimental Process** The noise included in Transient Measurement mode could be removed by simply introduce a bandpass filter. The problem of this is that the signal speed is still hard to be defined. Besides, currently we use pipetman to change the concentration of solution. This process can evoke undesired noise and sometimes may not be carried on smoothly. Both of these factors destroy or affect the speed of the signal. If the process is improved and the signal speed is decided, a filter can be introduced and the noise can be reduced.

Furthermore, for the measurement dealing with the device variability problem, a method to decide when to switch between DC-sweep and Transient Measurement mode is needed. This may be achieved by introducing digital circuit or by adding a feedback circuit for detecting whether the concentration changing reach a balance.

**7.2.0.0.3 The  $\Delta V$  Problem** In Section.6.3, the method is functional but not perfect. We have discussed the improvement methods. They should help the further development of design and finally remove the device variability problem.



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