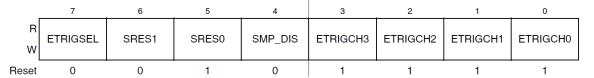
13.3.2.2 ATD Control Register 1 (ATDCTL1)

Writes to this register will abort current conversion sequence.

Module Base + 0x0001



1	6–5	A/D Resolution Select — These bits select the resolution of A/D conversion results. See Table 13-5 for
	SRES[1:0]	coding.

Table 13-5. A/D Resolution Coding

SRES1	SRES0	A/D Resolution
0	0	8-bit data
0	1	10-bit data
1	0	12-bit data
1	1	Reserved

Use table to find resolution #-bit data (mode) and assign remaining register bits 0s.

13.3.2.5 ATD Control Register 4 (ATDCTL4)

Writes to this register will abort current conversion sequence.

Module Base + 0x0004



7–5 Sample Time Select — These three bits select the length of the sample time in units of ATD conversion clock cycles. Note that the ATD conversion clock period is itself a function of the prescaler value (bits PRS4-0). Table 13-14 lists the available sample time lengths.

Table 13-14. Sample Time Select

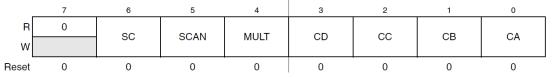
SMP2	SMP1	SMP0	Sample Time in Number of ATD Clock Cycles
0	0	0	4
0	0	1	6
0	1	0	8
0	1	1	10
1	0	0	12
1	0	1	16
1	1	0	20
1	1	1	24

Use table to find sample time per clock cycle on single channel and assign Remaining register bits 0s

13.3.2.6 ATD Control Register 5 (ATDCTL5)

Writes to this register will abort current conversion sequence and start a new conversion sequence. If external trigger is enabled (ETRIGE=1) an initial write to ATDCTL5 is required to allow starting of a conversion sequence which will then occur on each trigger event. Start of conversion means the beginning of the sampling phase.

Module Base + 0x0005



3–0
CD, CC,
CB, CA
Analog Input Channel Select Code — These bits select the analog input channel(s) whose signals are sampled and converted to digital codes. Table 13-16 lists the coding used to select the various analog input channels.

In the case of single channel conversions (MULT=0), this selection code specifies the channel to be examined.

Table 13-16. Analog Input Channel Select Coding

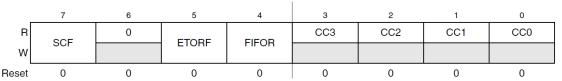
sc	CD	СС	СВ	CA	Analog Input Channel
0	0	0	0	0	AN0
	0	0	0	1	AN1
	0	0	1	0	AN2

Use table to find Analog input channel and assign Remaining register bits 0s

13.3.2.7 ATD Status Register 0 (ATDSTAT0)

This register contains the Sequence Complete Flag, overrun flags for external trigger and FIFO mode, and the conversion counter.

Module Base + 0x0006



Sequence Complete Flag — This flag is set upon completion of a conversion sequence. If conversion sequences are continuously performed (SCAN=1), the flag is set after each one is completed. This flag is cleared when one of the following occurs:

A) Write "1" to SCF

B) Write to ATDCTL5 (a new conversion sequence is started)

C) If AFFC=1 and read of a result register

O Conversion sequence not completed

1 Conversion sequence has completed

13.3.2.12 ATD Conversion Result Registers (ATDDRn)

The A/D conversion results are stored in 16 result registers. Results are always in unsigned data representation. Left and right justification is selected using the DJM control bit in ATDCTL3.

Reading the A/D data. (left justified by default)

ATD0DR0H: Contains the MSByte of the channel 0 result

ATD0DR1H - ATD0DR7H: Contains the MSBytes of the other 7 channels results