電機三 b03901065 林宣竹
電機三 b03901095 簡睿廷

# 積體電路設計 final project

Cell area = 45152 μm 2

Cycle time = 20 ns

Total time = 2719140 ns (gate-level 的 simulation 結果)

Cell area*Total time = 122774609280 μm 2 · $ns$

**我們將 ENDCYCLE 改成 150000

RTL simulation:

```
                      streams:   8, words:  7629
       Loading native compiled code:     ..................... Done
       Building instance specific data structures.
       Design hierarchy summary:
                                Instances  Unique
              Modules:                  2       2
              Registers:               39      39
              Scalar wires:             6       -
              Vectored wires:           4       -
              Always blocks:            3       3
              Initial blocks:           6       6
              Cont. assignments:        0       1
              Pseudo assignments:       1       1
              Simulation timescale:  10ps
       Writing initial simulation snapshot: worklib.testfixture:v
Loading snapshot worklib.testfixture:v ..................... Done
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
-----------------------------------------------------

START!!! Simulation Start .....

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 Congratulations!!! Every outputs are correct!

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Simulation complete via $finish(1) at time 6797850 NS + 0
./testfixture.v:117         $finish;
ncsim> exit
[b03095@cad30 final]$
```

Area report:

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```
*************************************
Report : area
Design : imgproc
Version: G-2012.06
Date   : Mon Jun 26 15:41:17 2017
*************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    slow (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/slow.db)

Number of ports:                           50
Number of nets:                          2412
Number of cells:                         1321
Number of combinational cells:           1013
Number of sequential cells:               273
Number of macros:                           0
Number of buf/inv:                        117
Number of references:                     113

Combinational area:       36974.465399
Noncombinational area:     8178.073158
Net Interconnect area:    281074.758240

Total cell area:          45152.538557
Total area:               326227.296797
1
write -format verilog -hierarchy -output "imgproc_syn.v"
Writing verilog file '/home/raid7_2/userb03/b03095/ICD2017/final/syn/imgproc_syn.v'.
1
write_sdf -version 1.0  -context verilog  -load_delay net  imgproc_syn.sdf
Information: Writing timing information to file '/home/raid7_2/userb03/b03095/ICD2017/final/syn/imgproc_syn.sdf'. (WT-3)
1
1
dc_shell>
```

Timing report:

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : imgproc
Version: G-2012.06
Date   : Mon Jun 26 15:41:55 2017
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: array_reg_4__2__1_
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: imgproc_data_reg_7_
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  imgproc            tsmc13_wl10           slow

  Point                                                   Incr       Path
  --------------------------------------------------------------------------
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.50       0.50
  array_reg_4__2__1_/CK (DFFX1)                           0.00       0.50 r
  array_reg_4__2__1_/Q (DFFX1)                            0.68       1.18 r
  mult_245_3/a[1] (imgproc_DW_mult_uns_2)                 0.00       1.18 r
  mult_245_3/U52/Y (CLKBUFX2)                             0.23       1.41 r
  mult_245_3/product[1] (imgproc_DW_mult_uns_2)           0.00       1.41 r
  add_16_root_add_0_root_add_245_5/A_1_ (imgproc_DW01_add_19)
                                                          0.00       1.41 r
  add_16_root_add_0_root_add_245_5/U1_1/CO (ADDFXL)       0.74       2.15 r
  add_16_root_add_0_root_add_245_5/U1_2/CO (ADDFXL)       0.50       2.65 r
  add_16_root_add_0_root_add_245_5/U1_3/S (ADDFXL)        0.81       3.46 r
  add_16_root_add_0_root_add_245_5/SUM_3_ (imgproc_DW01_add_19)
                                                          0.00       3.46 r
  More
```

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```
                                                  0.00       3.46 r
U718/Y (XOR2X1)                                   0.39       3.86 r
add_5_root_add_0_root_add_245_5/B_3_ (imgproc_DW01_add_9)
                                                  0.00       3.86 r
add_5_root_add_0_root_add_245_5/U1_3/S (ADDFXL)   0.90       4.76 f
add_5_root_add_0_root_add_245_5/SUM_3_ (imgproc_DW01_add_9)
                                                  0.00       4.76 f
add_4_root_add_0_root_add_245_5/A_3_ (imgproc_DW01_add_7)
                                                  0.00       4.76 f
add_4_root_add_0_root_add_245_5/U1_3/S (ADDFXL)   0.73       5.49 r
add_4_root_add_0_root_add_245_5/SUM_3_ (imgproc_DW01_add_7)
                                                  0.00       5.49 r
add_2_root_add_0_root_add_245_5/A_3_ (imgproc_DW01_add_4)
                                                  0.00       5.49 r
add_2_root_add_0_root_add_245_5/U1_3/S (ADDFXL)   0.86       6.35 f
add_2_root_add_0_root_add_245_5/SUM_3_ (imgproc_DW01_add_4)
                                                  0.00       6.35 f
add_0_root_add_0_root_add_245_5/A_3_ (imgproc_DW01_add_2)
                                                  0.00       6.35 f
add_0_root_add_0_root_add_245_5/U23/Y (OAI21XL)   0.50       6.86 r
add_0_root_add_0_root_add_245_5/U22/Y (OAI2BB1X1) 0.27       7.13 f
add_0_root_add_0_root_add_245_5/U21/Y (OAI21XL)   0.48       7.61 r
add_0_root_add_0_root_add_245_5/U20/Y (OAI2BB1X1) 0.27       7.89 f
add_0_root_add_0_root_add_245_5/U19/Y (OAI21XL)   0.48       8.36 r
add_0_root_add_0_root_add_245_5/U18/Y (OAI2BB1X1) 0.27       8.64 f
add_0_root_add_0_root_add_245_5/U17/Y (OAI21XL)   0.48       9.12 r
add_0_root_add_0_root_add_245_5/U16/Y (OAI2BB1X1) 0.27       9.39 f
add_0_root_add_0_root_add_245_5/U15/Y (OAI21XL)   0.48       9.87 r
add_0_root_add_0_root_add_245_5/U14/Y (OAI2BB1X1) 0.27      10.15 f
add_0_root_add_0_root_add_245_5/U13/Y (OAI21XL)   0.48      10.63 r
add_0_root_add_0_root_add_245_5/U12/Y (OAI2BB1X1) 0.27      10.90 f
add_0_root_add_0_root_add_245_5/U11/Y (OAI21XL)   0.48      11.38 r
add_0_root_add_0_root_add_245_5/U10/Y (OAI2BB1X1) 0.27      11.65 f
add_0_root_add_0_root_add_245_5/U9/Y (OAI21XL)    0.48      12.13 r
add_0_root_add_0_root_add_245_5/U8/Y (OAI2BB1X1)  0.27      12.41 f
add_0_root_add_0_root_add_245_5/U7/Y (OAI21XL)    0.48      12.89 r
add_0_root_add_0_root_add_245_5/U6/Y (OAI2BB1X1)  0.27      13.16 f
add_0_root_add_0_root_add_245_5/U5/Y (OAI21XL)    0.48      13.64 r
add_0_root_add_0_root_add_245_5/U4/Y (OAI2BB1X1)  0.27      13.92 f
add_0_root_add_0_root_add_245_5/U1/Y (OAI21XL)    0.48      14.40 r
add_0_root_add_0_root_add_245_5/U3/Y (OAI2BB1X1)  0.20      14.60 f
```

```
add_0_root_add_0_root_add_245_5/U1_14/CO (ADDFXL)        0.52      15.11 f
add_0_root_add_0_root_add_245_5/U1_15/CO (ADDFXL)        0.53      15.64 f
add_0_root_add_0_root_add_245_5/U1_16/CO (ADDFXL)        0.53      16.17 f
add_0_root_add_0_root_add_245_5/U1_17/CO (ADDFXL)        0.53      16.70 f
add_0_root_add_0_root_add_245_5/U1_18/CO (ADDFXL)        0.53      17.22 f
add_0_root_add_0_root_add_245_5/U1_19/CO (ADDFXL)        0.53      17.75 f
add_0_root_add_0_root_add_245_5/U1_20/CO (ADDFXL)        0.53      18.28 f
add_0_root_add_0_root_add_245_5/U1_21/CO (ADDFXL)        0.52      18.80 f
add_0_root_add_0_root_add_245_5/U2/Y (XOR2X1)            0.38      19.19 r
add_0_root_add_0_root_add_245_5/SUM_22_ (imgproc_DW01_add_2)
                                                         0.00      19.19 r
add_250/A[7] (imgproc_DW01_inc_5)                        0.00      19.19 r
add_250/U1/Y (XOR2X1)                                    0.39      19.57 r
add_250/SUM[7] (imgproc_DW01_inc_5)                      0.00      19.57 r
U916/Y (AOI22X1)                                         0.19      19.77 f
U915/Y (OAI21XL)                                         0.30      20.06 r
imgproc_data_reg_7_/D (DFFSRXL)                          0.00      20.06 r
data arrival time                                                  20.06

clock clk (rise edge)                                   20.00      20.00
clock network delay (ideal)                              0.50      20.50
clock uncertainty                                       -0.10      20.40
imgproc_data_reg_7_/CK (DFFSRXL)                         0.00      20.40 r
library setup time                                      -0.32      20.08
data required time                                                 20.08
-----------------------------------------------------------------------------
data required time                                                 20.08
data arrival time                                                 -20.06
-----------------------------------------------------------------------------
slack (MET)                                                        0.02
```

Simulation result:

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```
                        streams:   9, words:  8370
        Loading native compiled code:     ..................... Done
        Building instance specific data structures.
        Design hierarchy summary:
                                    Instances  Unique
                Modules:                 2259     120
                UDPs:                     274       3
                Primitives:              6958       8
                Timing outputs:          3343      48
                Registers:                284      22
                Scalar wires:            3651       -
                Expanded wires:             8       1
                Always blocks:              1       1
                Initial blocks:             7       7
                Pseudo assignments:         1       1
                Timing checks:           2077     267
                Interconnect:            5984    3305
                Delayed tcheck signals:   659     250
                Simulation timescale:     1ps
        Writing initial simulation snapshot: worklib.testfixture:v
Loading snapshot worklib.testfixture:v ..................... Done
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
-----------------------------------------------------

START!!! Simulation Start .....

-----------------------------------------------------

=================================================

 Congratulations!!! Every outputs are correct!

=================================================

Simulation complete via $finish(1) at time 2719140 NS + 0
./testfixture.v:117         $finish;
ncsim> exit
[b03095@cad30 final]$
```