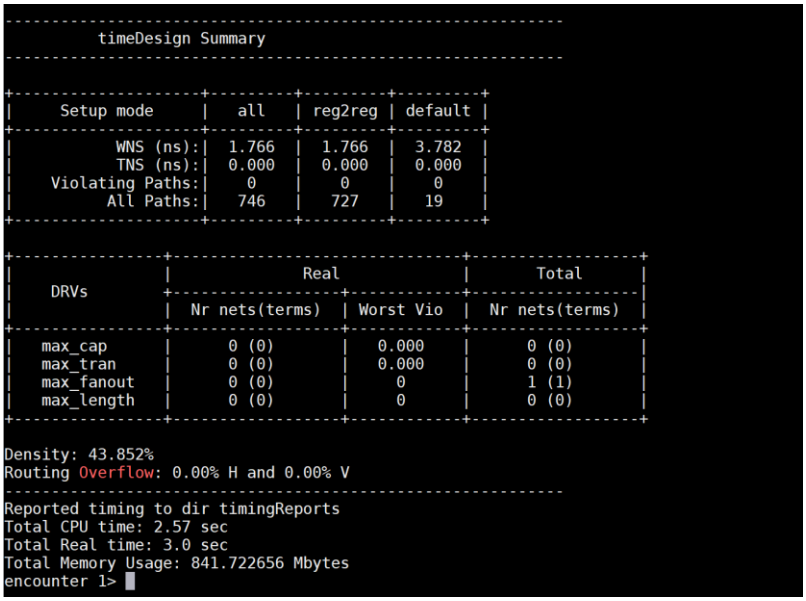
CVSD HW6 Report

**LMFE.v from b03901142

Basic (75%)

1. Topic & timing/delay information.
   A. Pre-CTS timing report



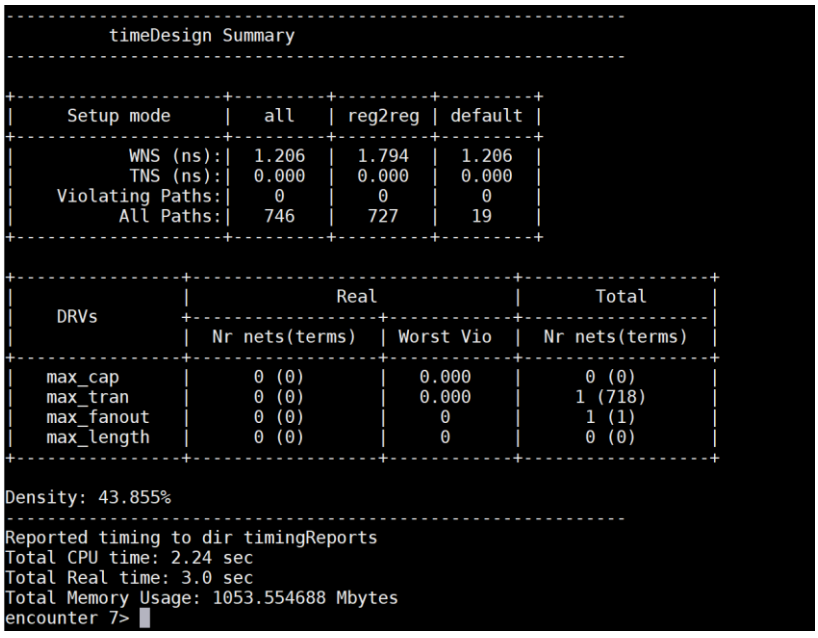
```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  1.766  |  1.766  |  3.782  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   746   |   727   |   19    |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      1 (1)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 43.852%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 2.57 sec
Total Real time: 3.0 sec
Total Memory Usage: 841.722656 Mbytes
encounter 1>
```

   B. Post-route timing report



```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  1.206  |  1.794  |  1.206  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   746   |   727   |   19    |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |     1 (718)      |
|   max_fanout   |      0 (0)       |     0      |      1 (1)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 43.855%
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 2.24 sec
Total Real time: 3.0 sec
Total Memory Usage: 1053.554688 Mbytes
encounter 7>
```

   C. Design constraints:
      i. func_mode: (LMFE_DC.sdc)

```
# You can only modify clock period
set cycle   10.0

#don't modify the following part
create_clock -period $cycle [get_ports  clk]
set_dont_touch_network      [get_clocks clk]
set_clock_uncertainty 0.1  [get_clocks clk]
set_clock_latency     2  [get_clocks clk]
set t_in [expr $cycle/2]
set_input_delay  1  -clock clk [remove_from_collection [all_inputs] [get_ports clk]]
set_output_delay 3      -clock clk [all_outputs]
set_load         1     [all_outputs]
set_drive        1     [all_inputs]

set_operating_conditions -max_library slow -max slow
set_wire_load_model -name tsmc13_wl10 -library slow

set_max_fanout 20 [all_inputs]
```

ii. scan_mode: (CHIP_scan_ideal.sdc)

```
# You can only modify clock period
set cycle   100.0

#don't modify the following part
create_clock -period $cycle [get_ports  clk]
set_clock_latency     2  [get_clocks clk]
set_input_delay  1  -clock clk [remove_from_collection [all_inputs] [get_ports clk]]
set_output_delay 3      -clock clk [all_outputs]
```

2. Synthesis reports & DFT-related reports (summarized).
***由於後來助教說明不一定需要插入scan chains，以下只附上synthesis後的timing, area, power report。

Timing report: (LMFE_syn_timing.rpt)

```
clock clk (rise edge)                    10.00      10.00
clock network delay (ideal)               2.00      12.00
clock uncertainty                        -0.10      11.90
PE24/state_reg/CK (DFFRX1)                0.00      11.90 r
library setup time                       -0.27      11.63
data required time                                  11.63
-----------------------------------------------------------
data required time                                  11.63
data arrival time                                  -11.63
-----------------------------------------------------------
slack (MET)                                         0.01
```

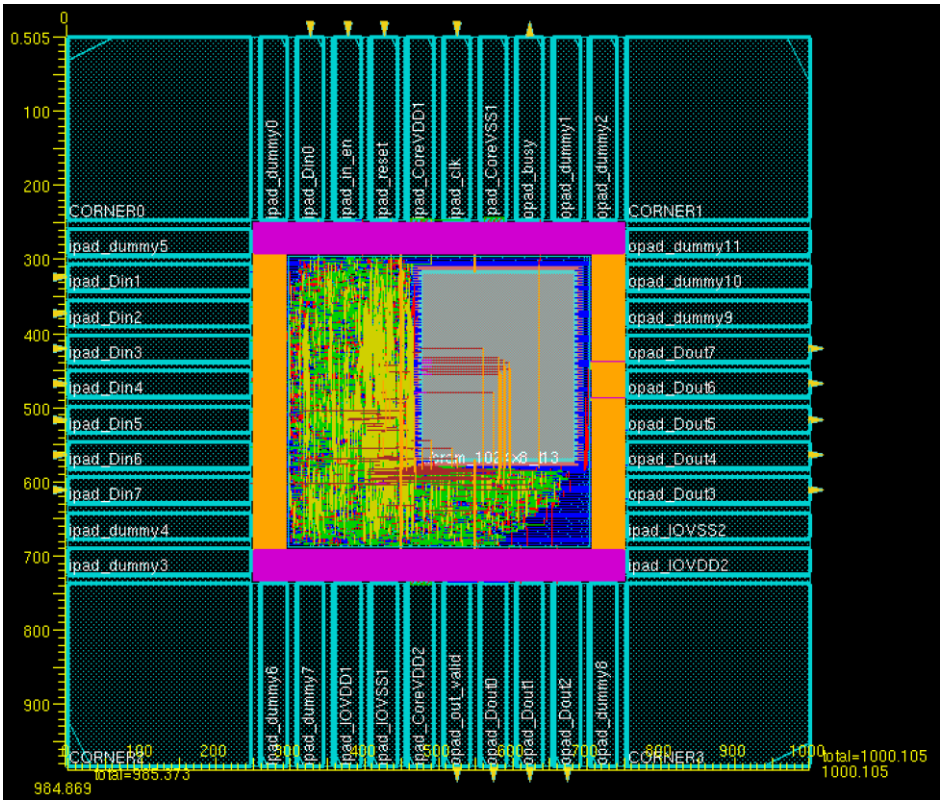
Area report: (LMFE_syn_area.rpt)

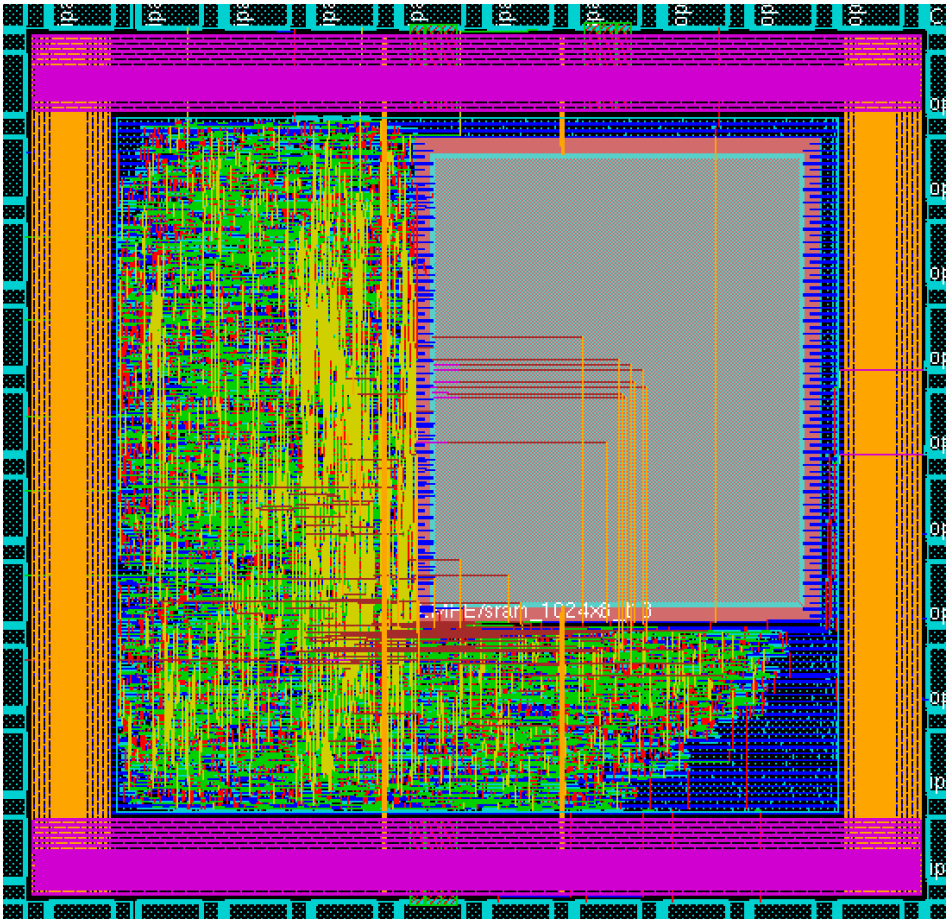
```
Combinational area:              18735.901210
Buf/Inv area:                     1800.941380
Noncombinational area:           23237.405247
Macro/Black Box area:            69557.296875
Net Interconnect area:          390695.345673

Total cell area:                111530.603332
Total area:                     502225.949004
```

3. Final chip layout figure (big & clear enough to see) & chip size (*um x um*).

A. Chip layout figure





B. Chip size

984.869*1000.105=984972.411 um^2

4. Pre-layout & post-layout simulation results (summarized).

A. Pre-layout Simulation

clock = 10ns

```
Output pixel: 0 ~ 16000 are correct!

----------------------------------------------------

Congratulations! All data have been generated successfully!

------------------------PASS------------------------

Simulation complete via $finish(1) at time 2931251 NS + 0
./ori_testfixture.v:135       #(`CYCLE/2); $finish;
ncsim> exit
[b03095@cad29 HW6_ref]$
```

B. Post-layout Simulation

clock = 100ns (somehow influenced by scan.sdc)

```
Output pixel: 0 ~ 16000 are correct!

----------------------------------------------------

Congratulations! All data have been generated successfully!

------------------------PASS------------------------

Simulation complete via $finish(1) at time 29312501 NS + 0
./testfixture1.v:136       #(`CYCLE/2); $finish;
ncsim> exit
[b03095@cad29 HW6_ref]$
```

Advanced (25%)

5. Complete power planning (VDD/VSS/IOVDD/IOVSS number, power ring/strips width, voltage drop & electron migration figures…).

A. Figure

Power Analysis:

```
Total Power
-----------------------------------------------------------------------------------------
Total Internal Power:       17.28671642           93.9270%
Total Switching Power:       1.05695994            5.7430%
Total Leakage Power:         0.06074363            0.3300%
Total Power:                18.40441993
-----------------------------------------------------------------------------------------
```

B. VDD/VSS/IOVDD/IOVSS number:

VDD: 2

VSS: 1

IOVDD: 2

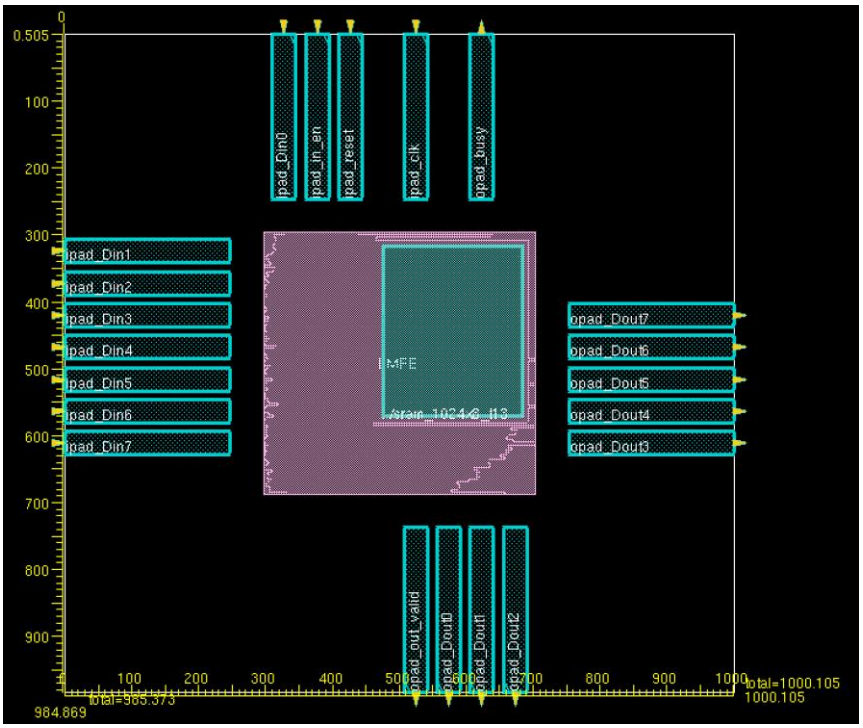
IOVSS: 2

C. Power ring/strips width

Power ring width: 1.2

Power strips width: 1

6. Better I/O & modules' placement (explanations, amoeba view…).



Explanation:

將data input ports集中放在左邊，data output ports集中放在右下，control input在上，dataflow由左到右、由上到下，主要是參考Lab6的CHIP.ioc pad擺放方式。除了I/O之外，也加入幾個dummy pad(沒有連接到任何i/o, power)讓chip的面積增加，P&R的時候比較容易符合design constraints。

7. Other related discussions.

None.