Group 24
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DPA Design Report

1. Layout Area: 27032.13

```
************************* Analyze Floorplan **************************
    Die Area(um^2)             : 34146.36
    Core Area(um^2)            : 27032.13
    Chip Density (Counting Std Cells and MACROs and IOs): 78.959%
    Core Density (Counting Std Cells and MACROs): 99.739%
    Average utilization        : 100.000%
    Number of instance(s)      : 1998
    Number of Macro(s)         : 0
    Number of IO Pin(s)        : 93
    Number of Power Domain(s)  : 0
************************* Estimation Results *************************
**********************************************************************
```

2. Total Power: 1.34e-05

```
                                  Int      Switch   Leak     Total
Hierarchy                         Power    Power    Power    Power    %
-------------------------------------------------------------------------
DPA                               5.97e-06 1.16e-06 6.25e-06 1.34e-05 100.0
```

```
                                  Peak     Peak           Glitch   X-tran
Hierarchy                         Power    Time           Power    Power
-------------------------------------------------------------------------
DPA                               3.22e-03 152506500-152506510
                                                          9.80e-11    0.000
```

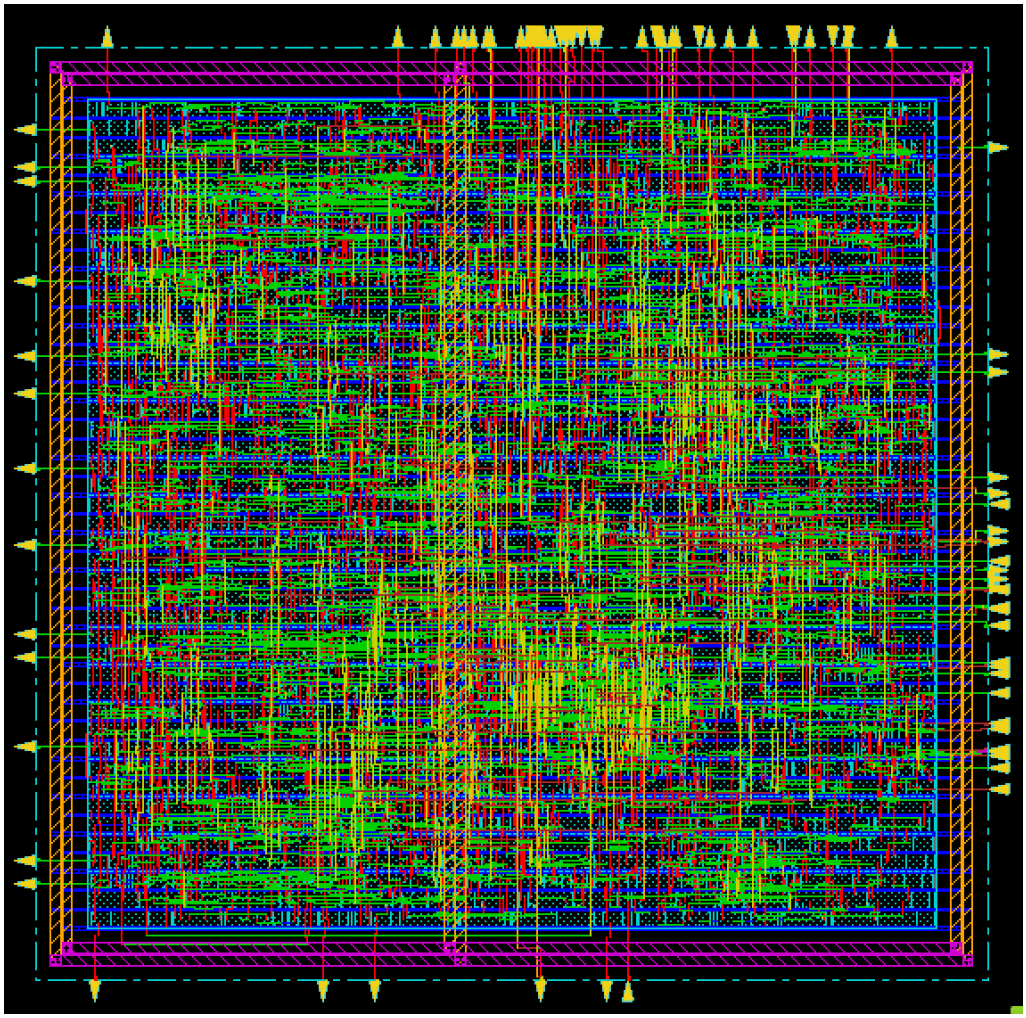
3. Area * Power = 0.362230542, pass baseline.
   (baseline = 1.49e-05 * 25002.92 = 0.3725435508)
4. DRC 錯誤總數量: 0

```
 *** Starting Verify Geometry (MEM: 889.5) ***

  VERIFY GEOMETRY ..... Starting Verification
  VERIFY GEOMETRY ..... Initializing
  VERIFY GEOMETRY ..... Deleting Existing Violations
  VERIFY GEOMETRY ..... Creating Sub-Areas
                  ..... bin size: 8320
  VERIFY GEOMETRY ..... SubArea : 1 of 1
  VERIFY GEOMETRY ..... Cells          :  0 Viols.
  VERIFY GEOMETRY ..... SameNet        :  0 Viols.
  VERIFY GEOMETRY ..... Wiring         :  0 Viols.
  VERIFY GEOMETRY ..... Antenna        :  0 Viols.
  VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 2.00
Begin Summary ...
  Cells       : 0
  SameNet     : 0
  Wiring      : 0
  Antenna     : 0
  Short       : 0
  Overlap     : 0
End Summary

  Verification Complete : 0 Viols.  0 Wrngs.

**********End: VERIFY GEOMETRY**********
```

5. LVS 錯誤總數量: 0

```
******** Start: VERIFY CONNECTIVITY ********
Start Time: Wed Jun 27 14:21:01 2018

Design Name: DPA
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (186.7350, 182.8600)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Wed Jun 27 14:21:01 2018
Time Elapsed: 0:00:00.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.1  MEM: 0.000M)
```

6. Floorplan



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7. Design Technique
   A. 由 global_time 進行時間和 state 的控制，每個 clk 會往上加 1
   B. 由於轉場的時候必須先處理一部份的點，等 0.2 秒之後再處理剩下的點，因此，對於第一張不須轉場效果的相片，也是先處理前半部的點，再處理剩下的。至於時間的部分則是統一在第一部份處理。
   C. 因為在 512x512 時，處理每一個點的時間至少需 5 個 cycle，而且此 design 不需考慮 running time，因此決定對於 256x256、128x128，每一個點也用 5 個 cycle 處理，減少 code 的複雜度。
   D. 利用 x_addr, y_addr 進行 address 的控制：512x512 及 128x128 需讀取 4 個點、256x256 讀取一個點，利用 x_addr, y_addr 決定讀取 memory 的 address 及最後寫入 Frame buffer 的 address。
   E. 將時間資訊存在 Time_arr 中，再利用 y_addr 決定現在要讀取此數字的哪一個 addr。
      (i.e. y_addr = 232, Time_arr[i] = 1 => CR_A = 1*24 + 0 = 24
      y_addr = 234, Time_arr[i] = 3 => CR_A = 3*24 + 2 = 74)

8. Finite State Machine