SOC Encounter Homework

助教聯絡方式：

呂祐昇 yslu@eda.ee.ntu.edu.tw

王于哲 r05943016@ntu.edu.tw

Description

In this homework, you are going to implement your Verilog HW3 designs into GDSII layout. Please add to your synthesized design with scan chains, and include *pad cells* for SOC Encounter. Finally, you need to submit an electronic *report* (upload to FTP) describing what you have done. (There is no particular report style. However, please include the specified items.)

Design Libraries & Data Preparation

You can choose to add pad cells after synthesis, or before synthesis (use a wrapper-like gate-level top module with pad cells to include your RTL, more preferable). However, notice that the input/output delay's definitions will be different. The SDC file is not part of the library, so you should create it by yourself, or you can use *write_sdc* in DV to generate it automatically. If the memory compiler is needed, related information can be found in Verilog Lab2. Be sure to generate all the memory data/libraries for SOC Encounter. Finally, you can check the Lab for more hints.

Submission Deadline:

Online Submission (FTP):

Deadline	2018/06/12 12:00
IP	140.112.18.84
Port	1232
Account	CVSD_STUDENT
Password	cvsd2018

Please submit a zipped PDF report named *StudentID_HW6.zip*, including:

Basic (75%)

1. Topic & timing/delay information.

A. 15% (只要有看到 timing report or sdc content，基本上都會滿分)

B. 有一些不合常理的情況（例如 number of path = 0），會拿不到滿分

2. Synthesis reports & DFT-related reports (summarized).

A. 20% (只要有 Synthesis reports 和 DFT-related reports（必須顯示有 scan chain 發生作用，譬如 port、area 增加之類）)

B. 有人重複貼了相同內容上去或是只貼了 Synthesis reports 上去。這就只有拿到 Synthesis reports 分數（12%）

C. 只貼 DFT-related reports or scan chain 相關訊息上去，分數會高於只貼Synthesis reports，理由是這一步驟應該是為了確認有無操作 DFT。

3. Final chip layout figure (big & clear enough to see) & chip size (*um x um*).
A. 20%(只要有圖、有 size 出現就會滿分)
B. 只有圖（12%）
C. 只有 size (12%)

D. 另外有其他因素，會被減少一點分數（例如：不是" Final" chip layout figure）

4. Pre-layout & post-layout simulation results (summarized).
A. 20% (只要有測 Pre-layout & post-layout，就會滿分)
B. 只測 Pre-layout (12%)

C. 有一個 testbench 沒有過，會少一分。

Advanced (25%)

5. Complete power planning (VDD/VSS/IOVDD/IOVSS number, power ring/strips width, voltage drop & electron migration figures…).
A. 10% (有說明、要求的圖都有就會滿分)
B. 只有說明及 power ring/strips（4~7%）
C. 提供更少資訊，會再更少分數
6. Better I/O & modules' placement (explanations, amoeba view…).
A. 10% (有說明、有圖就會滿分)
B. 只有說明（5%~8%）
C. 提供更少資訊，會再更少分數
7. Other related discussions.

A. 5% (除非特別好、特別針對其他因素討論，才會滿分)

B. 有基本的說明（3~4%）

C. 只貼圖（2%）