電機四 b03901095 簡睿廷

CVSD HW5 Report

1. Faults in path.v

   (1) overflow assignment

   Original: overflow_o = valid_i && full;

   Failed assertion: assert_never_overflow_bb

   Modified: overflow_o = valid_i && full && !gnt_i;

   Explanation: 原本沒有考慮 full 時在 FIFO 同時有 read 和 write 的情況，儘管此時為 full，但同時有 read & write，也就是有 gnt，則不會有 overflow 發生。

   (2) underflow assignment

   Original: underflow_o = gnt_i && empty;

   Failed assertion: assert_never_underflow_bb

   Modified: underflow_o = gnt_i && empty && (write_i == 0);

   Explanation: 原本沒有考慮 empty & gnt 時，若此時有資料進入，則 data 會直接 assign 給 output，不會進入 FIFO(也就是發生 bypass)，因此不會發生 underflow

2. Faults in fifo.v

   (1) rd_ptr & wr_ptr increment

   Original:

```
rd_ptr <= (rd_ptr == ((1<<ADDR_WIDTH) - 1)) ?
    {ADDR_WIDTH{1'b0}} : rd_ptr + 1;
wr_ptr <= (wr_ptr == ((1<<ADDR_WIDTH) - 1)) ?
    {ADDR_WIDTH{1'b0}} : wr_ptr + 1;
```

   Failed assertions:

```
assert_full_ptr_wb
assert_empty_ptr_wb
assert_emptyDataBypass_wb
```

   Modified:

```
rd_ptr <= (rd_ptr == FDEPTH -1) ?
    {ADDR_WIDTH{1'b0}} : rd_ptr + 1;
wr_ptr <= (wr_ptr == FDEPTH -1) ?
    {ADDR_WIDTH{1'b0}} : wr_ptr + 1;
```

   Explanation: rd_ptr & wr_ptr increment 的時候(3’d0~3’d5)超過 FDEPTH(3’d4)，導致判斷 empty 和 full 的時候發生錯誤。

   (2) empty & full determination

Original:

```
empty <= (rd_ptr == wr_ptr - 1);
```

Failed assertions:

```
assert_data_good_bb
```

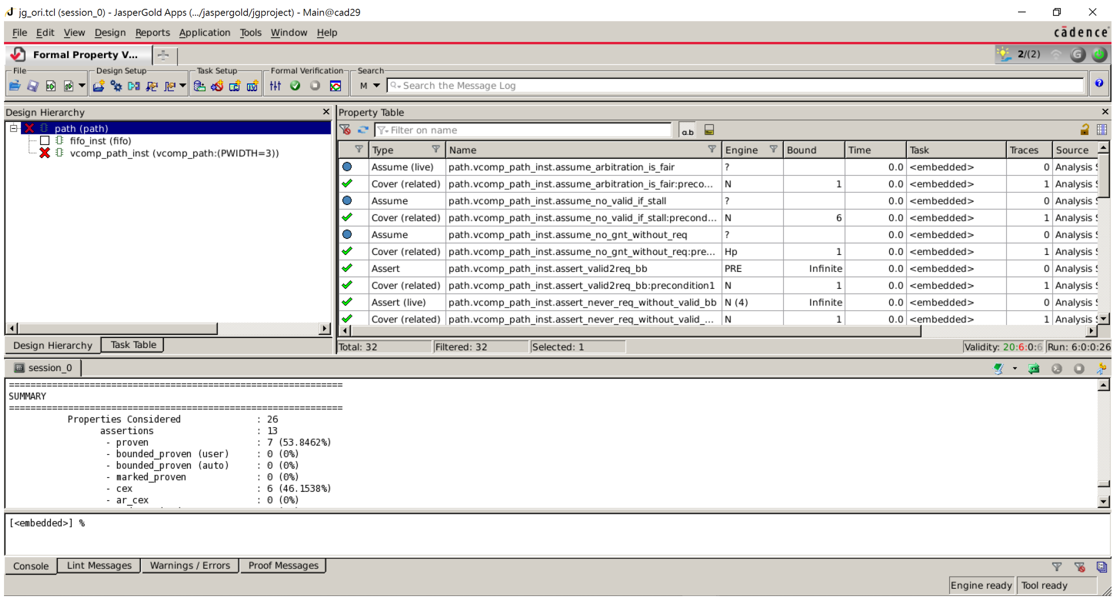
Modified:

```
empty <= (rd_ptr == wr_ptr - 1) || ((wr_ptr == 0) &&
(rd_ptr == FDEPTH -1));
```

Explanation:判斷 empty 的時候發生錯誤，沒有考慮到 wr_ptr == 0 且 rd_ptr == FDEPTH-1 時，做完 read 也會造成 empty，導致 path.v 沒有判斷到 bypass，因此在 output 發生錯誤，連帶造成 ptr 繼續出錯。

3.

Report with bugs:



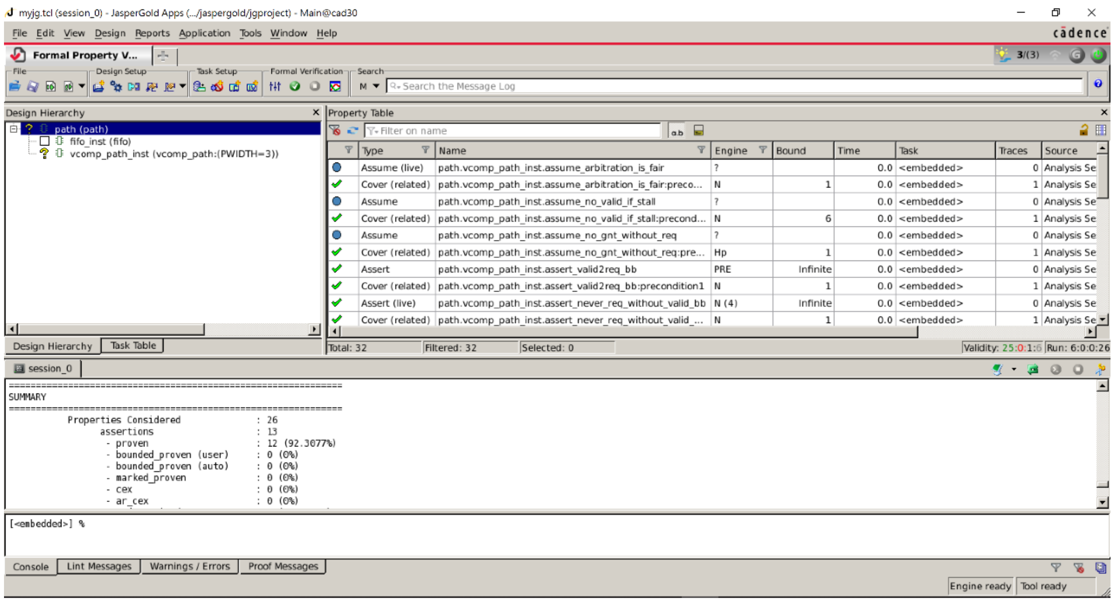
	Type	Name	Engine	Bound	Time	Task	Traces	Source
●	Assume (live)	path.vcomp_path_inst.assume_arbitration_is_fair	?		0.0	<embedded>	0	Analysis
✓	Cover (related)	path.vcomp_path_inst.assume_arbitration_is_fair:preco...	N	1	0.0	<embedded>	1	Analysis
●	Assume	path.vcomp_path_inst.assume_no_valid_if_stall	?		0.0	<embedded>	0	Analysis
✓	Cover (related)	path.vcomp_path_inst.assume_no_valid_if_stall:precond...	N	6	0.0	<embedded>	1	Analysis
●	Assume	path.vcomp_path_inst.assume_no_gnt_without_req	?		0.0	<embedded>	0	Analysis
✓	Cover (related)	path.vcomp_path_inst.assume_no_gnt_without_req:pre...	Hp	1	0.0	<embedded>	1	Analysis
✓	Assert	path.vcomp_path_inst.assert_valid2req_bb	PRE	Infinite	0.0	<embedded>	0	Analysis
✓	Cover (related)	path.vcomp_path_inst.assert_valid2req_bb:precondition1	N	1	0.0	<embedded>	1	Analysis
✓	Assert (live)	path.vcomp_path_inst.assert_never_req_without_valid_bb	N (4)	Infinite	0.0	<embedded>	0	Analysis
✓	Cover (related)	path.vcomp_path_inst.assert_never_req_without_valid_...	N	1	0.0	<embedded>	1	Analysis

Total: 32 Filtered: 32 Selected: 1 Validity: 20:6:0:6 Run: 6:0:0:26

```
============================================================
SUMMARY
============================================================
          Properties Considered             : 26
                assertions                  : 13
                 - proven                   : 7 (53.8462%)
                 - bounded_proven (user)    : 0 (0%)
                 - bounded_proven (auto)    : 0 (0%)
                 - marked_proven            : 0 (0%)
                 - cex                      : 6 (46.1538%)
                 - ar_cex                   : 0 (0%)
```

```
[<embedded>] %
```

Report with No bugs:



	Type	Name	Engine	Bound	Time	Task	Traces	Source
●	Assume (live)	path.vcomp_path_inst.assume_arbitration_is_fair	?		0.0	<embedded>	0	Analysis Se
✓	Cover (related)	path.vcomp_path_inst.assume_arbitration_is_fair:preco...	N	1	0.0	<embedded>	1	Analysis Se
●	Assume	path.vcomp_path_inst.assume_no_valid_if_stall	?		0.0	<embedded>	0	Analysis Se
✓	Cover (related)	path.vcomp_path_inst.assume_no_valid_if_stall:precond...	N	6	0.0	<embedded>	1	Analysis Se
●	Assume	path.vcomp_path_inst.assume_no_gnt_without_req	?		0.0	<embedded>	0	Analysis Se
✓	Cover (related)	path.vcomp_path_inst.assume_no_gnt_without_req:pre...	Hp	1	0.0	<embedded>	1	Analysis Se
✓	Assert	path.vcomp_path_inst.assert_valid2req_bb	PRE	Infinite	0.0	<embedded>	0	Analysis Se
✓	Cover (related)	path.vcomp_path_inst.assert_valid2req_bb:precondition1	N	1	0.0	<embedded>	1	Analysis Se
✓	Assert (live)	path.vcomp_path_inst.assert_never_req_without_valid_bb	N (4)	Infinite	0.0	<embedded>	0	Analysis Se
✓	Cover (related)	path.vcomp_path_inst.assert_never_req_without_valid_...	N	1	0.0	<embedded>	1	Analysis Se

Total: 32 Filtered: 32 Selected: 0 Validity: 25:0:1:6 Run: 6:0:0:26

```
================================================================
SUMMARY
================================================================
           Properties Considered             : 26
                 assertions                  : 13
                  - proven                   : 12 (92.3077%)
                  - bounded_proven (user)    : 0 (0%)
                  - bounded_proven (auto)    : 0 (0%)
                  - marked_proven            : 0 (0%)
                  - cex                      : 0 (0%)
                  - ar_cex                   : 0 (0%)
```

```
[<embedded>] %
```

4. 即使是有 bug 的 RTL code，也會被 proved 的 assertions

(1) assert_valid2req_bb : assert property (@(posedge clk) (valid_i |-> req_o));

(2) assert_never_req_without_valid_bb : assert property (@(posedge clk) valid_i |-> (##[0:$] req_o));

(3) assert_data_bypass_bb : assert property (@(posedge clk) (($rose(req_o) && gnt_i) |-> (data_o == data_i)));

(4) assert_never_full_empty_wb : assert property (@(posedge clk) !(full && empty));

(5) assert_noPopRemainFull_wb : assert property (@(posedge clk) ((full && !read_i) |=> full));

(6) assert_noPushRemainEmpty_wb : assert property (@(posedge clk) ((empty && !write_i) |=> empty));

(7) assert_emptyData_wb : assert property (@(posedge clk) ((empty && valid_i && gnt_i) |-> (data_i == data_o)));