A Fixed Point Variable Sample Rate Frequency Adaptive Bandpass Filter for Extraction of Synchronization Information from AC Utility Network Signals

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1 Abstract

This paper presents design procedures for two adaptive bandpass filters with variable sample rates and fixed point implementations. Each bandpass filter can be used as an integral part of a Multirate Phase Lock Loop (MPLL) for extracting the fundamental component from an input signal. The MPLL provides synchronization information from zero crossings of power system AC signals. The MPLL incorporates frequency adaptation intrinsically by generating a sample signal which is an integer multiple of the fundamental frequency component. The integer multiple frequency is used as a sampling signal for all signal processing/filtering blocks within the MPLL. The bandpass filter ensures that the MPLL is robust against disturbances that appear on the power system. Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) architectures are studied for the design of bandpass filters. The FIR architecture offers unconditional stability and ease of implementation and hence is selected for the MPLL. The FIR filter is implemented on a Xilinx field programmable gate array.

2 Introduction

The supply of high quality electrical energy is a major objective of power system operators [1]. Accurate estimation and quick access to synchronization information such as frequency, amplitude, and phase are indispensable goals in achieving a high quality power supply [2, 3]. In a three phase system, the synchronization information is obtained by extracting the positive sequence component of the fundamental component. In single phase systems the line to line voltage is acquired for synchronization purposes. A simplified block diagram showing a synchronization system for a converter application is shown in Figure 1.

Utility applications, in most cases, have a constant frequency which varies by only a small percentage. In contrast, in the airline industry the frequency can vary over a much wider frequency range and this poses challenges for the synchronization system. In both cases, the incoming signal has superimposed disturbances that introduce additional constraints on the design of a robust synchronization system.

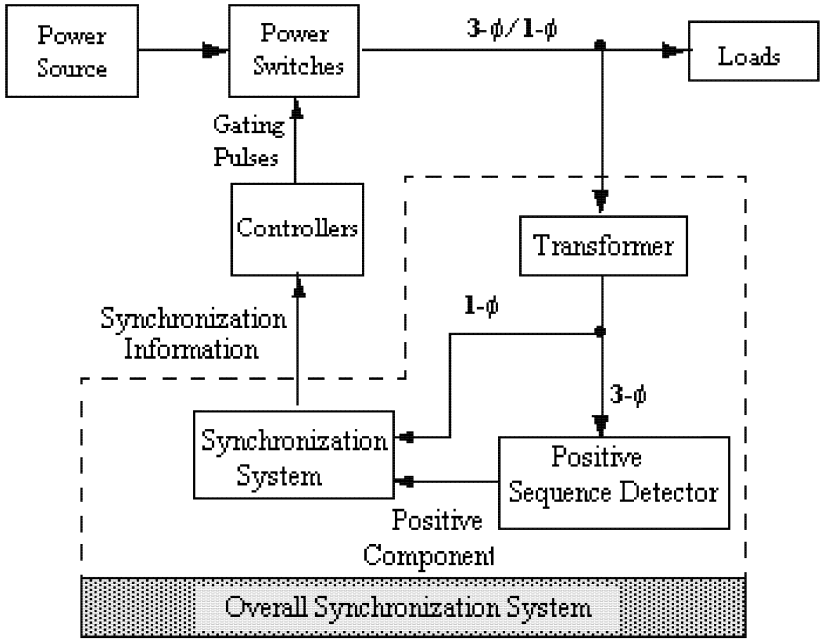


Fig. 1: A simplified block diagram of a typical synchronization for control of a converter.

A common approach for synchronization to a single phase input is to employ an analog phase locked loop (PLL). This PLL is not immune to input line distortion and does not lend itself well to designs that require frequency adaptation. Recently an Enhanced Phase Lock Loop (EPLL) that is based on a phase locked loop (PLL) architecture has been proposed [4]. The EPLL allows the designer to extract the amplitude, phase angle, and frequency of the fundamental component of an input signal [5]. The frequency range of the EPLL is restricted to utility networks and no experimental results have been provided. Another approach to synchronization that has been proposed is an Adaptive Fourier Transform [6]. This method was designed as a zero crossing detector for power converter applications. Harmonics or notches are removed and the system is frequency adaptive. However, the results that were presented were only preliminary and hence the limitations of the system are not currently known.

An approach for synchronizing to a positive sequence component given an undistorted line voltage has been proposed in [7, 8]. A positive sequence synchronization approach that is immune to distortion has been reported in [9]. The latter approach does not lend itself well to applications where the line frequency deviates significantly. This stems from the fact that the positive sequence detector implementation is not frequency adaptive. In summary, the existing synchronization methods are frequency adaptive over a limited frequency range or their performance has been verified experimentally under a limited set of disturbance conditions.

The conventional way of removing specific frequency components from a nonstationary signal is to use an adaptive filter. The transfer function coefficients of the adaptive filter are changed using least-mean squares (LMS) or recursive least-squares (RLS) algorithms [10] and reflect a change in the fundamental frequency. However the adaptive LMS and RLS algorithms have their own limitations for convergence speed and computational complexity [10]. The computational resources required to implement algorithms become problematic as the order of the adaptive filters increase.

An alternate approach to transfer function coefficient adaptation is to adjust the sample rate so as to maintain a constant ratio between the sampling frequency (f_s) and the fundamental component frequency (f_b) based on the following relation,

$$N = \frac{f_s}{f_b}, \quad (1)$$

where N, the oversampling ratio, is constant.
Coefficient adaptation is accomplished by means of a Phase Locked Loop (PLL). This results in an adaptive filter with a frequency response that is adjusted according to the fundamental frequency of the input signal. For variable sample rate adaptation, the transfer function coefficients change implicitly. However, the control problem becomes more complicated; the control model is represented by a nonlinear discrete time system.

An implementation that allows for synchronization to a single phase signal is shown in Figure 2. This approach has been described in greater detail in [11] and is referred to as a multirate phase locked loop (MPLL). The MPLL provides synchronization information in the presence of severe disturbances on power lines and a time varying signal frequency. The extraction of synchronization information from the positive sequence component of the line voltage using variable sample rate frequency adaptation has been recently proposed [12]. This implementation requires three analog digital converters cascaded with a positive sequence filter. This combination replaces the block A/D in Figure 2. The output of the positive sequence filter becomes the input to the block B.

The basic idea in the MPLL is to extract the zero crossings of the fundamental component of the incoming signal by utilizing a downsampling process, represented by the block N (sample rate reduction block). The MPLL has two different sample rates. To avoid aliasing downstream of the downsampling block, a digital bandpass filter represented by block B must precede the sample rate reduction block (down sampler). The choice of oversampling ratio (N), wordlength and filter order and their impact on phase accuracy are important design issues. The bandpass filter is designed to extract the fundamental component with a zero degree phase shift between input and output. The bandpass filter can be implemented as either a finite impulse response filter (FIR) or an infinite response filter (IIR). The AGC block decouples the effect of amplitude changes on the phase tracking characteristics. The NCO block produces an output frequency which under steady state operating conditions is an integer multiple N of the incoming fundamental component frequency. The controller is designed so as to achieve a stable response to frequency and phase steps. The incoming data is quantized by the A/D converter at a rate determined by the NCO output frequency. All computations are processed synchronously, with respect to the input frequency, and post-processed in a fixed point format.

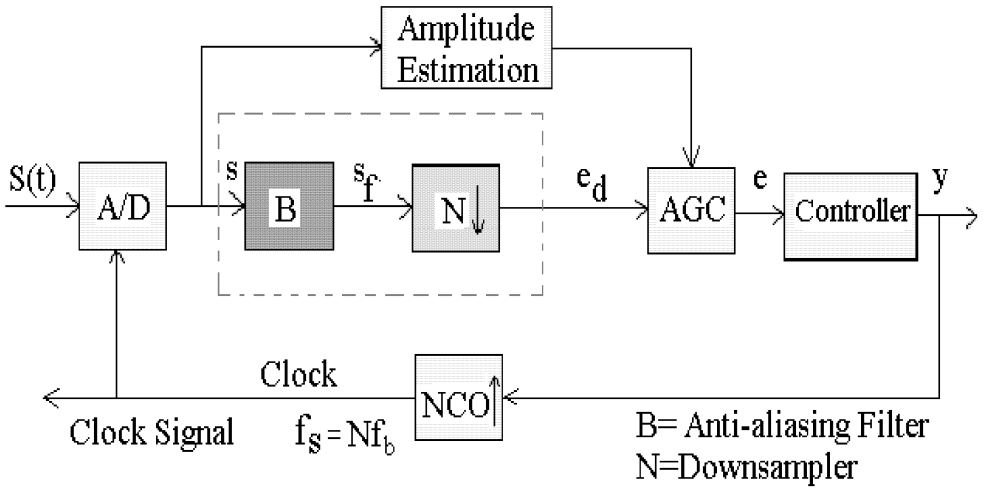


Fig.2: Block diagram of the MPLL [11].

The design of the bandpass filter in previous work [11] was not discussed in any detail, hence the objective of this paper is to present the design procedure for FIR and IIR based filters. Implementation issues are also described.

This paper is organized as follows. The design procedure and results for the FIR and IIR filters are presented in Sections 3 and 4 respectively. Section 5 presents conclusions for the paper.

3 Design Procedure for a FIR Bandpass Filter

FIR filters are nonrecursive filters and are thus all zero filters, i.e. they have no poles. Hence these filters are unconditionally stable. Another feature exclusive to a FIR filter is the linear phase response. For a FIR bandpass filter, the condition for zero steady state phase error is given by $t_d = kT_q$, where t_d is the filter delay and T_q is the input signal period. This yields a FIR filter length of $N_B = 2kN$ where k is an integer.

A Blackman window is considered for the design of a bandpass filter since it provides a maximum stopband attenuation as compared to other windows. For example, the minimum stopband attenuation for a Blackman window is 74dB. In contrast the minimum stopband attenuation for a Hamming and a Hanning window is 53dB and 44dB respectively.

Figure 3 shows the magnitude and phase response of a FIR filter of length N_B=256. The phase response indicates zero phase at 60Hz (fundamental component). This phase response remains unchanged as the input frequency changes given that the sampling frequency generated by the NCO block is always N times greater than the input frequency. Figure 4 shows the harmonic attenuation of the FIR filter for different wordlengths. Wordlengths greater than 12 bits have only marginal effects on the main lobe characteristics of the bandpass filter.

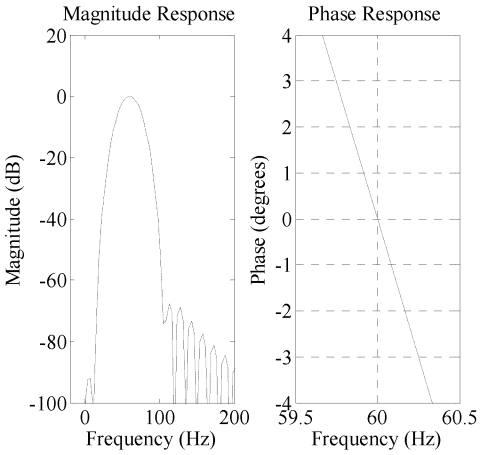


Fig.3: FIR Filter Frequency Response at the base frequency of 60 Hz.

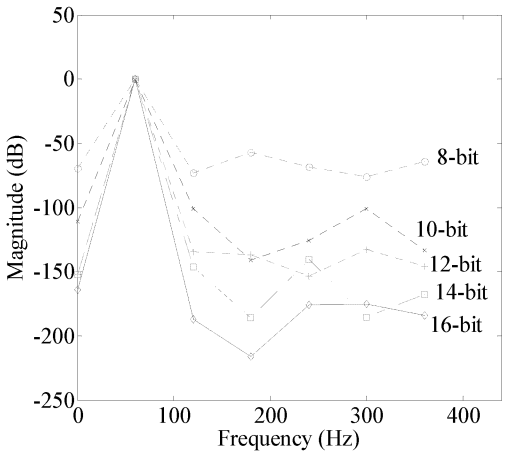
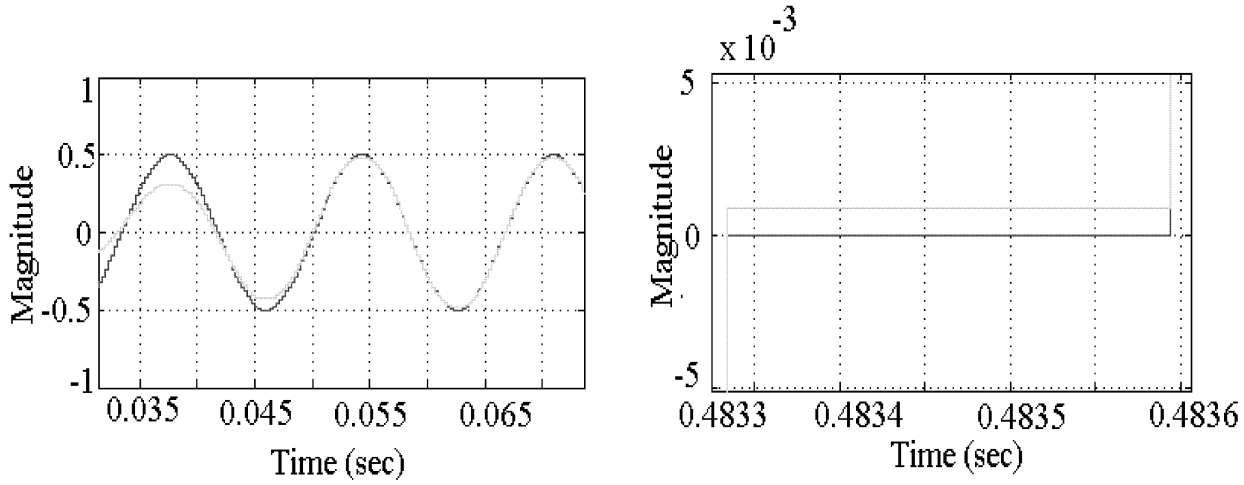


Fig. 4: Harmonic Attenuation at the base frequency of 60 Hz.

The time domain input and output signal with an 8-bit implementation are shown in Figure 5(a). The first 20 ms of the waveform are of no particular relevance since they represent a numerical transient. The sampling frequency is f_s=3840 sample/sec, or T_s = 2.604x10^{-4} sec. The zoomed view of Figure 5(a) is shown in Figure 5(b). This figure indicates that the maximum possible delay for the quantized signals is 2.60x10^{-4} sec. This value corresponds to a non integer delay of 0.99 sample period.



(*a*) (*b*)

Fig. 5: (*a*) Input and output signal, for 8-bit wordlength (*b*) Zoomed view of (*a*).

The FIR filter was simulated with the Virtex-II family device X2V6000 manufactured by Xilinx, with a 16-bit wordlength. The total equivalent gate count for the design was 399k. The additional JTAG gate count for input output blocks (IOBs) was 5.5k and the peak memory usage was 452MB. A filter with 12 bits was also implemented. The total equivalent gate count was 232 k. The additional JTAG gate count for input output blocks (IOBs) was 4.1k and the peak memory usage was 333MB.

4 Design Procedure for an IIR Bandpass Filter

IIR filters are generally advantageous in applications requiring filters with sharp cutoffs (high Q), since a FIR implementation with a similar main lobe width requires a larger filter length [14]. A high *Q* filter leads to poles that are close to or outside the unit circle. This causes instability [13]. The transient response of an IIR filter distorts the output of the filter on startup, rendering the situation similar to that of the FIR filter, that is, an initial segment of data is used to initialize the filter. It is possible to initialize the internal memories with values other than zero to improve the transient performance of the IIR filter [14, 15]. However, this results in increased computational resources and thus negates the advantages of the IIR filter.

The design procedure for a second order IIR based implementation is considered since it gives a similar stopband attenuation characteristic to a FIR Blackman filter of length 256. Consider the general form of a discretized second order transfer function for an IIR filter given below:

$$H(e^{j\omega T_s}) = \frac{a_0 + a_1 e^{-j\omega T_s} + a_2 e^{-2j\omega T_s}}{b_0 + b_1 e^{-j\omega T_s} + b_2 e^{-2j\omega T_s}}, \tag{2}$$

where T_s is the sample period and ω is the frequency of interest

The behavior of the filter in the bandpass region is of interest and hence the coefficients b_0 and a_1 are selected as follows: $b_0 = 1$ and $a_1 = 0$. The expression in (2) thus reduces to

$$H(e^{j\omega T_s}) = \frac{a_0 + a_2 e^{-2j\omega T_s}}{1 + b_1 e^{-j\omega T_s} + b_2 e^{-2j\omega T_s}}. \quad (3)$$

Equation 3 can be expressed in terms of real and imaginary parts as follows:

$$H(e^{j\omega T_s}) = \frac{a_0 + a_2\cos(2\omega T_s) - ja_2\sin(2\omega T_s)}{1 + [b_1\cos(\omega T_s) + b_2\cos(2\omega T_s)] - j[b_1\sin(\varpi T_s) + b_2\sin(2\omega T_s)]}. \quad (4)$$

The condition of zero phase error between input and output can be interpreted as the condition for which $H(e^{j\omega T_s})$ is real. Hence, the imaginary part of equation (4) can be set to zero.

$$[a_0 + a_2\cos(2\omega T_s)]\cdot[b_1\sin(\omega T_s) + b_2\sin(2\omega T_s)] - a_2\sin(2\omega T_s)\cdot [1 + b_1\cos(\omega T_s) + b_2\cos(2\omega T_s)] = 0. \quad (5)$$

An additional constraint is imposed in order to preserve the magnitude of the fundamental component to a unity gain. Therefore, equating the real and imaginary parts of (4) results in:

$$a_0 + a_2\cos(2\omega T_s) = 1 + b_1\cos(\omega T_s) + b_2\cos(2\omega T_s). \quad (6)$$

$$a_2\sin(2\omega T_s) = b_1\sin(\omega T_s) + b_2\sin(2\omega T_s). \quad (7)$$

This results in three equations and four unknowns. An equation for a second order IIR filter in terms of the quality factor (Q) can be written where Q is established in such a way as to provide a similar main lobe characteristic to that of the comparable FIR filter. A comparison of the general equation of a second order IIR filter with that of a second order analog filter results in:

$$Q = \frac{\sqrt{b_2}}{b_1}. \quad (8)$$

The outcome is four equations and four unknowns and thus a solution for the unknown four coefficients can be obtained.

Figure 6 shows the magnitude and phase response of an IIR bandpass filter where the constants a_0, a_2, b_1, b_2, have been selected to provide zero phase shift between the input and output at a base frequency ω of 60 Hz and a sampling period T_s = 2.604x10^{-4} sec. The conditions shown are for a nonzero phase error between the input and output at 60Hz. This phase shift between the input and output remains unchanged as the input frequency changes given that the product of ωT_s remains constant (N).

In fixed point implementations, an IIR filter is more sensitive to arithmetic round off noise then FIR filters. Even if all the poles of an IIR filter are inside the unit circle, stability is not guaranteed due to arithmetic round off noise. Furthermore, for the fixed point IIR implementation, the direct form implementation is not desirable. Instead, a cascaded form of IIR architecture is recommended. Zero phase error (at the base frequency) with an increase in stopband attenuation is difficult to achieve using a series of cascaded IIR filters.

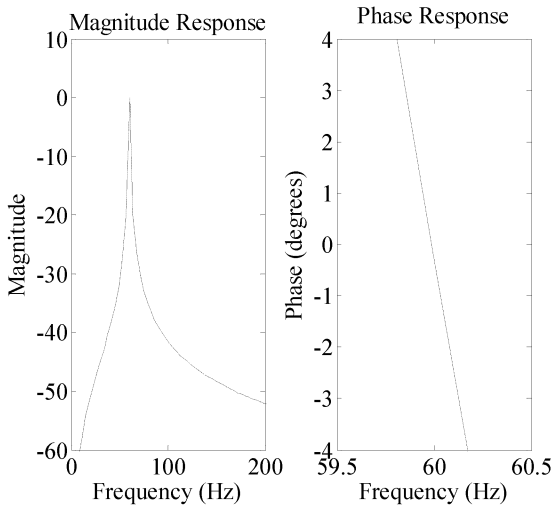


Fig.6: IIR Filter Frequency Response at a base frequency of 60 Hz.

Implementation of the IIR filter within the MDPLL was not attempted because of concerns over the numerical stability of the IIR filter within the MDPLL loop. The dynamic response of the MDPLL will be slower than that of an equivalent FIR filter and thus the bandwidth of the MDPLL will be compromised. Numerical stability concerns associated with the fixed point representation and a high Q design will necessitate the use of a more complex implementation. Hence the number of gates used will increase over and above a design that relies on the simplest implementation.

5 Conclusions

A procedure for designing an antialiasing FIR and IIR bandpass filter for a multirate digital phase locked loop (MDPLL) has been presented. Both bandpass filters operate with a variable sample rate. The product of the fundamental frequency and sampling frequency are forced to remain constant by the MDPLL. The FIR bandpass filter has been chosen because it is unconditionally stable and requires only a modest increase in hardware resources when compared to an IIR filter with the same frequency attenuation characteristics.

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