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Work In Progress: Remote FPGA Lab - An Interactive Online Environment for Teaching FPGA Development Fundamentals

Mr. Ze Yang, University Of Toronto

A master of engineering student at University of Toronto.

Dr. Hamid S Timorabadi P.Eng., University of Toronto

Hamid Timorabadi received his B.Sc, M.A.Sc, and Ph.D. degrees in Electrical Engineering from the University of Toronto. He has worked as a project, design, and test engineer as well as a consultant to industry. His research interests include the application of digital signal processing in power systems.

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Abstract

This paper presents the development and implementation of a remote Field-Programmable Gate Array (FPGA) lab system, designed to provide students with flexible, remote access to FPGA hardware. By integrating the Altera DE1 Board with an in-house designed and developed Digital Design Trainer (DDT) board, the system allows students to engage with FPGA technology from any location, overcoming the limitations of traditional on-site labs. The remote lab enables real-time FPGA programming through a web-based interface and live camera feedback, replicating the in-person lab experience. In traditional labs, students are typically restricted by two to three hours of lab time, often leaving insufficient time to explore beyond the core lab assignments. With the Remote FPGA Lab, students can experiment with course concepts at their own pace, ensuring equitable access to hands-on FPGA experience regardless of geographic location. This system enhances students' technical skills and better prepares them for careers in fields requiring custom hardware solutions. The initial evaluation of the system has shown promising results. A pilot study with a group of students is conducted with valuable feedback, which is used to enhance the system's design. In the current semester, students in the digital systems course use the Remote FPGA Lab, and their feedback is collected to refine further and optimize the system.

Introduction

FPGAs are integral in the education and development of digital systems, providing students with hands-on experience in designing and testing complex digital circuits. However, current FPGA education methods often require physical access to specialized hardware, limiting flexibility and accessibility [1], particularly for remote learners.

Previous efforts to address these challenges have included virtual simulation tools [2], remote labs with limited interaction capabilities [3], and hybrid setups that combine simulation with occasional hardware access [4]. While these solutions have advanced FPGA accessibility, they often fall short in providing an integrated environment where students can design, deploy, and test digital circuits as if they were physically present in the lab. Moreover, many existing systems lack the middleware necessary to ensure seamless interaction between the user and the FPGA hardware.

To address these limitations, this paper introduces a remote FPGA lab system that leverages a middleware component, the DDT Board, to interface with the Altera FPGA Board. This system provides a comprehensive remote learning experience, allowing students to engage with FPGA

hardware from any location. By bridging the gap between physical and virtual learning environments, this approach ensures flexibility, accessibility, and a high level of interactivity, surpassing the capabilities of previous solutions.

Related Work

In the last five years, several systems have been developed to provide remote FPGA lab services, including web-based remote FPGA labs [5], cloud-based remote FPGA labs [6], and server-based remote FPGA labs [7]. However, many of these systems offer only limited FPGA functionalities and impose restrictions on students' access time to the hardware. Typically, these systems involve a lab station or server set up within the laboratory, enabling students to connect through a private network. For instance, researchers at the Pontifical Catholic University of Peru implemented a system where a camera displays the FPGA's physical output to students [8].

Three main methods have emerged for implementing remote FPGA lab systems. The first approach connects the FPGAs to a private server, allowing students to remotely deploy their code onto the FPGA [9][10]. The second approach involves using a lab computer connected to the FPGA, which students access remotely through a Virtual Private Network (VPN) [8][11][12], effectively replicating the experience of a physical lab environment. The final approach relies on pure software simulations to emulate the FPGA's operation [13].

The initial development of the proposed system utilized an approach that connected FPGAs to a private server, where multiple virtual containers were created to manage individual FPGA access. This configuration enabled students to interact with the hardware through a custom-built middleware board. While the setup was functional, it proved insufficient for several key reasons. Most notably, students were unable to directly observe outputs on the physical FPGA board, instead relying on scripts and returned data, which significantly diminished the hands-on experience intended to replicate in-person lab work. Furthermore, the use of a private server introduced substantial costs, rendering it unsustainable as a long-term solution. An alternative approach based on software simulation was also explored, but it failed to deliver the realism required to adequately prepare students for working with actual hardware components. Ultimately, both methods fell short of the system's core objectives: providing an engaging, cost-effective remote learning experience that authentically mirrors physical lab interactions.

Ultimately, the VPN and lab computer solution was selected as the final target for the system. To ensure its effectiveness, it was necessary to introduce meaningful improvements over prior implementations. The next section outlines the structure of the proposed system and the enhancements made to address previously identified limitations.

System Architecture

The remote FPGA lab system is composed of three primary components: the Altera DE1 FPGA Board, the DDT Board, and a web-based application. These components collectively enable students to engage with FPGA hardware in a manner that replicates the hands-on experience of an in-person lab.

Altera DE1 Board

The Altera DE1 FPGA Board serves as the main hardware platform where students deploy their digital designs. Featuring a Cyclone V SoC with 85K programmable logic elements and multiple peripheral interfaces, the DE1 Board is well-suited for both educational and industrial applications. In the proposed system, the DE1 Board is connected to the lab computer and the DDT Board, forming the core of the physical setup.

DDT Board

The DDT Board acts as a middleware, enabling students to generate and interact with physical input signals for the FPGA remotely. Connected to the DE1 Board's General-Purpose Input/Output(GPIO) pins, the DDT Board facilitates the bidirectional transfer of signals. This setup ensures that students can observe the FPGA's output while interacting with real-world input signals, closely simulating the physical lab experience.

Web-Based Application

The web-based application provides the interface for students to remotely access the lab computer. By connecting to the campus network via Wi-Fi or VPN, students can log into the lab computer and interact with the FPGA setup. The application features a graphical user interface (GUI) for the DDT Board, where students can configure input signals, deploy code to the DE1 Board, and view live camera feeds of the physical hardware in operation.

Clock Concurrency

In FPGA-based designs, clock signals are essential for driving the sequential logic of digital circuits. The proposed system ensures clock concurrency, synchronizing clock signals across all components to maintain consistent timing behavior. Two clock sources are employed in the system: the DDT Board's configurable clock and the DE1 Board's onboard clock.

DDT Board Clock

The DDT Board includes a configurable clock capable of operating at frequencies ranging from 1Hz to 100Hz. This clock serves as the master clock when the DDT Board is the active source. Through the DDT Board's GUI, students can adjust the clock rate, enabling them to experiment with different operational speeds and observe the performance of their designs under varying conditions.

DE1 Board Clock

The DE1 Board features a 50MHz onboard clock (CLOCK50) [14]that drives its internal logic. This clock is particularly useful for designs requiring higher operational frequencies or specific timing constraints.

Synchronization and Consistency

The system ensures that only one clock source is active at a time to prevent timing conflicts. When the DDT Board's clock is in use, the DE1 Board's onboard clock is disabled, and vice versa. If the DDT Board's clock is selected, it synchronizes all input signals before sending them to the DE1 Board. Conversely, when the DE1 Board's onboard clock is active, it drives the internal logic, and the DDT Board ensures its input signals align with the DE1 Board's clock cycles. This synchronization avoids timing mismatches that could lead to errors in circuit behavior.

Working Process

The remote FPGA lab system operates by enabling students to connect to the campus network through Eduroam Wi-Fi or a VPN. Once connected, they use a web-based application to access the lab computer remotely. Through this interface, students interact with the DDT Board's GUI to configure input signals, deploy their digital designs, and monitor results. The DDT Board generates input signals, which are sent to the DE1 FPGA Board via predefined GPIO mappings, allowing the FPGA to process the student's code. Results are observed in two ways: through a live camera feed streaming the DE1 Board's physical output and through data returned directly from the DDT Board, offering both visual and quantitative feedback. The system allows students to adjust parameters such as the clock rate, providing flexibility to test their designs under varying operational conditions.

This system introduces some improvements over previous implementations. By combining live camera feeds with data feedback from the DDT Board, the system provides a more comprehensive remote lab experience, closely simulating physical interactions with FPGA

hardware. Unlike purely software-based or server-limited systems, this setup ensures that students engage with real hardware, bridging the gap between theoretical knowledge and practical application. The ability to independently control the camera's angle and zoom through a Python program further enhances the user experience, enabling precise observation of specific hardware components. Moreover, the system supports multiple users simultaneously, ensuring scalability for broader adoption in digital design education. These enhancements collectively ensure an accessible, hands-on learning environment, even in remote settings.

Student Reception

A survey was conducted using SurveyMonkey to gather feedback from a group of students. The focus was on getting advice and hearing how they think the remote FPGA lab system could be improved.

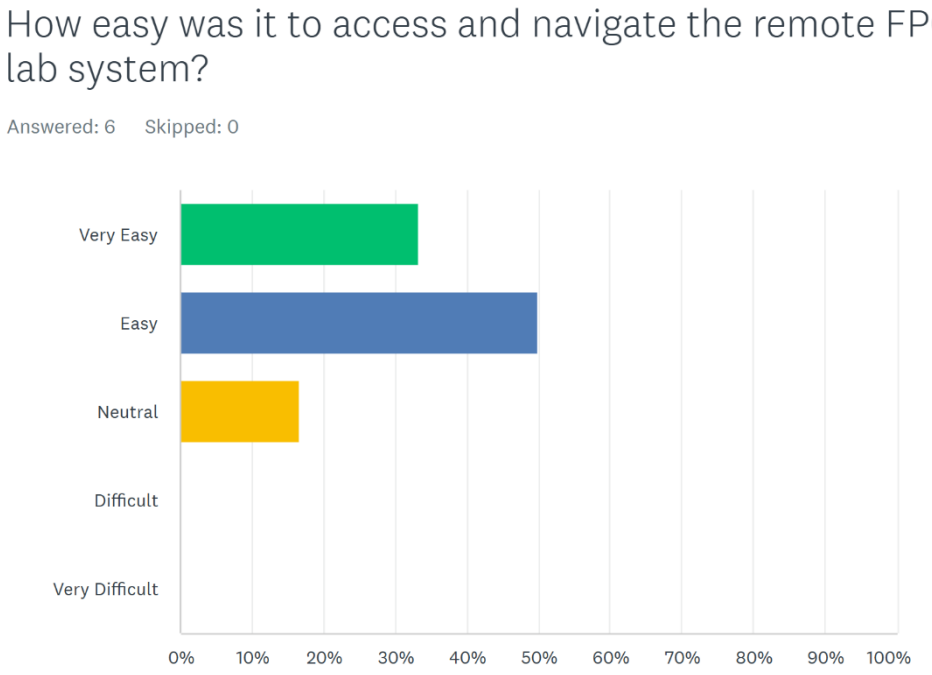

Figure 1: Students' responses to the ease of use of a system [15]

Fig. 1 illustrates how easy it is for students to access and navigate the remote FPGA lab system. About fifty percent of students who participated in the survey think the system was easy to use and the other fifty percent think it is easy to use.

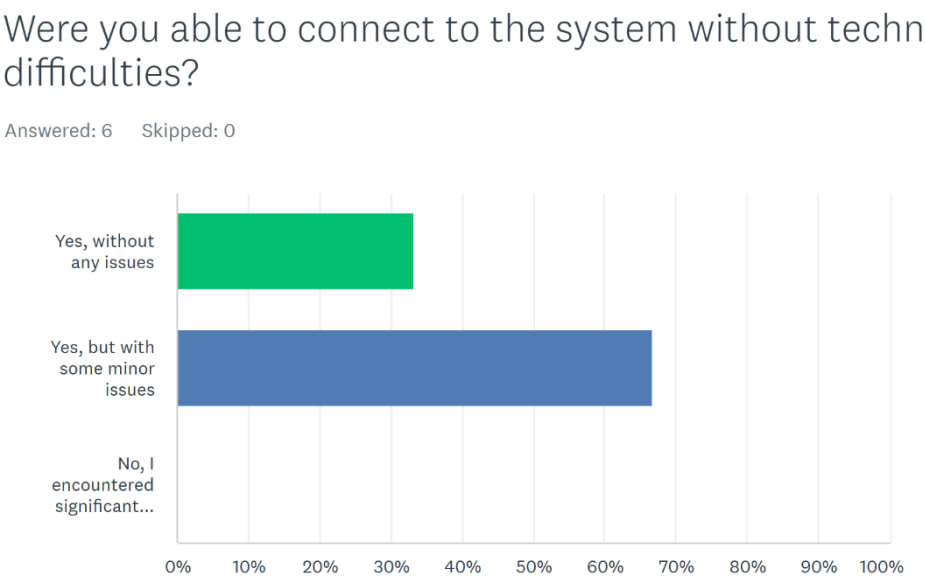

Figure 2: Students' responses to technical difficulties [15]

Fig. 2 shows the noticeable responses from students that most of them have some minor problems while connecting to the system. Around sixty- seven percent of the students who tested the system experienced some minor technical issues when connected to the system.

Although a formal comparative analysis of student performance between remote and traditional laboratory cohorts has yet to be undertaken, qualitative evidence provides valuable insights into the pedagogical effectiveness of the remote lab environment. Students participating in the remote format successfully completed all laboratory assignments, including advanced tasks such as clock synchronization and manipulation of GPIO signals. Teaching assistants reported that these students exhibited notable engagement and a high degree of autonomy in diagnosing and resolving technical issues independently—attributes likely facilitated by the extended availability of the remote platform and the flexibility it affords in pacing. Furthermore, student self-reports indicated enhanced confidence in utilizing hardware tools remotely, aligning closely with the course's intended learning outcomes focused on developing technical proficiency in FPGA systems. These preliminary findings suggest that the remote laboratory environment is conducive to achieving substantial learning outcomes, with future research planned to incorporate systematic evaluations to substantiate these observations.

Conclusion and Future Work

Overall, the feedback from students has been positive, with many finding the system useful and effective. While some students have encountered minor issues, these are typically resolved by revisiting the provided documentation, highlighting the importance of clear and comprehensive guides. To further enhance the experience, future versions will include improved documentation to address any lingering confusion. The prototype of the system has been successfully completed as expected, but there is room for refinement based on student feedback. Enhancements could include addressing usability issues, such as adding a disconnect button to easily end sessions and power off the board, which would provide students with better control over their interactions. Additionally, incorporating a small indicator in the user interface to show the status of the DDT board would make the system more intuitive. Simplifying the setup process is also a priority; a single .py script or .exe file could be developed to launch the UI, camera angle controller, and VideoLAN Client(VLC) display simultaneously, allowing students to set up the system with a single click. Alternatively, integrating all three functions into a unified UI could further streamline operations. The system has been intentionally designed with scalability as a core principle. Its architecture accommodates the integration of additional FPGA workstations, each managed through a modular backend capable of supporting simultaneous user access. To address periods of high demand, a round-robin queuing system can be introduced to promote fair and efficient resource allocation. Notably, the infrastructure leverages standard laboratory computers and commonly available FPGA boards, rendering the model easily replicable across institutions with minimal need for customization. Planned enhancements include the incorporation of usage analytics and load-balancing mechanisms to proactively manage server performance. Additionally, the development team is investigating containerization strategies—such as Docker-based environments—to streamline both deployment and maintenance processes, thereby promoting broader cross-institutional implementation.

In response to minor technical challenges reported by students, forthcoming versions of the system will prioritize a more streamlined setup experience. A key enhancement currently in development is a unified launcher script designed to initialize the graphical user interface, camera control, and video streaming functionalities in a single execution step. Over the longer term, the system aims to feature a fully integrated user interface that consolidates these elements, enabling users to establish VPN connections, configure input signals, and observe board outputs through a centralized dashboard. This level of automation is expected to significantly reduce setup time and improve the overall accessibility and user-friendliness of the remote lab environment. Furthermore, the introduction of a user activity log and individual board health status dashboard will facilitate proactive diagnostics by both students and instructors, thereby enhancing system reliability and instructional effectiveness.

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