A Predictive Phase Locked Loop Applicable to Utility and Non-Utility AC Power Systems

H. Shokrollah Timorabadi, *Member, IEEE*, and F. P. Dawson, Member, *IEEE*.

***Abstract*—A predictive phase locked loop (PPLL) suitable for applications in utility and non-utility power systems and power electronics is presented. The PPLL is frequency adaptive and can provide time variant information about the frequency and amplitude of the fundamental component of an input signal. The PPLL offers a high degree of immunity to wide-band noise, harmonics, inter-harmonics and impulse disturbances. Analytical methods for modeling the PPLL are developed to achieve high execution speed and low real-estate utilization. The mathematical properties of the analytical methods are presented. The PPLL is implemented on a field programmable gate array (FPGA). The locking range of the PPLL is from a fraction of Hz to a few kHz and from 3% to 100% of the nominal input amplitude. The worst case response time of the PPLL is 2 cycles of the input signal period for any realistic perturbation in frequency, amplitude, and/or phase angle. The proposed method is faster, more flexible and more robust than currently available methods.**

***Index Terms*— Adaptive signal processing, EPLL, MPLL, PLL, power systems.**

I. Introduction

PHASE locked loops (PLLs) are employed in power systems and power electronics for monitoring, control, and protection applications [1-6]. Some of these applications include inverters connected to the utility mains [7], paralleling of multiple converters [8], and power converters controlled by synchronized phase information [9].

In utility related power systems, the supply frequency is 50/60 Hz and typically varies by a few Hz. Non-utility applications such as the power transfer from ground to airplane [10] and micro turbine generators [11] may operate at a much higher or lower frequency and can undergo rapid and significant frequency variations [12-14]. Therefore, the PLL should be applicable to a wider range of operating points including utility and non-utility. The PLL should be robust; it should be immune to harmonics, inter-harmonics, wideband stationary/non-stationary noise, and notch-type disturbances.

Existing PLLs in the area of AC power systems and power electronics mainly target utility network applications [1-4]. The existing methods exhibit a large transient response time [3] and low immunity to harmonics/inter-harmonics and noise [15]. In addition, the performance of the existing methods are restricted by trade offs between noise immunity and the response time [16], [5].

This paper proposes a predictive phase locked loop [PPLL] architecture that addresses utility and non-utility applications and can extract frequency, voltage, and phase information from voltage or current signals on a cycle by cycle basis. The PPLL operates over a wide range of frequency and amplitude variations and is highly immune to noise, harmonics/inter-harmonics, and disturbances. The PPLL is realized using a combination of two analytical methods [17]. The strengths of each method are exploited so as to achieve high execution speed and low real estate utilization that facilitate the implementation process of the PPLL. The proposed PPLL is implemented on a field programmable gate array (FPGA) platform. The extended operational range for frequency and amplitude as well as tracking performance and noise immunity are verified.

Section II provides a summary of the performance of existing PLL methods. Section III presents the detailed analysis of the proposed PPLL and section IV presents the implementation and the experimental results. Conclusions are presented in section V.

II. Exisiting Phase Locked Loop Methods

A summary of the existing PLL techniques is described below.

A. Enhanced Phase Locked Loop

The algorithm introduced in [6] and [4] is based on a phase locked loop (PLL) architecture and determines the amplitude, phase angle, and frequency of the dominant component of an input signal. The mathematical relations require knowledge of three constant values that determine the gains for different operations such as the integrator blocks in the algorithm. The choice of the constants is critical in terms of influencing the performance of the algorithm and is typically optimized for a pre-selected operating point, i.e. 60 Hz. The algorithm is incapable of maintaining a set of optimized values for the constants as the frequency of the fundamental component changes. Hence, the algorithm performance depends on the choice of constants. For instance, a faster response time is achieved at the expense of a degraded enhanced phase locked loop (EPLL) resolution. An approximate assessment of the algorithms performance is summarized below [16], [6], and

The authors are with the Edward S. Rogers Sr. Department of Electrical and Computer Engineering at University of Toronto, 10 King's College Road, Toronto, ON M5S 3G4, Canada (Email: hamid@ele.utoronto.ca; dawson@ele.utoronto.ca).

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[4]:

- A nominal frequency of 50/60 Hz,
- A frequency range of 20-120 Hz, and
- A transient response time of 6 cycles based on the nominal frequency value.

B. Multi-rate Phase Locked Loop

A digital implementation of a multi-rate phase locked loop (MPLL) that operates with two different sampling rates is presented in [3]. One sampling rate is called the fast sample rate and is an integer multiple of the input signal frequency. The other is equal to the input signal frequency and is referred to as the slow sample rate. If the frequency changes, an error signal is generated. The fast sample rate is adapted such that the MPLL remains phase locked.

The response time of the MPLL to a 1 Hz step frequency perturbation exceeds 600 msec. (over 36 cycles of a 60 Hz signal). Furthermore, the response time is in the order of seconds for a 4 Hz step frequency change from 60 Hz to 64 Hz. The long delay time is a direct result of the tradeoff that exists between the dynamic response and noise immunity of the MPLL; this is a direct consequence of an infinite impulse response implementation. A performance summary of the algorithm is provided below:

- A nominal frequency of 50/60 Hz,
- A frequency range of 48-72 Hz, and
- A slow response time in the order of seconds.

C. Phase Detecting Method

A phase detecting method for a balanced three-phase system that consists of a phase detector and a loop filter is reported in [5], [18], and [19]. The phase detection is designed using a *dq*-transformation frame. The loop filter consists of a PI regulator that generates a phase error employed by a voltage controlled oscillator (VCO). The design of the loop filter involves a trade off between the dynamic performance and filtering of undesired distortion on the input signals. The loop filter requires a low bandwidth to become effective in filtering input signals superimposed with harmonics and/or DC-offset. The low bandwidth results in a poor dynamic response.

The performance of the phase detecting method is summarized as follows:

- Poor dynamic response due to a low bandwidth implementation of the loop filter, and
- Lack of frequency adaptation.

III. Predictive Phase Locked loop

The existing PLL systems are restricted by the limited frequency range and low response time and cannot process an input signal with the following characteristics:

- *Frequency* – from near zero to a few hundreds of Hertz,
- *Amplitude* - from near zero up to a rated value, and
- *Phase* (with respect to a reference frame) - from approximately zero to a few degrees.

superimposed with the following undesired signals,

- Wideband stationary/non-stationary noise,
- Harmonics/inter-harmonics, and
- Impulse or notch type disturbances.

A predictive phase locked loop (PPLL) is considered that determines the frequency (f_1), amplitude (A_1), and phase-difference (Φ_{Diff}) of the fundamental component of the input signal. The phase-difference is defined as the phase of the input fundamental component with respect to a reference frame. The input signal, $x(t)$, is defined as:

$$x(t) = s_1(t) + n(t) \tag{1}$$

where $n(t)$ is any superimposed signal and $s_1(t)$ is the fundamental component of x(t) such that:

$$s_1(t) = A_1 \cdot cos\left(2 \cdot \pi \cdot f_1 \cdot t - \phi_{Diff}\right) \tag{2}$$

A_1 and f_1 are the amplitude and frequency of the input fundamental component respectively.

The PPLL also generates a signal denoted as a tracking signal that is an exact duplicate of the input fundamental component when the system is in steady state. This signal is employed as the reference for Φ_{Diff}. Under disturbance conditions, the frequency, amplitude, and/or phase variations of the input signal are detected by the PPLL and then the tracking signal is adjusted to match the input fundamental component. The tracking signal ($S_{TS}(t)$) is defined by the following expression:

$$S_{TS}(t) = A_{TS} \cdot cos\left(2\pi f_{TS} \cdot t\right) \tag{3}$$

where A_{TS} and f_{TS} are the magnitude and frequency of the tracking signal respectively.

In the steady state, $f_{TS} = f_1$, $A_{TS} = A_1$, and $\Phi_{Diff} = 0$, consequently, (3) reduces to (2) and hence the tracking signal represents a duplicate of the input fundamental component. Figure 1 shows the PPLL consisting of the following blocks: data acquisition, predictor, and oscillator/phase-shifter that are discussed as follows.

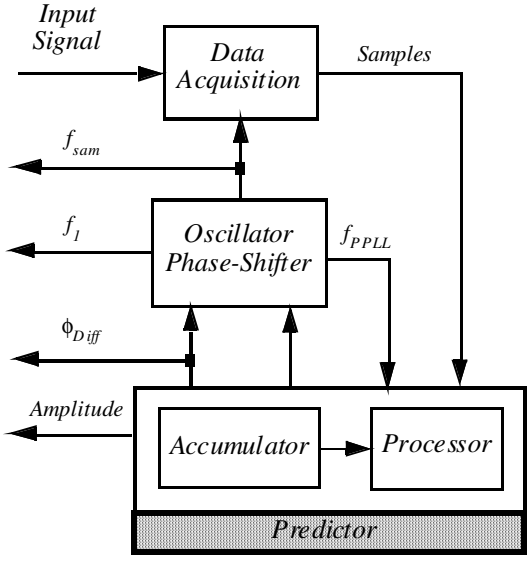

Fig. 1. The schematic of predictive phase locked loop (PPLL).

A. Predictor

The predictor block of Figure 1 is the core of the PPLL. The predictor receives samples from data acquisition block and computes a triplet of f_1, A_1, and Φ_{Diff} from the input fundamental component. The predictor utilizes the information from this triplet to generate the tracking signal. The predictor consists of an accumulator and processor sub-blocks that are described as follows.

B. Accumulator

The accumulator acquires three 120° equidistant samples from the input fundamental component. These equidistant samples are referred to as s_0, s_{120}, and s_{240} and are used to characterize one period of a sinusoidal waveform. They are henceforth referred to as a three-sample cosine-wave. Figure 2 shows of the three-sample cosine-wave that lie on the trajectory of the sinusoidal waveform (dotted line). Figure 2 also depicts the tracking signal where $f_{TS} \neq f_1$ and $A_{TS} \neq A_1$.

The samples of the three-sample cosine-wave are obtained by shifting phase in (1) by 120° such that:

$$s_0 = A_1 \cdot \cos\left(\alpha - \phi_{Diff}\right) , \tag{4}$$

$$s_{120} = A_1 \cdot \cos\left(\alpha - \phi_{Diff} - \frac{2\pi}{3}\frac{f_1}{f_{TS}}\right) , \tag{5}$$

$$s_{240} = A_1 \cdot \cos\left(\alpha - \phi_{Diff} - 2\cdot\frac{2\pi}{3}\frac{f_1}{f_{TS}}\right) , \tag{6}$$

where $\alpha = 2\pi.f_1.t_0$.

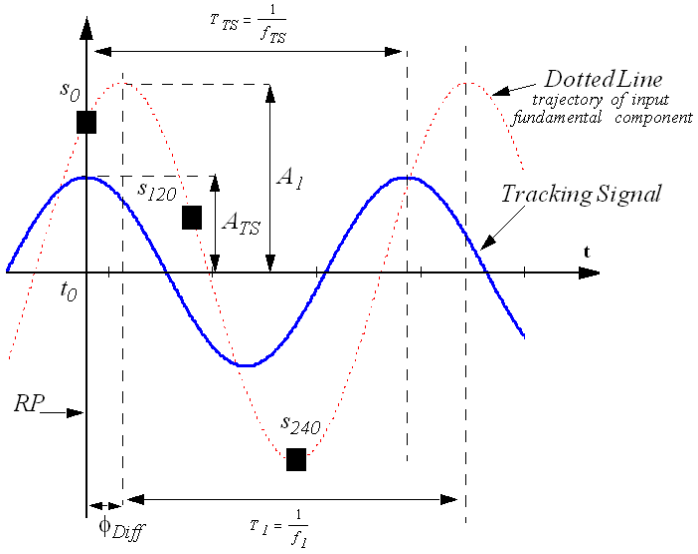

Fig. 2. The three-sample cosine-wave (squares) and the tracking signal.

C. Processor

The processor employs s_0, s_{120}, and s_{240} from the three-sample cosine-wave and computes the triplet. A set of mathematical expressions is executed by the processor that addresses the following two objectives:

- The computation speed is maximized, and
- The real estate required for implementation is minimized.

These objectives are achieved by:

- Computing the triplet so that calculations are not performed sequentially. Hence, the algorithm can be implemented by means of parallel processing. This leads to a faster execution speed especially when f_1, A_1, and Φ_{Diff} change simultaneously.
  The parallel processing should not lead to a significant increase in hardware real estate, and
- Utilizing expressions requiring simple mathematical operations such as additions and/or multiplications so that the real estate consumed is minimized.

Two schemes for classifying the computation of f_1, A_1, and Φ_{Diff} are: the transformed method and the sequential method [20].

The analytical expressions for each method and a comparison of each method are provided below.

D. Transformed Method

The triplet (f_1, A_1, and Φ_{Diff}) is computed from (4)-(6) as follows:

$$A_1 = \sqrt{s_d^{\,2} + s_q^{\,2}} , \tag{7}$$

$$\phi_{Diff} = \arctan\left(\frac{s_q}{s_d}\right) . \tag{8}$$

where

$$s_d = \frac{2\cdot s_0 - s_{120} - s_{240}}{3} , \tag{9}$$

$$s_q = \frac{\sqrt{3}}{3}\cdot\left(s_{120} - s_{240}\right) , \tag{10}$$

and s_0, s_{120}, and s_{240} are the samples from the three-sample cosine-wave.

The frequency (f_1) is computed using the Newton-Raphson iteration method:

$$f_1 = f_{TS} - \frac{G\left(f_1\right)}{\frac{d}{df_1}G\left(f_1\right)} , \tag{11}$$

where G is defined as a function of f_1 given by:

$$G\left(f_1\right) = \frac{A_1}{3}\cdot\left(\cos\left(2\cdot\pi\cdot\frac{f_1}{f_{TS}}\right) + \cos\left(2\cdot\pi\cdot\frac{f_1}{3\cdot f_{TS}}\right) + \cos\left(2\cdot\pi\cdot\frac{2\cdot f_1}{3\cdot f_{TS}}\right)\right) - s_z , \tag{12}$$

and

$$s_z = \frac{s_0 + s_{120} + s_{240}}{3} \quad . \tag{13}$$

The derivative of (12) is:

$$\frac{d}{df_1} G(f_1) = -\frac{2\pi}{3} \frac{A_1}{f_{TS}} \left(sin\left(2\pi \frac{f_1}{f_{TS}}\right) + \frac{1}{3} \cdot sin\left(2 \cdot \pi \cdot \frac{f_1}{3 \cdot f_{TS}}\right) + \frac{2}{3} \cdot sin\left(2 \cdot \pi \cdot \frac{2 \cdot f_1}{3 \cdot f_{TS}}\right) \right) \quad . \tag{14}$$

The relation in (11) is computed for f_1 and then f_{TS} is replaced by the resulting f_1. The accuracy of the resulting f_1 depends on the number of iterations of equation (11).

E. Sequential Method

The triplet is computed based on s_0, s_{120}, and s_{240} (the three-sample cosine-wave) in three consecutive steps:

1 – Frequency (f_1) is computed based on the following expression:

$$f_1 = f_{TS} \cdot \frac{3}{2 \cdot \pi} \cdot arccos\left(\frac{s_{120} + s_{240}}{2 \cdot s_0} \right) \quad . \tag{15}$$

2 – Phase-difference (Φ_{Diff}) is computed based on the following expression by substituting the computed frequency (f_1) from step 1:

$$\phi_{Diff} = arctan\left(\frac{\frac{s_0}{s_{120}} \cdot cos\left(\frac{2\pi}{3} \frac{f_1}{f_{TS}}\right) - 1}{\frac{s_0}{s_{120}} \cdot sin\left(\frac{2\pi}{3} \frac{f_1}{f_{TS}}\right)} \right) \quad . \tag{16}$$

3 – Amplitude (A_1) is computed by substituting the phase-difference (Φ_{Diff}) determined in step 2 into the following expression:

$$A_1 = \frac{s_0}{cos(\phi_{Diff})} \quad , \tag{17}$$

F. Comparison of Transformed and Sequential Methods

A comparison of the expressions developed indicates that:

- Expression (15) as opposed to (11) is computationally less complex and does not rely on any iteration, therefore, it is the preferred approach for computing the frequency (f_1).
- Expressions (16) and (17) require four trigonometric calculations and four divisions whereas expressions (7) and (8) only require one square root, one division, and two squares operations. The computation of trigonometric functions requires complex algorithms that reduces the execution speed and increases the real estate utilized and hence causes an increase in power dissipation. Consequently the expressions in (7) and (8) are employed to compute Φ_{Diff} and A_1 respectively.

The parallel processing of the expressions in (7), (8), and (15) does not increase the utilization of resources. These expressions are executed by the predictor and illustrated in Figure 3.

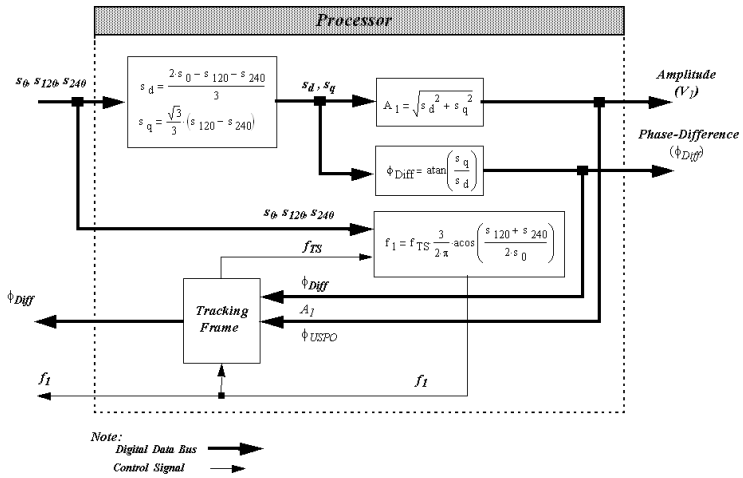

Fig. 3. Operation of each sub-block in the predictor.

G. Discussion

An examination of the preferred expressions (7), (8), and (16) for the processor reveals two division operations where equation (8) and (15) are divided by s_d and s_0 respectively. A division by zero when s_d or s_0 is zero results in an undefined condition. A zero crossing reference-point leads to zero values for s_d and s_0 in steady state which is not acceptable. Conditional states must be introduced in order to avoid a division by zero. A process of conditional states causes a reduction in execution speed and an increase in circuit complexity. A choice of positive peak value as the reference-point becomes preferable and is thus adapted in the design of the PPLL.

H. Phase Locking of PPLL

The objective of this section is to describe the PPLL phase locking mechanism that forces the tracking signal to become equal to the input fundamental component and hence the system reaches steady state operation.

The computation of the synchronization information using (7), (8), and (15) from the three-sample cosine-wave requires knowledge of the three 120°-samples extracted from the input signal. The three-sample cosine-wave is generated by first digitizing the input signal with an analog-to-digital converter (ADC) and then extracting the input fundamental component with a digital band-pass filter. The center frequency of the digital band-pass filter coincides with the fundamental component of the input signal during steady state. The input signal frequency may vary in the range given below:

$$f_{1Min} \le f_1 \le f_{1Max} \quad , \tag{18}$$

where f_{1Min} and f_{1Max} are the minimum and maximum values of the input fundamental frequency respectively.

A frequency adaptive finite impulse response (FIR) band-pass filter is employed to (*a*) filter frequencies above and below the center frequency, (*b*) maintain a minimum phase shift between the input and output fundamental component, and (c) maintain a constant amplitude as the frequency is varied. The digital FIR band-pass filter operates on the basis of a sample window [21]. Frequency adaptation of the filter is achieved by employing synchronous sampling to maintain the number of samples within the sample window constant. The concept of variable sampling has been described in [14], [3] where the sampling frequency (f_{sam}) of the ADC is varied to maintain a constant number of samples (N_s) per input fundamental component such that:

$$N_S = \frac{f_{sam}}{f_1}, \tag{19}$$

where the sampling frequency varies in the range of:

$$f_{samMin} \le f_{sam} \le f_{samMax}, \tag{20}$$

with f_{samMin} and f_{samMax} being the minimum and maximum sampling frequencies respectively.

The operation of the phase locking mechanism is shown in Figure 4.

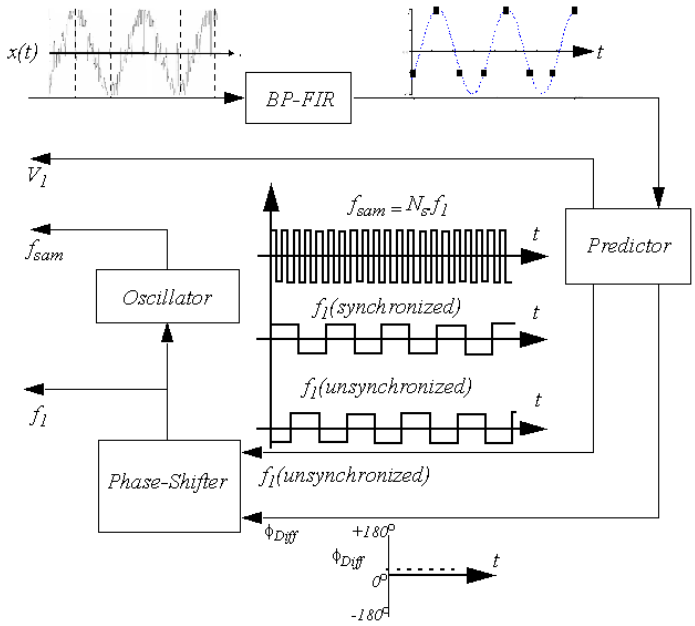

Fig. 4. A block diagram of the PPLL illustrating the phase locking operation.

The frequency calculated in (15) is independent of the phase-difference (Φ_{Diff}) and hence is not necessarily aligned with the reference-point. The phase-shifter sub-block adjusts the edge of the unsynchronized f_1 so that its rising edge becomes aligned with the reference-point. This results in a phase locking of f_1 with respect to the input fundamental component.

The sampling frequency (f_{sam}) is an integer multiple of f_1 (synchronized) and this allows the analog to digital converter to operate with synchronous sampling. This synchronized sampling is enforced by the phase locking mechanism of the PPLL. The sampling frequency controls the ADC and hence performs the task of synchronous sampling.

The PPLL functionality:

- Differs from the conventional PLL architecture [22] in that the PPLL employs analytical expressions for computing the frequency, amplitude, and phase-difference, and
- Resembles the PLL since the PPLL locks to the phase of the input signal.

The name "predictive" in predictive phase locked loop stems from the fact that the PPLL precisely predicts f_1, A_1, and Φ_{Diff} prior to expiry of the current period of the input signal.

IV. Implementation

This section describes the implementation of the PPLL along with the experimental results. The implementation platform consists of a field programmable gate array (FPGA) based platform [23]. The FPGA platform allows a gate level design as well as parallel processing that leads to higher execution speeds and bandwidth as compared to a microprocessor platform. The FPGA platform consists of a FPGA device from the Virtex-II family (XC2V2000-4FG676) manufactured by Xilinx.

The test signal and the results from implementations are provided below.

A. Performance Verification

The performance of the PPLL is verified by:

- Extracting the fundamental component of the input signal, and
- Generating a synchronization signal that locates the position of the three samples of s_0, s_{120}, and s_{240} that are 120° apart during steady state. Figure 5 shows this signal along with a sinusoidal input signal.

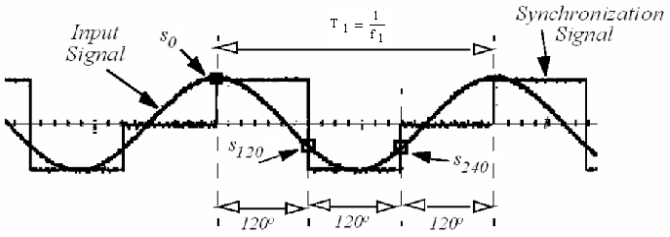

Fig. 5. The input signal and the synchronization signal.

B. Experimental Results

The experiments consider two sets of operating conditions: steady state and transients. The input signal is a contaminated sinusoidal signal with harmonics that presents a worst case scenario for power systems voltage/current signals. Triangular and square input signals are also considered since they are

readily available from a function generator and represent signals with various harmonics. A frequency domain representation is also obtained by employing the Fast Fourier transform (FFT) available on an oscilloscope.

Figure 6 shows the steady state operation with a pure sinusoidal input signal at 800 Hz.

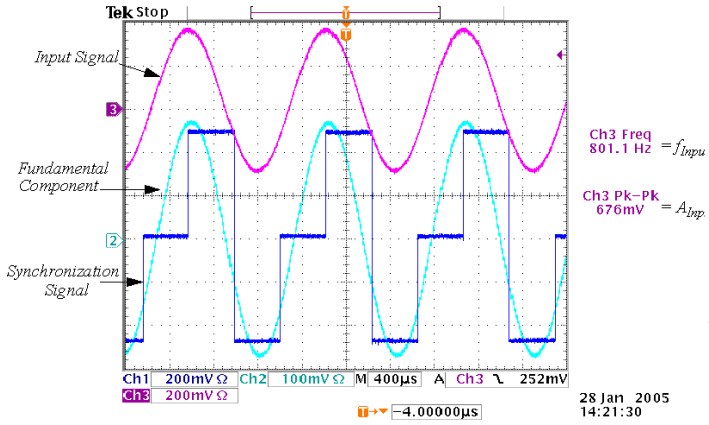

Fig. 6. Steady state sinusoidal input signal at 800 Hz.

Figures 7 and 8 show input signals at 60 Hz consisting of (*a*) the fundamental, 3rd, and 5th harmonics and (*b*) a square wave at 60 Hz with amplitude modulation respectively.

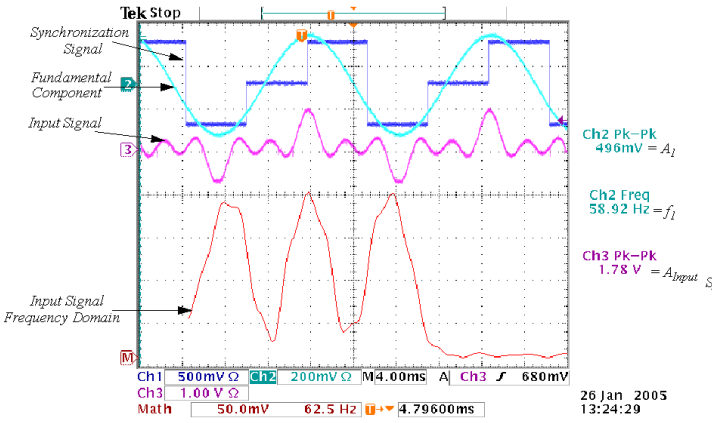

Fig. 7. Input signal with fundamental, 3rd, and 5th harmonics at 60 Hz.

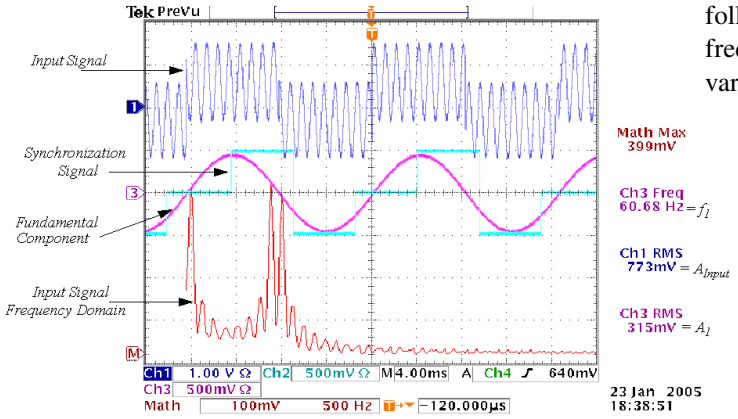

Fig. 8. Square wave input signal at 60 Hz with severe amplitude modulation.

The frequency range is examined under severely distorted conditions and a minimum fundamental component amplitude. Figure 9 shows a square wave input signal with a frequency of 2 kHz, a DC-offset, and a minimum amplitude of 0.098 volts.

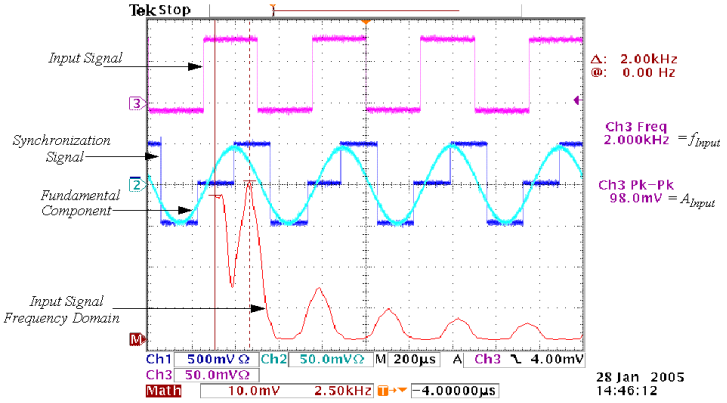

Fig. 9. Square wave input signal with a 2 kHz frequency, a DC offset and a 0.098 volt amplitude.

Figure 10 shows a frequency step change of 4 Hz from an operating point of 60 Hz.

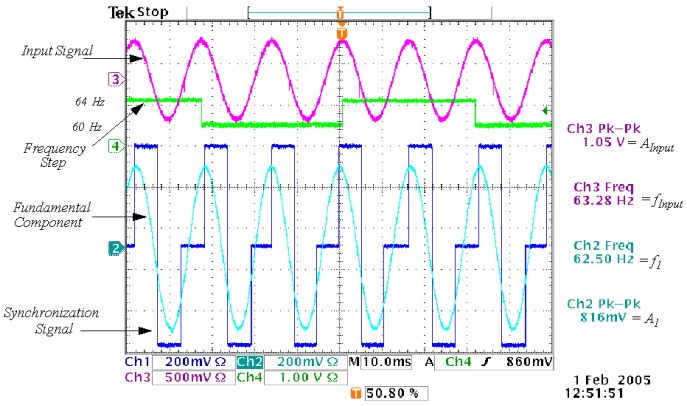

Fig. 10. Frequency step change of 4 Hz from a 60 Hz operating point.

The frequency of the input signal is ramped up/down following the shape of a triangular path. Figure 11 shows the frequency ramp with a rate of 120 Hz/sec where the frequency varies between 40 Hz and 160 Hz.

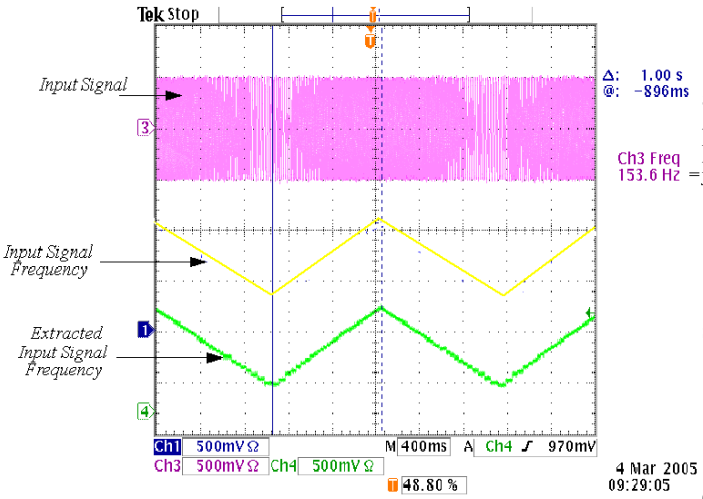

Fig. 11. Response to a 120 Hz/sec change in the input signal frequency.

Figure 12 illustrates the amplitude ramped up/down and the extracted amplitude. The rate of change of amplitude is approximately 66% of the maximum allowable amplitude imposed by the FPGA platform.

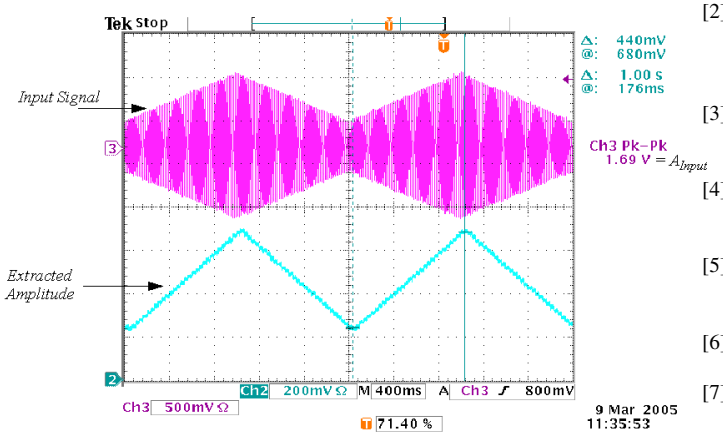

Fig. 12. Response of WSS to an amplitude ramp.

The phase step response of the PPLL for a phase step of 30° is shown in Figure 13.

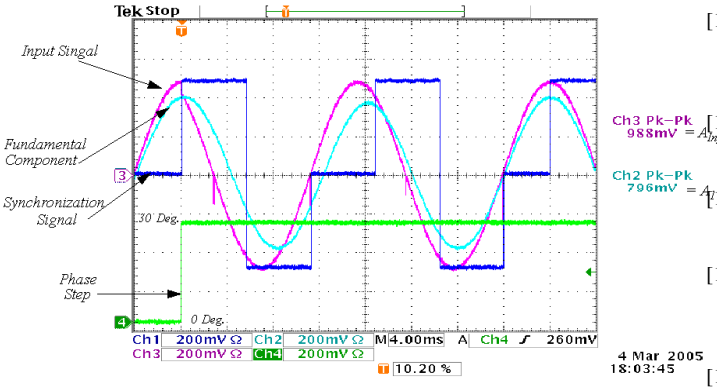

Fig. 13. Response of PPPL to a phase step of 30°.

V. CONCLUSIONS

The analysis and experimental validation for a new PLL architecture; a predictive phase locked loop (PPPL) is presented. The implementation results indicate that the PPLL remains operational under the following input conditions:

- *Frequency* - from approximately a fraction of a Hz to 2 kHz, and
- *Amplitude* - from approximately 3% to 100% of the nominal value,

superimposed with:

- *Noise* - up to 60% of the amplitude of the fundamental component of the input signal.
- *Frequency rate of change* – 120 Hz/sec.

The tracking properties of the PPLL are verified and exhibit a two cycle response time under worst case conditions.

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VII. BIOGRAPHIES

Hamid Shokrollah Timorabadi (M'2004) received his B.Sc, M.A.Sc, and Ph.D. degrees in Electrical Engineering from the University of Toronto in 1996, 1998, and 2005 respectively. He worked as a project, design, and test engineers in industry and also acted as a switch mode power supply consultant. He is currently a Post Doctoral Fellow at the University of Toronto. His research interests include the application of digital signal processing in utility and non-utility power system applications, FPGA implementations and software-based algorithms.

He is a member of the Association of Professional Engineers of Ontario.

Francis Dawson (S'86-M'87) received the B.Sc degree in physics and the B.ASc., M.A.Sc., and Ph.D degrees in electrical engineering from the University of Toronto in 1978, 1982, 1985, and 1988, respectively.

He worked as a process control engineer in the pulp and paper, rubber and textile industries during the period 1978-1980. From 1982 to 1984 he acted as a consultant on various projects. Development areas included high-frequency link power supplies, power supplies for specialized applications and high current protection circuits. Since 1988 he has been with the Department of Electrical and Computer Engineering, University of Toronto where he is engaged in teaching and research.

His areas of research interest include static power converters and their applications, signal processing in power engineering applications and device or process modeling. He has also participated as a Consultant or Project Leader in several industrial projects.

Dr. Dawson is a member of the Association of Professional Engineers of Ontario.