REDUCED COMPLEXITY PROCESSOR FOR TEACHING COMPUTER ARCHITECTURE

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This paper proposes the application of a Reduced Complexity Processor (RCP) as a tool in teaching computer architecture. The design and implementation of the RCP as well as its effectiveness is reported. The proposed RCP is a single-cycle, 8-bit processor. The processor currently used in the course is a soft-processor, Nios-II, by Altera. Nios-II is a complex, single-cycle, 32-bit processor that cannot easily be dissected for students' realization of computer architecture. Teaching RCP alongside Nios-II allows to eliminate some of the unnecessary complexities that prevent students from achieving a rather better realization of computer system functionality. The intention is also to actively involve students in design process by providing a platform that allows students to modify and build their own processor.

A course on computer architecture should conceptually teach the relation between software (S.W.) and hardware (H.W.) and how programming tasks are executed by H.W. This involves the design of an assembler, instruction set, and the mapping of instructions to H.W.

An assembler is implemented that converts assembly code written in ASCII text into binary data. The binary data are run by the physical processor. The assembler can be invoked from both Windows and Linux platforms. The physical processor considers a Harvard architecture with an instruction memory and a data memory. The assembler supports binary, octal, hexadecimal, and decimal number systems for both positive and negative numbers. The assembler supports 10 basic instructions. This limited number of instructions allows to reduce the complexity of architecture in the assembler, instruction-set, and H.W. design without any loss of performance. The instruction-set is complete and allows aggregation of complicated functions and architecture to RCP. Hence, any desired pseudo-instruction can be introduced.

A physical processor is achieved by implementation of the processor blocks on an FPGA board, DE0 development kit from Altera. The processor includes four registers forming the register file (RF). In the case of a single-cycle processor, each instruction takes one clock cycle to complete. Often this is not readily understood by students. RCP is a straight forward tool to understand. It clarifies the notion of a single-cycle processor functionality in how an instruction can be executed within one clock-cycle. Programs written in assembly language can be assembled for the processor using the assembler. The assembler generates memory files which are used to initialize the DE0's instruction and data memories when the Verilog project is compiled.

The platform provides a means for resetting and stepping through the program via DE0 input keys. In addition, the keys and LEDs on the DE0 platform are configured to allow the user to reset or step through the running program while employing the LEDs for debugging purposes. Users can modify the provided Verilog test-bench to include any desired functionality or have a gate-level realization of a processor implementation.

The implementation of the Reduced Complexity Processor (RCP) is complete and tested by students taking a computer organization course. Students unanimously confirmed the effectiveness of RCP in conducted surveys. RCP allows students to gain an overall view of the processor's functionality without being entangled with details. Consequently, this facilitates teaching a complex processor, Nios-II, and provides an enhanced learning experience.