

A Wide-Range Synchronization System for AC Power Systems

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Abstract—A wide-range synchronization system (WSS) for applications in utility and non-utility AC power systems is presented. The synchronization system provides information about the frequency, amplitude, and phase. The WSS is fully adaptive, extracts synchronization information from frequency and/or amplitude variant voltage/current signals and offers a high degree of immunity to wide-band noise, harmonics, inter-harmonics and impulse disturbances. A set of analytical expressions is developed to achieve high execution speed and low real estate utilization. The mathematical properties of the analytical expressions are presented. The WSS is implemented on a field programmable gate array (FPGA). The operating range of the implemented WSS is from a fraction of Hz to a few kHz and from 3% to 100% of nominal amplitude.

I. INTRODUCTION

Synchronization is often required in monitoring and control applications in power systems and industrial electronic equipment. The control applications are concerned with any impacts that might occur from variations or interruptions in the supply of electric power such as voltage sags/swells, transients from capacitor bank switching, momentary interruptions, harmonic distortion, notch-type disturbances from converters, and wide-band noise. A mediation of these impacts results in a high power quality (PQ) and reliability in the supply of power [1]. The parameters monitored include: frequency, amplitude, and phase angle. These parameters taken together are referred to as synchronization information. The control applications employ the synchronization information to compensate for any reduction in PQ and to improve power system reliability.

Fig. 1 depicts the schematic of a synchronization system configured within a larger system; power delivery from the generating source to consuming loads and an overall synchronization system example are shown.

In Fig. 1 the input signal amplitude is suitably scaled by instrumentation transformers to make the input signal compatible with the hardware components of the synchronization system. The synchronization information is extracted from a single-phase or three-phase power system and then used to generate the gating pulses that in turn control the power switches. Three-phase signals can be decomposed into positive, negative, and zero sequence components [2].

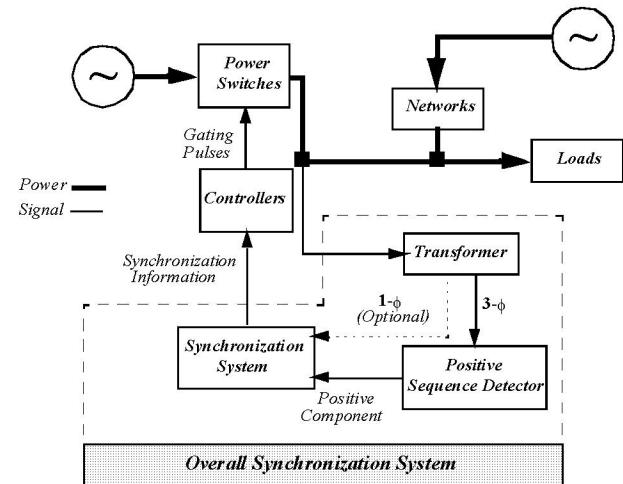


Figure 1. Example of an overall synchronization system.

The need for synchronization is not restricted to utility networks where the frequency is 50/60 Hz. It is also required for non-utility applications such as the aerospace industry where the frequency is 400 Hz with variations in the range of 360-800 Hz.

Synchronization systems in the literature target utility network applications [3]-[6], and have properties that exhibit a large transient response time [5], and a low immunity to harmonics/inter-harmonics and wide-band noise [7]. The performance of these methods are restricted by trade offs between noise immunity, and the response time [8], [9].

A wide-range synchronization system (WSS) is proposed that addresses a broader range of applications and can extract synchronization information from time and/or amplitude varying voltage or current signals. The WSS is operational under a wider range of frequency and amplitude variations and is highly immune to noise, harmonics/inter-harmonics, and disturbances. The underlying architecture of the WSS is based on a set of analytical expressions where high execution speed and low real estate utilization are of paramount importance [10]. The WSS is implemented on a field programmable gate array platform. The extended operational range for frequency and amplitude as well as tracking performance and noise immunity are experimentally verified.

Section II provides a summary of requirements for synchronization systems. Section III provides a

performance evaluation of the synchronization systems available. Section IV presents the detailed analysis of the proposed WSS and section V provides the implementation and experimental results. A summary and conclusions are provided in section VI.

II. SYNCHRONIZATION REQUIREMENTS

Utility network applications typically operate at 115V/60Hz (North America) and 220V/50Hz (Europe). The voltage variations are limited to approximately -12% to +6% of the nominal value under extreme conditions. The utility network frequency may also vary by as much as ± 5 Hz from the nominal value of 50/60 Hz [11]-[12].

Non-utility applications operate at a frequency other than 50/60 Hz. The non-utility applications may also have large frequency variations. For instance, an onboard aircraft AC power supply may include: (a) a 400 Hz constant frequency (*CF*) and (b) a wide-range variable frequency (*VF*) that can vary from 360 Hz to 800 Hz [13]-[14]. A no-break power transfer from a ground power unit (GPU) to an onboard power unit (OPU) of an airplane is an example where synchronization information is required [15]. In such a case the synchronization system operates over a frequency range of 360-800 Hz with voltage variations from 84% to 116% of the nominal value [13], [16]-[17].

The reported requirements of different synchronization systems in power utility, industrial electronics and aerospace market applications are summarized in Table I. The last row of Table I presents requirements of a synchronization system that considers a wider range of applications.

TABLE I.
A SUMMARY OF REQUIREMENTS FOR A SYNCHRONIZATION SYSTEM.

Application	Frequency		Amplitude	
	Rated (Hz)	Range (Hz)	Rated (V)	Range (% of Rated Value)
Utility [18]	60 50	58–62 48–52	115 220	88–106
Synchrophasor [19]	60 50	55–65 45–5	115 220	10–200
Aircraft [16]-[17]	<i>CF</i>	400	360–440	84–117
	<i>VF</i>	N/A	360–800	
VSSM* [20]	N/A	\approx 0–200	115 220	\approx 0–100
Micro Turbine [21]	N/A	1300–2000	115 220	88–106
COMBINED	50 60 400	\approx 0–2000	115 220	\approx 0–200

* Variable Speed Synchronous Machine

III. SYNCHRONIZATION METHODS

The synchronization methods available are restricted to utility network applications where the frequency is

50/60 Hz. Non-utility applications that operate at a higher frequency range or a lower frequency range than a utility network are not considered [13], [20], [22]. The following sections provide a summary of existing synchronization methods and highlight the performance issues.

A. Enhanced Phase Locked Loop

The algorithm introduced in [23] and [6] determines the amplitude, phase angle, and frequency of the dominant component of an input signal. The mathematical relations require knowledge of three constant values that determine the gains for different operations such as the integrator blocks in the algorithm. The choice of the constants is critical in terms of influencing the performance of the algorithm and is typically optimized for a pre-selected operating point, i.e. 60 Hz. The algorithm is incapable of maintaining a set of optimized values for the constants as the frequency of the dominant component changes. Hence, the algorithm performance depends on the choice of the constants. For instance, a faster response time is achieved at the expense of degradation in the noise immunity. An approximate assessment of the algorithms performance is summarized below:

- A nominal frequency of 50/60 Hz,
- A frequency range of 20–120 Hz, and
- A transient response time of 6 cycles based on the nominal frequency value.

B. Multi-rate Phase Locked Loop

A synchronization system based on a multi-rate phase locked loop (MPPLL) that operates with two different sampling rates is presented in [5]. One sampling rate referred to as the fast sample rate is higher than the input signal frequency. The other sample rate is equal to the input signal frequency and is referred to as the slow sample rate. If the frequency changes, an error signal is generated that consequently changes the fast sample rate such that the MPPLL remains phase synchronized with respect to the input signal. The response time of the MPPLL to a 1 Hz step frequency perturbation is in the order of seconds. The long delay time is a direct result of the tradeoff between the dynamic response and noise immunity of the MPPLL. A performance summary of the algorithm is provided below:

- A nominal frequency of 50/60 Hz,
- A frequency range of 48–72 Hz, and
- A slow response time in the order of seconds.

C. Three-Phase Phase Locked Loop

A three-phase PLL based synchronization system that consists of a phase detector and a loop filter is reported in [9], [24]. The phase detector is designed using a *dq*-transformation frame. The loop filter consists of a PI regulator that generates a phase error employed by a voltage controlled oscillator (VCO). The design of the loop filter involves a trade off between the dynamic

performance and filtering of undesired distortion on the input signals. The loop filter requires a low bandwidth to become effective in filtering input signals superimposed with harmonics and/or DC-offset. The low bandwidth results in a poor dynamic response. The performance of the three-phase PLL is summarized as follows:

- Poor dynamic response due to a low bandwidth implementation of the loop filter, and
- Lack of frequency adaptability.

IV. WIDE-RANGE SYNCHRONIZATION SYSTEM

The design of a wide-range synchronization system (WSS) based on a predictive phase locked loop (PPLL) architecture is proposed [10]. The term wide-range signifies the capability of the system to respond to a wide range of changes in the input signal. The WSS can determine the frequency, amplitude, and phase angle of the input signal as well as synchronization signal. Fig. 2 shows the overall WSS block diagram consisting of input and output signals, a PPLL, and a signal generation block.

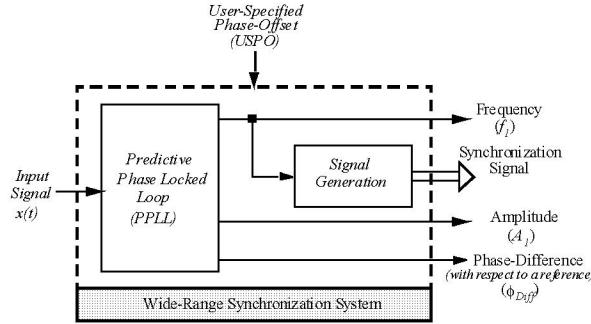


Figure 2. A schematic of the WSS.

The input signal ($x(t)$) is an AC voltage/current signal in the form of:

$$x(t) = s_I(t) + n(t) \quad , \quad (1)$$

where $n(t)$ is any superimposed signal such as harmonics, inter-harmonics, disturbances, DC offset, and noise and $s_I(t)$ is the fundamental component of $x(t)$ as follows:

$$s_I(t) = A_I \cdot \cos(2 \cdot \pi f_I \cdot t - \phi_{Diff}) \quad , \quad (2)$$

where A_I and f_I are the amplitude and frequency of the input fundamental component respectively and ϕ_{Diff} is the phase-difference that is the phase value with respect to a reference frame, to be described later.

User-specified phase-offset (USPO) is an input signal that enables the designer to dynamically offset the reference-point with respect to the selected reference-point while the WSS is operational. For example, it may be necessary to compensate for a phase shift due to components upstream such as a transformer.

The predictive phase locked loop (PPLL) enables the WSS to lock to the input signal phase and determines the frequency (f_I), amplitude (A_I), and phase-difference (ϕ_{Diff}). The PPLL also generates a signal denoted as a tracking signal that is an exact duplicate of the input

fundamental component when the system is in steady state. This signal is employed as the reference frame for ϕ_{Diff} . Under disturbance conditions, the frequency, amplitude, and/or phase variations of the input signal are detected by the PPLL and then the tracking signal is adjusted to match the input fundamental component. The tracking signal ($S_{TS}(t)$) can have an arbitrary phase offset (ϕ_{USPO}) and is defined by the following expression:

$$S_{TS}(t) = A_{TS} \cdot \cos(2\pi f_{TS} \cdot t - \phi_{USPO}) \quad , \quad (3)$$

where A_{TS} and f_{TS} are the magnitude and frequency of the tracking signal respectively.

In the steady state, $f_{TS} = f_I$, $A_{TS} = A_I$, and $\phi_{Diff} = 0$, therefore, (3) reduces to (2) and hence the tracking signal represents a duplicate of the input fundamental component.

A more detailed description of the PPLL which is comprised of a predictor, oscillator/phase-shifter, and data acquisition blocks is described next.

A. Predictor

The predictor computes the synchronization information consisting of f_I , A_I , and ϕ_{Diff} based on three samples extracted from the input signal referred to as s_0 , s_{120} , and s_{240} . These samples are positioned at 120° intervals with respect to each other and are used to characterize one period of the input signal. These three sample points are referred to as a three-sample cosine-wave. Fig. 3 shows the three-sample cosine-wave as squares that lie on the trajectory of the sinusoidal waveform (dotted line) as well as the tracking signal where $f_{TS} \neq f_I$ and $A_{TS} \neq A_I$.

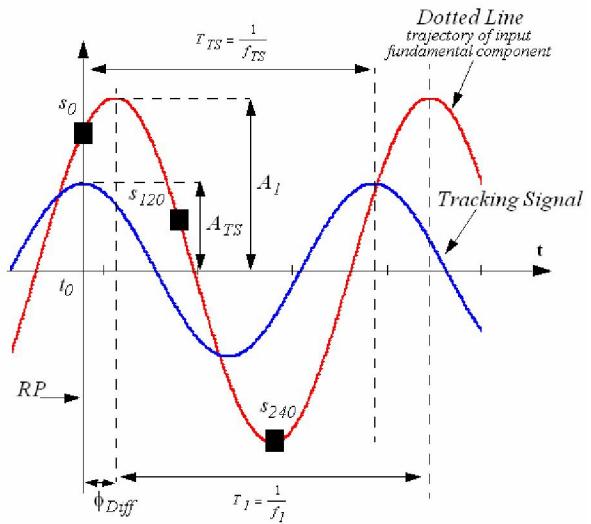


Figure 3. The three-sample cosine-wave (squares) and the tracking signal.

The synchronization information is determined based on a set of mathematical expressions such that [25]:

- The computation speed is maximized, and
- The real estate required for implementation is minimized.

The set of analytical expressions is as follows:

$$A_1 = \sqrt{s_d^2 + s_q^2}, \quad (4)$$

$$\phi_{Diff} = \arctan\left(\frac{s_q}{s_d}\right) \quad (5)$$

$$f_1 = f_{TS} \cdot \frac{3}{2\pi} \cdot \arccos\left(\frac{s_{120} + s_{240}}{2 \cdot s_0}\right), \quad (6)$$

where

$$s_d = \frac{2 \cdot s_0 - s_{120} - s_{240}}{3}, \quad (7)$$

$$s_q = \frac{\sqrt{3}}{3} \cdot (s_{120} - s_{240}), \quad (8)$$

B. Oscillator/Phase-Shifter

This block determines the sampling frequency (f_{sam}) given by:

$$f_{sam} = N_s \cdot f_1, \quad (9)$$

where N_s is the number of samples per cycle of the input signal.

Fig. 4 shows the input signal for $N_s = 12$ where this value is selected for ease of demonstration and s_0 , s_{120} , and, s_{240} are shown as squares.

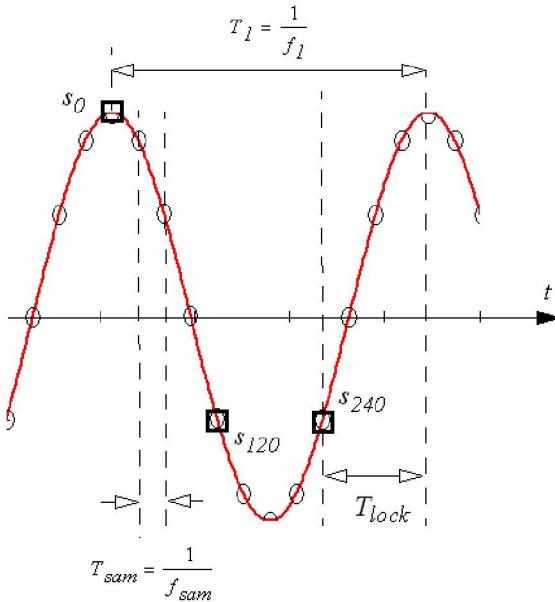


Figure 4. The input signal for $N_s = 12$ (squares denote s_0 , s_{120} , and, s_{240})

The computation of the synchronization information using (4)-(8) starts immediately after s_0 , s_{120} , and, s_{240} are accumulated. The computation begins $2/3$ of the way through a period of the input fundamental component (T_I), under steady state conditions. The remaining $1/3$ of the period, from s_{240} of the current period to s_0 of the next period, is referred to as the lock-time (T_{lock}), hence,

$$T_{lock} = \frac{T_I}{3}, \quad (10)$$

During T_{lock} , the following events occur:

- No samples are collected,
- Synchronization information is computed, and
- Phase locking of the PPLL is achieved.

During the occurrence of a frequency/phase change, ϕ_{Diff} becomes nonzero. ϕ_{Diff} is forced to zero by retarding or advancing the tracking signal with respect to the input fundamental component. The retardation/advancement is achieved by adjusting T_{lock} where

$$T_{lock} = \frac{1}{3}T_I + t_{RA}, \quad (11)$$

and t_{RA} is the retard/advance time.

t_{RA} is related to the phase-difference by the following expression:

$$t_{RA} = \frac{\phi_{Diff}}{2\pi} \cdot T_I \quad (12)$$

The period of the input fundamental component is related to the sampling period by the number of samples per period (N_s) as:

$$T_I = N_s \cdot T_{sam} \quad (13)$$

Combining (11), (12), and (13) results in:

$$T_{lock} = N_s T_{sam} \cdot \left(\frac{1}{3} + \frac{\phi_{Diff}}{2\pi} \right) \quad (14)$$

The expression (14) represents the time remaining from the acquisition of s_{240} until the arrival of s_0 associated with the next period. Therefore, a reduction in T_{lock} causes an advancement of the tracking signal by starting the next period earlier while an increase of T_{lock} delays the start of the next period.

The expression (14) refers to the value of T_{lock} required to advance, to retard, or not to change the tracking signal so that ϕ_{Diff} is forced to zero. The three possibilities are explained below.

Advance Tracking Signal

A negative ϕ_{Diff} occurs when f_1 increases. The increase in f_1 leads to a decrease in T_{lock} such that the start of the next cycle of the tracking signal is advanced in order to coincide with s_0 of the three-sample cosine-wave. The minimum T_{lock} is given by:

$$\lim_{f_1 \rightarrow \infty} T_{lockMin}(f_1) = 0 \quad (15)$$

In practice, the algorithm takes a finite amount of time (t_p) to compute f_1 , A_1 , and, ϕ_{Diff} , consequently, the minimum that T_{lock} can be decreased by is

$$T_{lockMin} = t_p \quad (16)$$

Steady State (No Change Required)

Under steady state operating conditions, ϕ_{Diff} is zero and hence T_{lock} is exactly equal to $1/3$ of the current input signal period. Thus, no retardation/advancement is required. As a result, the phase-shifter block waits for $T_I/3$ which is the same as the previous prediction period and the tracking signal remains unchanged.

Retard Tracking Signal

A positive nonzero Φ_{Diff} occurs when f_I decreases. The decrease in f_I leads to an increase in T_{lock} such that the start of the next cycle of the tracking signal is retarded in order to coincide with s_0 of the three-sample cosine-wave. The maximum time that T_{lock} can be increased by is

$$\lim_{f_I \rightarrow 0} T_{lockMax}(f_I) = \infty \quad (17)$$

V. IMPLEMENTATION

The WSS is implemented on a field programmable gate array (FPGA) based platform consisting of a FPGA device from the Xilinx Virtex-II family (XC2V2000-4FG676) [26].

Fig. 5 shows the input signal at 60 Hz including: fundamental component, 3rd harmonic, and 5th harmonic.

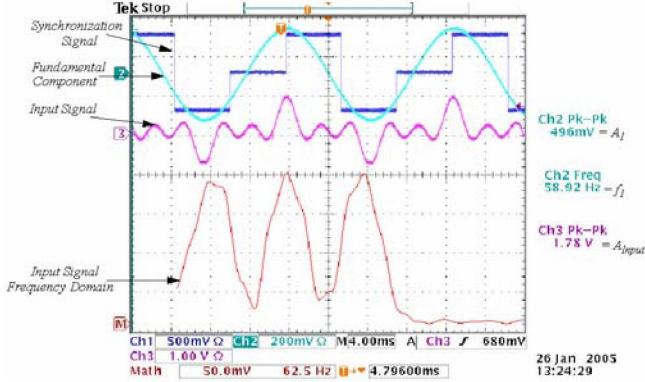


Figure 5. Input signal with fundamental, 3rd, and 5th harmonics at 60 Hz.

The performance of the WSS system at the upper frequency bound under conditions of severe distortion and a minimum amplitude is shown in Fig. 6; a square wave input signal with a frequency of 2 kHz, a DC-offset, and a minimum amplitude of 0.098 volts.

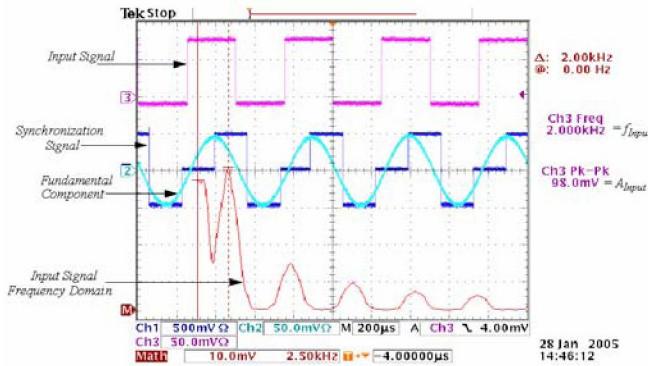


Figure 6. Square wave input signal with a 2 kHz frequency, a DC offset and a 0.098 volt amplitude.

Fig. 7 shows the tracking performance of the WSS system in response to a frequency ramp with a rate of 120 Hz/sec. The frequency is varied from 40 Hz to 160 Hz.

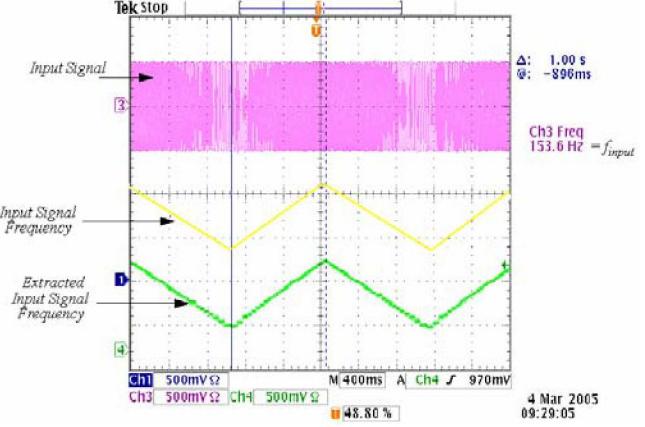


Figure 7. Response to a 120 Hz/sec change in the input signal frequency.

Fig. 8 illustrates the performance of the WSS system when the amplitude is ramped up/down. Channel 2 and 3 show the extracted amplitude and the input signal respectively. The rate of change of amplitude is approximately 66% of the maximum allowable amplitude imposed by the FPGA platform.

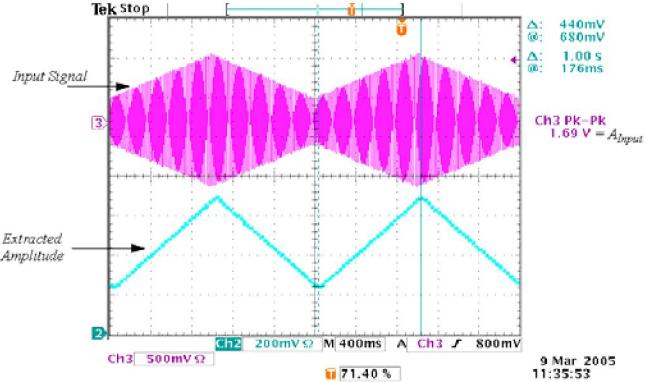


Figure 8. Response of WSS to an amplitude ramp.

The response of the WSS system to a phase step of 30° is shown in Fig. 9.

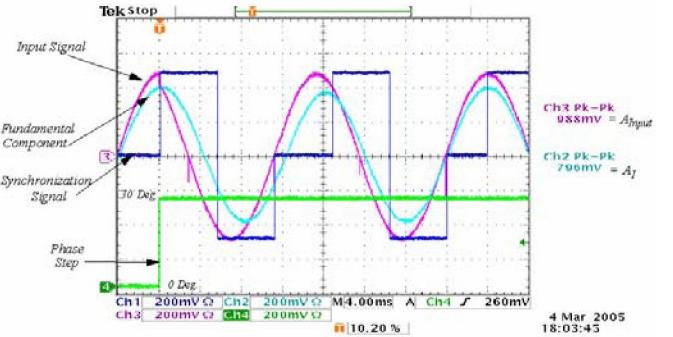


Figure 9. Response of WSS to a phase step of 30°.

The tracking properties of the WSS are verified and exhibit a two cycle response time under worst case conditions.

VI. CONCLUSIONS

A wide-range synchronization system (WSS) based on a predictive phase locked loop (PPLL) for application in utility and non-utility power systems is presented. The experimental results verify an amplitude range of approximately 3% to 100% of nominal value and a frequency range that spans approximately 0 to 2 kHz. The WSS remains functional under sever frequency variation up to 120 Hz/sec. in the presence of superimposed noise and harmonics/inter-harmonics. The WSS tracking performance exhibits a two cycle response time under worst case conditions.

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