A PEAK DETECTOR FOR MULTI-RATE PHASE LOCKED LOOP AND SEQUENCE DETECTOR COMBINATION FOR UTILITY AC POWER APPLICATIONS

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Abstract

Synchronization is of concern in AC power systems. Existing synchronization algorithms are hardware intensive. A single phase synchronization scheme referred to as a multi-rate phase locked loop (MPLL) has been reported. The stability of the MPLL is influenced by amplitude variations. An amplitude estimation module based on a fast Fourier transform (FFT) algorithm and an automatic gain control (AGC) are employed to decouple amplitude variations from phase variations. The implementation of the FFT-based amplitude-estimator is complex and hardware intensive. A peak detector module that utilizes only two multiplexers and one comparator is proposed to replace the FFT-based amplitude-estimator. A real-time positive sequence detector is also combined with the MPLL in order to allow process of the three-phase signals. The overall system is implemented and compared for both FFT-based and peak detector approaches and indicates a 60 dB immunity to impulse noise and harmonic contamination and a 20 dB dynamic range

Keywords*: Fast Fourier Transform, FPGA, Multi-rate Phase Locked Loop (MPLL), Positive Sequence Detector.*

1. Introduction

Accurate synchronization is of necessary requirements in distributed AC power systems and is an important requirement in any real-time measurement and control system [1, 2]. Existing synchronization algorithms impose great demands on computational hardware resources. In many cases the schemes are not robust against line disturbances/momentary outages or cannot accommodate input frequency variations. A dedicated hardware approach is required that addresses the conventional implementation complexity of existing synchronization schemes and the issue of robustness.

A single phase synchronization scheme referred to as a multi-rate phase locked loop (MPLL) has been reported [3]. The stability of the MPLL is influenced by amplitude variations, thus an amplitude estimation module based on a fast Fourier transform (FFT) algorithm and an automatic gain control (AGC) module are employed to decouple amplitude variations from phase variations. The design of FFT is complex and resource intensive. The FFT, in turn, affects the MPLL complexity and makes the MPLL not a preferred choice.

This paper proposes a peak detector that replaces FFT and offers a low complexity approach for amplitude estimation. Section 2 explains the structure of the multi-rate phase locked loop and positive sequence detector. Section 3 describes the design and experimental results of the peak detector. Section 4 provides the conclusion

2. Combined Method

A brief description of the combined method including multi-rate phase locked loop and positive sequence detector is provided in sections 2.1 and 2.2 respectively.

2.1. Multi-rate Phase Locked Loop

Utility networks and power systems require synchronization information. A multi-rate phase locked loop (MPLL) introduced earlier can provide the synchronization information [3]. The MPLL locks to the fundamental component of the input signal and then provides information from zero crossings of the input signal for synchronization purposes. This system provides synchronization information in the presence of severe disturbances on power lines and a time varying signal frequency and fundamental component amplitude.

Figure 1 shows a block diagram of the MPLL. A bandpass digital filter is used to attenuate the disturbances and any harmonics on the line. The resultant fundamental component of the input signal is provided to a downsampler block. An

amplitude estimator in combination with an automatic gain control (AGC) is used to make the controller response insensitive to changes in the input signal magnitude. The output of the controller is an error signal. A nonzero error signal, depending on its polarity, decreases or increases the sampling frequency of an analog-to-digital (A/D) converter and also ensures that the output fundamental component signal remains in phase with the input fundamental component signal.

The MPLL operates at two sample rates. These sample rates are referred to as fast ($f_{sampling}$) and slow (f_{in}) where f_{in} is equal to the input signal frequency. $f_{sampling}$ and f_{in} are related to each other by the number of samples per cycle (N) such that:

$$N = \frac{f_{sampling}}{f_{in}} \tag{1}$$

The sampling rate of the ADC is set by the fast sample rate ($f_{sampling}$). The MPLL unit synchronizes to the input frequency by varying the sampling rate which is generated by a numerical controlled oscillator (NCO) and hence maintaining a synchronous sampling.

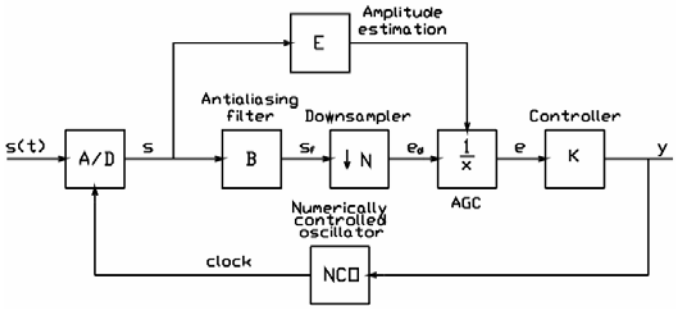


Fig. 1. Functional block diagram of the MPLL [3].

The MPLL is implemented on a microprocessor platform [4]. The implementation results indicate a 60 dB immunity to impulse noise and harmonic contamination as well as a 20 dB dynamic range.

Figure 2 illustrates the frequency tracking performance in the presence of a notch type disturbance. In Figure 2, the dashed line indicates the resulting synchronization signal whereas the solid line indicates the AC network voltage with notch type disturbances.

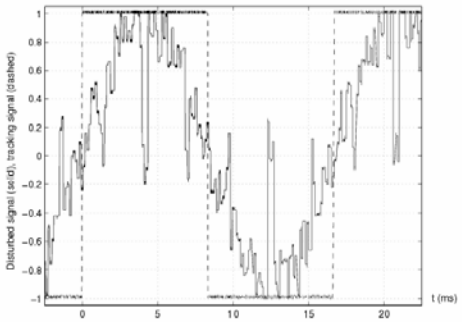


Fig. 2. Notch type tracking performance [3].

The MPLL tracking properties are also tested using an arc furnace voltage as the input signal. Arc furnaces are known for their ability to generate disturbances onto the AC utility network. Figure 3 illustrates this case where a typical estimate of the arc furnace voltage zero crossings is shown in the form of the rectangular signal drawn by the dashed line.

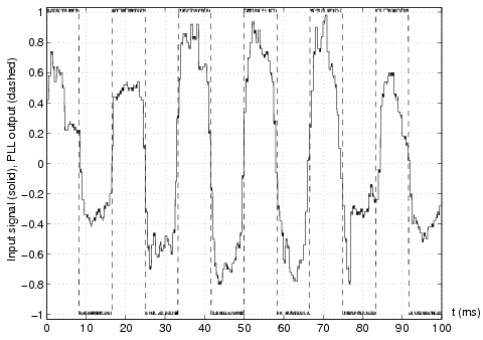


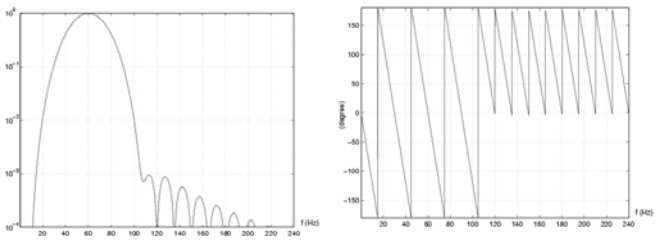
Fig. 3. Arc furnace tracking performance [3].

The bandpass filter is designed based on the specification summarized in Table 1.

Attenuation at DC	60 dB
Higher Stopband Frequency	120 Hz.
Stopband Attenuation	60 dB

Table. 1. Filter specification.

The filter design can be performed by employing the *fir1* function from the Matlab that allows implementation of a finite impulse response (FIR) filter. The magnitude and phase response of the bandpass filter which satisfies the specification in Table 1 for the case with an upsampling ratio of N=128, is shown in Figure 4 *(a)* and *(b)* respectively. The order of the filter is N = 512 and it is designed using the Blackman window since it gives a higher stopband attenuation as compared to other windows for the same filter order. The impulse response for the FIR filter is shown in Figure 5.



(a) *(b)*

Fig. 4. Magnitude *(a)* and phase response *(b)* of bandpass filter [3].

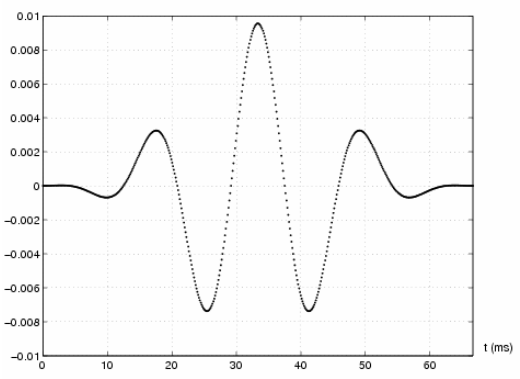


Fig. 5. Impulse response of the bandpass filter [3].

2.2. Positive Sequence Detector

Sequence components are employed in three-phase power networks to detect system unbalances. An unbalanced system leads to positive, negative, and zero sequence components while a balanced system produces only a positive sequence component. The positive sequence is the component that represents the main characteristics of the three-phase electric power. This is the signal employed by the MPLL for synchronization purposes.

The details of mathematical properties of positive sequence detector are reported in [5]. The experimental results are shown in Figure 6 [6]. In Figure 6 from *0* to t_2 the input is a symmetrical positive sequence and the magnitude changes at t_1. At t_2 and t_3, only zero and negative sequences are present respectively. Finally, at t_4, only the positive sequence reappears.

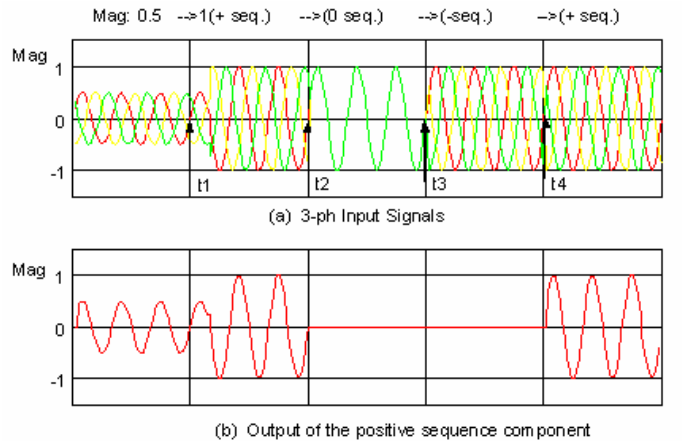


Fig. 6. Positive sequence outputs for different inputs [6].

3. Peak Detector

A peak detector module is developed to replace the FFT-based approach. The peak detection module is simple and offers a low complexity approach, hence, utilizes fewer hardware resources.

In power systems applications signals may be superimposed with noise, harmonics, inter-harmonics, and notch type disturbances. Thus, in the MPLL implementation, the design of a finite impulse response (FIR) filter becomes essential. The FIR Filter extracts the fundamental component of the positive sequence and delivers that to the downsampler block, see Figure 1. In the proposed method, however, the output of the FIR filter connects to a peak detector module as well as the downsampler. Figure 7 shows the peak detector included in the design of the MPLL. The peak detector block determines the amplitude of the fundamental component whereas the downsampler block extracts the zero-crossing value of the fundamental component. Under steady state conditions, the output of the downsampler is zero, which implies that the MPLL synchronizes to the fundamental component of the positive sequence. The amplitude and the zero-crossing values are then used by the automatic gain controller (AGC) for a normalization purpose. The normalization process ensures that the phase variations are decoupled from the amplitude variations. The normalized zero-crossing values are used by the controller to adjust the oscillation frequency of the numerically controlled oscillator (NCO) to achieve synchronization.

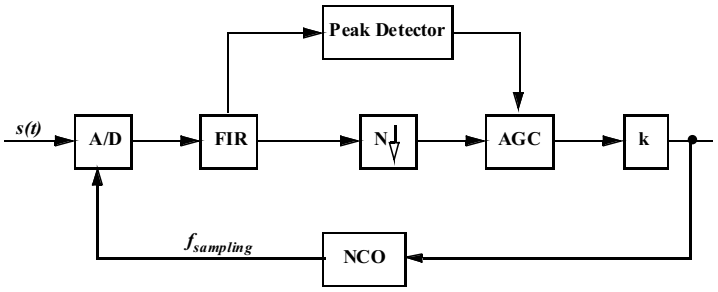


Fig. 7. Block diagram of the MPLL including peak detector.

The peak detector is implemented on a field programmable gate array (FPGA) platform [4]. The peak detector utilizes two multiplexers and one comparator and operates on a per cycle basis; it compares two consecutive samples, stores the larger one, and resets itself every cycle. A constant zero is employed to initialize the first comparison at startup. Figure 8 shows the a block diagram of the peak detector including the bit width flow. In Figure 8 "A" shows connection to the FPGA clock frequency (broken line), the control signals are indicated with a broken line with two dots, and the solid lines indicate the data flows.

The peak detector reduces the design complexity and hardware requirements. The experimental results indicate that peak detector approach offers identical tracking performance to the FFT-based amplitude-estimator. The dynamic range and the immunity to noise remain at 20 dB and 60 dB respectively.

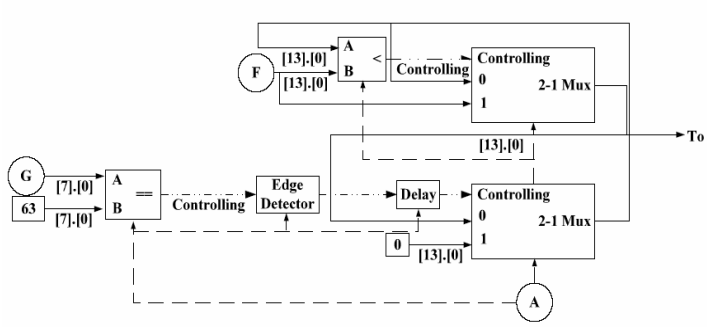


Fig. 8. Peak detector structure including bit width flow.

4. Conclusions

The design of a mutlirate phase locked loop (MPLL) for synchronization purposes in power system networks is revisited. The MPLL requires knowledge of the input signal amplitude. In the MPLL earlier design, a Fast Fourier Transform (FFT) block estimates the input signal amplitudes. The design of a FFT-based amplitude-estimator is resource intensive and requires 128 complex multipliers with 128 points if implemented on a FPGA platform. A peak detector module is proposed to replace FFT-based amplitude-estimator. The peak detector utilizes two multiplexers and one comparator and operates on a per cycle basis that offers a fast response time. The peak detector also reduces the design complexity and hardware requirements. To apply this synchronizing scheme to three phase applications, the MPLL operates in combination with a positive sequence detector module that generates the synchronizing source. The overall system including the MPLL and positive sequence detector is implemented on a FPGA platform and compared for both cases of the FFT-based and peak detector approaches. The results are identical.

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