A Three-Phase Frequency Adaptive Digital Phase Locked Loop for Measurement, Control, and Protection in Power Systems

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Abstract- **A three-phase phase locked loop (3-Φ PLL) for control and protection in power system applications is presented. The 3-Φ PLL is a frequency adaptive digital system that consists of a positive sequence detector and a single-phase predictive phase locked loop (PPLL). The 3-Φ PLL is fully adaptive in extracting frequency, amplitude, and phase angle in time variant systems. The modeling and mathematical properties of the positive sequence detector and the PPLL are presented. The 3-Φ PLL can accommodate a wide range of frequency and amplitude variations in the presence of noise and disturbances. The 3-Φ PLL is implemented on a field programmable gate array (FPGA). A number of analog-to-digital converters (ADCs) have been evaluated for this application. A successive approximation type ADC offers the best tradeoff between resolution and sampling frequency. The synchronization information is extracted within two cycles of the input signal period. The operation of the 3-Φ is verified for balanced and unbalanced loads in the presence of noise, harmonics, and DC-offsets over a frequency range of a fraction of Hz to a few kHz and over an amplitude range of about 3% to 120% of the nominal voltage.**

Key Words: Digital phase locked loop, FPGA, multi-rate sampling, sequence component detection.

I. INTRODUCTION

In recent years, the significance of the power losses due to power outages emphasizes the importance of a high power quality (PQ) and the reliability of electric power supply to consumers [1]-[4]. The avoidance of nuisance trips that lead to downtime, the maximization of system availability or improvements in PQ are becoming increasingly more important given that modern equipment is more susceptible to PQ problems, let alone the cost of downtime [5]. Active and passive power electronics controllers along with control algorithms are being used to improve PQ. The control algorithms require real-time voltages/currents from the power lines.

The power system experiences disturbances from event driven processes occurring in the network; for example, voltage sags/swells, transients from switching capacitor banks, momentary interruptions, harmonic distortions, notch-type disturbances from converters, and other unquantifiable noise.

The monitoring of a power system is performed from generation to end user at each step of the power chain. The monitoring provides parameters such as frequency, amplitude, phase angle, harmonic components, power delivered, and power factor. The control applications employ the monitored parameters to compensate for any reduction in PQ and to improve power system reliability.
The monitored parameters can be determined from knowledge of line frequency, amplitude, and phase angle obtained from voltages and currents. Henceforth, the data set consisting of frequency, amplitude, phase angle, and time of zero crossing is referred to as synchronization information. Algorithms are used to generate some or all of this data.

Existing algorithms are capable of operation only at the utility frequency (50/60 Hz.) over a range of about 40 to 72 Hz [6], [7]. The response times of these algorithms are slow; from 5 cycles of the nominal frequency value up to seconds. These algorithms place a constraint on the software resources, can be susceptible to line disturbances and focus on stiff utility applications (small frequency variations).

The 3-Φ PLL, proposed in this paper, addresses a broader range of applications and has the following features and performance.

- A positive sequence detector extracts in real time the positive sequence component from the three-phase signals while a predictive phase locked loop (PPLL) extracts the synchronization information from the positive sequence component.
- The combined system uses a low complexity algorithm and is suitable for utility and non-utility power systems applications.
- The 3-Φ PLL is implemented on a field programmable gate array (FPGA) device.
- The PPLL is immune to wide band stationery or non-stationery noise, harmonics/inter-harmonics, and disturbances.

Section II provides a description of the positive sequence detector and Section III presents an analysis of the PPLL. Section IV describes the properties of the combined system. The experimental implementation and results are provided in Section V. Section VI presents the conclusions.

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II. SEQUENCE COMPONENT DETECTOR

The voltage/current signals obtained from power lines are in the form of three-phase sinusoidal signals. The three phase signals can be processed or transformed into a different reference frame and then post-processed. For synchronization applications, it is advantageous to extract the positive sequence component of the three phase signals for the following reason [8]. A three-phase system may be unbalanced. The unbalanced system can occur because of faults between the phases and/or ground, open phases, and/or unbalanced loading such as static power equipment and single-phase devices. A system unbalance will generate negative and zero sequence components while a balanced system produces only a positive sequence component. The positive sequence component is derived from the generating source and hence it is the correct signal to employ for extracting the synchronization information. The extraction of the positive sequence component from three-phase signals is presented next.

A. Extraction of Positive Sequence Component

Unbalanced voltages or currents can be determined from the sequence components using the following set of equations [8]:

$$\begin{pmatrix} V_a \\ V_b \\ V_c \end{pmatrix} = \begin{pmatrix} 1 & 1 & 1 \\ \alpha^2 & \alpha & 1 \\ \alpha & \alpha^2 & 1 \end{pmatrix} \cdot \begin{pmatrix} V_+ \\ V_- \\ V_0 \end{pmatrix}, \qquad (1)$$

where

V_a, V_b, and V_c are the three phase unbalanced line to neutral phasors, and

V_+, V_- and V_0 are positive, negative and zero sequence component phasors.

From equation (1), the positive sequence component can be written as:

$$3V_+ = V_a + V_b e^{-j240^\circ} + V_c e^{-j120^\circ} \qquad (2)$$

and in the time domain, equation (2) may be written as:

$$3V_+(t) = V_a(t) + V_b(t - \frac{2T}{3}) + V_c(t - \frac{T}{3}), \qquad (3)$$

where T is the fundamental period.

Fig. 1 shows the response time which is a consequence of equation (3). This algorithm generates a 2/3 of a period delay that is considered too large [9]. Also, this algorithm generates an incorrect positive sequence component during input signal changes. This is due to the change in the data window when the input signal changes. Fig. 1 also shows that the data window contains both pre- and post-change data that corrupts the outcome of equation (3).

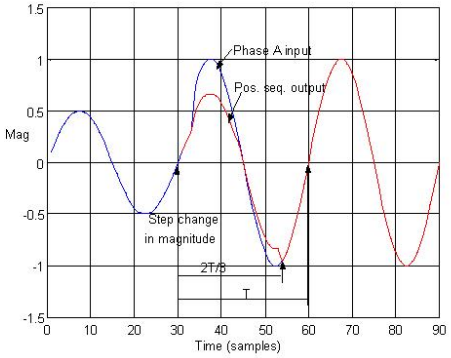

Fig. 1. Time response of conventional symmetrical component extraction method [9].

These drawbacks are corrected by considering sinusoidal signals with frequency f_1 at a sampling rate f_{sam}, where the phase shift α of one sample delay is equal to $2\pi f_1/f_{sam}$. Hence, equation (2) can be written as:

$$3V_+ = V_a + P_b V_b - Z_b V_b e^{-j\alpha} - P_c V_c + Z_c V_c e^{-j\alpha}. \qquad (4)$$

where the coefficients in the equation (4) can be derived as follows:

$$P_b = \frac{1}{\tan(30^\circ + \alpha)\cos 30^\circ - \sin 30^\circ}, \qquad (5)$$

$$Z_b = \frac{1}{\sin(30^\circ + \alpha) - \cos(30^\circ + \alpha)\tan 30^\circ}, \qquad (6)$$

$$P_c = \frac{1}{\sin 30^\circ - \tan(30^\circ - \alpha)\cos 30^\circ}, \qquad (7)$$

$$Z_c = \frac{1}{\cos(30^\circ - \alpha)\tan 30^\circ - \sin(30^\circ - \alpha)}. \qquad (8)$$

The time domain representation of equation (4) can be used to extract the positive sequence component and has the following discrete form:

$$3V_+(k) = V_a(k) + P_b V_b(k) - Z_b V_b(k-1) - P_c V_c(k) + Z_c V_c(k-1) \qquad (9)$$

The positive sequence component output waveforms, as shown in Fig. 2, show the existence of impulses when the input signal changes, however, the delay times are now considerably shorter. These impulses are removed by employing a median filter, as shown in Fig. 2.

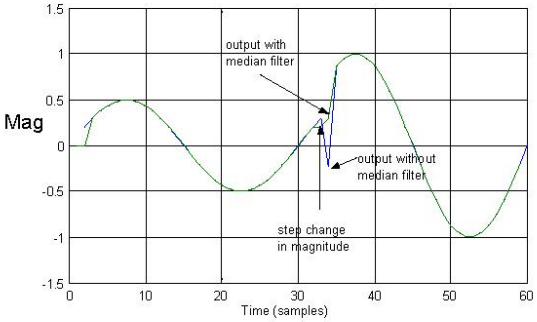

Fig.2. Comparison of positive sequence output with/without a median filter [9].

The frequency characteristics of the positive sequence

algorithm is obtained by substituting $\alpha - 2\pi f_1 / f_{sam}$ into equation (4) and expressing V_b and V_c in terms of V_a. This results in:

$$\frac{3V_+(f_1)}{V_a} = 1 + P_h e^{j240^\circ} - Z_h e^{j(240^\circ - \frac{2\pi f_1}{f_{sam}})} - P_c e^{j120^\circ} + Z_c e^{j(120^\circ - \frac{2\pi f_1}{f_{sam}})} \quad (10)$$

B. Simulation Results

A number of simulations were performed using MATLAB. A step change in the input signal magnitude indicates that equation (9) generates the correct output results after one sample delay. In contrast, the delay for the conventional method in providing the correct output is equal to 2/3 of one period. Fig. 3 shows the results.

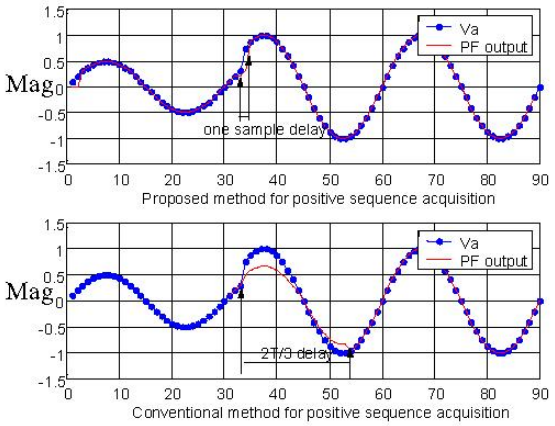

Fig. 3. Comparison of two sequence extraction methods [9].

III. SINGLE-PHASE PREDICTIVE PHASE LOCKED LOOP

This section explains the design of a predictive phase locked loop (PPLL) [10], [11]. The PPLL can be applied to input signals with a wide range of frequency, amplitude, and phase-angle variations. The PPLL extracts frequency (f_1), amplitude (A_1), and phase-difference (Φ_{Diff}) from single-phase voltage/current signals superimposed with wideband stationary/non-stationary noise, harmonics/inter-harmonics, and impulse or notch type disturbances.

The PPLL generates a signal denoted as a tracking signal that is an exact duplicate of the input fundamental component when the system is in steady state (i.e. identical frequency, amplitude, and phase). Under disturbance conditions, the frequency, amplitude, and/or phase variations of the input signal are detected by the PPLL and then the tracking signal is adjusted to match the input fundamental component. Fig. 5 provides a simplified block diagram illustrating the operation of the PPLL. The fundamental component is extracted by first digitizing the input signal with an analog-to-digital converter and then extracting the input fundamental component with a digital band-pass filter. The center frequency of the digital band-pass filter coincides with the input signal fundamental component. The input signal frequency may vary in the range of:

$$f_{1Min} \le f_1 \le f_{1Max} \quad , \quad (11)$$

where f_{1Min} and f_{1Max} are the minimum and maximum values of the input fundamental frequency respectively.

A frequency adaptive digital band-pass filter is implemented to; (*a*) filter frequencies above and below the center frequency; (*b*) maintain a zero degree phase shift between the input and output fundamental component; (c) maintain a constant amplitude as the frequency is varied. The digital filter operates based on a sample window [12] and for an adaptive filter, synchronous sampling is employed to maintain the number of samples within the sample window constant [13], [14].

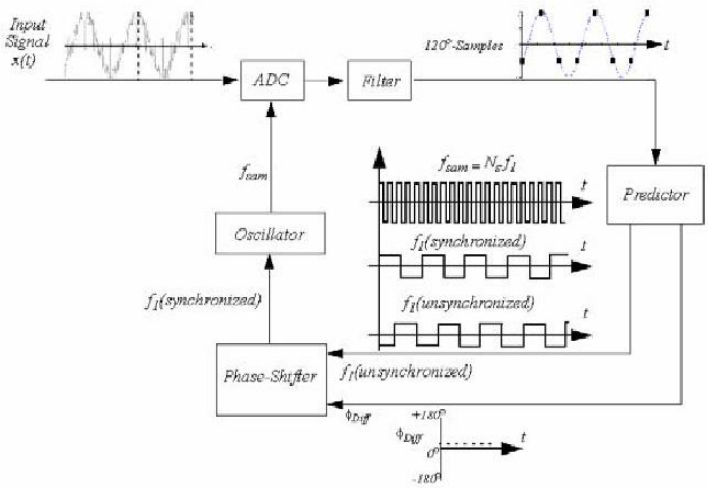

Fig. 5. A simplified block diagram showing the operation of the PPLL.

The predictor is the core of the PPLL. The predictor acquires three 120° equidistant samples from the input fundamental component referred to as s_0, s_{120}, and s_{240}. The three 120°-samples are used to characterize one period of a sinusoidal waveform and are henceforth called a three-sample cosine-wave. Fig. 6 shows the samples of the three-sample cosine-wave as squares that lie on the trajectory of the sinusoidal waveform (dotted line).

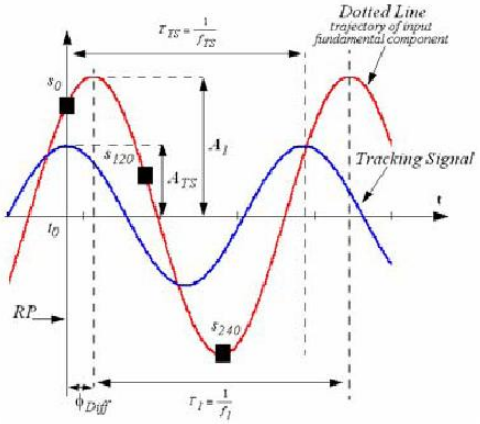

Fig. 6. The three-sample cosine-wave (squares) and the tracking signal.

The three-sample cosine-wave is given by the following three equations:

$$s_0 = A_1 \cdot \cos(\alpha - \phi_{Diff}) \quad , \quad (12)$$

$$s_{120} = A_1 \cdot \cos\left(\alpha - \phi_{Diff} - \frac{2\pi}{3} \frac{f_1}{f_{TS}} \right) , \quad (13)$$

$$s_{240} = A_1 \cdot \cos\left(\alpha - \phi_{Diff} - 2 \cdot \frac{2\pi}{3} \frac{f_1}{f_{TS}} \right) . \quad (14)$$

The frequency, amplitude, and phase angle of the three-phase cosine-wave are determined from equations (11) to (13) based on a set of mathematical expressions for frequency, amplitude, and phase-difference as given below respectively:

$$f_1 = f_{TS} \cdot \frac{3}{2 \cdot \pi} \cdot acos\left(\frac{s_{120} + s_{240}}{2 \cdot s_0} \right) , \quad (15)$$

$$A_1 = \sqrt{s_d^2 + s_q^2} , \quad (16)$$

$$\phi_{Diff} = atan\left(\frac{s_q}{s_d} \right) , \quad (17)$$

where

$$s_d = \frac{2 \cdot s_0 - s_{120} - s_{240}}{3} , \quad (18)$$

$$s_q = \frac{\sqrt{3}}{3} \cdot \left(s_{120} - s_{240} \right) . \quad (19)$$

The frequency calculated in (15) is independent of the phase-difference (Φ_{Diff}) and hence is not necessarily aligned with the reference-point. The phase-shifter block adjusts the edge of the unsynchronized f_1 so that its rising edge becomes aligned with the reference-point. This results in synchronization with respect to the input fundamental component.

The sampling frequency (f_{sam}) is an integer multiple of f_1 (synchronized) and this allows the analog to digital converter to operate with synchronous sampling.

IV. COMBINED SYSTEM

The PPLL extracts the frequency (f_1), amplitude (A_1), and phase-difference (Φ_{Diff}) denoted as synchronization information from the positive sequence component. Frequency feedback, provided by the PLL, is used to synchronize the frequency of the positive sequence detector, in real-time, to the frequency of the input signal.

Fig. 7 shows a block diagram of the 3-Φ PLL. The PPLL extracts the synchronization information including frequency, amplitude, and phase angle from the positive sequence component. The PPLL uses the input signal frequency to generate a sampling rate such that:

$$f_{sam} = f_1 . N_s \quad (20)$$

where f_{sam} is the sampling frequency, f_1 is the fundamental input signal frequency, and N_s is the number of samples per period of the input signal.

This sampling rate (f_{sam}) forces synchronous sampling by maintaining the number of samples per period (N_s) constant [6], [7]. As a result, the positive sequence detector and the fundamental sample extractor (FSE) track the input signal frequency. The rate at which ADCs sample the input signal is denoted as f_{ADC} such that $f_{ADC} >> f_{sam}$. This results in an over-sampling of the input signal that reduces the design requirements of the front-end ADC low pass filter. The over-sampled input signals are down-sampled by the ADS blocks at a rate set by the sampling frequency (f_{sam}).

The positive sequence detector has a high-pass filter characteristic and hence a band-pass filter is required to attenuate higher harmonic components and extract the fundamental component of the input signal. This band-pass filter is referred to as a fundamental sample extractor (FSE). It filters only samples that are 120°-apart and hence reduces the implementation complexity. The accumulator block collects three samples 120°-apart and transfers them to the processor. The processor determines the frequency (f_1), amplitude (A_1), and the phase-difference (Φ_{Diff}) from the positive sequence component signal using expressions (15) to (17). The phase-shifter accounts for the value of the phase-difference (Φ_{Diff}) and advances or retards the frequency (f_1). Finally, the oscillator computes the values of the sampling rate (f_{sam}) and the ADC frequency (f_{ADC}).

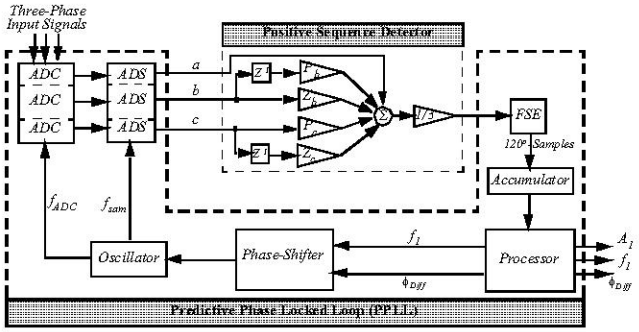

Fig. 7. Block diagram of the 3-Φ PLL including the positive sequence detector and the PPLL.

A. Analog-to-Digital Converters

The analog to digital converters (ADCs) are required at the front-end of the 3-Φ PLL to convert the continuous time input signal into a digital form. ADCs are available in various speeds, with different interfaces, and provide different levels of accuracy. The performance of the ADCs is summarized in Table 1.

Design	Speed	Resolution (*Bits*)	Power Dissipation	Group Delay	Cost
SAR	Medium	10 – 6	Medium	N/A	Medium
Flash	Fast	4 – 8	High	N/A	Low
Delta-Sigma	Slow	20 - 24	Low	Yes	High

Table 1: Summary of the ADC comparison.

The flash ADCs offer a very fast sampling frequency that is not required for power systems applications. These applications are concerned with signals with low frequencies of the order of a few kHz and hence do not

require very fast sampling rates. The flash ADCs offer very few bits and hence the accuracy of the sampled data is reduced.

The sigma-delta ADCs offer very high resolution capabilities and thus the input sampled signal is recorded with high accuracy. The sigma-delta ADC suffers from relatively low sampling rates. Another problem with the sigma-delta ADCs is their group delays. The group delay introduces a phase shift to the input signal. The phase shift introduced by the sigma-delta ADC does not allow real-time acquisition and processing of the incoming power systems signals.

Successive approximation register (SAR) based ADCs offer a reasonably high sampling frequency that can accommodate the power system applications requirements. The SAR is also capable of providing resolutions comparable to those from sigma-delta ADCs. The cost of the SAR-based ADCs is also relatively low. Hence, the SAR-based ADC is selected for the implementation of the 3-Φ PLL. The SAR-based ADC provides a compromise between fast sampling frequency and a high accuracy and hence is employed for implementation of the 3-Φ PLL.

Delta-sigma and SAR ADCs with resolutions of 12, 14, 16, and 24 bits have been experimentally tested for the 3-Φ PLL. A 16-bit SAR-based ADC proved to provide the best trade off between the sampling frequency and the resolution.

V. Implementation and Results

The 3-Φ PLL comprised of the positive sequence detector and the PPLL is implemented on a Xilinx field programmable gate array (FPGA) [15]. This section provides the experimental results for different test scenarios.

A. Balanced Three-Phase Steady State

The 3-Φ PLL is connected to the utility network with a frequency of 60 Hz. Fig. 8 shows the result of the experiment. Channel 1 is the extracted fundamental component from phase *a* and the other channels are the three-phase input signals from the utility network.

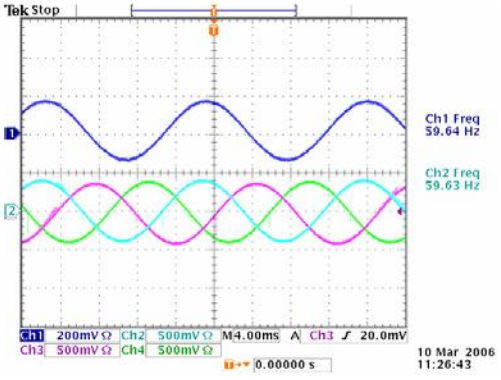

Fig. 8. 3-Φ PLL: three-phase balanced input where the system is connected to the utility network at 60 Hz.

B. Balanced Three-Phase with Minimum Amplitude

The 3-Φ PLL is tested for a minimum amplitude and the result is shown in Fig. 9. The minimum amplitude tested is 0.083 volts p-p which is approximately 2.5% of the nominal value of 3.6 volts p-p allowable by the platform.

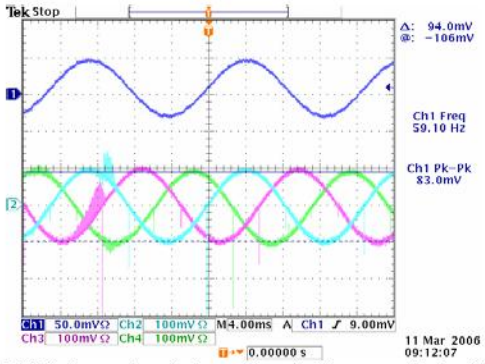

Fig. 9. 3-Φ PLL: three-phase balanced input with an amplitude of 83 mV.

C. Balanced Three-Phase Superimposed with Harmonics

Fig. 10 shows the result for a three-phase input at 60 Hz with a 3rd harmonic (at 120 Hz) added to phase *a*. Fig. 11 illustrates a three-phase 60 Hz with DC-offset and 3rd, and 5th harmonics added to phase *a*. Fig. 12 shows a three-phase input signal at 60 Hz with a 3rd harmonic added to phases *a* and *c*. In Figs. 10 to 12, channel 1 is the extracted fundamental component from phase *a*. A microprocessor was used to generate the input signals.

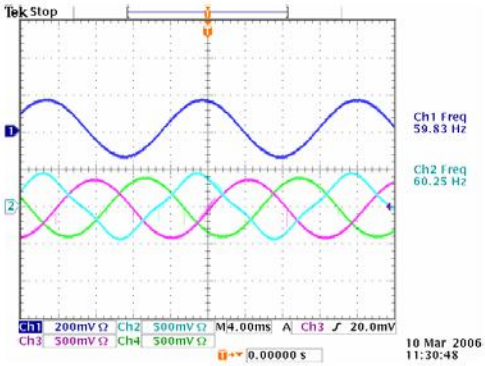

Fig. 10. 3-Φ PLL: three-phase balanced input at 60 Hz with 3rd harmonic added to phase *a*.

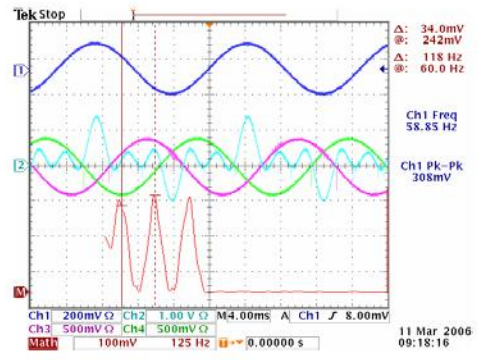

Fig. 11. 3-Φ PLL: three-phase balanced input at 60 Hz with DC-offset, 3rd, and 5th harmonics added to phase *a*.

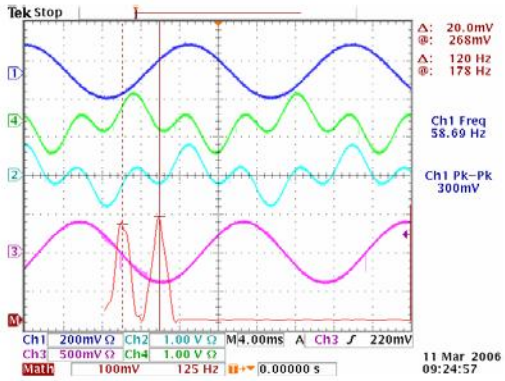

Fig. 12. 3-Φ PLL: three-phase balanced input at 60 Hz with 3rd harmonic added to phase *a* and *c*. Channel 2 and 4 are phases *a* and *c* respectively and channel 3 is phase *b*.

D. Unbalanced Three-Phase

Figs. 13 to 15 illustrate the implementation results for unbalanced three-phase inputs where phases a, *b* and *c* have phases 5°, 20°, and 48°, respectively rather than being 120° apart with respect to each other. Fig. 16 shows the condition where phase *b* and *c* are 48° apart instead of 120° and a minimum amplitude of 70 mV is maintained.

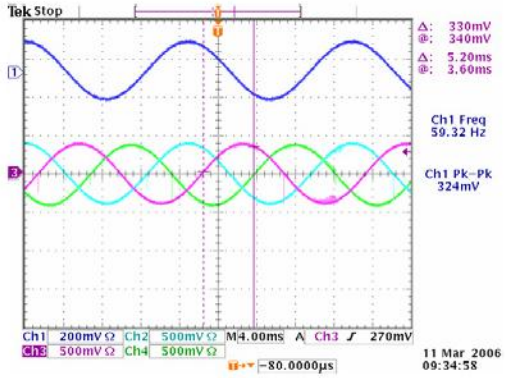

Fig. 13. 3-Φ PLL: three-phase unbalanced input at 60 Hz where phase *b* and *c* are 5° apart instead of 120°.

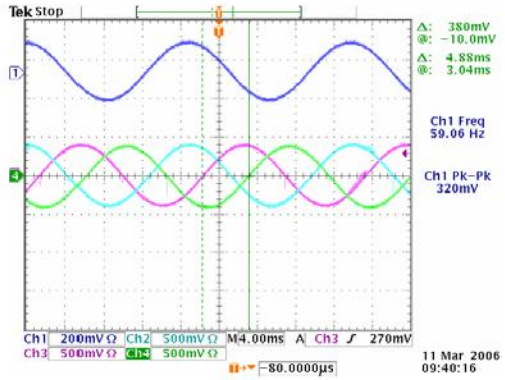

Fig. 14. 3-Φ PLL: three-phase unbalanced input at 60 Hz where phase *b* and *c* are 20° apart instead of 120°.

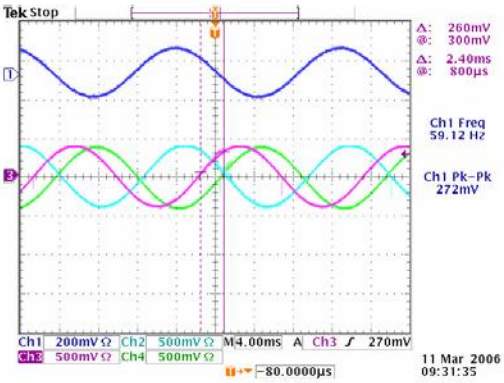

Fig. 15. 3-Φ PLL: three-phase unbalanced input at 60 Hz where phase *b* and *c* are 48° apart instead of 120°.

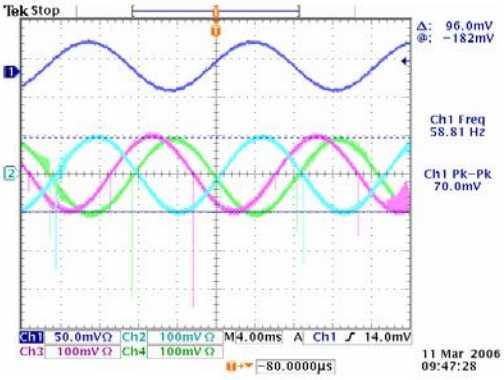

Fig. 16. 3-Φ PLL: three-phase unbalanced input at 60 Hz where phase *b* and *c* are 48° apart instead of 120° and a minimum amplitude is maintained at 70 mV.

E. Unbalanced Three-Phase Superimposed with Harmonics

The result for an unbalanced three-phase input is presented where an unbalance of 48° between phase *b* and *c* is maintained while harmonics are added. Fig. 17 shows a DC-offset and 3rd, and 5th harmonics superimposed on phase *a* and Fig. 18 illustrates a 3rd harmonic added to phases *a* and *b* while the unbalance is maintained. In these Figs. channel M shows the frequency domain for phase *a*.

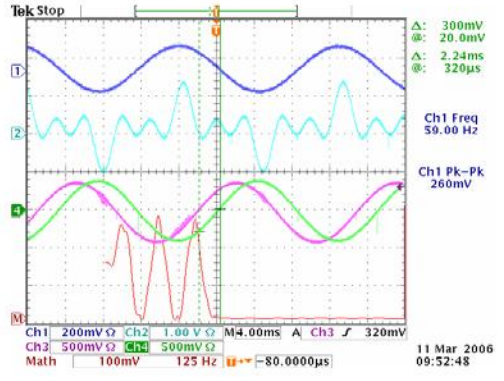

Fig. 17. 3-Φ PLL: three-phase unbalanced input at 60 Hz with DC-offset, 3rd, and 5th harmonics superimposed on phase *a* while an unbalance between phases *b* and *c* is maintained. Phases *b* and *c* are 48° apart instead of 120°. Channel M shows the frequency domain for phase *a*.

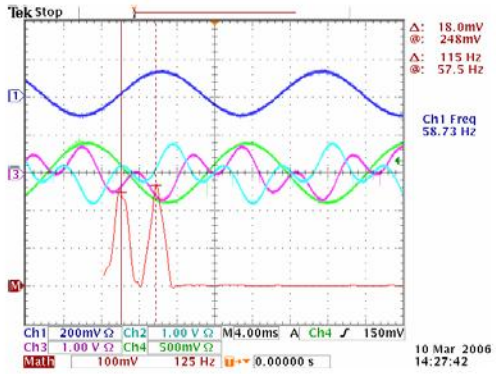

Fig. 18. 3-Φ PLL: three-phase unbalanced input at 60 Hz with 3rd harmonic added to phase *a* and *b* while an unbalance between phases *b* and *c* is maintained. Channel M shows the frequency domain for phase *a*.

F. Unbalanced Three-Phase with Harmonics at Different Frequencies

The results for unbalanced three-phase inputs superimposed with harmonics at different frequencies are provided in this section. The phase angle between phases *b* and *c* is 48°.

Fig. 19 shows the unbalanced case in presence of harmonic in phase *a*. Fig. 20 illustrates a 3rd harmonic added to phases *a* and *b* while the system imbalance is maintained. Fig. 21 shows the unbalanced case with DC-offset and a 3rd, and 5th harmonic superimposed on phase *a*.

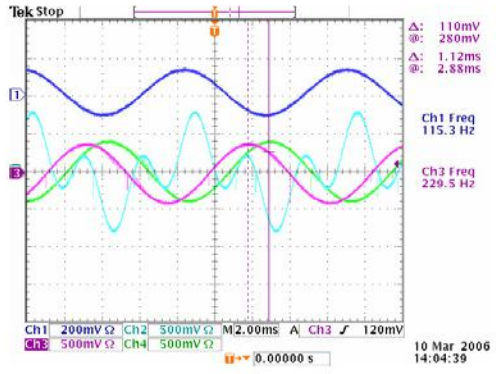

Fig. 19. 3-Φ PLL: three-phase unbalanced input at 115 Hz with 3rd harmonic added to phase *a*. Note: unbalance between phases *b* and *c*.

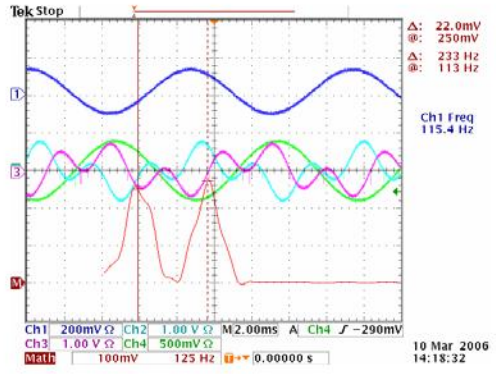

Fig. 20. 3-Φ PLL: three-phase unbalanced input at 115 Hz with 3rd harmonic added to phase *a* and *b*. Note: unbalance between phases *b* and *c*. Channel M shows the frequency domain for phase *a*.

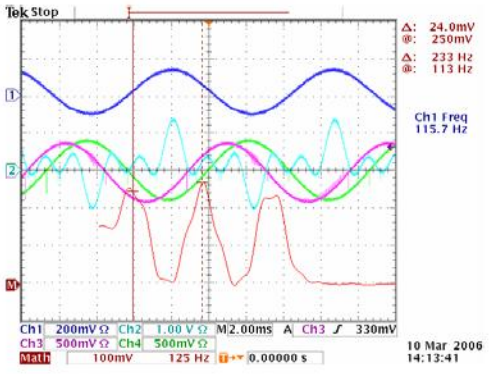

Fig. 21. 3-Φ PLL: three-phase unbalanced input at 115 Hz with DC-offset 3rd and 5th harmonics added to phase *a*. Note: unbalance between phases *b* and *c*. Channel M shows the frequency domain for phase *a*.

VI. CONCLUSIONS

The 3-Φ PLL presented combines a positive component detector and a predictive phase locked loop and is implemented on a FPGA platform. The implementation results indicate that the 3-Φ PLL can extract the real-time information from voltages/currents with a wide range of frequency and amplitude variations while providing a high level of immunity to harmonics/inter-harmonics.

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VIII. BIOGRAPHY

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