Virtual Memory: *Address translation 3: Multilevel Page Tables*

Multi-Level Page Tables

Suppose:

4KB (2¹²) page size, 48-bit address space, 8-byte PTE

Problem:

- Would need a 512 GB page table!
 - $2^{48} * 2^{-12} * 2^3 = 2^{39}$ bytes

Multi-Level Page Tables

Suppose:

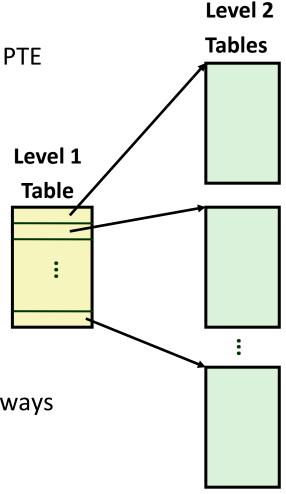
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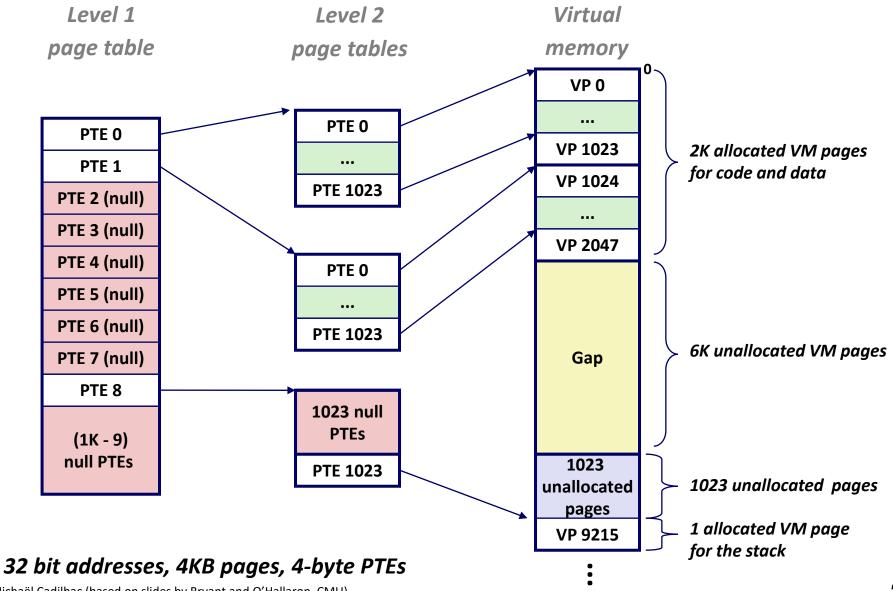
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- Example: 2-level page table
 - Level 1 table: each PTE points to a page table (always memory resident)
 - Level 2 table: each PTE points to a page (paged in and out like any other data)

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A Two-Level Page Table Hierarchy



Translating with a k-level Page Table

