

Revision	Date	Author	Comments
1A	2020-09-14	Tim S. timothystotts08@gmail.com	First publishable draft of the HYGRO Sensor Readings Tester-Zynq
2A	2020-09-14	Tim S. timothystotts08@gmail.com	Clerical update to document
1B	2020-12-10	Tim S. timothystotts08@gmail.com	Descriptions were updated from Vivado/SDK 2019.1 to Vivado/Vitis 2020.2 to match project sources update.

<https://github.com/timothystotts/fpga-iic-hygro-tester-1>

Copyright 2020 Timothy Stotts

MIT License

HYGRO Sensor Readings-Zynq-Tester Experiment

HYGRO Sensor Readings-Zynq-Tester Experiment: Folder Structure

HYGRO Sensor Readings equivalent function of polling a HDC1080 sensor via IIC bus; displaying reading in multiple formats on a 16x2 character LCD; and displaying sensor reading display selection on a two-digit seven-segment display.

Project Folder	Project Description
HYGRO-Tester-Design-Zynq (Vivado 2020.2 and Vitis 2020.2)	A utility designed for polling a temperature and relative humidity sensor once per second and displaying the readings in Celsius, Fahrenheit, and RH Percent. The design is completely in Zynq-7000 AXI subsystem with standard Xilinx IP Integrator components, vendor Xilinx IP Integrator components, and Standalone C language program executing on the first ARM A9 soft processor.

To successfully open the project, it is necessary to add the directory zybo-z7-20 from the directory board_files/ to the installation directory of Vivado 2020.2 but not to the installation directory of Vitis 2020.2. For example:

```
$ which vivado
/opt/Xilinx/Vivado/2020.2/bin/vivado
$ cd ./board_files
$ sudo cp -R ./zybo-z7-20 /opt/Xilinx/Vivado/2020.2/data/boards/board_files/
# (do not copy the board_files to
# /opt/Xilinx/Vitis/2020.2/data/boards/board_files/)
```

Note that the Digilent Guide at <https://reference.digilentinc.com/vivado/installing-vivado/v2019.2> indicates to install the board files by copying to the install directory of the tool, so that the board files are always found.

HYGRO Sensor Readings-Zynq-Tester Experiment: Methods of Operation

The purpose of the design is to boot a Digilent Inc. Zybo-Z7-20 (Zynq-7000) development board with Pmod CLS, Pmod HYGRO, and Pmod SSD peripheral boards, which are a 16x2 Character dot-matrix LCD display, a IIC bus temperature and relative humidity sensor, and a two-digit seven-segment display, respectively. The PMOD CLS connects to the FPGA with its own dedicated SPI bus via a higher-speed plug and jack. The Pmod SSD connects to board Pmod port JE. The Pmod CLS connects to board Pmod port JB. The Pmod HYGRO connects to board Pmod port JC. The use of an extension cable makes the Pmod CLS able to connect to only one 2x6 Pmod port, and a

second extension cable makes the Pmod SSD able to connect to only one 2x6 Pmod port. See Figure 1: Zybo-Z7-20 Assembled with Pmod CLS, Pmod HYGRO, Pmod SSD.

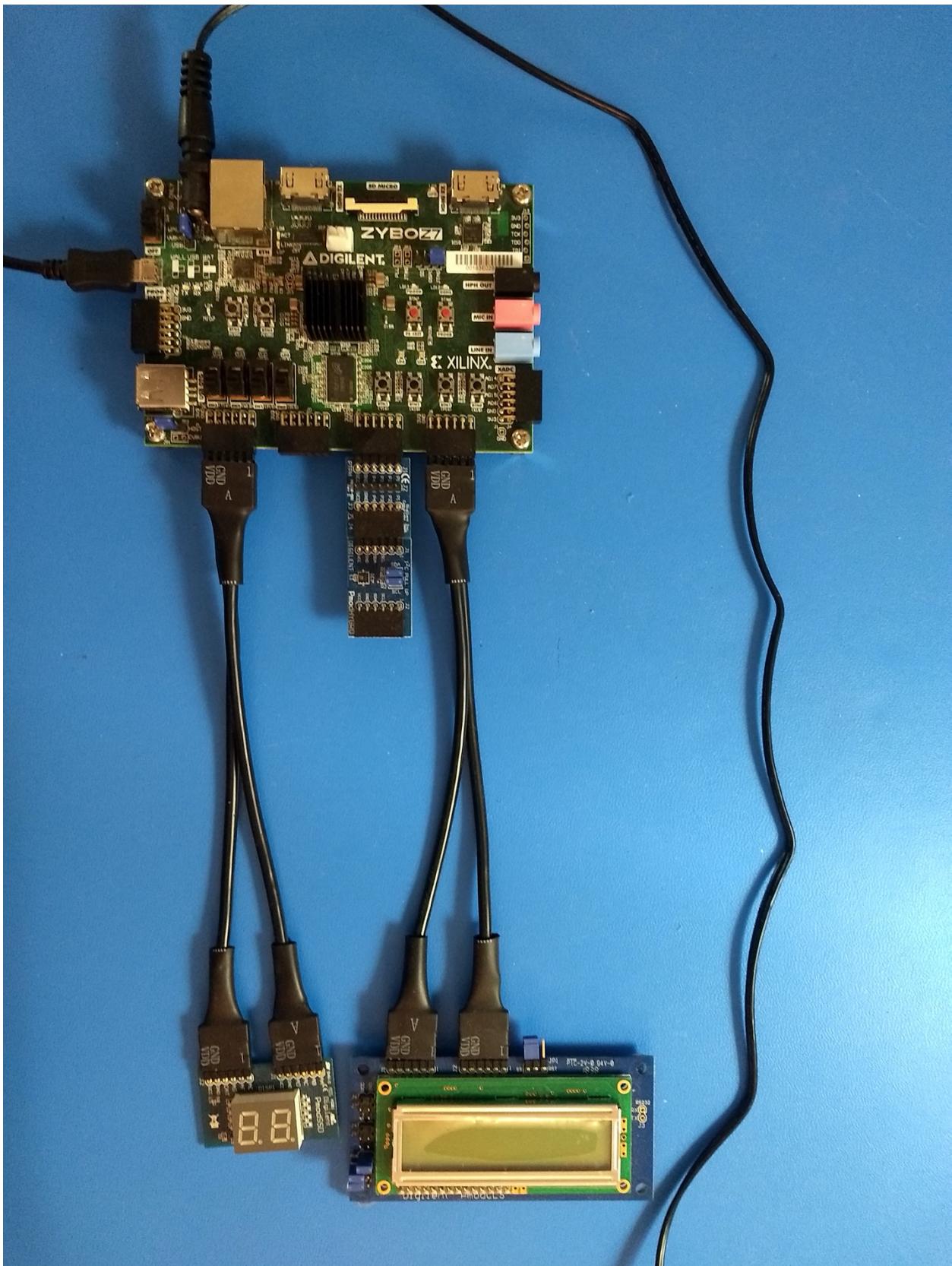


Figure 1: Zybo-Z7-20 Assembled with Pmod CLS, Pmod HYGRO, Pmod SSD

HYGRO Sensor Readings-Zynq-Tester Experiment: Method of Operation: iterative poll of sensor readings and display on LCD

HYGRO Sensor Readings-Zynq-Tester Experiment: Design Operation

By design, the four switches are processed as mutually exclusive inputs, as are the four buttons. To operate the design, the LCD displays an instruction to the operator to put Switch Zero in the ON position. After that, the LCD displays an instruction to the operator to momentarily push one of the four buttons.

While Switch Zero is in the ON position, the design polls the Pmod HYGRO HDC1080 sensor approximately once per second. Each time a button is depressed and then released while switch zero is positioned as ON, one of five selectable ASCII display formats is selected, and the incoming Pmod HYGRO sensor readings are converted to human readable content which in turn is displayed on the Pmod CLS LCD display. Pressing a different button (or the same button if button zero) changes the text and/or number format units on the LCD display.

Note that in this design, drivers downloaded from Digilent Inc. for the Pmod HYGRO and Pmod CLS are used in the block design with some minimal modification and update to target the Zybo-Z7-20 board instead of the original Arty board, as well as configure the IIC bus driver IP for the AXI speed of 50 MHz. The Zynq IPI-BD implementation integrates vendor components plus one custom driver. The SDK project incorporates the drivers provided by each IP module; and additional C code provides a working main program.

HYGRO Sensor Readings-Zynq-Tester Experiment: Design Theory

Note that in the IPI-BD Design, drivers downloaded from Digilent Inc. for the Pmod SF3 and Pmod CLS are used in the block design with some minimal modification to target the Zybo-Z7-20. Both drivers target the Zybo-Z7 instead of the Arty. The Git repository contains a submodule that pulls from a branch of the author's fork of the Digilent Vivado-library repository on GitHub.

Additionally, a custom IP module, MuxSSD, is found under the folder local_ip. This module enables the addition of the Pmod SSD on extension cable to be operated from a single Pmod port. Pmod port JE was selected as this is the only non-high-speed EMIO port on the board—that is, both low speed and controlled by the FPGA; not high speed or controlled by the ARM processor GPIO.

HYGRO Sensor Readings-Zynq-Tester Experiment: 3rd-party references:

Digilent Inc. References

Zybo Z7 Reference Manual

<https://reference.digilentinc.com/reference/programmable-logic/zybo-z7/reference-manual>

Vivado Board Files

<https://github.com/digilent/vivado-boards>

Master XDC files for all Digilent Inc. boards, including Zybo-Z7-20

<https://github.com/Digilent/digilent-xdc>

Digilent Inc IP library for Xilinx Vivado

<https://github.com/Digilent/vivado-library/>

Textbook References

Use of IP Integrator to create the Zynq-7000 diagram and synthesis:

- Tutorials followed from text to understand IPI block design,

L. H. Crockett, R. A Elliot, M. A. Enderwitz, and R. W. Stewart, *The Zynq Book: Embedded Processing with the ARM Cortex-A9 on the Xilinx Zynq-7000 All Programmable SoC*, First Edition, Strathclyde Academic Media, 2014.