

FPGA Serial Accelerometer Tester, Version 1

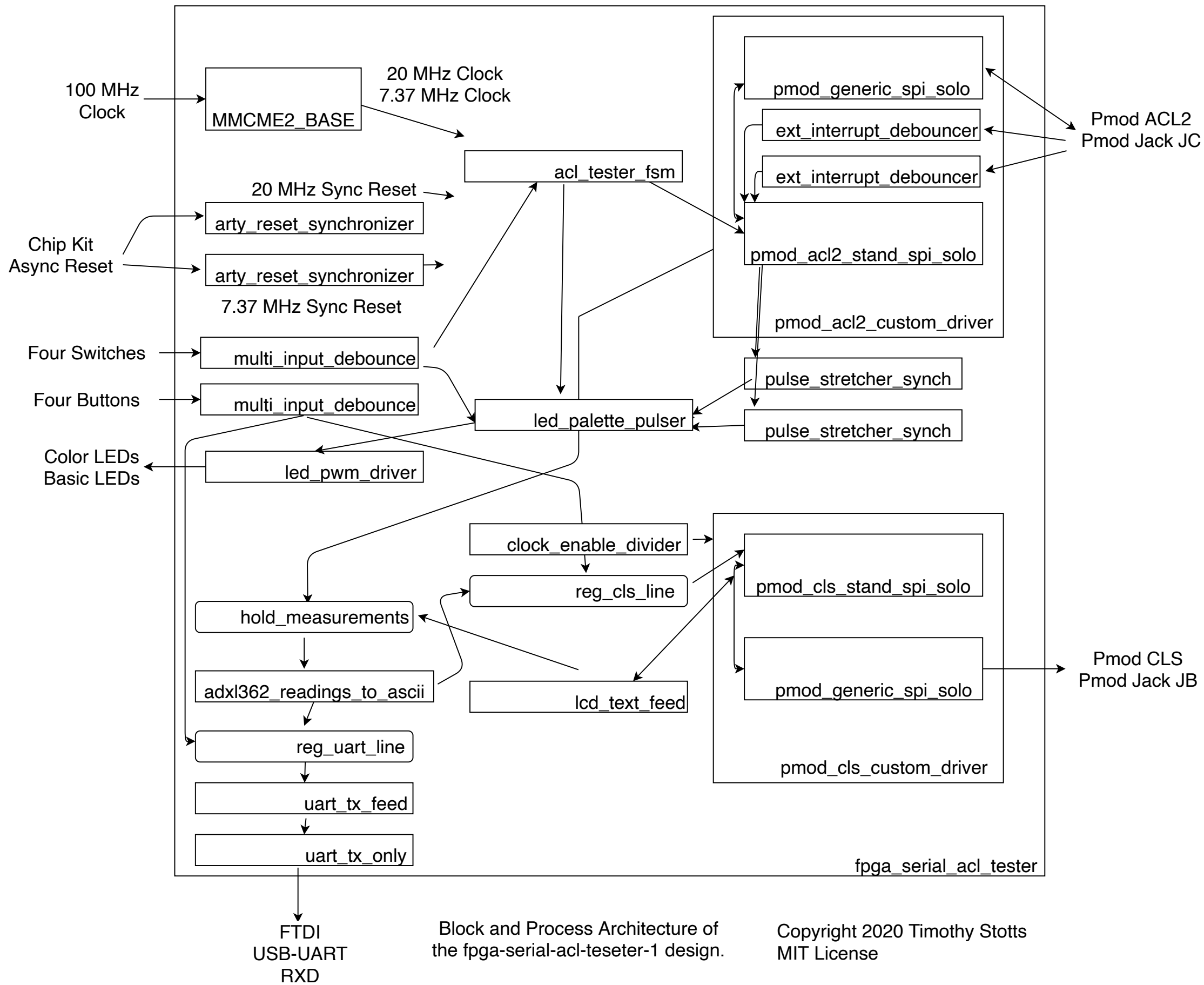
by Timothy Stotts

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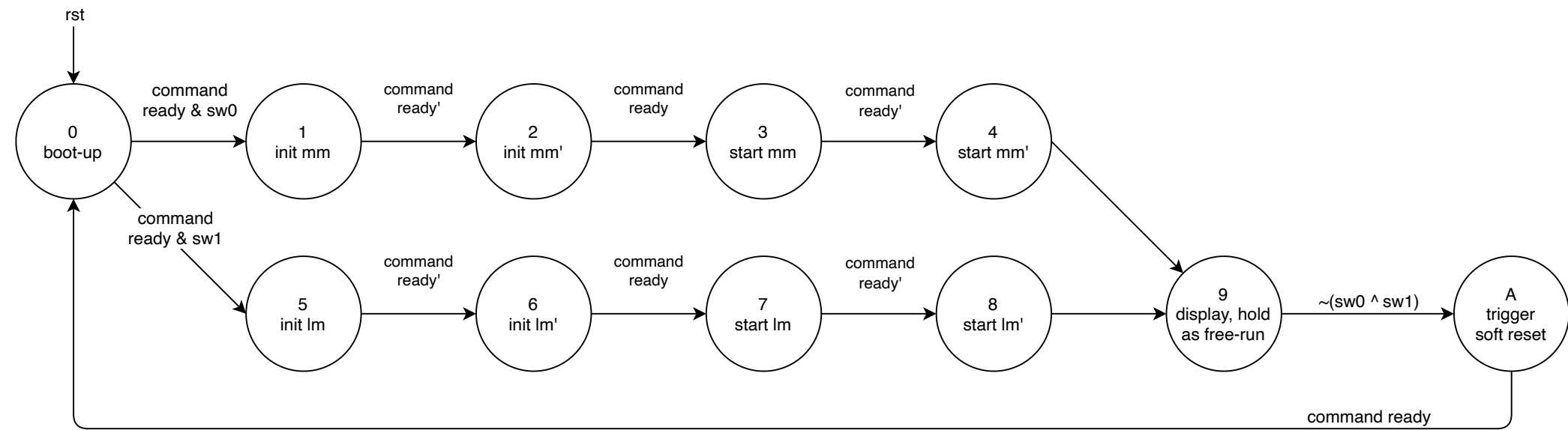
Hosted at:

<https://github.com/timothystotts/fpga-serial-acl-tester-1>

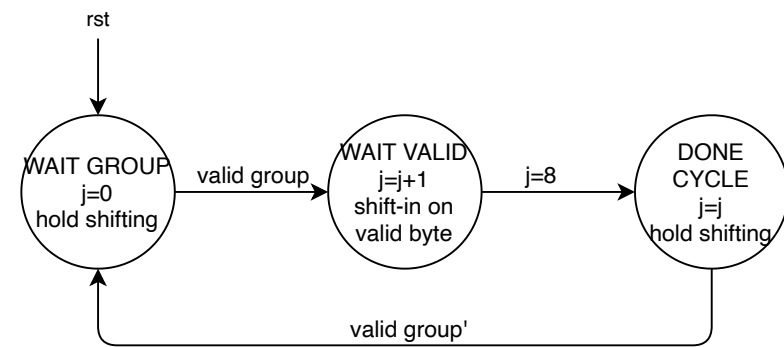
ACL-Tester-Design-Diagrams document revision 10A



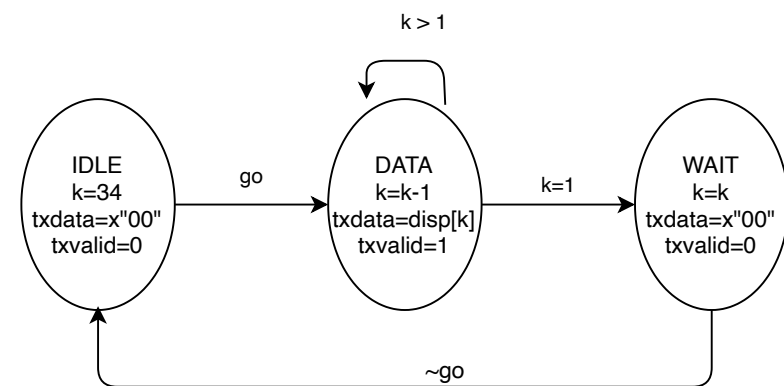




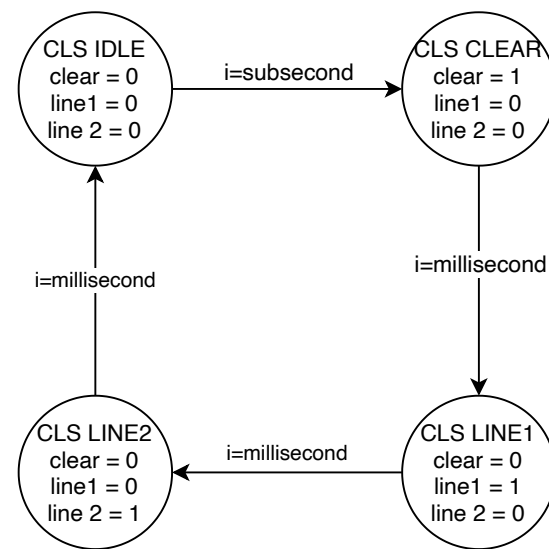
Tester FSM for operating the PMOD ACL2 driver commands.



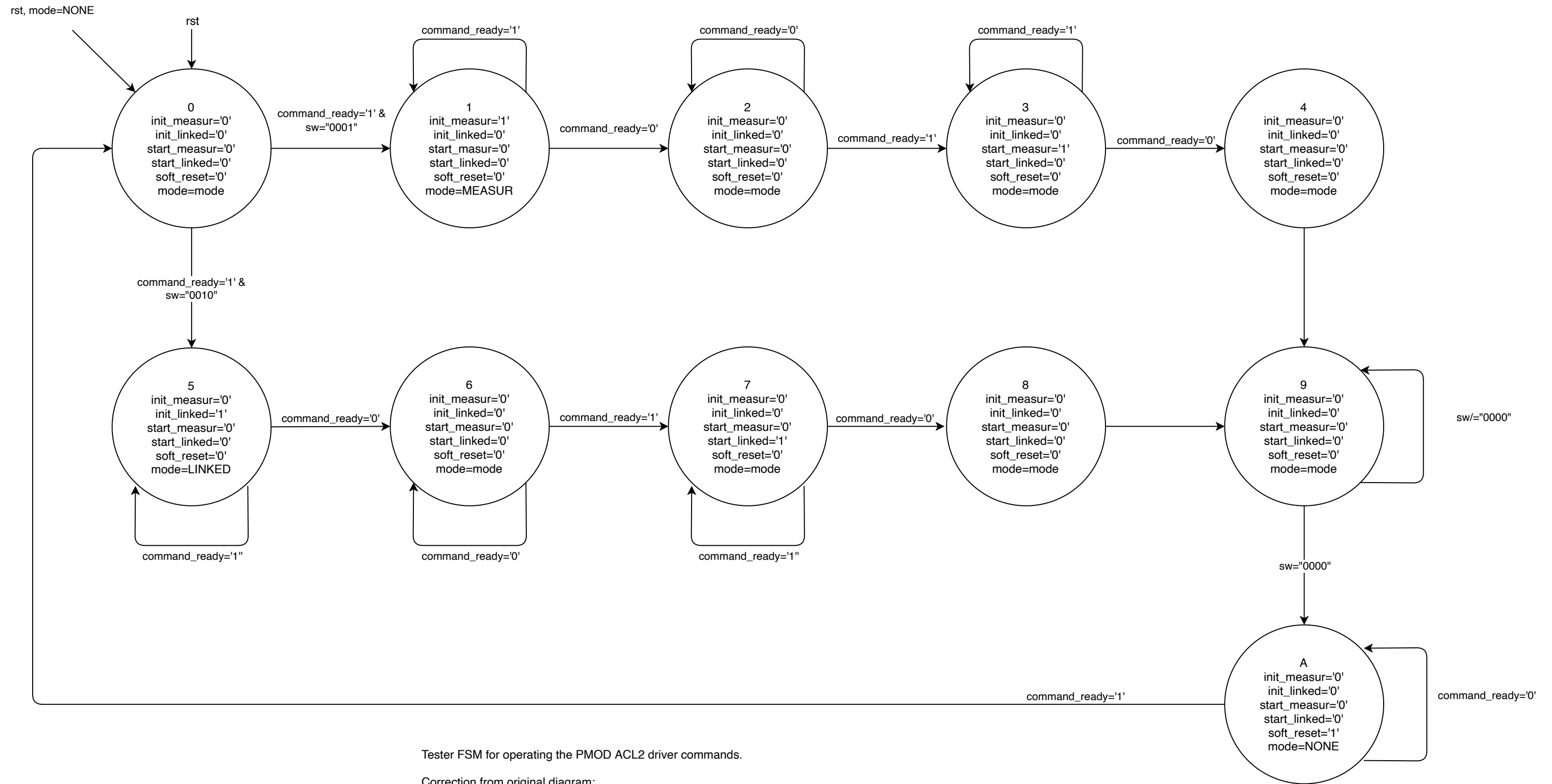
Tester FSM to receive the streamed measurements and shift them into a bit vector.



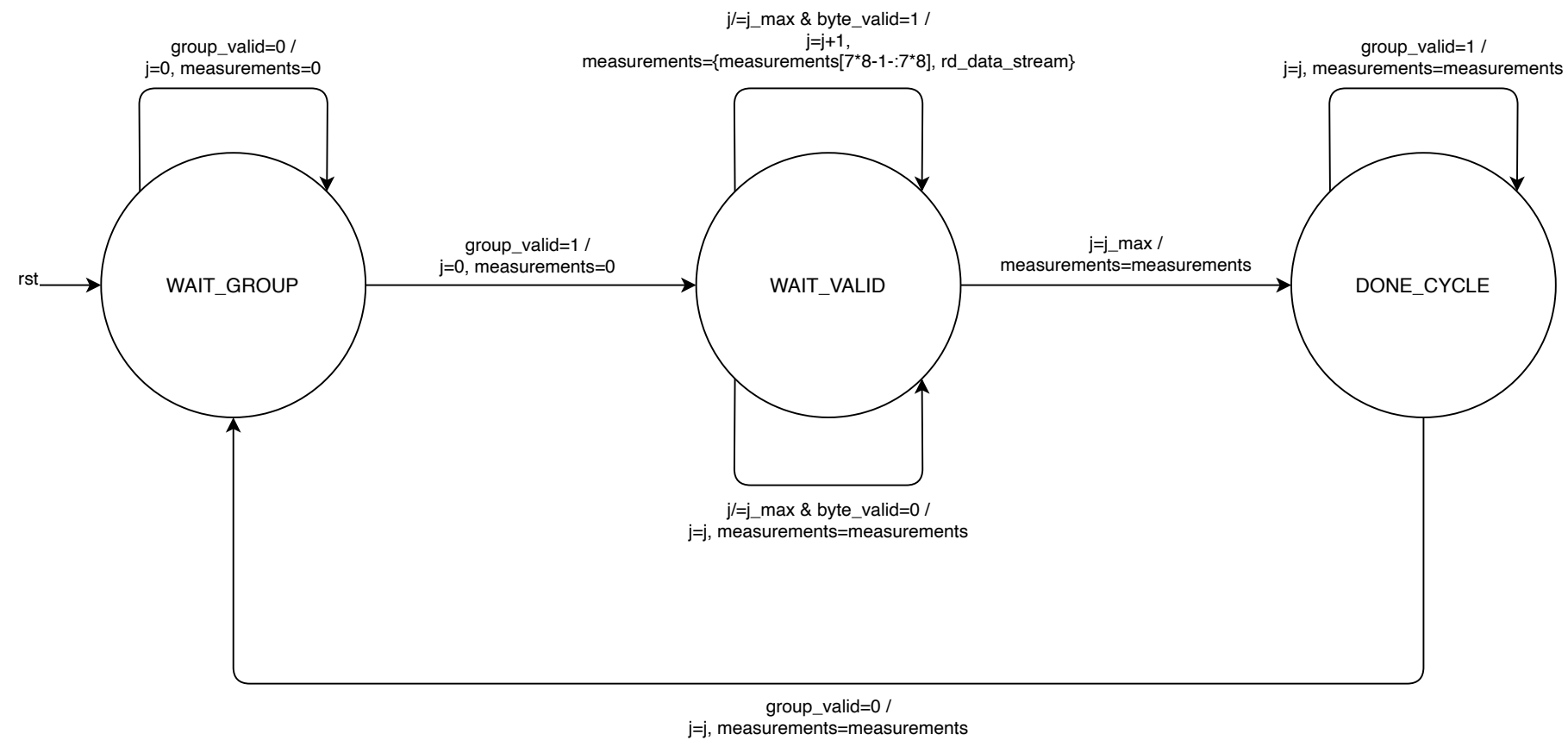
Tester FSM to load the TX ONLY UART with a 32 character text line, plus carriage return and new line.



Tester FSM for updating the PMOD CLS display.

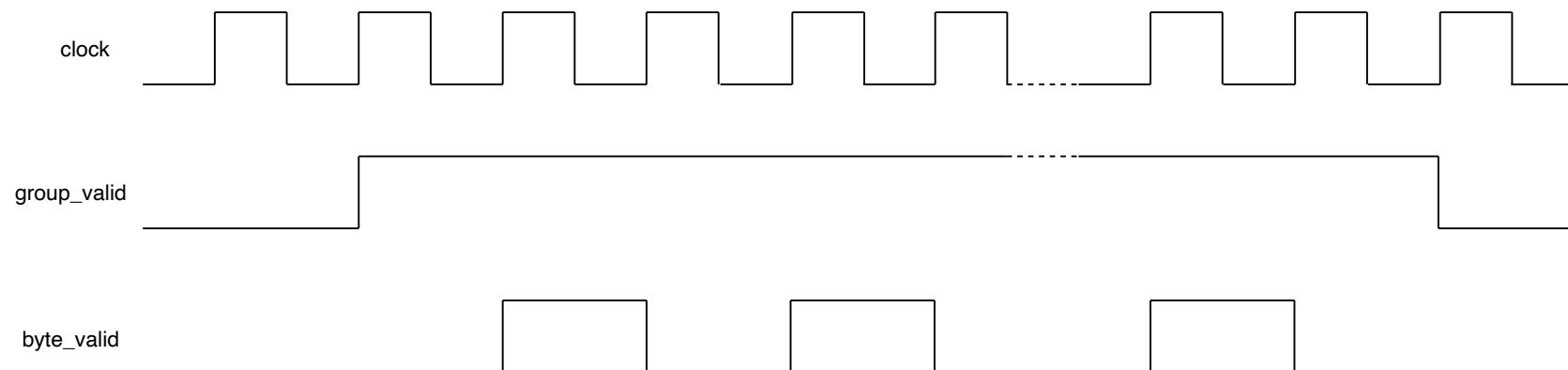


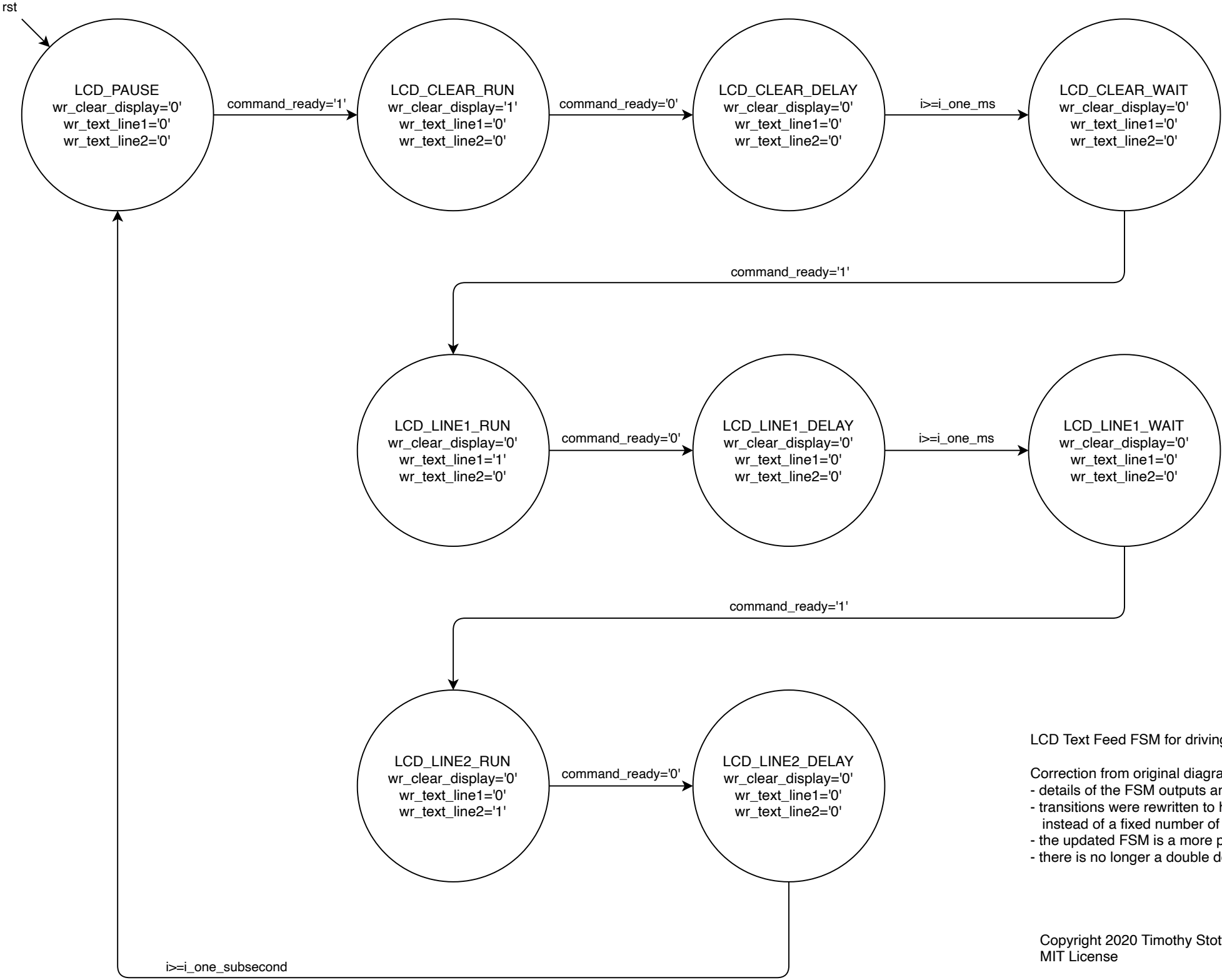
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Stream FSM for capturing RX FIFO output from the ACL2 Custom Driver.  
 A group\_valid input signal is held high to indicate a set of measurement values.  
 A byte\_valid input signal is pulsed for each new byte to shift into the measurement register.

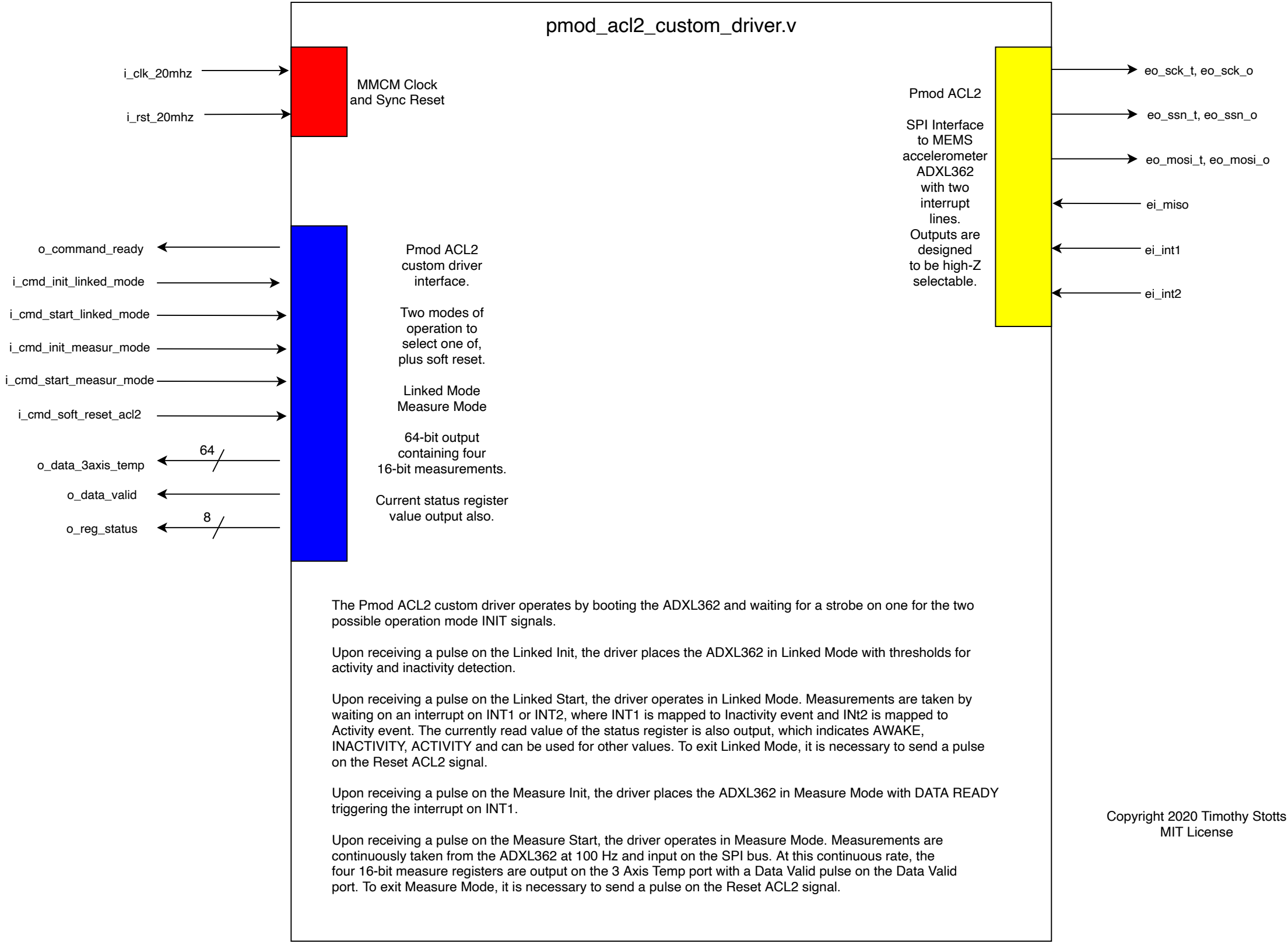
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LCD Text Feed FSM for driving the commands of the custom Pmod CLS driver.

Correction from original diagram:  
- details of the FSM outputs and timer "i"  
- transitions were rewritten to hold commands according to `command_ready` handshake instead of a fixed number of clock cycles during a state  
- the updated FSM is a more proper FSM diagram design  
- there is no longer a double delay between the end of Line 2 and the start of Clear.

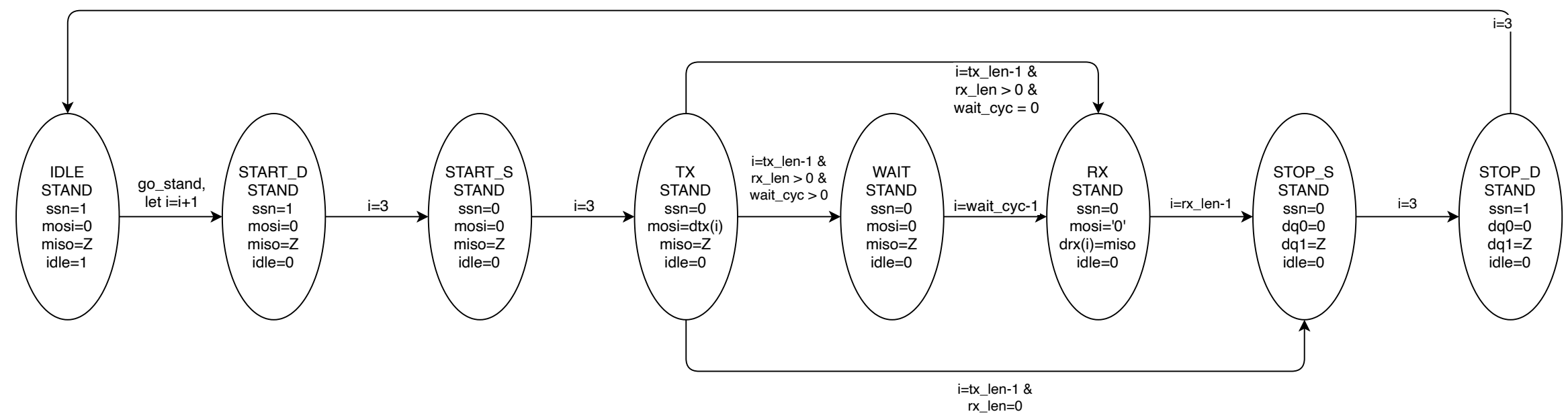






Operational driver for the Digilent PMOD ACL2, that drives the Standard SPI FSM. This diagram is incomplete and does not show Soft Reset operation, or boot-time delay. Also, not all state-bypass preventions and not all iterations are show.

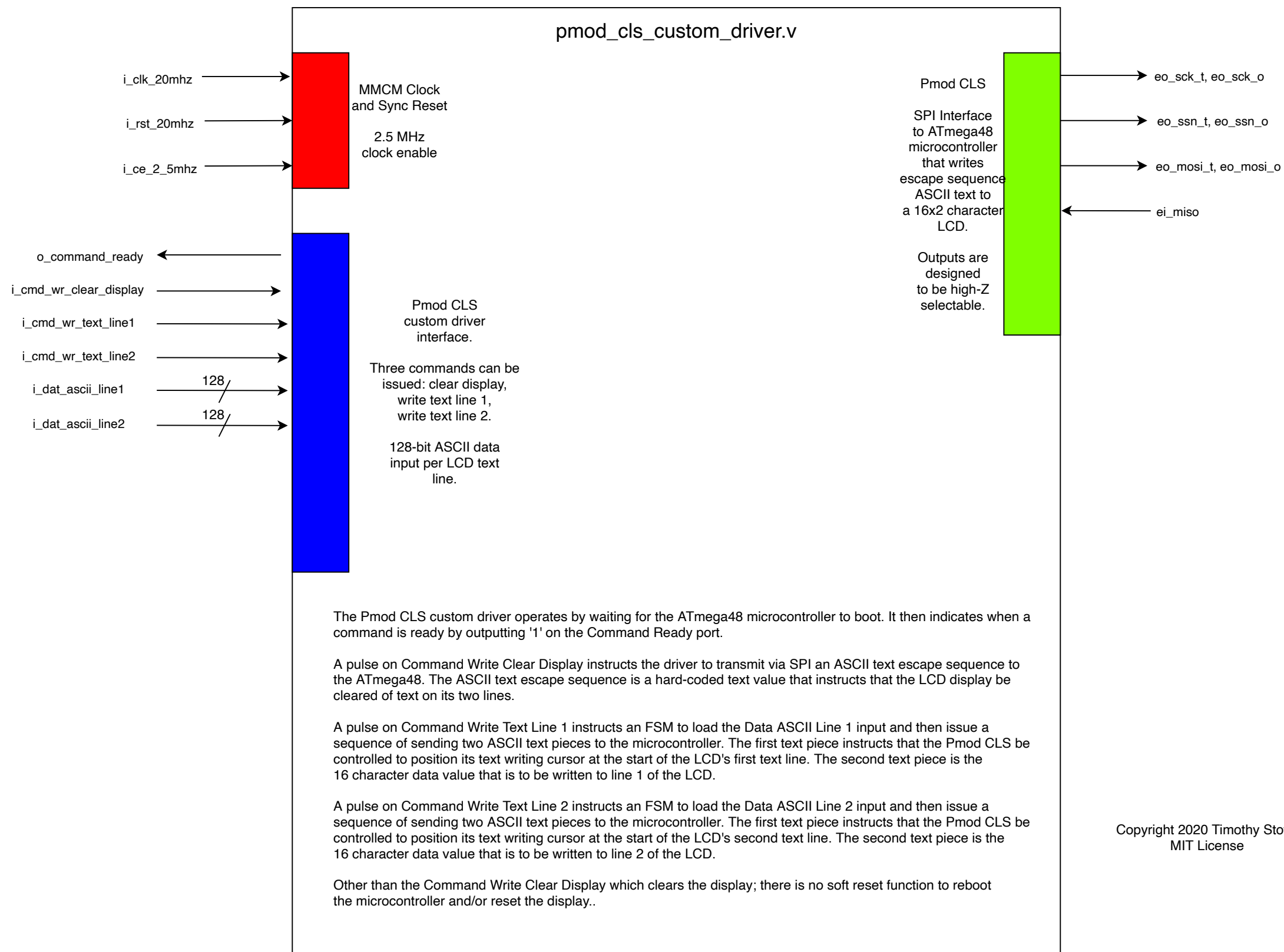
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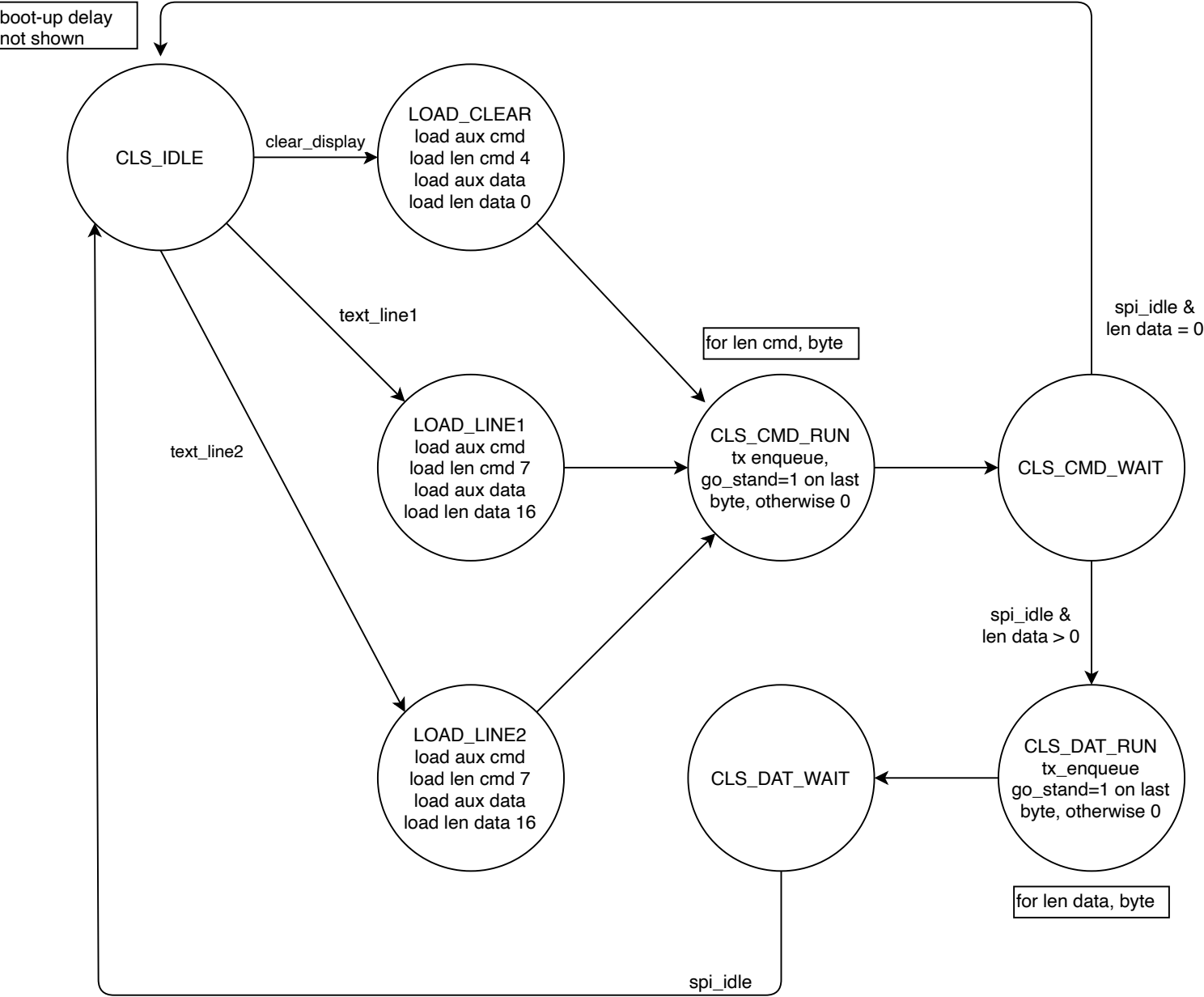


In each transition, tx\_len and rx\_len are to be multiplied by 8 from the FSM input signals, as it only makes sense to input into the FSM a byte count, while the FSM requires transitioning based upon a bit count.

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Generic SPI FSM, with only one SPI slave on the bus.

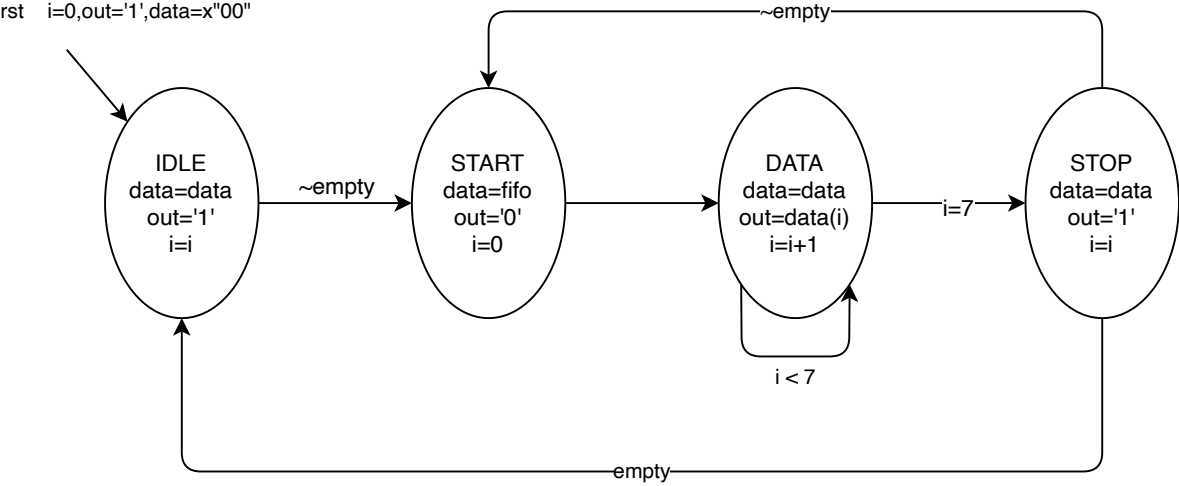




A FSM to operate the Digilent Inc. PMOD CLS LCD display communication via the single slave SPI-machine FSM of this document.

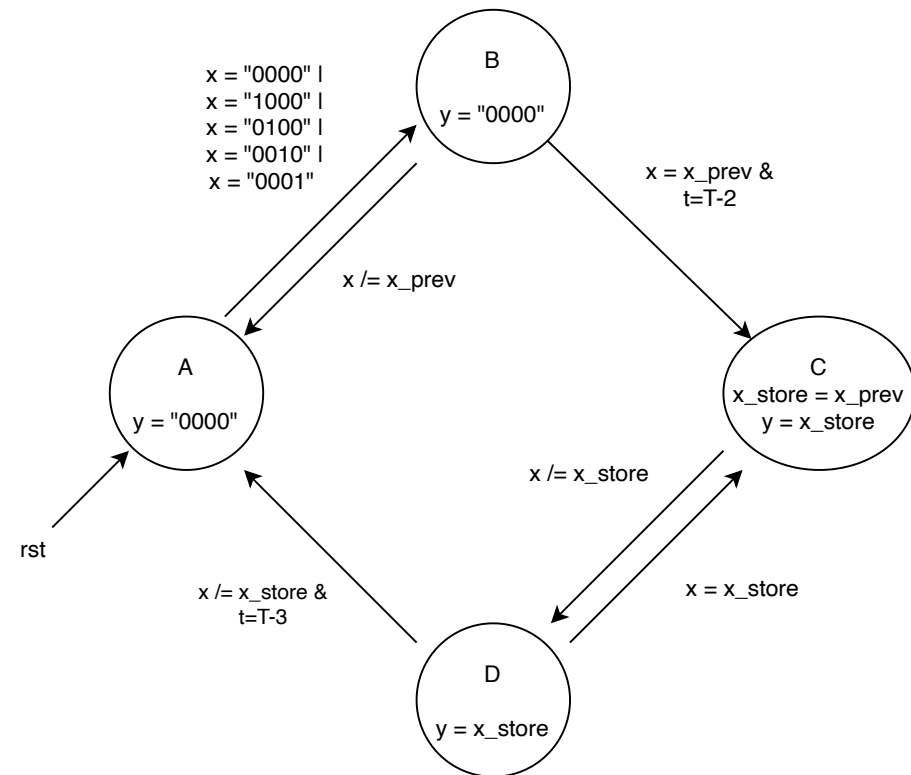
This diagram is incomplete and does not show boot-time delay. Also, some state-bypass preventions and iterations may not be shown.

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A TX ONLY UART output to UART chip from the FPGA, with the FSM executing at BAUD rate as its clock enable.

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Full 4-button combined debouncer.

x is defined as a four-bit value.

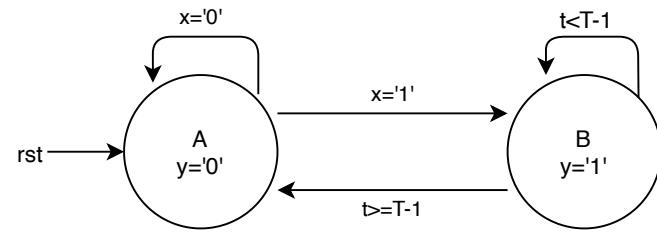
x\_prev is defined as a four-bit value that holds the previous clock cycle value of x.

x\_store is defined as a four-bit value that holds the value of x and updates the debouncer FSM entered state C during the transition BC..

The registers x\_prev and x\_store could be combined into one register, with its capture of X being a clock-enable during transitions and states of a more complex diagram.

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Moore FSM for a synchronous pulse stretcher of signal X that lasts for a duration less than T, with Y lasting exactly T cycles.

Textbook Figure 8.28. quoted from:

*Finite State Machines in Hardware: Theory and Design (with VHDL and SystemVerilog)*  
 by Volnei A. Pedroni,  
 reprinted courtesy of The MIT Press