Revision	Date	Author	Comments
1A	2020-06-22	Tim S. timothystotts08@gmail.com	First publishable draft of the serial accelerometer readings tester

Serial ACL Readings-Tester Experiment

Serial ACL Readings-Tester Experiment: Folder Structure

ACL Readings designs with equivalent function of performing a three-axis reading and displaying them on an LCD and USB terminal.

Project Folder	Project Description
ACL-Tester-Design-Single-Clock-Verilog (Vivado 2019.1)	A utility designed for a custom operation of a serial accelerometer and displaying milli-g-force readings on both an LCD and a serial terminal. The design is completely in Verilog RTL and visual VHDL test-bench without a soft processor. Multiple clock domains exist; and each 7 MHz or faster domain is controlled by a MMCM, and each slower domain is controlled by a clock enable divider RTL dividing a MMCM clock by clock enable pulse instead of clock division. Clock dividers are only used for the generation of an output clock that outputs at a bus port on the FPGA.
ACL-Tester-Design-AXI (Vivado 2019.1 and SDK 2019.1)	A utility designed for custom operation of a serial accelerometer and displaying milli-g-force readings on both an LCD and a serial terminal. The design is completely in Microblaze AXI subsystem with standard Xilinx IP Integrator components plus Digilent Inc. User IP, and C language program executing on the Microblaze soft processor.

For the ACL-Tester-Design-AXI project, the BSP of the bootloader and the BSP of the application require that the flash family parameter be set in the xilisf configuration on the BSP configure page. The default value is 1, but must be changed to 5 as the Arty-A7-100T board has a Spansion 128Mbit serial flash for booting the FPGA.

To successfully open the project, it is necessary to add the directory arty-a7-100 or arty-a7-35 from the directory board_files/ to the installation directory of Vivado 2019.1 and SDK 2019.1. For example:

$ which vivado
/opt/Xilinx/Vivado/2019.1/bin/vivado
$ cd ./board_files
$ sudo cp -R ./arty-a7-100 ./arty-a7-35 /opt/Xilinx/Vivado/2019.1/data/boards/board_files/
$ sudo cp -R ./arty-a7-100 ./arty-a7-35 /opt/Xilinx/SDK/2019.1/data/boards/board_files/

Note that the Digilent Guide at https://reference.digilentinc.com/vivado/installing-vivado/2018.2 indicates that an initialization script can be executed in the user's profile to set up a path to additional board files. It is the experience of this author that the TCL initialization script provides an intermittent or non-functional detection of the board files in the user's home folder. By copying to the install directory of the tool, the board files are always found. Otherwise, the following TCL command is supposed to instruct Vivado to locate the board files:

```
set_param board.repoPaths [list "<extracted path>/Vivado/board_files"]
```

Serial ACL Readings-Tester Experiment: Methods of Operation

The purpose of the design is to boot a Digilent Inc. Arty-A7-100T (Artix-7) development board with PMOD CLS and PMOD SF3 peripheral boards, which are a 16x2 Character dot-matrix LCD display, and a 256 Mbit serial flash, respectively. Each PMOD connects to the FPGA with its own dedicated SPI bus via a moderately high-speed plug and jack. The PMOD CLS connects to board PMOD port JB. The PMOD SF3 connects to board PMOD port JC.

Serial ACL Readings-Tester Experiment: Method of Operation: streaming three-axis readings and displaying them, with alternate mode of activity detection

Serial ACL Readings-Tester Experiment: Design Theory

In the both implementations (AXI and Verilog), the two switches sw0, sw1, are debounced and processed as mutually exclusive inputs. When switch 0 is exclusively selected to the ON position, the Tester design controls the PMOD ACL2 to stream three-axis and compensating temperature readings at a rate of 100 Hz, and display readings at a rate of under 5 Hz. When switch 1 is exclusively selected to the ON position, the Tester design controls the PMOD ACL2 to detect motion activity and inactivity by thresholds. Each time there is an activity event, LD3 is lit green instead of red momentarily and a single reading from the PMOD ACL is displayed. Each time there is an inactivity event, LD4 is lit green instead of red momentarily and a single reading from the PMOD ACL is displayed.

Conceptual-only FSM diagrams are also included in the PDF document `ACL-Design-Documents/ACL-Tester-Design-Diagrams.pdf`.

Note that in the AXI Design, drivers downloaded from Digilent Inc. for the PMOD SF3 and PMOD CLS are used in the block design with some minimal modification to target the Arty-A7-100T. The AXI example demonstrates integration of vendor components plus adding additional C code.

Serial ACL Readings-Tester Experiment: 3rd-party references:

How To Store Your SDK Project in SPI Flash
https://reference.digilentinc.com/learn/programmable-logic/tutorials/htsspisf/start

Master XDC files for all Digilent Inc. boards, including Arty-A7-100T
https://github.com/Digilent/digilent-xdc

Digilent Inc IP library for Xilinx Vivado
https://github.com/Digilent/vivado-library/