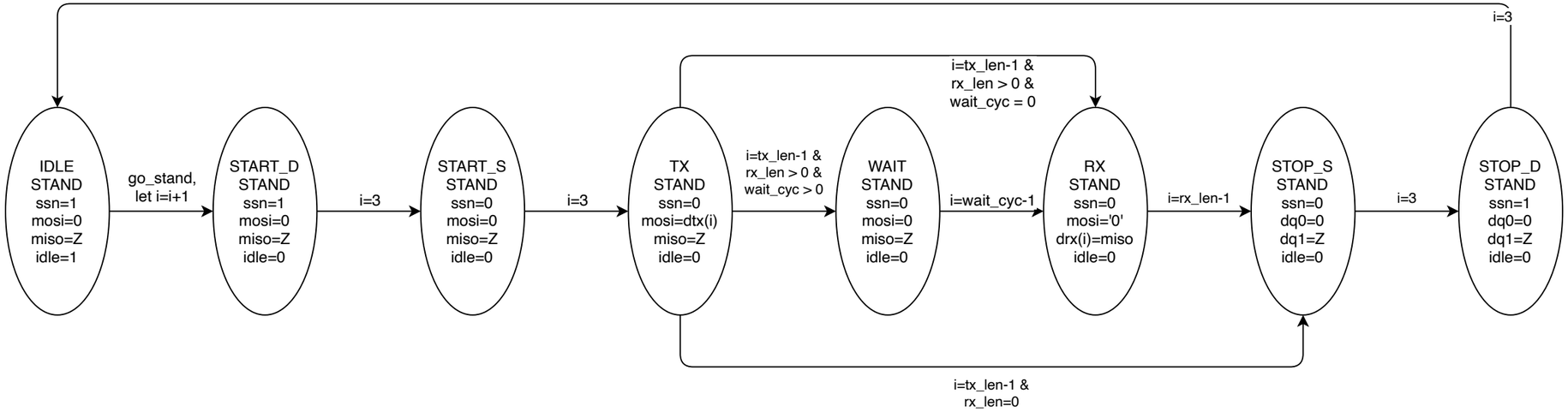
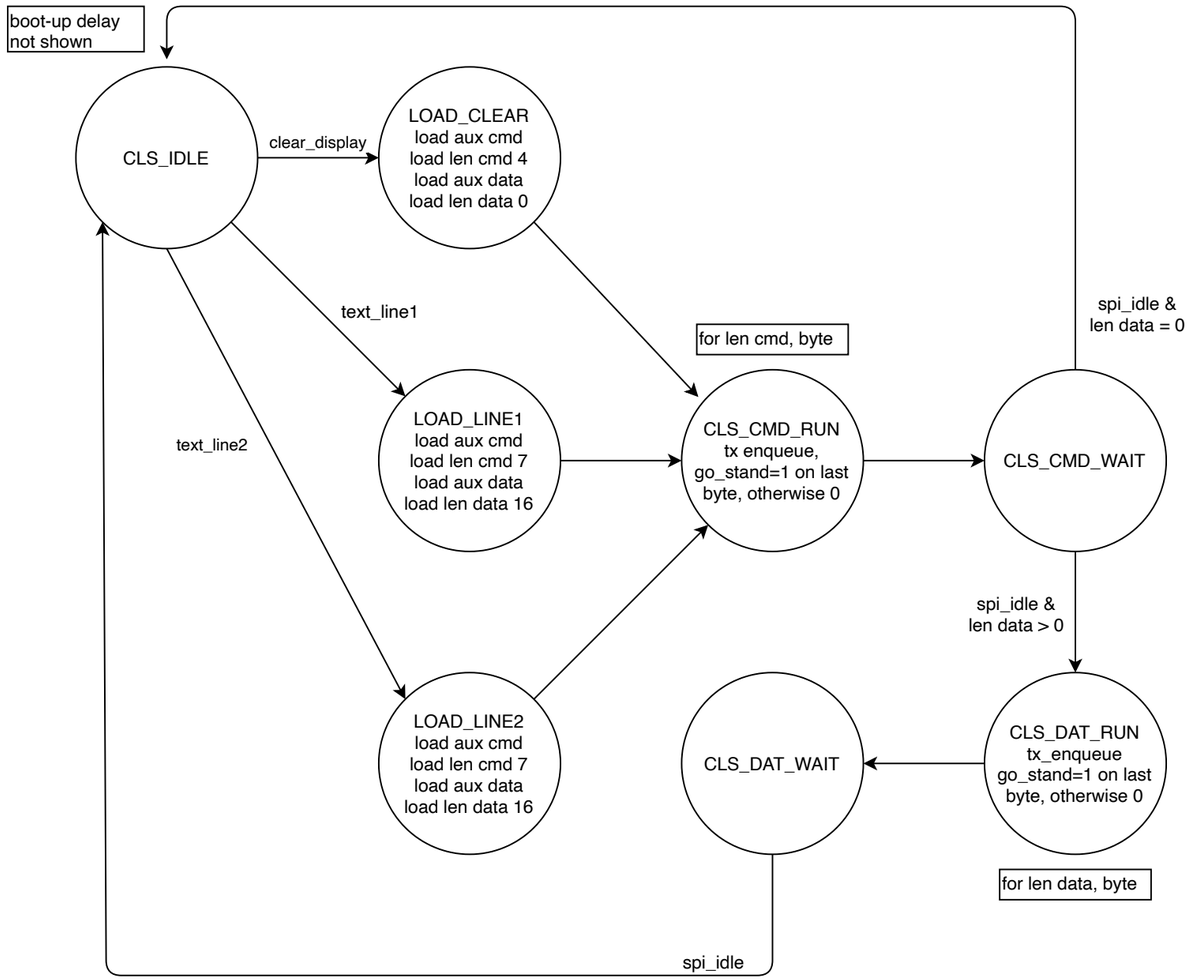
Operational driver for the Digilent PMOD ACL2, that drives the Standard SPI FSM. This diagram is incomplete and does not show Soft Reset operation, or boot-time delay. Also, not all state-bypass preventions and not all iterations are show.

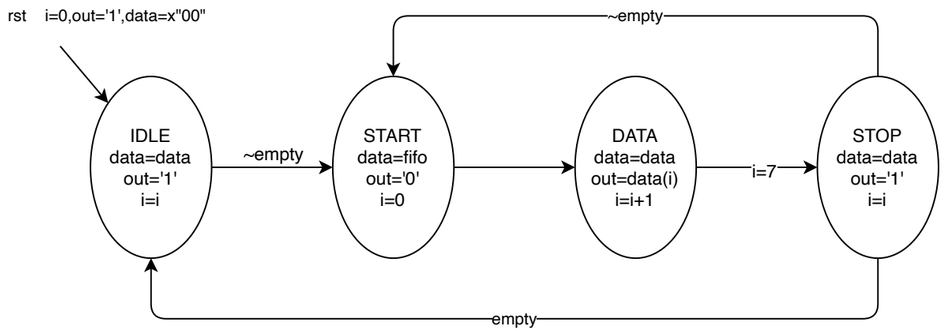


In each transition, tx_len and rx_len are to be multiplied by 8 from the FSM input signals, as it only makes sense to input into the FSM a byte count, while the FSM requires transitioning based upon a bit count.

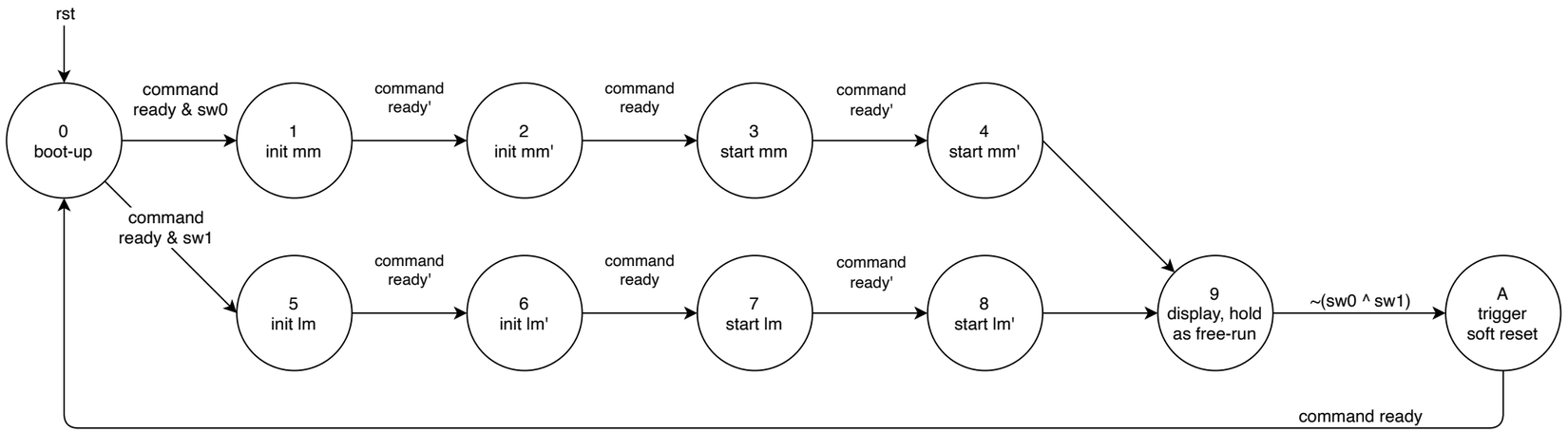
Generic SPI FSM, with only one SPI slave on the bus.



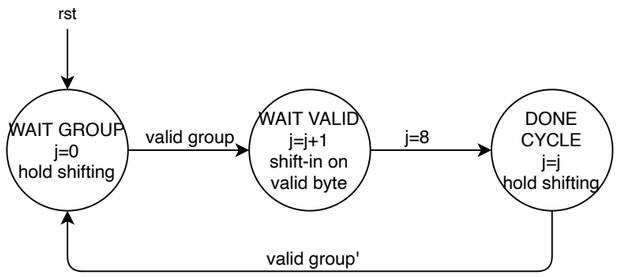
A FSM to operate the Digilent Inc. PMOD CLS LCD display communication via the single slave SPI-machine FSM of this document.



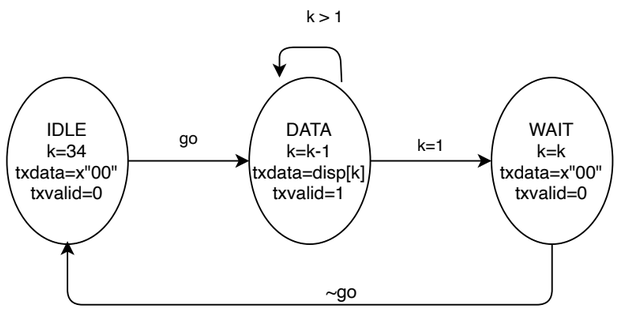
A TX ONLY UART output to UART chip from the FPGA, with the FSM executing at BAUD rate as its clock enable.



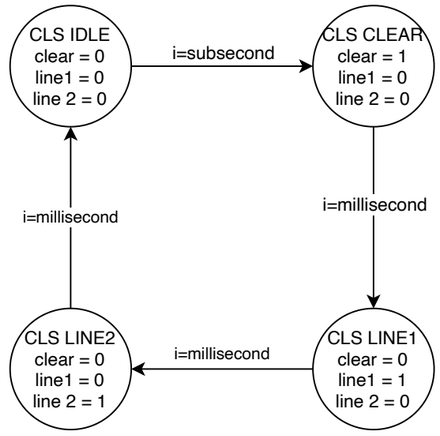
Tester FSM for operating the PMOD ACL2 driver commands.



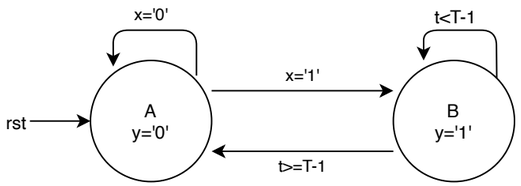
Tester FSM to receive the streamed measurements and shift them into a bit vector.



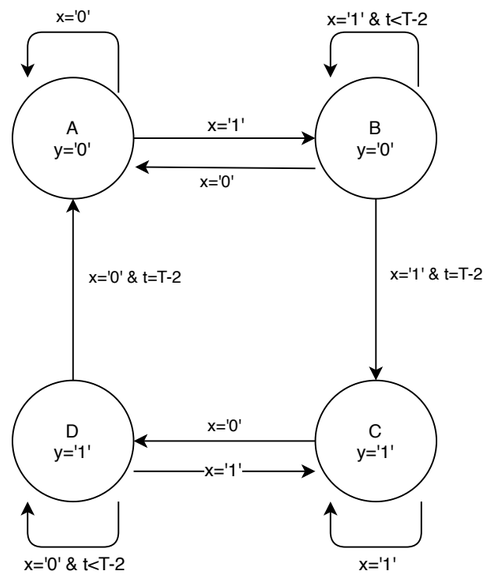
Tester FSM to load the TX ONLY UART with a 32 character text line, plus carriage return and new line.



Tester FSM for updating the PMOD CLS display.



Moore FSM for a synchronous pulse stretcher of signal X that lasts for a duration less than T, with Y lasting exactly T cycles. (Same as textbook figure 8.28.)



Moore FSM for a full switch debouncer, converting input X that has glitches to output Y that is glitch free. (Same as textbook figure 8.16.)