| Revision | Date | Author | Comments |
|---|---|---|---|
| 1A | 2020-06-22 | Tim S.<br>timothystotts08@gmail.com | First publishable draft of the serial accelerometer readings for Zynq tester |
| 2A | 2020-08-05 | Tim S.<br>timothystotts08@gmail.com | Credits to textbooks studied and applied for and IPI-BD design. Credits to Digilent Inc. Documentation. |
| 1B | 2020-12-09 | Tim S.<br>timothystotts08@gmail.com | Descriptions were updated from Vivado/SDK 2019.1 to Vivado/Vitis 2020.2 to match project sources update. |

https://github.com/timothystotts/fpga-serial-acl-tester-2


# Serial ACL Readings-Tester Experiment - Zynq

## Serial ACL Readings-Tester Experiment - Zynq: Folder Structure

ACL Readings Testing with function of performing a three-axis reading and displaying them on an LCD and USB terminal, in multiple modes of operation.

| Project Folder | Project Description |
|---|---|
| ACL-Tester-Design-Zynq<br>(Vivado 2020.2 and Vitis 2020.2) | A utility designed for custom operation of a serial accelerometer and displaying milli-g-force readings on both an LCD and a serial terminal. The design is completely in Zynq-7000 AXI subsystem with standard Xilinx IP Integrator components, and FreeRTOS C language program executing on the Zynq ARM hard processor. |

To successfully open the project, it is necessary to add the directory zybo-z7-20 from the directory board_files/ to the installation directory of Vivado 2020.2 but not to the installation directory of Vitis 2020.2. For example:

```
$ which vivado
/opt/Xilinx/Vivado/2020.2/bin/vivado
$ cd ./board_files
$ sudo cp -R ./zybo-z7-20 /opt/Xilinx/Vivado/2020.2/data/boards/board_files/
# (do not copy the board_files to
# /opt/Xilinx/Vitis/2020.2/data/boards/board_files/)
```

Note that the Digilent Guide at https://reference.digilentinc.com/vivado/installing-vivado/v2019.2 indicates to install the board files by copying to the install directory of the tool, so that the board files are always found.

## Serial ACL Readings-Tester Experiment: Methods of Operation

The purpose of the design is to boot a Digilent Inc. Zybo-Z7-20 (Zynq-7000) development board with PMOD CLS, PMOD ACL2, and PMOD SSD peripheral boards, which are a 16x2 Character dot-matrix LCD display, a 3-axis MEMS Accelerometer, and a two-digit 7-segment display, respectively. The PMOD CLS and PMOD ACL2 each connect to the FPGA with its own dedicated SPI bus via a higher-speed plug and jack. The PMOD CLS connects to board PMOD port JB. The PMOD ACL2 connects to board PMOD port JC. The PMOD SSD connects to board PMOD port JE. The use of extension cables makes, (a) the PMOD CLS able to connect to only one 2x6 PMOD port, (b) the PMOD SSD able to connect to only one 2x6 PMOD port, (c) the limited ability to move the PMOD ACL2 without requiring the

movement of the Zybo-Z7-20 board or the Pmod CLS display or the Pmod SSD display. See Figure 1: Zybo-Z7-20 Assembled with Pmod CLS, Pmod ACL2, Pmod SSD.

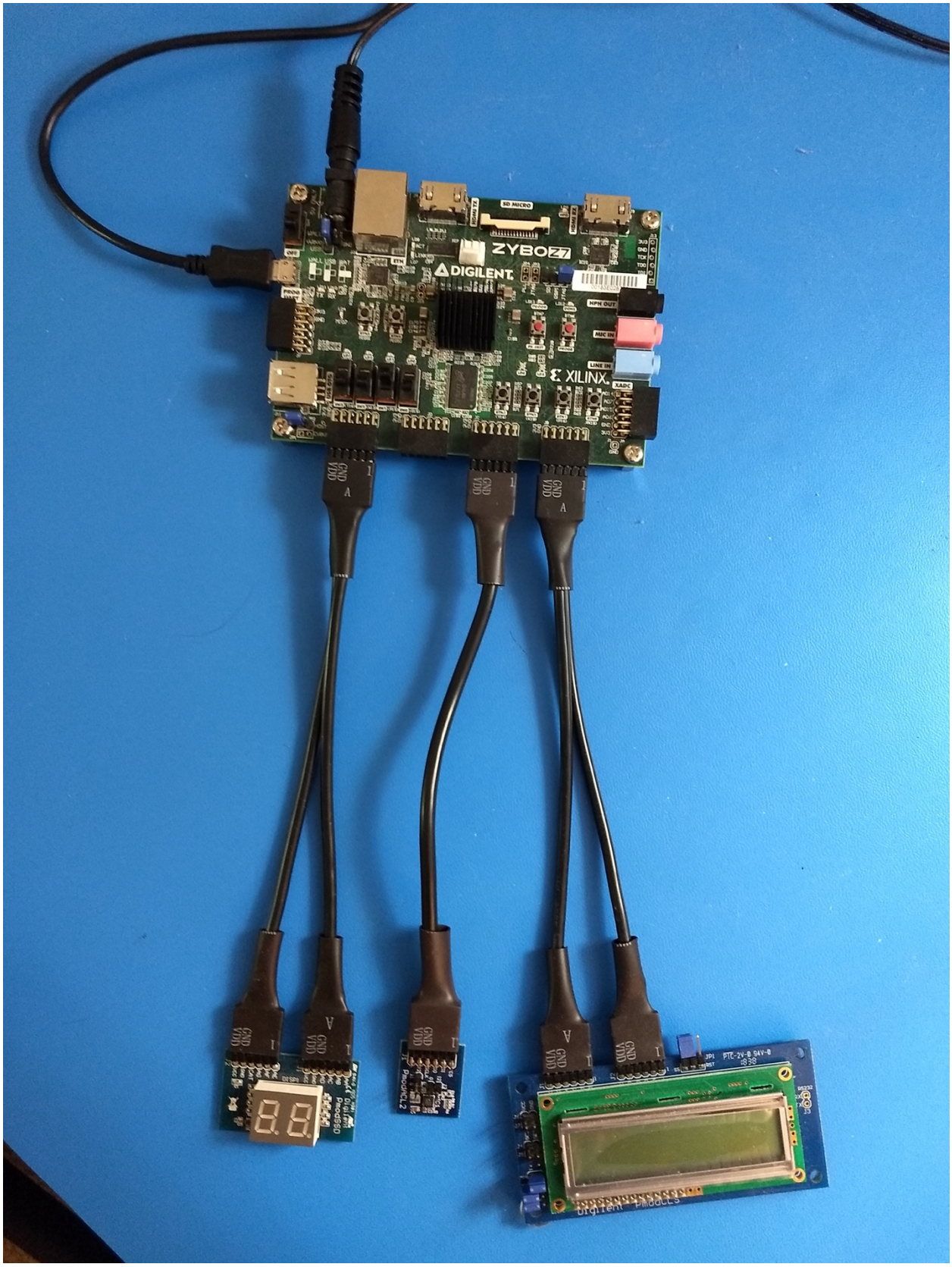


*Figure 1: Zybo-Z7-20 Assembled with Pmod CLS, Pmod ACL2, Pmod SSD.*

# Serial ACL Readings-Tester Experiment - Zynq: Method of Operation: streaming three-axis readings and displaying them, with alternate mode of activity detection

## Serial ACL Readings-Tester Experiment: Design Operation

In the IPI block design and SDK design, the four switches sw0, sw1, sw2, sw3, are debounced and processed as mutually exclusive inputs. When switch 0 is exclusively selected to the ON position, the Tester design controls the PMOD ACL2 to take 3-axis and compensating temperature readings at a rate of 100 Hz, poll these readings at at an approximated rate of under 5 Hz, and display readings at a rate of under 5 Hz. When switch 1 is exclusively selected to the ON position, the Tester design controls the PMOD ACL2 to detect motion activity and inactivity by thresholds. Each time there is an activity event, LD6 is lit green instead of red momentarily and a single reading from the PMOD ACL2 is displayed. Each time there is an inactivity event, LD5 is lit green instead of red momentarily and a single reading from the PMOD ACL is displayed.

LD0 through LD3 are used to display operational statuses. The LD0 is on when switch 0 is positioned to on, LD1 is on when switch 1 is positioned to on, LD2 is on when the accelerometer readings are being taken, and LD3 is on when the status register of the accelerometer indicates that it is in the AWAKE state. (Refer to the ADXL362 datasheet.) The LD1 displays Red to indicate that no operational mode is currently running. The LD2 and LD3 display Red to indicate Activity detection and Inactivity detection events, respectively, are not occurring.

Upon positioning switch 0 alone to ON, the LD2 is lit to indicate readings are being taken. The Pmod ACL2's ADXL362 chip is operating in Measurement Mode and that acceleration readings are polled from the ADXL362 to display in ASCII on the Pmod CLS and on the Digilent USB-UART at 115200 baud. The display on the Pmod CLS is in fixed-point milli-g-force and raw compensating temperature; and the display on the Digilent USB-UART is four raw register readings per line for ability to be parsed by a desktop utility. LD5 remains Red, and LD6 remains Red.

Upon positioning switch 1 alone to ON, the LD2 is lit to indicate readings are being taken. The ADXL362 is operating in Linked Mode with activity detection. Every time the Pmod ACL2 is moved above a modest threshold of motion, the LD6 displays Green momentarily to indicate that the ADXL362 has determined an Activity event. When the Pmod ACL2 is left motionless on a desk, the LD5 displays Green momentarily to indicate that the ADXL362 has determined an Inactivity event. Note that if an Activity event does not display even with modest movement of the Pmod ACL2, it may be necessary to wait several seconds with the Pmod ACL2 at rest for an Inactivity event to occur. After this, the ADXL362 is ready to detect the next Activity event.

The display text of the USB-UART and the Pmod CLS can be changed for purposes of debugging. If button 2 is held depressed, the Terminal will display fixed-point 3-axis milli-g readings and temperature reading decimal value to match the Pmod CLS display. When button 2 is released, the Terminal resumes displaying 16-bit hexadecimal readings from the four registers. If button 3 is held depressed, the Pmod CLS will display 16-bit hexadecimal readings from the four registers, matching the display of the Terminal.

The seven-segment display is used to indicate preset index for both activity events and inactivity events. If button 0 is pressed momentarily, the right digit of the Pmod SSD increments from zero to nine, and back to zero. Internally, the design selects a different Inactivity Threshold and Timer preset value for the next time the switch 0 is deselected and reselected for executing Linked Mode with Activity Events. If button 1 is pressed momentarily, the left digit of the Pmod SSD increments from zero to nine, and back to zero. Internally, the design selects a different Activity Threshold and Timer preset value for the next time the switch 1 is deselected and reselected for executing Linked Mode with Activity Events. (Refer to the ADXL362 datasheet and the "thresh_presets_include" sources.)

## Serial ACL Readings-Tester Experiment - Zynq: Design Theory

Note that in the IPI-BD (called AXI) Design, drivers downloaded from Digilent Inc. for the PMOD ACL2 and PMOD CLS are used in the block design with some minimal modification to target the Zybo-Z7-20 and support different modes of operating the Pmod ACL2. Both drivers target the Zybo-Z7-20 instead of the Arty; and the Pmod ACL2 User driver was copied, renamed, and expanded in the Xilinx SDK project, allowing for switching the ADXL326 between Measurement Mode and Linked Mode. The IPI design integrates the vendor components plus adds additional C code. The Git repository contains a submodule that pulls from a branch of the author's fork of the Digilent Vivado-library repository on GitHub.

### Coding style and choices of block design

The led_pwm.[ch] module was also refactored from Arty-A7-100T definitions to Zybo-Z7-20 definitions of the number and silkscreen number of the LEDs.

# Serial ACL Readings-Tester Experiment - Zynq: 3rd-party references:

## Digilent Inc. References

Zybo Z7 Reference Manual
https://reference.digilentinc.com/reference/programmable-logic/zybo-z7/reference-manual

Vivado Board Files
https://github.com/digilent/vivado-boards

Master XDC files for all Digilent Inc. boards, including Zybo-Z7-20
https://github.com/Digilent/digilent-xdc

Digilent Inc IP library for Xilinx Vivado
https://github.com/Digilent/vivado-library/

## Textbook References

Use of IP Integrator to create the Zynq-7000 AXI block diagram and synthesis:

- Tutorials followed from text to understand IPI block design,

L. H. Crockett, R. A. Elliot, M. A. Enderwitz, and R. W. Stewart, *The Zynq Book: Embedded Processing with the ARM Cortex-A9 on the Xilinx Zynq-7000 All Programmable SoC*, First Edition, Strathclyde Academic Media, 2014.

Study of Verilog HDL IEEE 1364-2001:

- FPGA-relevant homework studied and applied for comprehending Verilog-2001 language,

Samir Palnitkar, *Verilog HDL: A Guide to Digital Design and Synthesis*. 2nd ed., USA: SunSoft Press, 2003.