

Revision	Date	Author	Comments
1A	2020-07-30	Tim S. <a href="mailto:timothystotts08@gmail.com">timothystotts08@gmail.com</a>	First publishable draft of the serial flash sector tester for Zynq
2A	2020-07-31	Tim S. <a href="mailto:timothystotts08@gmail.com">timothystotts08@gmail.com</a>	Clerical change to wording.
3A	2020-08-04	Tim S. <a href="mailto:timothystotts08@gmail.com">timothystotts08@gmail.com</a>	Credits to textbooks studied and applied for and IPI-BD design. Credits to Digilent Inc. Documentation.
4A	2020-12-03	Tim S. <a href="mailto:timothystotts08@gmail.com">timothystotts08@gmail.com</a>	Descriptions were updated from Vitis/Vivado 2020.1 to 2020.2 .

<https://github.com/timothystotts/fpga-serial-mem-tester-2>

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## Serial Flash Sector-Tester Experiment - Zynq

### Serial Flash Sector-Tester Experiment - Zynq: Folder Structure

Serial Flash Sector Testing with function of performing an erase/program/read cycle in 1/32 address steps of a 256 Mbit Serial Flash.

Project Folder	Project Description
SF-Tester-Design-Zynq (Vivado 2020.2 and Vitis 2020.2)	A utility designed for custom operation of a serial flash and displaying erase/program/read-back byte error count on both an LCD and a serial terminal. The design is completely in Zynq-7000 AXI subsystem with standard Xilinx IP Integrator components, and FreeRTOS C language program executing on the Zynq ARM hard processor.

To successfully open the project, it is necessary to add the directory zybo-z7-20 from the directory board\_files/ to the installation directory of Vivado 2020.2 but not to the installation directory of Vitis 2020.2. For example:

```
$ which vivado
/opt/Xilinx/Vivado/2020.2/bin/vivado
$ cd ./board_files
$ sudo cp -R ./zybo-z7-20 /opt/Xilinx/Vivado/2020.2/data/boards/board_files/
# (do not copy the board_files to
# /opt/Xilinx/Vitis/2020.2/data/boards/board_files/)
```

Note that the Digilent Guide at <https://reference.digilentinc.com/vivado/installing-vivado/v2019.2> indicates to install the board files by copying to the install directory of the tool, so that the board files are always found.

### Serial Flash Sector-Tester Experiment- Zynq: Methods of Operation

The purpose of the design is to boot a Digilent Inc. Zynq-7000 development board with PMOD CLS and PMOD SF3 peripheral boards, which are a 16x2 Character dot-matrix LCD display, and a 256 Mbit N25Q serial flash, respectively. The PMOD CLS and PMOD SF3 each connect to the FPGA with its own dedicated SPI bus via a higher-speed plug and jack. The PMOD CLS connects to board PMOD port JB. The PMOD SF3 connects to board

PMOD port JC. The use of an extension cable makes the PMOD CLS able to connect to only one 2x6 PMOD port. See Figure 1: Zybo-Z7-20 Assembled with Pmod CLS, Pmod SF3.

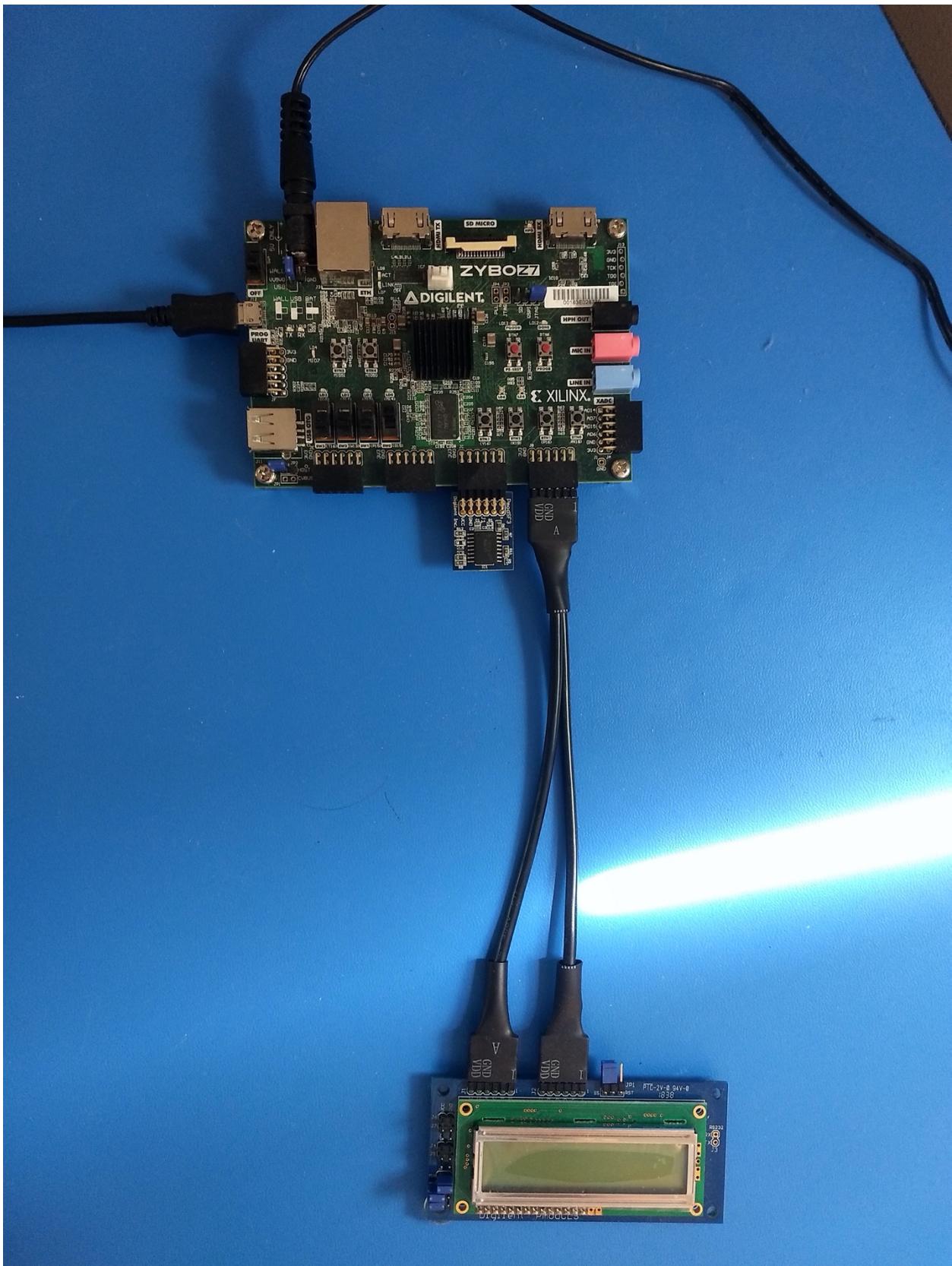


Figure 1: Zybo-Z7-20 Assembled with Pmod CLS, Pmod SF3

## Serial Flash Sector-Tester Experiment - Zynq: Method of Operation: iterative erase/program/read-back byte memory test from beginning to end of the serial flash

### Serial Flash Sector-Tester Experiment: Design Operation

In the APSoC implementation, the four switches are processed as mutually exclusive inputs, as are the four buttons. Each time a button is depressed and then released, or a switch position held as ON, a single pass of 1/32 of the memory space at the current memory index is tested for erase/program/read-back byte errors. Upon the next button depress or switch position held as ON, the subsequent 1/32 of the memory space is tested with cumulative results displayed. To test the whole memory without needing to press a button 32 times; a switch can be placed in the on position and will select the same pattern index (A, B, C, or D) as the button of the same index would have. Button 0 and Switch 0 select test pattern A. Button 1 and Switch 1 select test pattern B. Button 2 and Switch 2 select test pattern C. Button 3 and Switch 3 select test pattern D. A red color on the two LD5, LD6, indicate that the test is paused and waiting for user input; or that the test has completed. A green color on LD5, or LD6; or a blue color on LD5 or LD6, indicates which switch or button was depressed. A white LED indicates ERASE (ERS), PROGRAM (PRO); and a cyan LED indicates TEST READ-BACK (TST), or DISPLAY INCREMENT (END), to show the sequential advancement of the testing of each memory area in four steps, starting with a white color on LD5, then LD6, then a cyan color on LD5, then LD6. Note that the design will pause between testing steps and display an orange color on LD5 or LD6, after having displayed a white color or cyan color.

Note that in the AXI design, drivers downloaded from Digilent Inc. for the PMOD SF3 and PMOD CLS are used in the block design with some minimal modification and update to Xilinx Vivado and Vitis release 2020.2. The AXI implementation integrates vendor components plus adding additional C code. Note that the AXI implementation is much slower to execute each of the 1/32 cycles.

### Serial Flash Sector-Tester Experiment: Design Theory

Note that in the IPI-BD (called AXI) Design, drivers downloaded from Digilent Inc. for the PMOD SF3 and PMOD CLS are used in the block design with some minimal modification to target the Zybo-Z7-20 and correct bugs. Both drivers target the Zybo-Z7-20 instead of the Arty. The Make files and SPI sources were updated to match usage with Xilinx Vitis 2020.2 . Updates were fetched from Digilent branch feature/pmod\_update, and then additional modifications were made in the author's fork with branch zybo-z7-20-vivado-2020.2 . The AXI example integrates the vendor components plus adds additional C code. The Git repository contains a submodule that pulls from a branch of the author's fork of the Digilent Vivado-library repository on GitHub.

### Coding style and choices of block design

The led\_pwm.[ch] module was also refactored from Arty-A7-100T definitions to Zybo-Z7-20 definitions of the number and silkscreen number of the LEDs.

## Serial Flash Sector-Tester Experiment - Zynq: 3<sup>rd</sup>-party references:

Digilent Inc. References

Zybo Z7 Reference Manual

<https://reference.digilentinc.com/reference/programmable-logic/zybo-z7/reference-manual>

How To Store Your SDK Project in SPI Flash

<https://reference.digilentinc.com/learn/programmable-logic/tutorials/htsspisf/start>

Vivado Board Files

<https://github.com/digilent/vivado-boards>

Master XDC files for all Digilent Inc. boards, including Zybo-Z7-20

<https://github.com/Digilent/digilent-xdc>

Digilent Inc IP library for Xilinx Vivado

<https://github.com/Digilent/vivado-library/>

Textbook References

Use of IP Integrator to create the Zynq-7000 AXI block diagram and synthesis:

- Tutorials followed from text to understand IPI block design,

L. H. Crockett, R. A. Elliot, M. A. Enderwitz, and R. W. Stewart, *The Zynq Book: Embedded Processing with the ARM Cortex-A9 on the Xilinx Zynq-7000 All Programmable SoC*, First Edition, Strathclyde Academic Media, 2014.

Study of Verilog HDL IEEE 1364-2001:

- FPGA-relevant homework studied and applied for comprehending Verilog-2001 language,

Samir Palnitkar, *Verilog HDL: A Guide to Digital Design and Synthesis*. 2<sup>nd</sup> ed., USA: SunSoft Press, 2003.