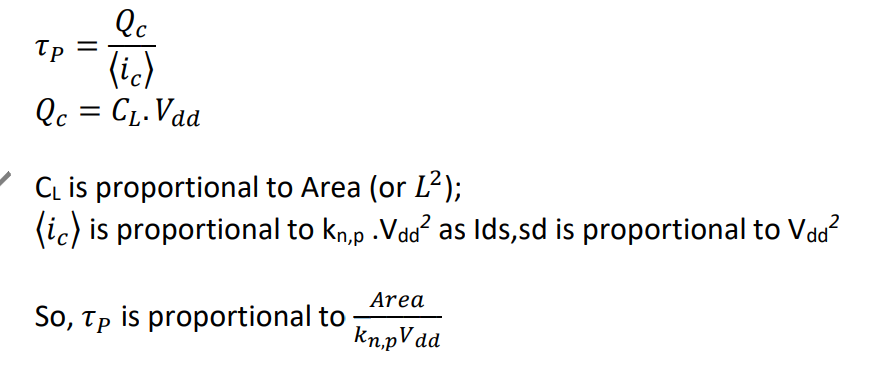
4a.



We should increase Vdd to make the design operate faster. The propagation is based off the current generated by the MOSFETS. Current is proportional to Vdd^2. Thus, a higher Vdd will increase the current of the system, which will change the output faster.

4b.

4c. We use CMOS technology since NMOS and PMOS alone do not give a ‘good 1’ and ‘good 0.’ NMOS does not have a ‘good 1’ since the voltage across the drain and source do not reach VDD. Whereas the PMOS does not have a ‘good 0’ since it cannot reach the minimum voltage, typically ground 0V. Since CMOS is able to reach the bounds of VDD and Ground, having multiple CMOS transistors will make sure we keep a consistent logic low and logic high.

4d.