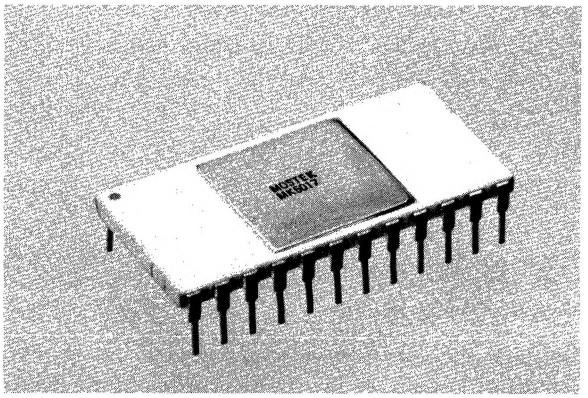
MOS Clock Circuit

MOSTEK

FEATURES

- ☐ 6-digit display
- ☐ 12/24 hour operation and display
- ☐ 50/60 Hz input
- ☐ Single power supply operation
- ☐ Easy to set
- ☐ Standard products available

Alarm Clock	MK 5017 P AA
Clock Radio Clock	MK 5017 P AN
Calendar Clock	MK 5017 P BB



SEGMENT IDENTIFICATION

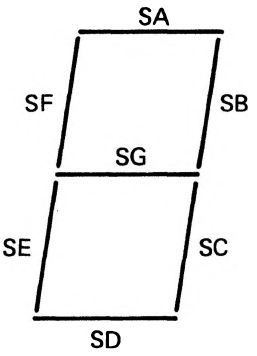


FIGURE 1

SEGMENT CODING

	SA	SB	SC	SD	SE	SF	SG
0	1	1	1	1	1	1	
1		1	1				
2	1	1		1	1		1
3	1	1	1	1			1
4		1	1			1	1
5	1		1	1		1	1
6	1		1	1	1	1	1
7	1	1	1				
8	1	1	1	1	1	1	1
9	1	1	1	1		1	1

DESCRIPTION

The MK 5017 P is a versatile MOS/LSI clock circuit manufactured by MOSTEK using its depletion-load, ion-implantation process and P Channel technology. Intended for a wide range of timing applications, all of these clock circuits may be used with either four or six digit displays. Operation from either a 50 Hz or 60 Hz input frequency may be selected. Another MOSTEK circuit (the MK 5009 P) is available to provide a 50 Hz signal from a 1 MHz crystal, where line frequency control is unavailable or inaccurate. A 50/60 Hz oscillator on the chip provides a temporary time base during momentary line frequency interruptions so that timekeeping can continue if a backup battery is provided to maintain V_{DD}.

Only a single power supply is required for operation. All segments are turned on (pulled toward V_{SS}) causing an all "8's" display as a power failure indication when V_{DD} is below the operating range.

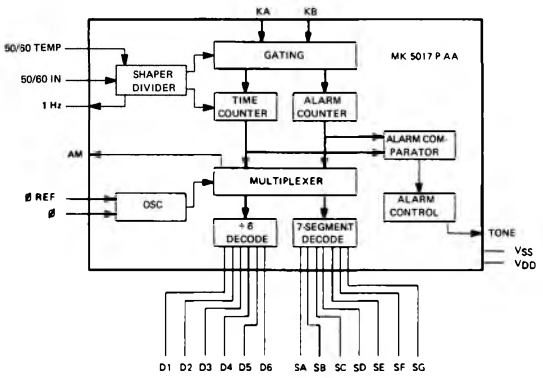
Data is multiplexed out of the clock in the form of six sequential seven-segment decoded digits. The segment coding is shown in figure 1.

A scanning technique is employed to sense control switch closures in order to minimize input pin connections. Using this method only two pins, KA and KB, are required to sense up to 12 control switch closures.

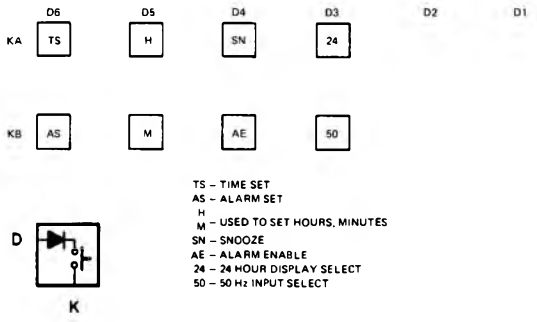
Consumer

MOSTEK MK 5017 AAP Digital Alarm Clock

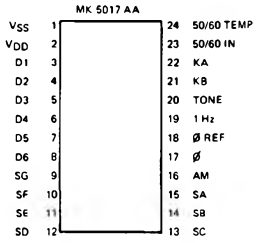
FUNCTIONAL DIAGRAM



INPUT MATRIX



MOS/LSI DIGITAL ALARM CLOCK



FEATURES

- ☐ Alarm with 24 hour operation
- ☐ Alarm tone generated on-chip
- ☐ AM/PM indication
- ☐ Snooze
- ☐ 1 Hz output

DESCRIPTION

Time may be set in the Run mode while the clock circuit is counting or the clock may be set in the Time Set mode while the counters are stopped. Contents of the time counters is displayed in both the Time Set and Run modes. The clock is in the Time Set mode when the (TS) switch located at the intersection of the KA and D6 lines in the input matrix is closed. in the Time Set mode the time counters are stopped and the seconds and tens of seconds digits are reset to zero.

The clock is in the Run mode when both the (TS) and the Alarm Set (AS) switches are open. In the Run mode, counters less significant than the one being set continue counting.

Switches (M) and (H) in the input matrix are closed to cause individual digits to be incremented. The (M) switch causes the minutes digit to be incremented. The (H) switch causes the hours digits to be incremented. Closing both the (H) and (M) switches simultaneously causes the tens of minutes digit to be incremented. Incrementing of a selected digit occurs at a 2 Hz rate and with the exception of the tens of hours digit, digits more significant than the one being set will not increment.

In order to accurately set the time to the nearest second the clock should be placed in the Time Set mode. After setting the time ahead, the clock should then be returned to the Run mode at the proper time in order to start the clock.

The clock must be placed in the Alarm Set mode by closing the (AS) switch to set the alarm. In the Alarm Set mode the time counters continue timekeeping and the contents of the alarm counter is displayed. The alarm may be set to the nearest minute by manipulating the (H) and (M) switches in the same manner as when setting the time.

Both the time counters and the alarm counters have an AM/PM indication which allows the time and the alarm to be set on a 24 hour basis, rather than a 12 hour basis.

The Tone output occurs when coincidence between the alarm counters and the time counters is detected internally, if the alarm is enabled. The Tone output signal is a train of positive going pulses whose nominal frequency is equal to the frequency of the scan oscillator divided by 140

and modulated at a 1 Hz rate. For a scan rate oscillator frequency of 100 KHz the Tone output frequency is approximately 700 Hz. The duty cycle of the Tone output pulses is approximately 3%. This signal suitably buffered may be used to drive a speaker, eliminating the need for mechanical buzzers or external alarm oscillators. Unless the alarm is disabled, the Tone output lasts for one hour after coincidence is detected.

The alarm is enabled while the (AE) switch in the input matrix is closed. To disable the alarm the (AE) switch should be opened. After the alarm is disabled, it may be immediately enabled again in order to utilize the 24 hour capability.

The Snooze feature provides a temporary reset to allow "sleep over". When the (SN) switch is momentarily closed, the Tone output ceases for a period of seven minutes. After this period the Tone output becomes active again unless the alarm has been disabled. This temporary reset may be utilized repeatedly up to one hour.

Either a 12 or 24 hour display may be selected by the (24) switch located at the intersection of the D3 and KA lines in the input matrix. When the (24) switch is closed a 24 hour display sequence from 00:00:00 to 23:59:59 is selected. When the (24) switch is open or absent a 12 hour display mode is selected.

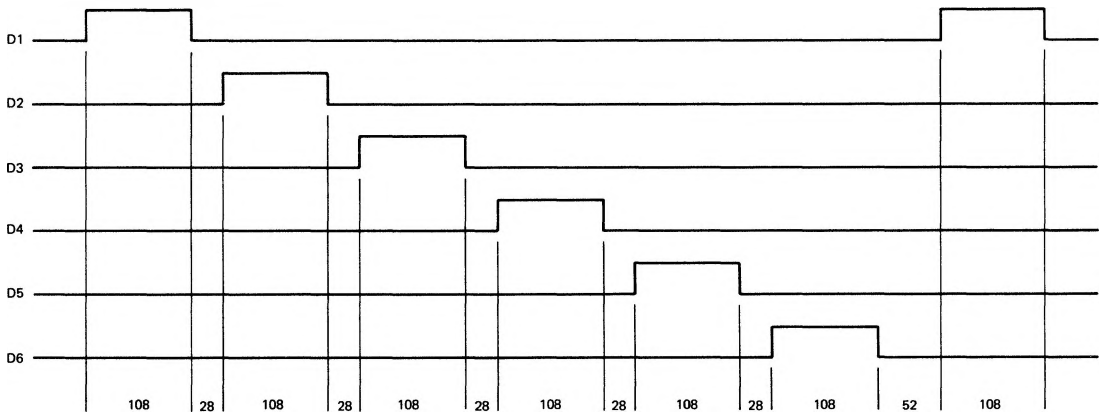
An AM output is provided to distinguish between AM and PM during 12 hour display. The AM output is at a logical one to indicate AM and is at a logical zero to indicate PM. This output switches logic levels every 12 hours in both 12 and 24 hour display modes.

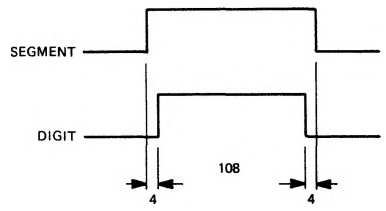
The (50) switch located at the intersection of the D3 and KB lines in the input matrix should be closed for operation from a 50 Hz reference frequency. The (50) switch should be omitted or left open for operation from a 60 Hz reference frequency.

A 1 Hz output is also provided as a time reference signal or it may be used to blink an indicator as an indication that the clock is counting, if the seconds and tens of seconds digits are not displayed. This 1 Hz output is modulated by digit strobe D4 to maintain constant relative intensity between the blinking indicator and the remainder of the display.

Six sequential digit strobes identify the segment information being presented. Figure 2 shows the digit strobe timing and the timing relationship between the digit and segment data.

DIGIT AND SEGMENT TIMING



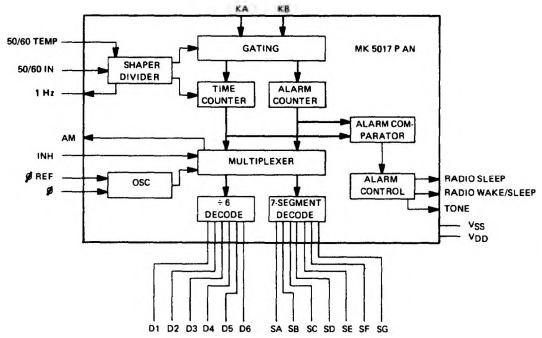


NOTES:

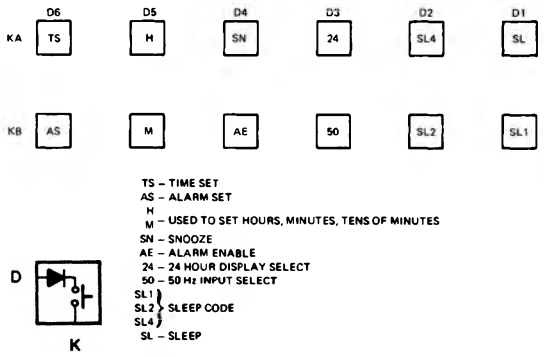
1. TIMES SHOWN ARE IN CLOCK PERIODS.

FIGURE 2

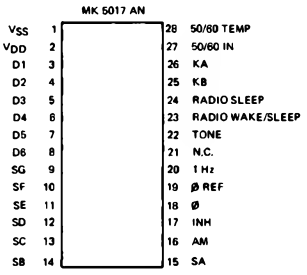
FUNCTIONAL DIAGRAM



INPUT MATRIX



MOS/LSI DIGITAL CLOCK WITH RADIO CONTROL



FEATURES

- ☐ Radio wake
- ☐ Radio sleep delay
- ☐ Snooze control
- ☐ Display inhibit
- ☐ Alarm with 24 hour operation
- ☐ Alarm tone generated on-chip
- ☐ AM/PM indication
- ☐ 1 Hz output

DESCRIPTION

Time may be set in the Run mode while the clock circuit is counting or the clock may be set in the Time Set mode while the counters are stopped. Contents of the time counters is displayed in both the Time Set and Run modes. The clock is in the Time Set mode when the (TS) switch located at the intersection of the KA and D6 lines in the input matrix is closed. In the Time Set mode the time counters are stopped and the seconds and tens of seconds digits are reset to zero.

The clock is in the Run mode when both the (TS) and the Alarm Set (AS) switches are open. In the Run mode, counters less significant than the one being set continue counting.

Switches (M) and (H) in the input matrix are closed to cause individual digits to be incremented. The (M) switch causes the minutes digit to be incremented. The (H) switch causes the hours digits to be incremented. Closing both the (H) and (M) switches simultaneously causes the tens of minutes digit to be incremented. Incrementing of a selected digit occurs at a 2 Hz rate and with the exception of the tens of hours digit, digits more significant than the one being set will not increment.

In order to accurately set the time to the nearest second the clock should be placed in the Time Set mode. After setting the time ahead, the clock should then be returned to the Run mode at the proper time in order to start the clock.

The clock must be placed in the Alarm Set mode by closing the (AS) switch to set the alarm. In the Alarm Set mode the time counters continue timekeeping and the contents of the alarm counter is displayed. The alarm may be set to the nearest minute by manipulating the (H) and (M) switches in the same manner as when setting the time.

Both the time counters and the alarm counters have an AM/Pm indication which allows the time and the alarm to be set on a 24 hour basis, rather than a 12 hour basis.

The Tone output occurs when coincidence between the alarm counters and the time counters is detected internally, if the alarm is enabled. The Tone output signal is a pulse train whose nominal frequency is equal to the frequency of the scan oscillator divided by 140 and modulated at a 1 Hz rate. For a scan rate oscillator frequency of 100 KHz the Tone output frequency is approximately 700 Hz. The duty cycle of the Tone output pulses is approximately 3%. This signal suitably buffered may be used to drive a speaker, eliminating the need for mechanical buzzers or external alarm oscillators. Unless the alarm is disabled, the Tone output lasts for one hour after coincidence is detected.

The alarm is enabled while the (AE) switch in the input matrix is closed. To disable the alarm the (AE) switch should be opened. After the alarm is disabled, it may be immediately enabled again in order to utilize the 24 hour capability.

The Snooze feature provides a temporary reset to allow "sleep over". When the (SN) switch is momentarily closed, the Tone output ceases for a period of seven minutes. After this period the Tone output becomes active again unless the alarm has been disabled. This temporary reset may be utilized repeatedly up to one hour.

Either a 12 or 24 hour display may be selected by the (24) switch located at the intersection of the D3 and KA lines in the input matrix. When the (24) switch is closed a 24 hour display sequence from 00:00:00 to 23:59:59 is selected. When the (24) switch is open or absent a 12 hour display mode is selected.

An AM output is provided to distinguish between AM and PM during 12 hour display. The AM output is at a logical one to indicate AM and is at a logical zero to indicate PM. This output switches logic levels every 12 hours in both 12 and 24 hour display modes.

The (50) switch located at the intersection of the D3 and KB lines in the input matrix should be closed for operation from a 50 Hz reference frequency. The (50) switch should be omitted or left open for operation from a 60 Hz reference frequency.

A 1 Hz output is also provided as a time reference signal or it may be used to blink an indicator as an indication that the clock is counting, if the seconds and tens of seconds digits are not displayed. This 1 Hz output is modulated by digit strobe D4 to maintain constant relative intensity between the blinking indicator and the remainder of the display.

Radio sleep time is selected by application of a binary code to the three sleep time select switches, SL1, SL2, and SL4. The sleep times that may be selected and the codes for selecting them are shown below.

RADIO SLEEP TIME TABLE

SLEEP TIME	SELECTION CODE		
	SL4	SL2	SL1
10 MIN	0	0	0
20 MIN	0	0	1
30 MIN	0	1	0
40 MIN	0	1	1
50 MIN	1	0	0
60 MIN	1	0	1
90 MIN	1	1	0
120 MIN	1	1	1

0 — AN OPEN SWITCH

1 — A CLOSED SWITCH

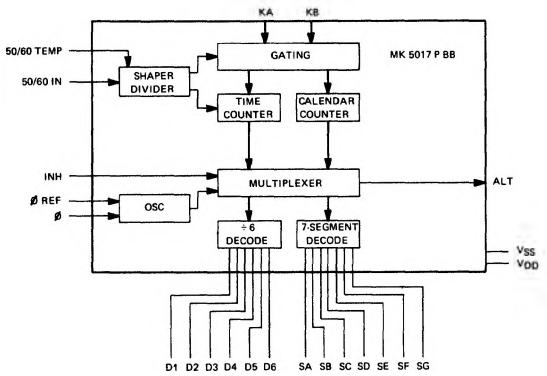
After selecting the desired time, the Sleep Switch (SL) is closed. This starts the proper interval and causes the RADIO SLEEP and RADIO WAKE/SLEEP outputs to switch to a logical zero. To terminate the count before the end of the sleep time, the SL switch is opened. If the SL switch is closed again, the selected sleep interval begins again.

The RADIO WAKE/SLEEP (RWS) output also switches toward V_{DD} whenever coincidence between the time and alarm counters is detected, if the Alarm Enable switch (AE) is closed. RWS remains at a logical zero for one hour after detection of coincidence and then switches to a logical one, toward V_{SS}.

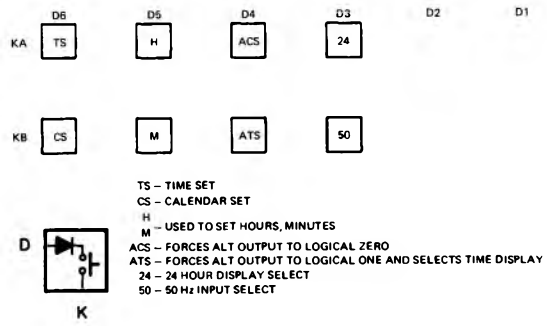
An inhibit input is provided to disable the digit and segment outputs so that they do not switch to V_{SS}. This input may be used to "wire or" multiple chips together. The output transistors are disabled when the INH input is connected to V_{SS}.

Six sequential digit strobes identify the segment information being presented. Figure 2 shows the digit strobe timing and the timing relationship between the digit and segment data.

FUNCTIONAL DIAGRAM

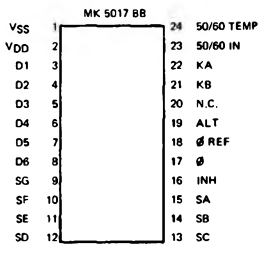


INPUT MATRIX



TS – TIME SET
CS – CALENDAR SET
H
M – USED TO SET HOURS, MINUTES
ACS – FORCES ALT OUTPUT TO LOGICAL ZERO
ATS – FORCES ALT OUTPUT TO LOGICAL ONE AND SELECTS TIME DISPLAY
24 – 24 HOUR DISPLAY SELECT
50 – 50 Hz INPUT SELECT

MOS/LSI DIGITAL CLOCK/CALENDAR



FEATURES

- ☐ Alternating time/calendar display
- ☐ Display inhibit

DESCRIPTION

Time may be set only in the Time Set mode. Contents of the time counter are displayed in the Time Set mode and the clock continues counting. The clock is in the Time Set mode when the (TS) switch, located at the intersection of the KA and D6 lines in the input matrix, is closed.

Switches (M) and (H) in the input matrix are closed to cause individual digits to be incremented. The (M) switch causes the minutes digit to be incremented. Closing the (H) switch causes the hours digit to be incremented. Closing the (H) and (M) switches simultaneously causes the tens of minutes digit to be incremented in the Time Set mode. Incrementing of a selected digit occurs at a 2 Hz rate. With the exception of the tens of hours digit, digits more significant than the one being set will not increment.

The clock must be placed in the Calendar Set mode by closing the (CS) switch in the input matrix to set the calendar. In the Calendar Set mode the contents of the calendar counter are displayed. When the (M) switch in the input matrix is closed in the Calendar Set mode, the days digit is incremented. Closing the (H) switch causes the months digit to be incremented. Closing both the (H) and (M) switches simultaneously has no effect in the Calendar Set mode. Incrementing of the digits being set occurs at a 2 Hz rate. Digits more significant than the one being set will increment.

When the day is changed during calendar setting, the time display resets to the AM portion of the day. Thus, the date continues to change at 12:00 A.M. instead of noon.

The clock is in the Run mode when both the (TS) and the calendar set (CS) switches are open. Neither the time counter nor the calendar counter can be set in the Run mode.

An inhibit input is provided to disable the digit and segment outputs so that they do not switch to V_{SS}. This input may be used to

"wire or" multiple clock circuit outputs together. A logical one on the inhibit input disables the outputs.

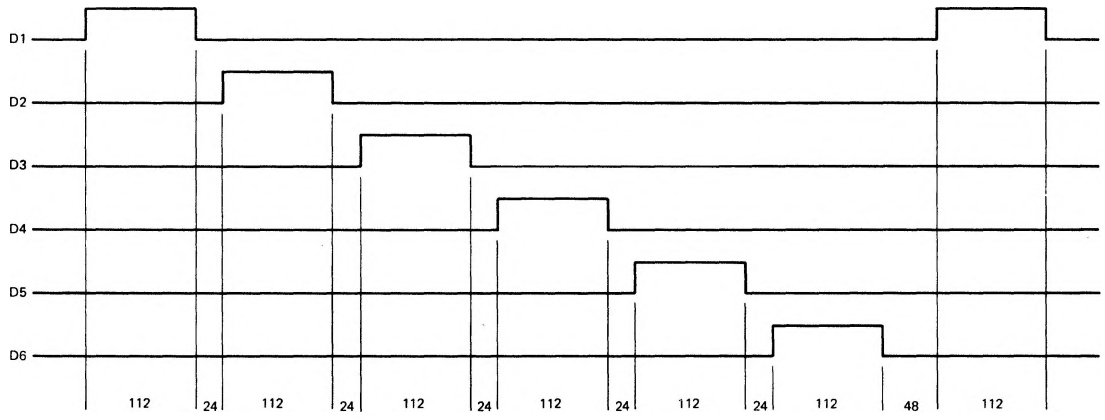
The ALT output indicates whether time or date is being displayed in the Run mode. Whie time is being displayed the ALT output is at a logical one. In either the Time Set or Calendar Set modes the ALT output continues alternating between a logical one and a logical zero. The ALT output is forced to remain at a logical one when the Alternate Time Set switch (ATS) is closed. Only time is displayed when the (ATS) switch is closed. When the Alternate Calendar Set switch (ACŞ) is closed, the ALT output is forced to remain at a logical zero.

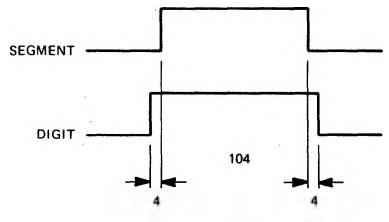
In the Run mode the display alternates between the time display and the calendar display, displaying time for 8 seconds and calendar information for 2 seconds.

Closing the 50/60 Hz (50) switch located at the intersection of the D3 and KB lines in the input matrix allows a 50 Hz reference frequency to be used. When the (50) switch is open, a 60 Hz reference frequency should be used.

Six sequential digit strobes identify the segment information being presented. Figure 3 shows the digit strobe timing relationship between the digit and segment data.

DIGIT AND SEGMENT TIMING





NOTES:

1. TIMES SHOWN ARE IN CLOCK PERIODS.

FIGURE 3

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE
(All voltages relative to V_{SS})

Supply Voltage Range
- V_{DD} . . . . . +0.3 to −20 Volts

Input Voltage Range
- KA, KB . . . . . +0.3 to −20 Volts
- 1NH, 50/60 IN, TEMP, Ø . . . . . +0.3 to −20 Volts

Output Voltage Breakdown
- D1–D6, SA–SG, AM . . . . . −35 Volts
- 1 Hz, RS, RSW, TN, Ø Ref, ALT . . . . . −25 Volts

Operating Free-Air Temperature Range . . . . . 0°C to +70°C

Storage Temperature Range . . . . . −55°C to 150°C

RECOMMENDED OPERATING CONDITIONS
(0°C to +70°C—All voltages relative to V_{SS})

PARAMETER	MIN	TYP	MAX	UNITS	NOTES
Operating Voltages V_{DD}	−11.0		−18.0	Volts	
Input Logic Levels					
KA, KB					
"1" Logic Level	− 4.0		+ 0.3	Volts	
"0" Logic Level	V_{DD} +1.0		−35	Volts	
50/60 In, Temp, Ø					
"1" Logic Level	− 3.0		+ 0.3	Volts	
"0" Logic Level	V_{DD} +0.3		−20	Volts	
INH					
"1" Logic Level	− 1		+0.3	Volts	
"0" Logic Level	− 5		V_{DD}	Volts	
Scan Oscillator Frequency (using external driver)	25		100	KHz	

ELECTRICAL CHARACTERISTICS—5017 AA/AN/BB
(11V ≤ V_{DD} ≤ 18V; 0°C ≤ T_A ≤ 70°C

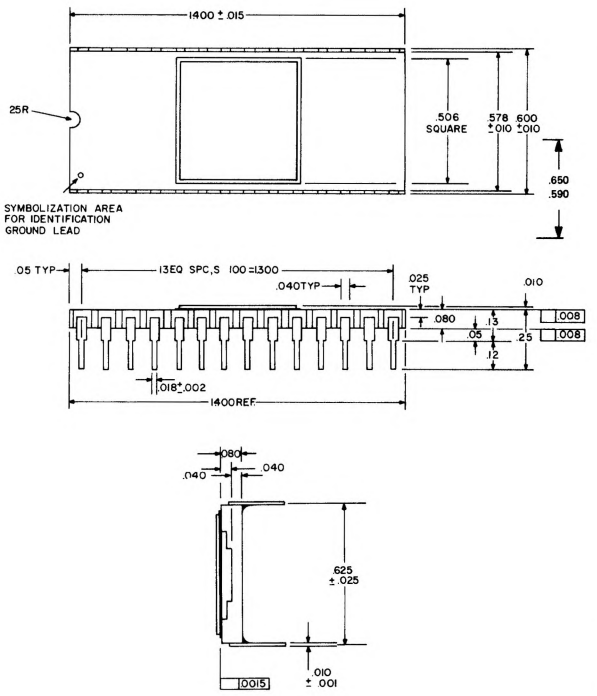
PARAMETER	MIN	TYP	MAX	UNITS	NOTES
Output Current					
D1–D6, 1 Hz, ALT					
"1" Logic Level	8			mA	3
"0" Logic Level					2
SA–SG, AM					
"1" Logic Level	200			μA	4
"0" Logic Level					2
TN, RWS, RS					
"1" Logic Level	0.8			mA	5
"0" Logic Level	50			μA	6
Supply Current, I_{DD}		10	16	mA	
Leakage, D1–D6, SA–SG, AM			10	μA	7
Leakage, 1 Hz, ALT			10	μA	8
Scan Oscillator Frequency	60		210	KHz	1
Input Current, KA, KB			0.5	mA	9
Input Current, INH			1.0	mA	10

Note 1 RØ = 18K, CØ = 51PF, T_A = 25°C
Note 2 External Resistor Required
Note 3 Output voltage equal to V_{SS}−3.0V
Note 4 Output voltage equal to V_{SS}−0.5V
Note 5 Output voltage equal to V_{SS}−2.0V
Note 6 Output voltage equal to V_{DD}+4.0V
Note 7 V_{DD} = V_{SS} = 0 volts, output voltage equal to −35 volts
Note 8 V_{DD} = V_{SS} = 0 volts, output voltage equal to −20 volts
Note 9 Input voltage equal to V_{SS}−3.0V
Note 10 Input voltage equal to V_{SS}

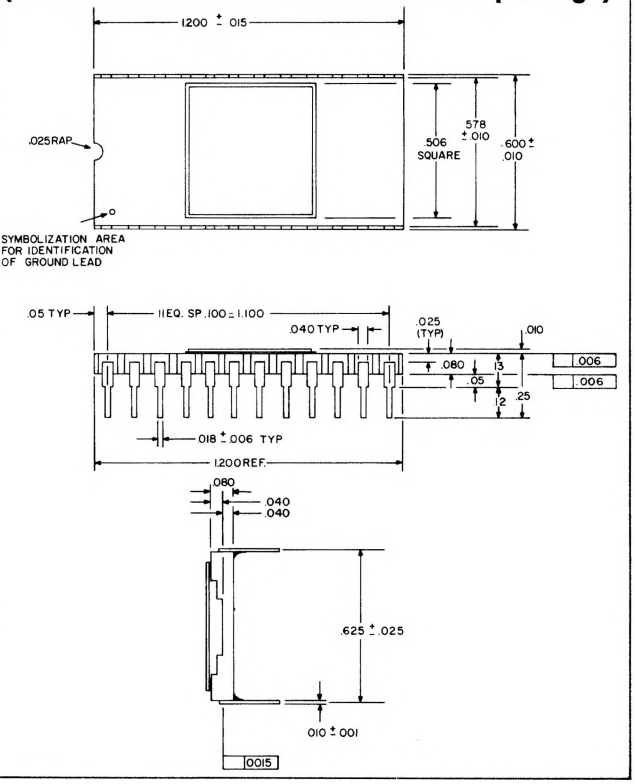
CLOCK CIRCUIT TYPES

PIN DESIGNATION	CLOCK CIRCUIT AA	AN	BB	FUNCTION
V_{SS}	X	X	X	Supply Voltage
V_{DD}	X	X	X	Supply Voltage
D1	X	X	X	Digit Strobe 1 Sec/Blank
D2	X	X	X	Digit Strobe, 10 Sec/Blank
D3	X	X	X	Digit Strobe, 1 Min/1 Day
D4	X	X	X	Digit Strobe, 10 Min/10 Day
D5	X	X	X	Digit Strobe, 1 Hr/1 Month
D6	X	X	X	Digit Strobe, 10 Hr/10 Month
SA	X	X	X	Segment A Data
SB	X	X	X	Segment B Data
SC	X	X	X	Segment C Data
SD	X	X	X	Segment D Data
SE	X	X	X	Segment E Data
SF	X	X	X	Segment F Data
SG	X	X	X	Segment G Data
Ø	X	X	X	Scan Oscillator Input
Ø Ref	X	X	X	Scan Oscillator Feedback
KA	X	X	X	Multiplexed Input
KB	X	X	X	Multiplexed Input
50/60 In	X	X	X	Input Count Frequency
50/60 Temp	X	X	X	Temporary Oscillator
AM	X	X		AM/PM Indication
1 Hz	X	X		Optional Output
Tone	X	X		Alarm Tone
INH		X	X	Inhibit
RS		X		Radio Sleep
RWS		X		Radio Wake/Sleep
ALT			X	Alternate

PHYSICAL DESCRIPTION
(28 lead ceramic dual-in-line hermetic package)



PHYSICAL DESCRIPTION
(24 lead ceramic dual-in-line hermetic package)



Consumer