# 3 In-Order Superscalar Processors

## 3.a Pipeline Diagram for Single-Issue PARCv1 Processor

| Cycle: | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| lw r1 , 0(r2) | F | D | X | M | W | | | | | | | | | | | | | |
| lw r3 , 0(r4) | | F | D | X | M | W | | | | | | | | | | | | |
| mul r1, r1, r6 | | | F | D | X | M | W | | | | | | | | | | | |
| mul r3, r3, r7 | | | | F | D | X | M | W | | | | | | | | | | |
| addu r8, r1, r3 | | | | | F | D | X | M | W | | | | | | | | | |
| addu r9, r9, r8 | | | | | | F | D | X | M | W | | | | | | | | |
| addiu r2, r2, 4 | | | | | | | F | D | X | M | W | | | | | | | |
| addiu r4, r4, 4 | | | | | | | | F | D | X | M | W | | | | | | |
| addiu r10, r10, -1 | | | | | | | | | F | D | X | M | W | | | | | |
| bne r10, r0, loop | | | | | | | | | | F | D | X | M | W | | | | |
| opA | | | | | | | | | | | F | D | - | - | - | | | |
| opB | | | | | | | | | | | | F | - | - | - | - | | |
| lw r1 , 0(r2) | | | | | | | | | | | | | F | D | X | M | W | |
| lw r3 , 0(r4) | | | | | | | | | | | | | | F | D | X | M | W |

Figure 7: Pipeline Diagram for Single-Issue PARCv1 Processor

As shown by the bold vertical lines, each loop takes 12 cycles to execute. The CPI is therefore 12/10 = 1.2. The IPC is 1/CPI = 0.833.
CPI = 1.2 cycles/instruction
IPC = 0.83 instructions/cycle

## 3.b Pipeline Diagram for Dual-Issue PARCv1 Processor

| Cycle: | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| lw r1 , 0(r2) | F | D | B0 | B1 | W | | | | | | | | | | | | |
| lw r3 , 0(r4) | F | D | D | B0 | B1 | W | | | | | | | | | | | |
| mul r1, r1, r6 | | F | F | D | A0 | A1 | W | | | | | | | | | | |
| mul r3, r3, r7 | | F | F | D | D | A0 | A1 | W | | | | | | | | | |
| addu r8, r1, r3 | | | | F | F | D | A0 | A1 | W | | | | | | | | |
| addu r9, r9, r8 | | | | F | F | D | D | B0 | B1 | W | | | | | | | |
| addiu r2, r2, 4 | | | | | | F | F | D | A0 | A1 | W | | | | | | |
| addiu r4, r4, 4 | | | | | | F | F | D | B0 | B1 | W | | | | | | |
| addiu r10, r10, -1 | | | | | | | | F | D | B0 | B1 | W | | | | | |
| bne r10, r0, loop | | | | | | | | F | D | D | A0 | A1 | W | | | | |
| opA | | | | | | | | | F | F | D | - | - | - | | | |
| opB | | | | | | | | | F | F | D | - | - | - | | | |
| opC | | | | | | | | | | | F | - | - | - | - | | |
| opD | | | | | | | | | | | F | - | - | - | - | | |
| lw r1 , 0(r2) | | | | | | | | | | | | F | D | B0 | B1 | W | |
| lw r3 , 0(r4) | | | | | | | | | | | | F | D | D | B0 | B1 | W |

Figure 8: Pipeline Diagram for Dual-Issue PARCv1 Processor

As shown by the bold vertical lines, each loop takes 11 cycles to execute. The CPI is therefore 11/10 = 1.1. The IPC is 1/CPI = 0.910.
CPI = 1.1 cycles/instruction
IPC = 0.91 instructions/cycle

## 3.c Optimized Pipeline Diagram for Dual-Issue PARCv1 Processor

```
1  lw r1 , 0(r2)
2  addiu r2, r2, 4
3  lw r3 , 0(r4)
4  addiu r4, r4, 4
5  mul r1, r1, r6
6  addiu r10, r10, -1
7  mul r3, r3, r7
8  addu r8, r1, r3
9  addu r9, r9, r8
10 bne r10, r0, loop
```

| Cycle: | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| lw r1 , 0(r2) | F | D | B0 | B1 | W | | | | | | | | |
| addiu r2, r2, 4 | F | D | A0 | A1 | W | | | | | | | | |
| lw r3 , 0(r4) | | F | D | B0 | B1 | W | | | | | | | |
| addiu r4, r4, 4 | | F | D | A0 | A1 | W | | | | | | | |
| mul r1, r1, r6 | | | F | D | A0 | A1 | W | | | | | | |
| addiu r10, r10, -1 | | | F | D | B0 | B1 | W | | | | | | |
| mul r3, r3, r7 | | | | F | D | A0 | A1 | W | | | | | |
| addu r8, r1, r3 | | | | F | D | D | B0 | B1 | W | | | | |
| addu r9, r9, r8 | | | | | F | F | D | B0 | B1 | W | | | |
| bne r10, r0, loop | | | | | F | F | D | A0 | A1 | W | | | |
| opA | | | | | | | F | D | - | - | - | | |
| opB | | | | | | | F | D | - | - | - | | |
| opC | | | | | | | | F | - | - | - | - | |
| opD | | | | | | | | F | - | - | - | - | |
| lw r1 , 0(r2) | | | | | | | | | F | D | B0 | B1 | W |
| addiu r2, r2, 4 | | | | | | | | | F | D | A0 | A1 | W |

Figure 9: Optimized Pipeline Diagram for Dual-Issue PARCv1 Processor

As shown by the bold vertical lines, each loop takes 8 cycles to execute. The CPI is therefore $8/10 = 0.8$. The IPC is $1/\text{CPI} = 1.25$.
CPI = 0.8 cycles/instruction
IPC = 1.25 instructions/cycle

## 3.d Optimized Pipeline Diagram for Quad-Issue PARCv1 Processor

```
1  lw r1 , 0(r2)
2  addiu r2, r2, 4
3  lw r3 , 0(r4)
4  addiu r4, r4, 4
5  mul r1, r1, r6
6  addiu r10, r10, -1
7  mul r3, r3, r7
8  addu r8, r1, r3
9  addu r9, r9, r8
10 bne r10, r0, loop
```

| Cycle: | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| lw r1 , 0(r2) | F | D | B0 | B1 | W | | | | | | | |
| addiu r2, r2, 4 | F | D | A0 | A1 | W | | | | | | | |
| lw r3 , 0(r4) | F | D | H0 | H1 | W | | | | | | | |
| addiu r4, r4, 4 | F | D | G0 | G1 | W | | | | | | | |
| mul r1, r1, r6 | | F | F | D | A0 | A1 | W | | | | | |
| addiu r10, r10, -1 | | F | F | D | B0 | B1 | W | | | | | |
| mul r3, r3, r7 | | F | F | D | G0 | G1 | W | | | | | |
| addu r8, r1, r3 | | F | F | D | D | H0 | H1 | W | | | | |
| addu r9, r9, r8 | | | | F | F | D | B0 | B1 | W | | | |
| bne r10, r0, loop | | | | F | F | D | A0 | A1 | W | | | |
| opA | | | | F | F | D | G0 | - | - | | | |
| opB | | | | F | F | D | H0 | - | - | | | |
| opC | | | | | | F | D | - | - | - | | |
| opD | | | | | | F | D | - | - | - | | |
| opE | | | | | | F | D | - | - | - | | |
| opF | | | | | | F | D | - | - | - | | |
| opG | | | | | | | F | - | - | - | - | |
| opH | | | | | | | F | - | - | - | - | |
| opI | | | | | | | F | - | - | - | - | |
| opJ | | | | | | | F | - | - | - | - | |
| lw r1 , 0(r2) | | | | | | | | F | D | B0 | B1 | W |
| addiu r2, r2, 4 | | | | | | | | F | D | A0 | A1 | W |
| lw r3 , 0(r4) | | | | | | | | F | D | H0 | H1 | W |
| addiu r4, r4, 4 | | | | | | | | F | D | G0 | G1 | W |

Figure 10: Optimized Pipeline Diagram for Quad-Issue PARCv1 Processor

As shown by the bold vertical lines, each loop takes 7 cycles to execute. The CPI is therefore $7/10 = 0.7$. The IPC is $1/\text{CPI} = 1.43$.
CPI = 0.7 cycles/instruction
IPC = 1.43 instructions/cycle

## 3.e Instruction Level Parallelism

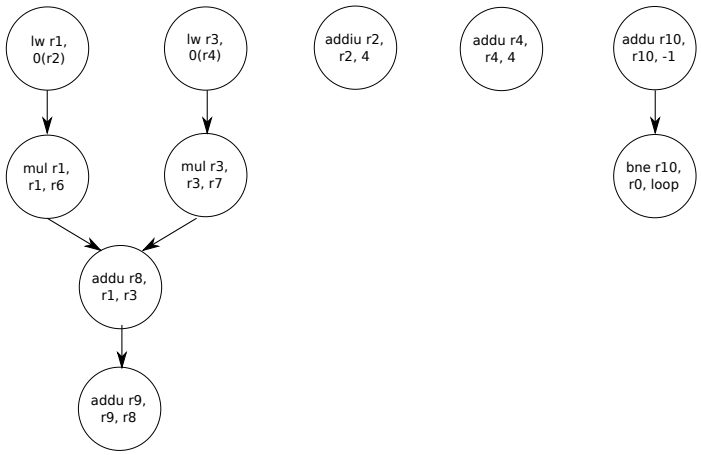


Figure 11: Instruction Dependency Graph for Single Iteration

The longest path contains 4 nodes. The ideal ILP for a single iteration is $10/4 = 2.5$.

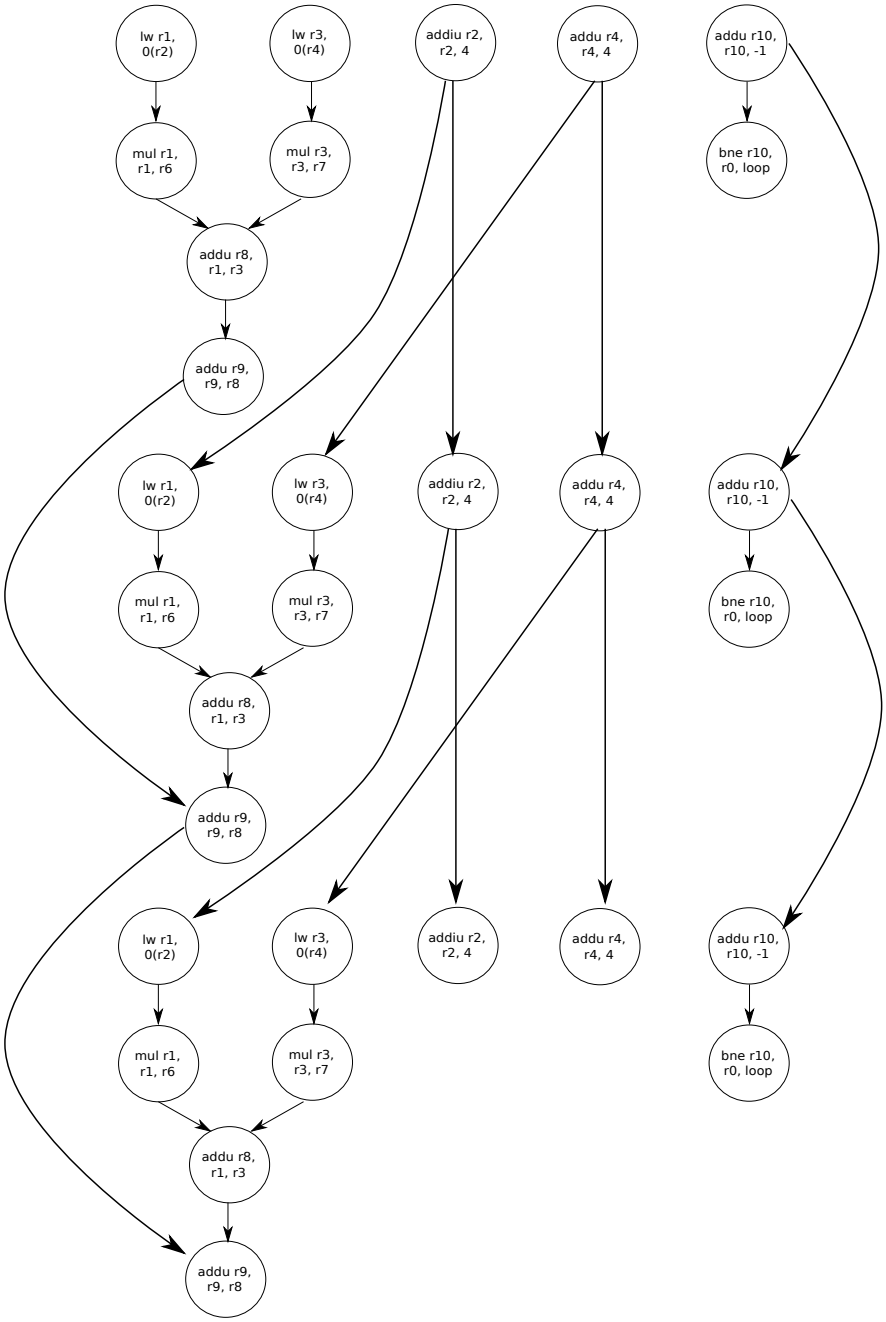


Figure 12: Instruction Dependency Graph for Three Iterations

The longest path contains 6 nodes. The ideal ILP for three iterations is $30/6 = 5$.

The ideal ILP for N iterations of the loop is simply $10N/(3+N)$.

The IPC of the quad-issue processor is less than the ideal ILP due to several different reasons. The first is that the quad issue processor can only execute at most 4 instructions simultaneously. This thereby limits the IPC to a max of 4. Then, the load word instructions are resolved in the second functional unit in the pipeline, which means that a RAW hazard on the next set of instructions will need to be stalled by 1 cycle. There is also a RAW hazard within a fetch block, so this requires 1 cycle of stalling. Finally, the branch instruction introduces another 2 cycles of delay. There are also 2 squashed instructions in the fetch block with the branch instruction, so this reduced the number of executed instructions for calculating the IPC. In the ideal case, we can execute 12 instructions in 3 cycles, but after adding in the squashed instructions and various delays, we are actually executing 10 instructions in 7 cycles.