ECE 4750 PSET 2

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1 PARCv1 Instruction Cache

1.a Categorizing Cache Misses

Addr	Instruction	Iteration 1	Iteration 2
	loop:		
0x108	addiu r1, r1, -1	compulsory	
0x10c	addiu r2, r2, -1		
0x110	j foo	compulsory	conflict
	...		
	foo:		
0x218	addiu r6, r6, 1	compulsory	conflict
0x21c	bne r1, r0, loop		

Figure 1: Cache Miss Type

1.b Average Memory Access Latency

Looking at iteration 2, we can see that there are 2 misses out of the 5 instructions. Therefore the miss rate for 64 iterations of the loop is 0.4.
The average memory access latency is:
AMAL = (Hit Time) + (Miss Rate $\times$ Miss Penalty)
AMAL = $1 + (0.4 \times 5)$
AMAL = 3 cycles
The AMAL is dominated by conflict misses, as shown by the miss chart above. Compulsory misses only occur on the first iteration of the loop.

1.c Set-Associativity

The cache performance will increase significantly, because there will no longer be conflict misses during the loop. With this new cache microarchitecture, only compulsory misses will be left.