Phase Disposition PWM (PD-PWM) Technique to Minimize WTHD from a Three-Phase NPC Multilevel Voltage Source Inverter

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Abstract—**Neutral-point clamped multilevel inverter (NPC-MLI) has become a widely accepted choice in the area of industrial drive applications. The problem concerning the higher harmonic content and the higher switching frequency still exist in the conventional NPC-MLI topology. In this paper, a phase disposition pulse width modulation (PD-PWM) technique is proposed for a three-phase five-level NPC-MLI, which is proficient in reducing the high-frequency weighted total harmonic distortion (WTHD) content of the inverter output voltage by employing a mathematically formulated harmonic mitigation algorithm. The experimental results of a three-phase NPC-MLI prototype hold a good resemblance with the theoretical calculation and simulated results of the proposed control scheme. Besides, a quantitative comparative investigation affirms that the proposed PD-PWM technique exhibits the lowest WTHD content among all the earlier-proposed PWM schemes under study, which verifies the pre-eminence of the proposed work.**

Keywords—PD-PWM, NPC Inverter, Multilevel, WTHD, Harmonic.

I. INTRODUCTION

Compared to conventional inverters, multilevel inverter (MLI) topologies are widely accepted to the researchers and power electronics industries especially in high power applications. These MLIs offer improved efficiency owing to the reduction of harmonic percentage from the inverter output voltage waveform and reduced production cost as lower-rated components are used in the experimental prototype [1]. The merits of the MLI include lower *dv/dt* stress, transient fault tolerance capability, and a higher level of voltage utilization [2]. These MLIs can be classified further, viz. Cascaded H-bridge (CHB), neutral-point clamped (NPC), and flying capacitor (FC) [1]- [3]. NPC inverter has become the most popular topology over the years due to the following advantages:

a. Semiconductor switching voltage becomes half of the dc-bus voltage.
b. As the voltage levels (n) are higher, the output voltage contains less harmonics which in turn reduces the complexity of filter circuitry.
c. The overall cost of the inverter reduces as the number of levels (n) is higher.

The clamping diodes of the NPC-MLI boost the voltage stress equal to $V_{DC}.(n-1)/n$ as shown in Fig. 1; where V_{dc} is termed as the input DC voltage. Thus, an array of series-connected power electronics components is sometimes used in the topology to increase the system reliability and to reduce the voltage stress.

In order to achieve a multilevel (n level) output voltage, quite a few pulse width modulation (PWM) techniques have been adapted in the NPC topology [4]-[8].A modified space

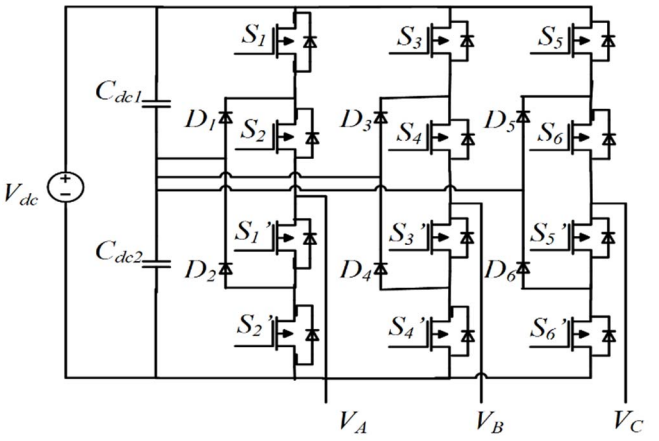

Fig. 1. Combination of different switching components of a three-phase NPC-MLI topology.

vector PWM (SVPWM) method was proposed in [4]-[5],which solves the DC-link balancing issue of the three-level NPC-MLI. An adaptive control technique was introduced in a three-phase Z-NPC inverter to replenish its non-linear characteristics [6]. An improved SVPWM method was employed in a Z-source DC-link cascaded NPC inverter [7], to mitigate the common-mode voltage and leakage current issue of the grid-connected application, but the technique increases the overall system complexity. Multi-carrier modulation techniques can be categorized depending upon the arrangement of carrier signals, such as; phase disposition (PD), phase opposite disposition (POD), and alternate phase opposite disposition (APOD) strategy. PD-PWM technique is one of the most extensively used strategies among all the multi-carrier modulation techniques. Some PD-PWM triggered n-level CHB-MLI topologies were introduced in [8]-[11], to restrict the harmonic content of the output voltage waveform and to increase the efficiency of the inverter. Though the harmonic strategies adopted in [10]-[11] offers a lower percentage of total harmonic distortion (THD) in the output voltage of the inverter, it generates some low-frequency odd harmonic components in the waveform. Thus, a selective harmonic elimination PWM (SHE-PWM)-based optimization technique was introduced in [12], for mitigating the effects of the low-frequency harmonics by adjusting the variable modulation index (MI), but rapid changes in MI was found challenging due to fast switching response of the semiconductor switches. Hence, MI variation is found suitable only for a restricted value. The typical way of measuring the harmonic component of a signal is THD (%), by using mathematical calculation, e.g., Fourier expansion series. Though THD (%) plays a pivotal role in evaluating

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the harmonic content of a waveform, Holmes *et. al.* [13] explained the risk of using THD widely as a waveform quality indicator. It was observed that two completely different square waveform can result in identical THD (%), whereas the two similar waveforms can draw a different value of THD. Thus, a new waveform quality indicator i.e., weighted THD (WTHD) was introduced in [13]. The analytical calculation of WTHD for a three-level inverter is explained in [14], but the calculation does not fit for a higher-level output voltage.

A PD-PWM strategy-based three-phase NPC-MLI topology exhibits the following advantages over the other schemes:

1) The PD-PWM method is flexible to be adapted in different PWM techniques such as conventional sinusoidal PWM and SVPWM, etc.
2) It reduces the total number of clamping diodes; thus, the overall power rating is decreased.
3) Moreover, the PD-PWM based NPC topology presents an enhanced control strategy with higher switching frequency and higher efficiency for controlling the neutral point voltage than the conventional topology [15].

This paper provides a quantitative analysis of PD-PWM triggered three-phase five-level NPC-MLI performance using an FPGA-based small-scale experimental prototype. The primary focus is to decrease WTHD of the inverter output voltage by employing a harmonic mitigation algorithm. With the PD-PWM technique, NPC-MLI can achieve a high-frequency response than the conventional modulating techniques. The experimental results hold a close agreement with the theoretical analysis which validates the acceptability of PD-PWM technique.

The logic diagram of the PD-PWM pulse generation technique is demonstrated in Section II whereas; Section III elaborates the detailed harmonic mitigation algorithm for the reduction of WTHD in the inverter output waveform. Section IV and V represent the simulation and experimental results, respectively. Lastly, performance comparison amongst similar works is illustrated in Section VI followed by a conclusion in Section VII.

II. PD-PWM Control Technique

In the proposed PD-PWM pulse generation technique, an n number of carrier triangular signals is juxtaposed with a reference sinusoidal signal. The output pulses are thereby obtained to produce the respective n-level staircase output voltage waveform. The triangular signals are organized in such a way that, on the top of the zero reference termed as 'upper triangular' is denoted as; $T_{un} = \{T_{un}, T_{un}, T_{un}\}$ and the carriers below the zero reference called 'lower triangular' is denoted as $T_{ln} = \{T_{l1}, T_{l2}, T_{l3}\}$. The logic of the proposed PWM strategy is depicted in Fig. 2. If the amplitude of the upper carrier is lower than the reference sinusoidal signal, the comparator generates 'u_n' and generates '$(u_n - 1)$' if the condition is not satisfied. Similarly, for the lower carrier being lesser than the reference signal, the comparator generates '$-(l_n - 1)$' and generates '$-l_n$' if the condition is not fulfilled. The output waveform contains the same number of steps as of the aggregated signal. The gate pulses are further acquired by decoding the aggregated signal as per the switching sequence.

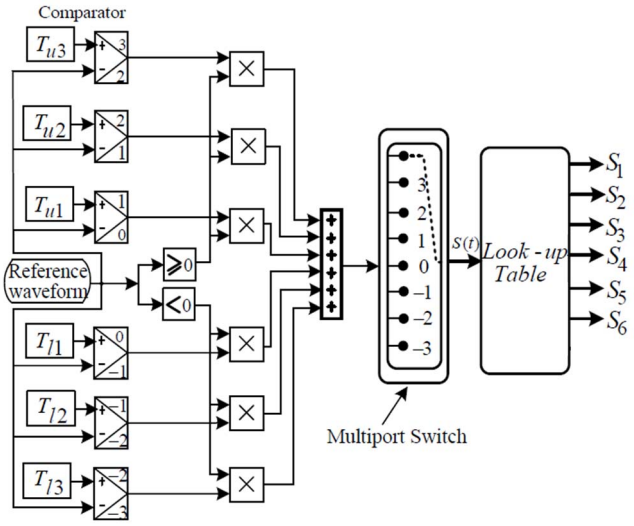


Fig. 2. Proposed PD-PWMcontrol strategy of the NPC-MLI topology.

Table I presents the switching state of the anticipated NPC-MLI, showing different states of operation with the associated voltage levels. As an example, to generate $+2V_{dc}$,power switches S_1 , S_2 , S_3 , S_4 ,and S_5 operates whereas;power switches S_1' , S_2' , S_3' , S_5' , S_6 and S_6' operates to generate $-2V_{dc}$. Similarly, the rest of the operating mode can be characterized by Fig. 2 and Table I.

TABLE I. SWITCHING STATES OF THENPC-MLI

States	Conducting Switches 1 = ON; 0 = OFF								Output phase voltage
	S_1	S_1'	S_2, S_4	S_2', S_4'	S_3, S_5	S_3', S_5'	S_6	S_6'	
1	1	0	1	0	1	0	0	0	$+2V_{dc}$
2	0	1	1	0	1	0	0	0	$+V_{dc}$
3	0	1	0	1	1	0	0	0	0
4	0	1	0	1	0	1	1	0	$-V_{dc}$
5	0	1	0	1	0	1	1	1	$-2V_{dc}$

III. Harmonic Mitigation Strategy

The switching angle placement of the proposed PD–PWM technique is depicted according to the multilevel waveform, shown in Fig. 3 [11]. It combines a set of nonlinear equations to derive the triggering angles $(\theta_l - \theta_k)$ of the PWM pulse-train. For a five-level inverter, only two switching angles are to be determined i.e., $(\theta_1 \text{and } \theta_2)$. The Fourier expanded series of the output voltage waveform can be formulated as below;

$$V_q = M_0 + \sum_{n=1}^{\infty} N_n \cos(k\theta + \emptyset_n) \quad (1)$$

$$\text{where, } N_n = \sqrt{X_n^2 + Y_n^2}, \text{ and} \quad (2)$$

$$\emptyset_n = \tan^{-1}\frac{Y_n}{X_n} \quad (3)$$

The generalized expressions of X_n, Y_n, and M_0 are written in (4)-(6).

$$N_0 = \frac{1}{2\pi}[\sum_{k=1}^{Q_1}(-1)^k \theta_k + \sum_{k=Q_1+1}^{Q_2}(-1)^{k-1} \theta_k + \cdots + \sum_{k=Q_5+1}^{Q_6}(-1)^k \theta_k] \quad (4)$$

$$X_n = \frac{1}{n\pi}[\sum_{k=1}^{Q_1}(-1)^k \sin n\theta_k + \sum_{k=Q_1+1}^{Q_2}(-1)^{k-1} \sin n\theta_k + \ldots + \sum_{k=Q_5+1}^{Q_6}(-1)^{k-1} \sin n\theta_k] \quad (5)$$

$$Y_n = \frac{1}{n\pi}[\sum_{k=1}^{Q_1}(-1)^k \cos n\theta_k + \sum_{k=Q_1+1}^{Q_2}(-1)^{k-1} \cos n\theta_k + \ldots + \sum_{k=Q_5+1}^{Q_6}(-1)^{k-1} \cos n\theta_k] \quad (6)$$

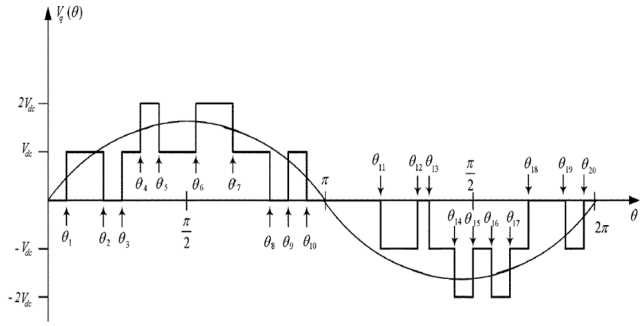


Fig. 3. Switching angle placement of the proposed PD–PWM technique.

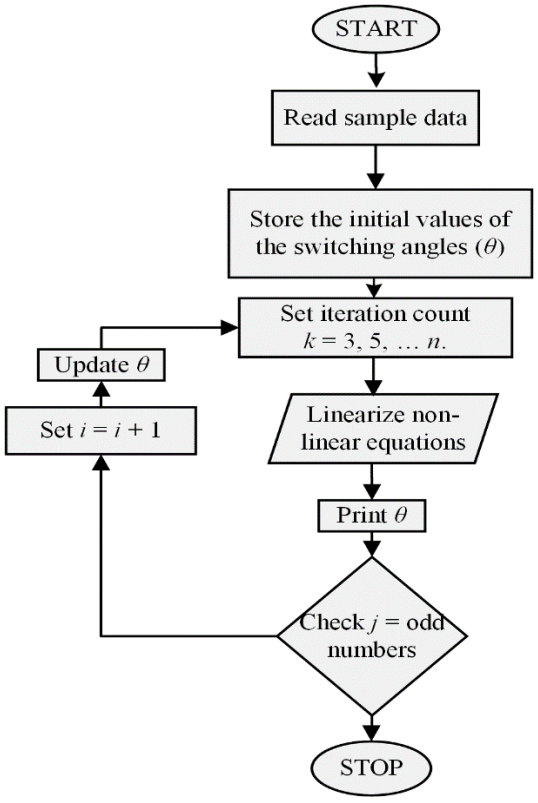


Fig. 4. Flow diagram of the harmonic mitigationstrategy.

Simplifying (1), (7) can be derived as,

$$V_q = \frac{4V_s}{\pi}\sum_n[\cos(k\theta_1) + \cos(k\theta_2)]\sin(k\omega t)/n \; k = 3, 5, 7, \ldots, n \quad (7)$$

where, $0 \leq \theta_1 \leq \theta_2 < \frac{\pi}{2}$.

In order to govern the exact switching angles, the following equations are to be resolved.

$$\cos(\theta_1) + \cos(\theta_2) - 2m = 0$$
$$\cos(k\theta_1) + \cos(k\theta_2) = 0 \quad (8)\ [9]$$

where, k^{th} order harmonic is to be eliminated and m is the experimental modulation index (MI).

By introducing a new function $E(\theta)$; (8) can be rewritten as below [10]; where $E = (E_1, E_2)$ and $\theta = (\theta_1, \theta_2)$arethe polynomial function.

$$E_1(\theta_1, \theta_2) = \cos(\theta_1) + \cos(\theta_2) - 2m$$
$$E_2(\theta_1, \theta_2) = \cos(k\theta_1) + \cos(k\theta_2) \quad (9)$$

In the above formulation of (8)-(9), k is replaced with $\{k = 3, 5, 7, \ldots n\}$ to eliminate the odd number of harmonics. These odd harmonics lead to the use of LC filter, which in turn increase the cost and capacity of the system. The number of triggering angles can be increased to reduce the percentage of harmonic content. The PD-PWM harmonic mitigation strategy is elaborated through a flow-chart and is presented in Fig. 4.

IV. Simulated Outcomes

MATLAB/SIMULINK software is chosen to simulate the phase voltage and load current profile of the projected three-phase NPC-MLI, in order to measure the efficacy of the projected PD-PWM technique. Table II summarizes the parameters used in the simulation model.

TABLE II. SIMULATIONPARAMETERS

DC voltage (V_{dc})	48 V
DC-link capacitors (C_{dc1}– C_{dc2})	100 µF
Modulation Index (m)	0.83
Switching frequency (f_{sw})	15 kHz
Sampling frequency (f_{sw})	4 MHz
Reference frequency (f_{ref})	50 Hz
Output Load ((R_l, L_l)	20 Ω, 100mH

To achieve the aggregated five-level voltage waveform, six carrier signals are contrasted with a reference sinusoidal signal at an MI of 0.83, as demonstrated in Fig. 5. The PD-PWM gate pulses (S_1-S_6) of the NPC-MLI topology are depicted in Fig. 6. The rest of the signals (S_1'-S_6') are designed in the complementary pattern of (S_1-S_6). The phase voltage and load current profile of the NPC-MLI topology has been presented in Fig 7(a) and 7(b), respectively.

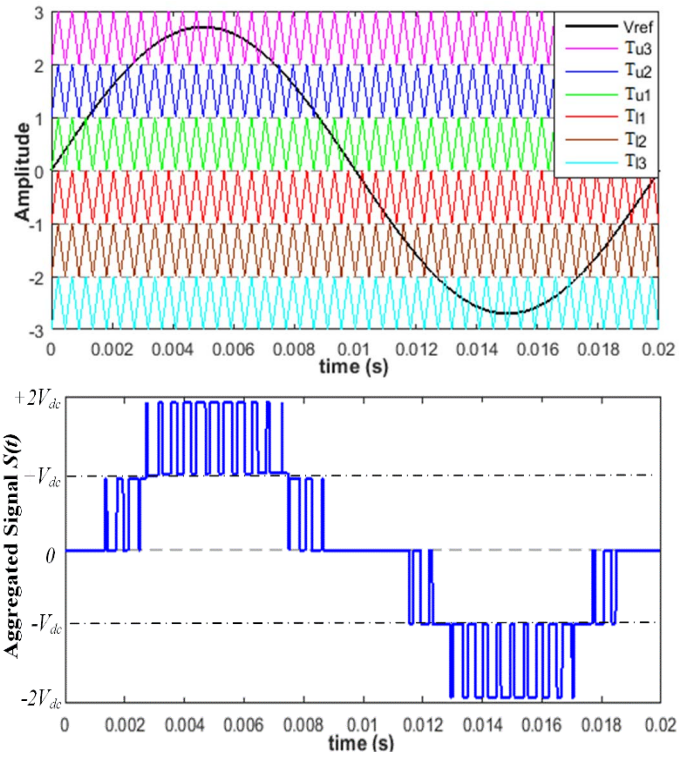


Fig. 5. Reference and carrier signal arrangement for the proposed PD-PWM switching technique and aggregated signal "$S(t)$".

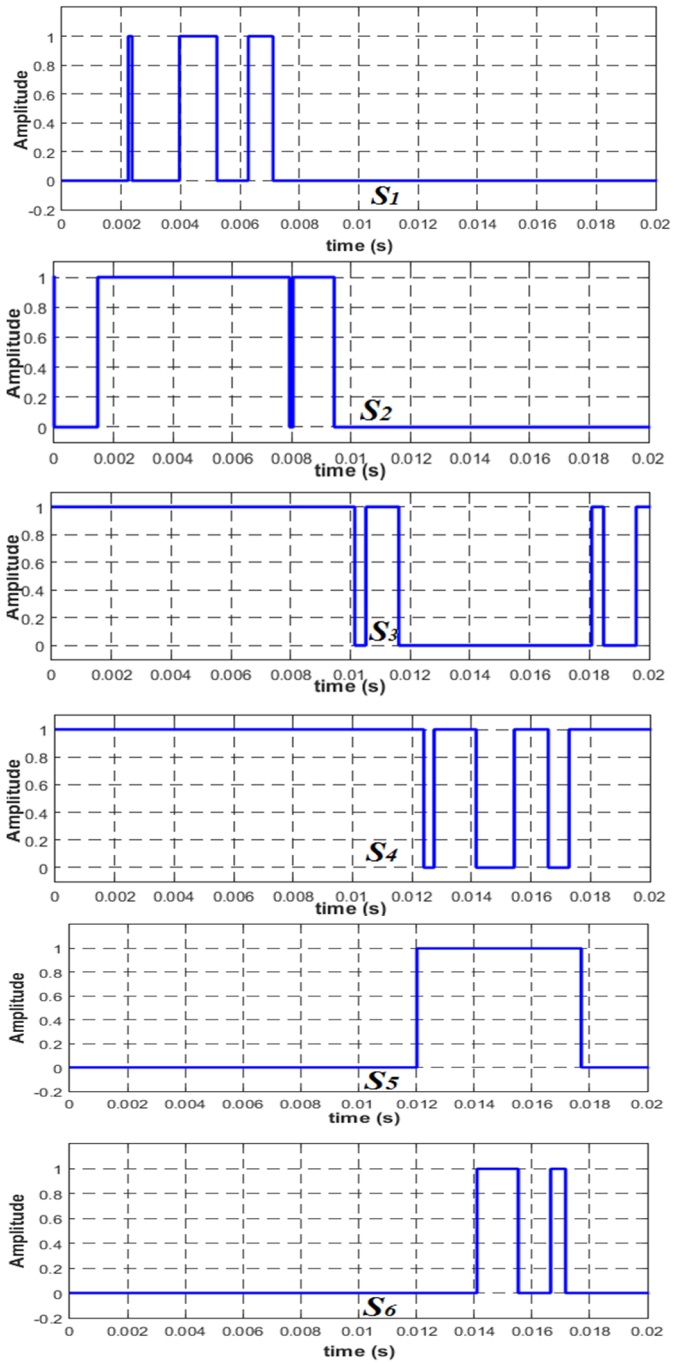
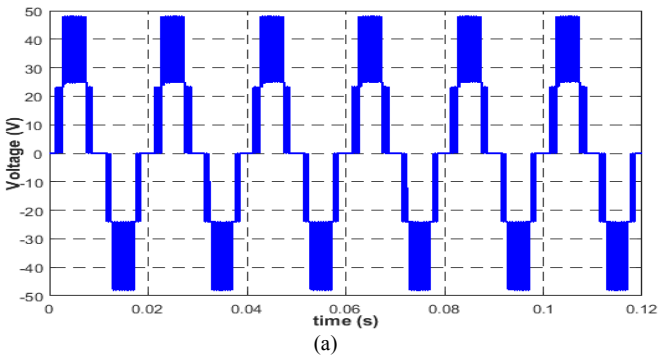
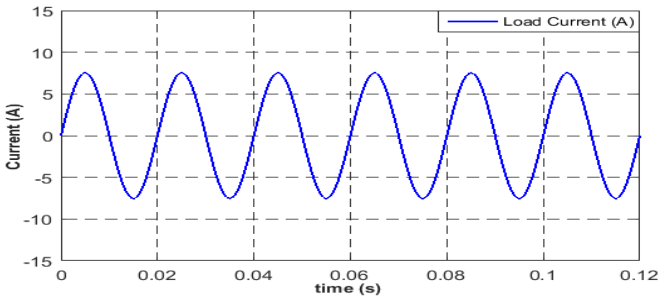


Fig. 6. PD-PWM switching pulses (S_1-S_6) for a three-phase NPC-MLI.



(a)



(b)

Fig. 7. Simulated output: (a) Phase voltage waveform, and (b) Load current of the PD-PWM based NPC-MLI at a f_{sw} = 15 kHzand m = 0.83.

V. Experimental Validation

An experimental prototype of a five-level NPC-MLI topology has been constructed to analyse the suitability of the proposed PD-PWM technique. The digital control algorithm has been developed within a VHDL-coded Vivado Design Suite software. A Spartan-6 FPGA development board has been utilized to synthesize the harmonic mitigation algorithm. All the experimental parameters are kept identical to the simulation parameters. Fig. 8 presents the inverter phase output voltages and load current under a resistive-inductive (R-L) load.

The experimental results for different modulator setting such as f_{sw}, f_s, m, V_{dc} are analysed and the results are in a close agreement with the simulated results; which verifies the adaptability of the proposed PD-PWM triggered NPC inverter in practical applications.

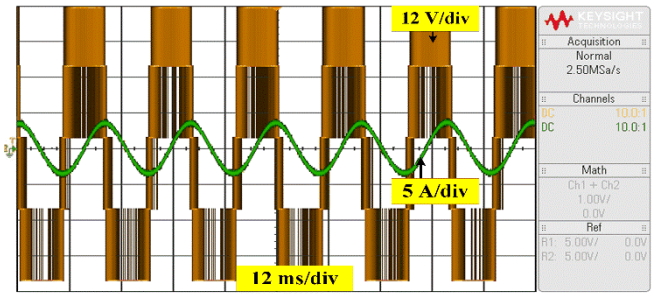


Fig. 8. Experimental output: (a) phase voltage waveform, and (b) associated load current of the proposed PWM based inverter at a f_{sw} = 15 kHz and m = 0.83 under R-L load of 20 Ω, 100 mH.

VI. Performance Evaluation

In order to quantify the pre-eminence of the projected PD-PWM technique, an inspection is performed in terms of WTHD, which is considered to be more precise than THD analysis, especially in industrial drive applications. Per unit WTHD is formulated as below;

$$WTHD_{p.u.} = \frac{\sqrt{\sum_{k=2}^{\infty}(\frac{V_k}{k})^2}}{V_1} \quad (10)$$

where V_1 and V_k are the rms value of the fundamental voltage (e.g., 50 Hz) and the k^{th} harmonic inverter output voltage. The third-order harmonics do not participate in line-to-line voltage of three-phase inverter, underbalanced condition. Thus, in order to exclude those harmonics, (10) is modified to achieve the minimal distorted output voltage. Fig. 9 port rays a quantitative comparative analysis of

$WTHD_{p.u}$ among the experimentally obtained PD-PWM and the earlier reported different PWM techniques at a variable MI and fixed f_{sw} = 15 kHz. It was observed that the experimental inverter voltage waveform with the proposed PD-PWM scheme offers the lowest WTHD deviation among all the similar PWM schemes.

Another investigation is conducted to testify the performance of the PD-PWM technique under a variable switching frequency (10 kHz – 1 MHz) at a constant MI, as depicted in Fig. 10. It was detected that the PD-PWM exhibits slightly higher WTHD value when compared to [4], at a lower range of f_{sw}. As the f_{sw} is higher, PD-PWM offers a less-distorted output voltage waveform than all the earlier-reported PWM techniques [4]-[5], which validates its adaptability in the industrial drive application.

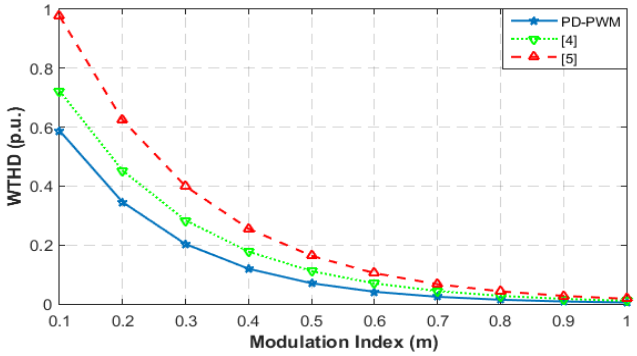


Fig. 9. WTHD comparison among the proposed PD-PWM technique and other earlier reported PWM techniquesata variable MI under a fixed f_{sw}= 15 kHz.

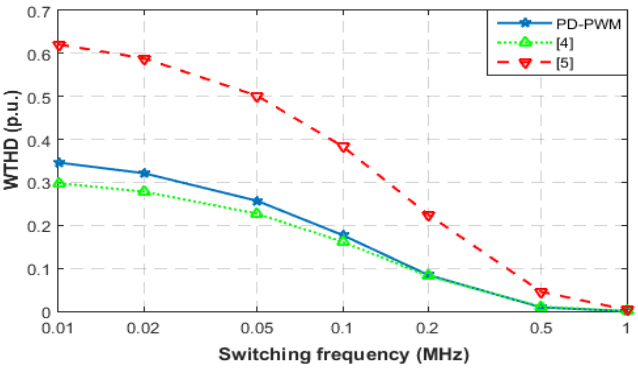


Fig. 10. WTHD comparison between PD-PWM technique and other earlier reported PWM techniques at a variable switching frequency undera fixed m= 0.83.

VII. Conclusion

Aiming to the reduction of WTHD for a five-level neutral-point clamped multilevel inverter, this work proposes a mathematically pre-formulated PD-PWM technique which reduces the odd harmonic content of the output voltage by employing a harmonic mitigation algorithm. The simulation and experimental results of the mathematically formulated switching angle-based PD-PWM algorithm testify that the proposed method exhibits the lowest WTHD content among all the earlier-proposed PWM schemes under study. Moreover, a comparative assessment is executed to validate the adaptability of the proposed work in fault tolerance application, where a tradeoff is concerned between reduced WTHD and higher switching frequency.

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