Phase Opposition Disposition PWM (POD-PWM) Strategy to Reduce WTHD Content from an NPC Inverter-Fed Electric Vehicle System

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***Abstract*—Neutral-point clamped Multilevel inverter (NPC-MLI) has transformed into a broadly accepted choice in the field of electric vehicle (EV) applications. In the traditional NPC-MLI-fed EV system, the problem regarding the higher harmonic content and the lower switching frequency still persists. In this paper, a phase opposition disposition pulse width modulation (POD-PWM) technique is proposed for a three-phase NPC-MLI, which is proficient in reducing the high-frequency weighted total harmonic distortion (WTHD) content of the inverter output voltage by employing a double Fourier integration-based harmonic mitigation algorithm. The experimental results of an FPGA-based NPC-MLI prototype hold a good resemblance with the theoretical analysis and simulated results. In addition, a comparative investigation affirms that the proposed strategy exhibits the highest efficiency and lowest WTHD content among all the previously-reported PWM schemes under study, which verifies the adaptability of the proposed work in electric vehicle applications.**

Keywords— POD-PWM, NPC-MLI, WTHD, Harmonics, Electric Vehicle (EV).

I. INTRODUCTION

Carbon dioxide emission from the vehicle has been a significant challenge to the green-energy climate. Electric vehicle (EV) offers an alternative option to improve the situation. Different nations e.g., Japan, China have already promoted the usage of EVs in metropolitan regions to reduce emission rates [1]. The two major control sources of EVs are IC engine with a battery cell and an electric motor-drive system. Such an EV system is demonstrated in Fig. 1, where the DC/AC converter performs a pivotal part in shaping the performance of the electric motor. The usage of an inverter is a critical step toward achieving the satisfactory performance of the electric motor [2]. The conventional EV inverter currently uses a DC-DC boost converter to upsurge the battery voltage so that the inverter can deliver higher power to the motor [3]. The inverter's salient property is to step down the voltage, which is a major challenge for most of the implementations as it generates low-frequency harmonics. Thus, the modulation schemes of the inverter in EV application needs to be designed and controlled in accordance with specific requirements of the EV drive [3]. Most of the EV system have been using multi-level inverter (MLI) topologies in recent years to minimize harmonic contents from the inverter output voltage waveform and to reduce the

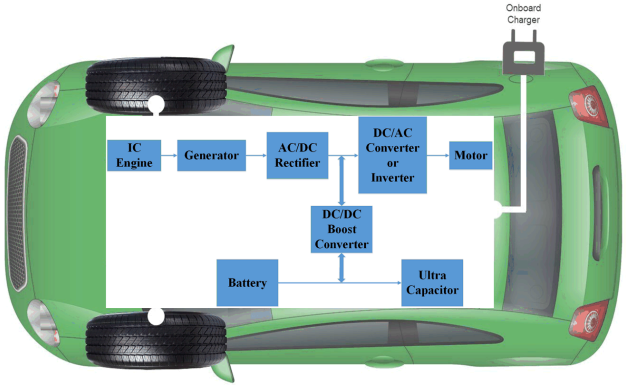


Fig. 1. Schematic diagram of an EV system.

production cost, as lower-rated components can be effectively used in the experimental prototype. The merits of the MLI include lower *dv/dt* stress, transient fault tolerance capability, and a higher level of voltage utilization. Based on their application specification, these MLIs can be further classified; i.e., Flying capacitors (FC) [4], Cascaded H-bridges (CHB) [5], and Neutral Point Clamped (NPC) [6].

Over the years, NPC inverter (see in Fig. 2) has become the most popular topology among the aforementioned categories, due to the following benefits, such as:

i. Semiconductor switching voltage becomes half of the dc-bus voltage.
ii. As the voltage levels (*n*) are higher, a lower percentage of harmonics are generated in the voltage waveform which reduces the size of the filter circuitry.

Several pulse width modulation (PWM) strategies have been adapted in the NPC topology [6]-[9] in order to obtain a multilevel (*n* level) output voltage. An improved space vector PWM (SVPWM) technique was reported to resolve the DC-link balancing problem of a three-level NPC-MLI [6]-[7]. A flexible control scheme was introduced in a three-phase Z-NPC inverter to replenish its non-linear characteristics [8]. An improved SVPWM method was adapted in a Z-source DC-link cascaded NPC inverter [9], to mitigate the common-mode voltage and leakage current problem of the grid-connected application, but the technique increases the complexity of the system. Based on the arrangement of the carrier signals, multi-level strategies can be broadly categorized i.e., phase disposition (PD), phase opposite

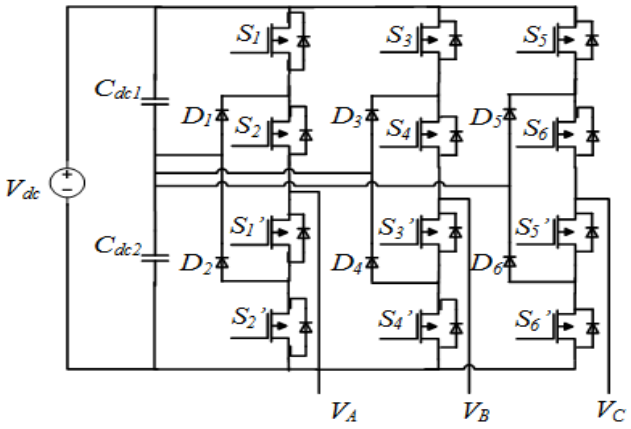


Fig. 2. Circuit layout of the NPC-MLI.

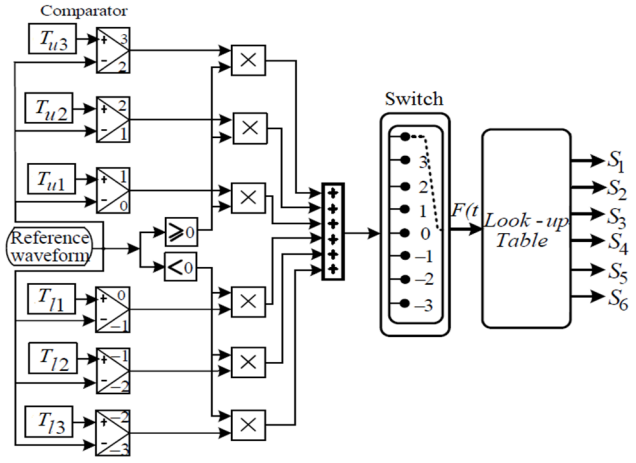


Fig. 3. Proposed POD-PWM control strategy of the NPC-MLI topology.

disposition (POD), and alternate phase opposite disposition (APOD) strategy. One of the most widely used strategies among all the multi-carrier modulation strategies is the POD-PWM technique. A POD-PWM modulated *n*-level NPC-MLI topology was proposed in [10]-[12], to limit the harmonic content of the output voltage waveform and to enhance the performance of the inverter. The POD-PWM method is flexible enough to be adapted in various PWM techniques such as conventional sinusoidal PWM and SVPWM, etc. In addition, the POD-PWM-based NPC topology presents an enhanced control strategy with higher switching frequency and greater efficiency for controlling the neutral point voltage than the conventional topology [10]. Fig. 2 presents the circuit layout of such an NPC inverter.

This paper provides a comprehensive analysis of a POD-PWM triggered three-phase NPC-MLI topology using an FPGA-based small-scale experimental prototype. The key focus is to reduce the total harmonic distortion (THD) and the weighted total harmonic distortion (WTHD) content from the inverter output voltage by employing a harmonic mitigation algorithm. Furthermore, with the proposed POD-PWM technique, NPC-MLI can achieve higher efficiency and high-frequency response than the conventional modulating techniques. The experimental results hold a close agreement with the theoretical and simulation results which testify the acceptability of the POD-PWM technique in the inverter-fed electric vehicle system.

The POD-PWM pulse generation strategy is illustrated in Section II whereas; Section III elaborates the detailed analysis of the harmonic mitigation algorithm from the inverter output voltage waveform. Section IV and V represent the simulation and experimental results, respectively. Lastly, performance comparison amongst the previously-reported similar works is performed in Section VI followed by a conclusion in Section VII.

II. POD-PWM Strategy

In the proposed POD-PWM pulse generation technique, an *n* number of carrier triangular signals is juxtaposed with a reference sinusoidal signal. The output pulses are thereby obtained to produce the respective *n*-level staircase output voltage waveform. The triangular signals are organized in such a way that, on the top of the zero reference termed as 'upper triangular' is denoted as; $T_{un} = \{T_{u1}, T_{u2}, T_{u3}\}$ and the carriers below the zero reference called 'lower triangular' is denoted as $T_{ln} = \{T_{l1}, T_{l2}, T_{l3}\}$. Fig. 3 explains the control logic schematic of the projected PWM scheme. If the magnitude of the upper carrier is lower than the reference sinusoidal signal, the comparator generates 'u_n' and generates '$(u_n - 1)$' if the condition is not satisfied. Similarly, for the lower carrier being lesser than the reference signal, the comparator generates '$-(l_n - 1)$' and generates '$-l_n$' if the condition is not fulfilled. The output waveform contains the same number of steps as of the aggregated signal. The gate pulses are further acquired by decoding the aggregated signal as per the switching sequence.

III. Harmonic Analysis of POD-PWM

The double Fourier integral calculation is selected to eliminate the odd harmonics of the proposed POD-PWM technique [12]. If *F (x, y)* is depicted as a controlled variable, the rest of the calculation can be explained as follows;

$$F(x,y) = \left[\frac{C_{00}}{2} + \sum_{q=1}^{\infty}\left(C_{q0}\cos qx + D_{q0}\sin qx\right) + \sum_{p=1}^{\infty}\left(C_{q0}\cos px + D_{p0}\sin px\right) + \sum_{p=1}^{\infty}\sum_{\substack{q=-\infty \\ q\neq 0}}^{\infty}\{C_{pq}\cos(px + qy) + D_{pq}\sin(px+qy)\}\right] \quad (1)$$

where, $C_{pq} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi} F(x,y)\cos(px+qy)dxdy$ (2)

and $D_{pq} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi} F(x,y)\,sin(px+qy)dxdy$ (3)

Eqn. (4)-(5) is used to determine the initial triangular carrier T_{ul}, and naturally sampled PWM output $V_{PWM\text{-}phase}$ is calculated as;

$$V_{PWM-phase} = \begin{bmatrix} \frac{E}{2} + \frac{Em}{2}\cos(\omega_s t) + \frac{2E}{\pi}\cos\ (\omega_s t)\sum_{p=1}^{\infty}\frac{1}{p}J_0\left(p\frac{\pi}{2}m\right) \\ \sin p\frac{\pi}{2}\cos(p\omega_c t) + \frac{2E}{\pi}\cos\ (\omega_s t)\sum_{p=1}^{\infty}\sum_{\substack{q=-\infty \\ q\neq 0}}^{\infty}\frac{1}{p}J_q\left(p\frac{\pi}{2}m\right) \\ (p\frac{\pi}{2}m)\sin\left\{(p+q)\frac{\pi}{2}\right\}\cos(p\omega_c t + q\omega_s t) \end{bmatrix} \quad (4)$$

$$-V_{PWM-phase} = \begin{bmatrix} \frac{E}{2} - \frac{Em}{2}\cos(\omega_s t) - \frac{2E}{\pi}\cos\ (\omega_s t) + \sum_{p=1,3,5}^{\infty}\frac{1}{p}J_0\left(p\frac{\pi}{2}m\right) \\ \sin p\frac{\pi}{2}\cos(p\omega_c t) + \frac{2E}{\pi}\cos\ (\omega_s t) + \sum_{p=2,4,6}^{\infty}\sum_{\substack{q=-\infty \\ q\neq 0}}^{\infty}\frac{1}{p}J_q\left(p\frac{\pi}{2}m\right) \\ (p\frac{\pi}{2}m)\sin\left\{(p+q)\frac{\pi}{2}\right\}\cos(p\omega_c t + q\omega_s t) \end{bmatrix} \quad (5)$$

where, m, J_n are the modulation index and n^{th} order Bessel function, respectively.

Finally, the phase output voltage ($V_{out\text{-}phase}$) is calculated as;

$$V_{out-phase} = V_{PWM-phase} - (-V_{PWM-phase}) \quad (6)$$

$$V_{out-phase} = \begin{bmatrix} E\cos\ (\omega_s t) + \frac{4E}{\pi}\sum_{p=2,4,6}^{\infty}\sum_{\substack{q=-\infty \\ q\neq 0}}^{\infty}\frac{1}{p}J_n \\ (p\frac{\pi}{2}m)\sin\left\{(p+q)\frac{\pi}{2}\right\}\cos(p\omega_c t + q\omega_s t) \end{bmatrix} \quad (7)$$

Eqn. (7) is simplified as follows;

$$V_{out-phase} = \begin{bmatrix} E\cos\ (\omega_s t) + \frac{4E}{\pi}\sum_{p=2,4,6}^{\infty}\sum_{q=\pm 1\pm 3\pm 5}^{\infty}\frac{1}{p}J_n \\ (p\frac{\pi}{2}m)\cos(p\omega_c t + q\omega_s t) \end{bmatrix} \quad (8)$$

The output voltage odd harmonics lead to the use of an LC filter, which in turn increase system volume and budget. From the theoretical calculation, it was determined that the odd carrier harmonics and sideband harmonics are completely mitigated from the proposed POD-PWM strategy, which satisfies the objective of this work. In addition, Fig. 4 demonstrates the harmonic mitigation property of POD-PWM.

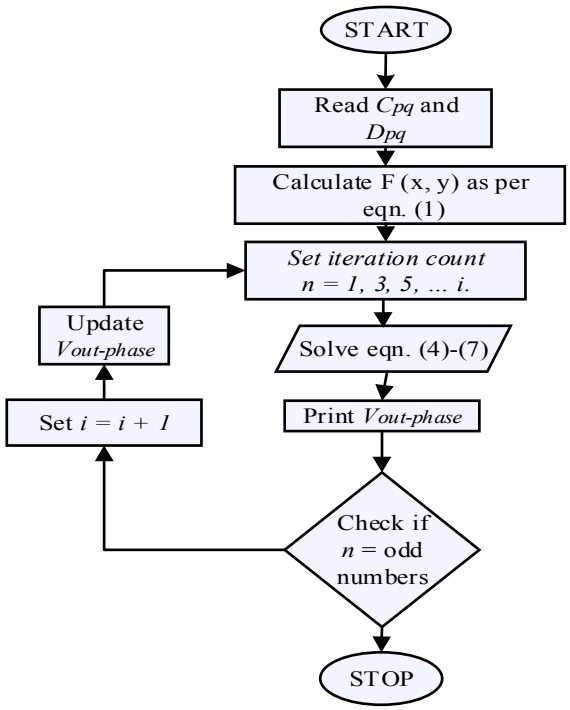


Fig. 4. Flow diagram of the harmonic mitigation strategy.

IV. Simulated Results

To calculate the efficacy of the projected POD-PWM technique, MATLAB/SIMULINK software is chosen to simulate the phase voltage and the load current profile of the projected three-phase NPC-MLI. Table I summarizes the technical parameters used in the simulation process.

TABLE I
SIMULATION PARAMETERS

DC voltage (V_{dc})	48 V
DC-link capacitors ($C_{dc1} - C_{dc2}$)	10 µF
Modulation Index (m)	0.85
Switching frequency (f_{sw})	20 kHz
Sampling frequency (f_s)	8 MHz
Reference frequency (f_{ref})	50 Hz
Output Load (R_l, L_l)	25 Ω, 110 mH

Six carrier signals are contrasted with a reference sinusoidal signal at a switching frequency of 20 kHz to attain the aggregated output voltage waveform, as shown in Fig. 5(a) and (b). The line-to-line voltage and load current profile with respective total harmonic distortion THD (%) of the conventional PWM modulated NPC-MLI has been shown in Fig 6(a) and (b), respectively; which is then compared with the proposed POD-PWM triggered line-to-line voltage and load current profile at Fig. 7(a) and (b). It was found that the projected modulation strategy exhibits a lower percentage of THD than that of the conventional modulation technique. Moreover, the POD-PWM offers a better load current waveform than the conventional PWM-based current waveform (see Fig. 7(a) and 6(a)), which validates the supremacy of the suggested modulation technique in terms of the EV system's power efficiency.

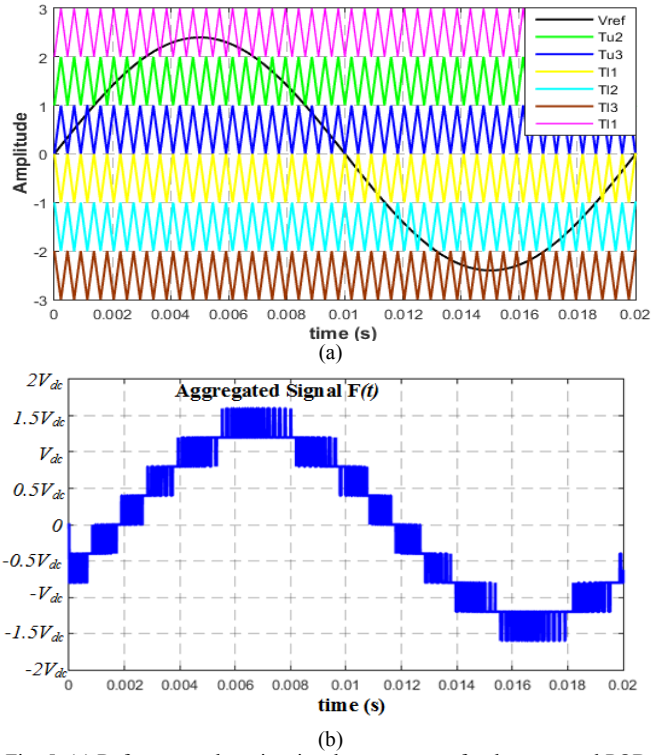
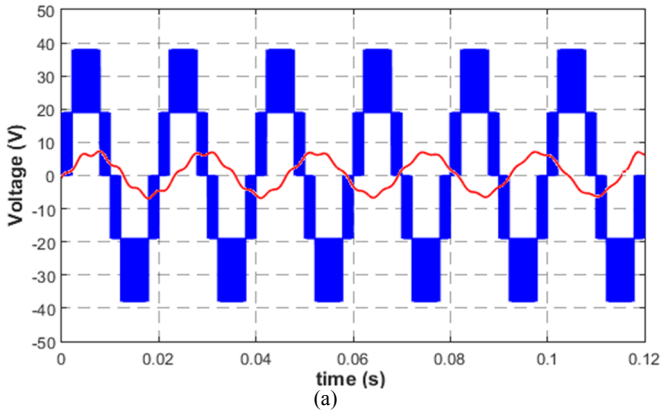
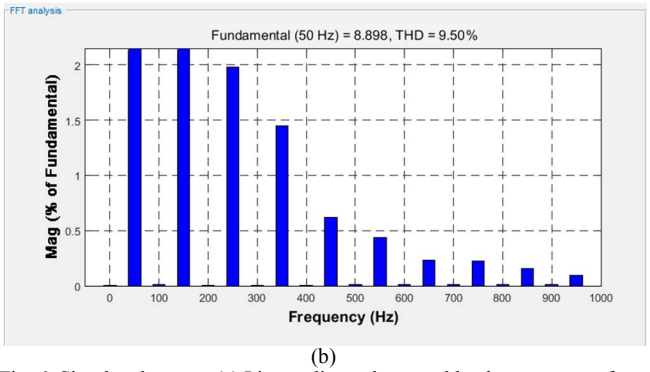


Fig. 5. (a) Reference and carrier signal arrangement for the proposed POD-PWM switching technique and (b) the aggregated signal "$F(t)$", at an MI of 0.85.

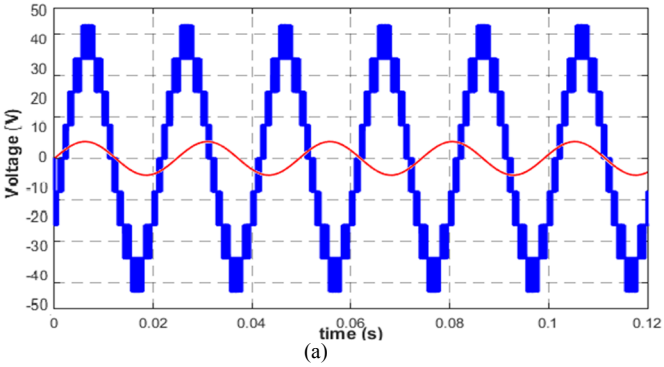


(a)

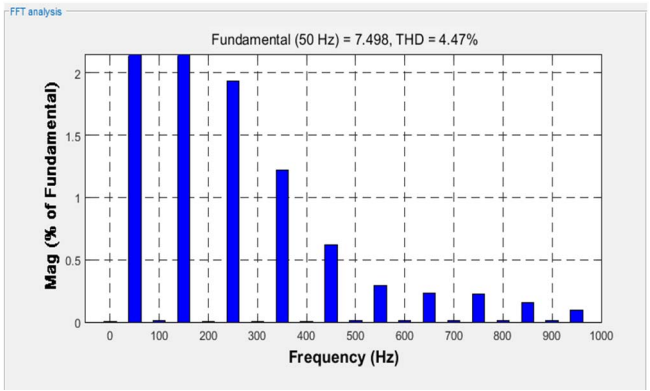


(b)

Fig. 6. Simulated output: (a) Line-to-line voltage and load current waveform of the conventional PWM based NPC-MLI, under f_{sw} = 20 kHz and m = 0.85, and (b) associated THD (9.50%) of the voltage waveform.

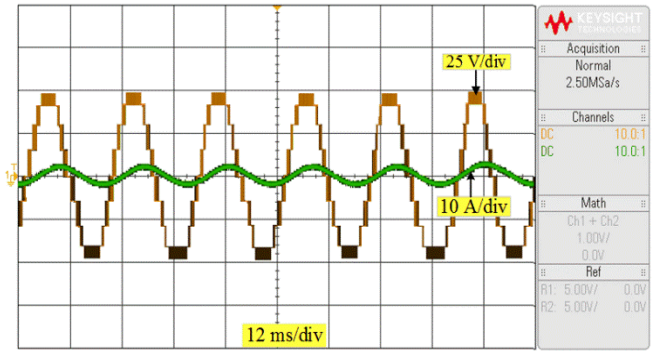


(a)

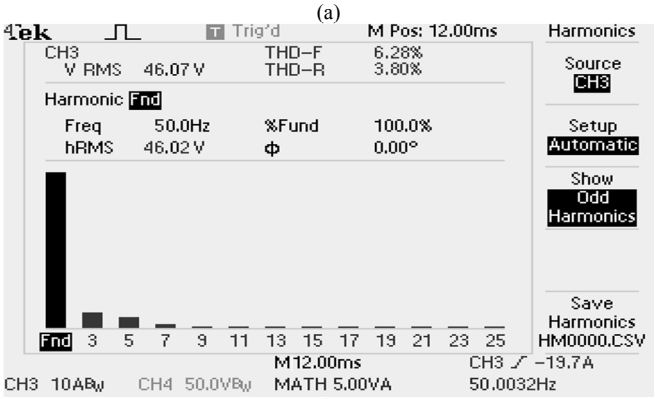


(b)

Fig. 7. Simulated output: (a) Line-to-line voltage and load current waveform of the proposed POD-PWM based NPC-MLI, under f_{sw} = 20 kHz and m = 0.85, and (b) associated THD (4.47%) of the voltage waveform.



(a)



(b)

Fig. 8. Experimental output: (a) Line-to-line voltage and load current waveform of the proposed POD-PWM triggered NPC-MLI, under f_{sw} = 20 kHz and m = 0.85, and (b) associated THD (6.28%) of the voltage waveform., under R-L load of 25 Ω, 110 mH.

V. Experimental Validation

An experimental model of an NPC-MLI topology was designed to demonstrate the appropriateness of the proposed POD-PWM strategy. The VHDL-coded control algorithm was developed within a Vivado Design Suite program. The harmonic mitigation algorithm was synthesized using a Spartan-6 FPGA development surface. All evaluation parameters are kept the same as the simulation. Fig. 8(a) presents the digital storage oscilloscope (DSO)-measured inverter phase output voltage and load current waveform under an R-L load bank, whereas the associated phase voltage THD (%) profile was assessed in a Tektronix Harmonic Analyser, as portrayed in Fig. 8(b).

The experimental results for different modulator setting such as f_{sw}, f_s, m, V_{dc} are analysed and the results show a good resemblance with the simulated results; which testifies the adaptability of the POD-PWM strategy in practical applications.

VI. Performance Evaluation

In order to evaluate the pre-eminence of the anticipated POD-PWM strategy, a weighted total harmonic distortion (WTHD) inspection is performed, which is recognized to be more accurate than the THD analysis, especially in the industrial drive applications. Per unit WTHD is expressed as shown below;

$$WTHD_{p.u.} = \frac{\sqrt{\sum_{n=2}^{\infty}(\frac{V_n}{n})^2}}{V_1} \quad (9)$$

where V_1 and V_n are the fundamental voltage (rms) and the n^{th} order inverter output voltage. Under the balanced condition, the 3rd order harmonics do not take part in line-to-line voltage of the three-phase inverter. Thus (9) is adapted to exclude those harmonics in imbalanced condition. Fig. 9 illustrates a comprehensive assessment of $WTHD_{p.u}$ among the experimentally obtained POD-PWM and the earlier reported different PWM techniques [6]-[7], at a fixed f_{sw} = 20 kHz under a variable MI. The experimental inverter voltage waveform with the proposed POD-PWM scheme was observed to offer the lowest WTHD deviation among all similar PWM schemes.

Another investigation is carried out to testify the performance of the POD-PWM strategy under a variable switching frequency (10 kHz – 1 MHz) at a constant MI, as depicted in Fig. 10. It was observed that at a lower range of f_{sw}, POD-PWM possesses a significantly higher WTHD value relative to [7]. Since the f_{sw} is higher, POD-PWM provides a less-distorted output voltage waveform than all the previously reported PWM techniques under review which validates its adaptability in the application of industrial drives.

A comparative efficiency curve is plotted in Fig. 11, as a function of the output power. The proposed POD-PWM triggered NPC-MLI exhibits a higher efficiency with a maximum value of 97.38%, higher than the conventional three-level inverter topology [6]. The greater efficiency in the projected inverter is due to lower harmonics and reduced EMI losses.

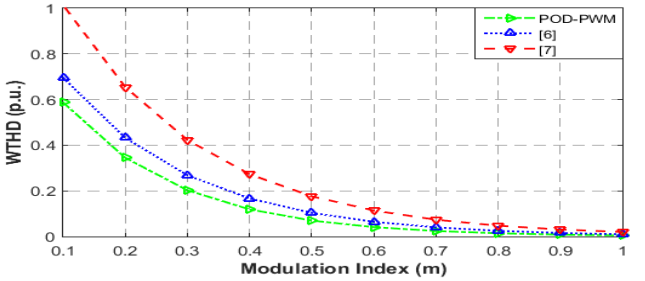


Fig. 9. Comparison of WTHD between POD-PWM and other previously reported PWM techniques under study at variable MI and fixed f_{sw} = 20 kHz.

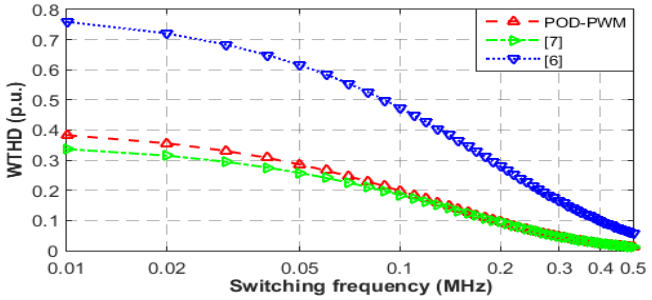


Fig. 10. Comparison of WTHD between POD-PWM and other earlier reported PWM techniques under review at a fixed m = 0.85 under a variable switching frequency.

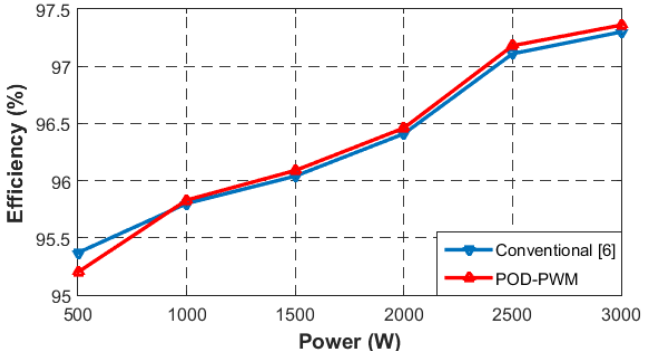


Fig. 11. Efficiency of the proposed POD-PWM modulated NPC inverter and conventional NPC inverter, with V_{dc} = 48 V at a switching frequency of 20 kHz.

VII. Conclusion

In order to minimize the THD and WTHD content of a neutral-point clamped multilevel inverter, a double Fourier transformation-based POD-PWM strategy is proposed in this work. The simulation and experimental results of the POD-PWM strategy testify that the projected method exhibits a higher level of output voltage and a lower percentage of THD content than that of the conventional PWM strategy. As the proposed control technique exhibits several benefits including reduced power loss, lower switching stress, and distortion less output voltage; the POD-PWM strategy can be effectively applied to the medium voltage applications such as electric vehicles (EVs), traction system, etc., under a high modulation index at a higher switching frequency.

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