Demo/Poster Abstract: Enabling Time-Critical Applications over Next-Generation 802.11 Networks

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***Abstract*—We present a demonstration of two end-to-end applications that illustrate the impact of latency on real-time operation. To enable low latency and high reliability we develop optimizations in both the MAC and PHY, including a time-aware scheduling scheme for medium access, and a low-latency FPGA baseband implementation for 802.11ax.**

***Index Terms*—Time-Sensitive Networking, time-critical wireless communications, Tactile Internet.**

I. Introduction

Time-critical applications require time-synchronized computing and deterministic communication between distributed components. Time-critical systems, such as industrial processes, may involve life-critical control tasks. Such tasks typically run over highly reliable and synchronous wired links (e.g., Deterministic Ethernet [1]) because existing wireless technologies, such as 802.11/Wi-Fi and Cellular Systems (e.g. 3G, 4G/LTE), have not yet demonstrated capabilities that guarantee low latencies (e.g., under 10 ms) and high reliability. Enabling reliable and deterministic low-latency wireless communication would lead to reduced wiring costs, greater deployment flexibility, and improved system mobility; these are key emerging application attributes in flexible manufacturing (Industry 4.0), wireless autonomous systems, and tactile teleoperation [2]. This demo intends to demonstrate the operation of time-critical applications over a time-sensitive wireless network. We have chosen two interactive systems that allow the audience to experience the impact that latency and reliability in wireless links have on latency sensitive applications. These applications are enabled by two main research thrusts: 1) a time-aware Wi-Fi protocol stack based on 802.11ac off-the-shelf radios, and 2) a new 802.11ax-based stack, optimized for low latency and implemented in a software-defined radio platform. The demonstrations provide a visual and interactive experience directly correlated to network latency and reliability.

II. Demonstrations

A. Synchronous Wireless Control of a 600 LED Array

The first demo consists of a 600 LED array where each LED is individually toggled over a wireless link in a synchronous pattern (Fig. 1). As each LED turns on/off, the audience can visualize the impact of latency and reliability on the lighting pattern. The AP generates a sequence of commands, where each command includes the address of an LED. The interval between two commands is constant and configurable. An actuator application running on the STA platform processes these commands, and toggles the LED that corresponds with the input LED address. A low-latency wireless link is deployed to close the loop between the AP and STA nodes. The wireless node implementations are described in Section 0. The controller and actuator are designed to operate over a link that tries to facilitate communication within a maximum latency bound. Both application endpoints are time-synchronized wirelessly, as described in Section III. If any data packet (command) that controls a LED is not delivered, or is delayed by more than the maximum allowed latency, the corresponding LED will not be toggled. As the LEDs turn on/off (or fail to do so), observers can visualize the packet loss and latency performance of the wireless link. Furthermore, by configuring the command interval and latency bound, it is possible to evaluate the limits of each wireless link in terms of low latency and reliability.

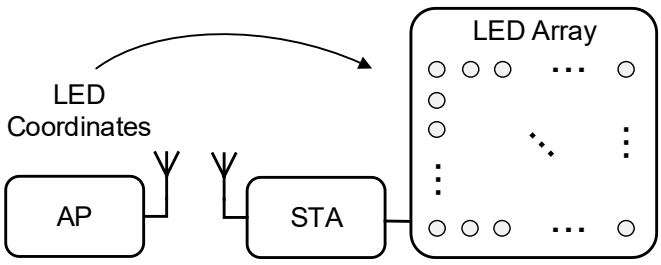

Fig. 1. *600 LED array demo. LED coordinates that arrive at the STA outside of a specified latency bound are discarded.*

B. Time-Critical Wireless Control System (Balance Board)

The second demo enables users to interact with a real kinematic control system (Fig. 2). The kinematic system comprises of 1) a ball and a balancing board controlled by x and y position servo-motors, and 2) a 2D resistive touch sensor [3]. The touch sensor provides 2D position feedback to a controller, which then drives the servo-motors accordingly. Different modes of operation and configuration parameters can be adjusted through a GUI. In the commercially available system [3], all communications are wired (over USB and Ethernet). In this demonstration, wired

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links are replaced with the experimental time-sensitive wireless links, as described in Section 0. A user control mode is enabled, so that the manual commands from a game-console controller are sent over a wireless link to drive the servo-motors. The latency and reliability have a direct impact on the user's ability to control the system. A large latency leads to excessive lag in response, resulting in degraded stability and user experience; an unreliable link causes commands to be dropped, leading to a similar result. As the radios operate in the unlicensed bands (2.4 and 5 GHz), the system will also be subject to interference from other devices. The latency performance is expected to vary with the amount of traffic in the channel. The operating channels may also be adjusted based on local channel activity to reduce interference from other Wi-Fi devices.

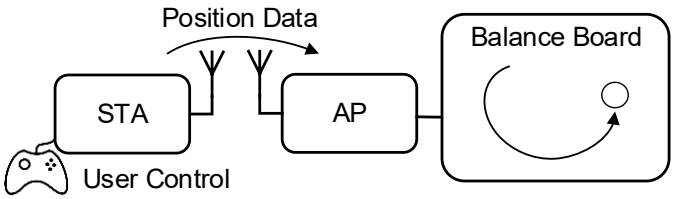

Fig. 2. *Balance board wireless control system demo. Excessive data-transfer latency leads to instability in the control system, or degraded user-experience.*

II. Wireless Time-Sensitive Networks

Next-generation wireless standards in both 3GPP (5G new radio) and IEEE (802.11ax and ay) have begun to consider deterministic low-latency requirements, in contrast to previous standards that primarily targeted throughput. This work focuses on the evolution of 802.11 and addresses new latency and reliability requirements. Two complementary research directions are considered. The first approach focuses on networking and medium-access enhancements, re-using standard 802.11ac radios. The second approach addresses PHY-level (baseband) challenges in the 802.11ax standard, which is still under development. In particular, the second approach relies on an FPGA-based implementation to enable both flexibility and deterministic computation. Both solutions assume a managed wireless network as an extension of a managed time-sensitive network (TSN) domain [1], where a central controller provides time-synchronization (e.g., based on IEEE 1588/PTP) and time-aware scheduling as defined in 802.1Qbv. This is a realistic assumption in many practical deployments, in particular for industrial and enterprise scenarios.

A. Time-Aware Wi-Fi Stack

The first research contribution leverages over-the-air time synchronization capabilities as defined in 802.1AS to enable TSN time-aware scheduling [4] in an 802.11 network. A time-aware stack is implemented to avoid channel access contention. Service periods (SP) are defined according to the required latency bound, and the number of devices that are allowed to access the channel. The number of allowed devices is managed to ensure that transmissions (including re-transmissions) are completed with very high probability within the latency bound. An access point (AP) is responsible for providing a common reference time, and for distributing the time-aware schedule with allocated SPs. The demo illustrates the tradeoffs between latency and reliability that can be achieved with an optimized time-aware stack and existing 802.11ac radios.

B. Low-Latency 802.11ax Stack

The second research contribution focuses on the implementation challenges associated with the next-generation 802.11ax standard, using an FPGA-accelerated radio platform to meet hard latency requirements. Among several new features, 802.11ax introduces an OFDMA-trigger based access mode, which enables the AP to better manage access to the channel, an important feature to guarantee low-latency and high reliability. A basic 802.11ax baseband experimental implementation (with select features) was developed on an Intel Arria 10 FPGA platform [5], and integrated with an off-the-shelf analog front end [6] (Fig. 3). Several optimizations were developed to enable low-latency operation, including a novel parallelization technique for binary convolutional codes, low-latency streaming Fourier transforms, and tightly-pipelined transmit and receive processing chains. The proposed demonstration provides an initial validation of 802.11ax features, as well as techniques to optimize latency in FPGA and ASIC-based implementations. Although the prototype can operate over the air, the demo will be done over a coaxial cable.

Fig. 3. *FPGA wireless research platform using off-the-shelf components.*

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