TEXAS INSTRUMENTS

TLV62569, TLV62569P

SLVSDG1 – DECEMBER 2016

# TLV62569 2-A High Efficiency Synchronous Buck Converter in SOT Package

## 1 Features

- Up to 95% Efficiency
- Low $R_{DS(ON)}$ Switches 100 mΩ / 60 mΩ
- 2.5-V to 5.5-V Input Voltage Range
- Adjustable Output Voltage from 0.6 V to $V_{IN}$
- Power Save Mode for Light Load Efficiency
- 100% Duty Cycle for Lowest Dropout
- 35-µA Operating Quiescent Current
- 1.5-MHz Typical Switching Frequency
- Power Good Output
- Over Current Protection
- Internal Soft Startup
- Thermal Shutdown Protection
- Available in SOT Package
- Pin-to-Pin Compatible with TLV62568

## 2 Applications

- General Purpose POL Supply
- Set Top Box
- Network Video Camera
- Wireless Router
- Hard Disk Driver

## 3 Description

The TLV62569 device is a synchronous step-down buck DC-DC converter optimized for high efficiency and compact solution size. The device integrates switches capable of delivering an output current up to 2 A.

At medium to heavy loads, the device operates in pulse width modulation (PWM) mode with 1.5-MHz switching frequency. At light load, the device automatically enters Power Save Mode (PSM) to maintain high efficiency over the entire load current range. In shutdown, the current consumption is reduced to less than 2 µA.

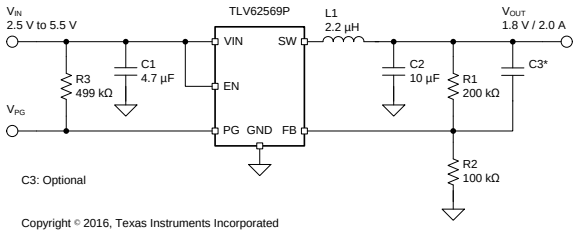
The TLV62569 provides an adjustable output voltage via an external resistor divider. An internal soft start circuit limits the inrush current during startup. Other features like over current protection, thermal shutdown protection and power good are built-in. The device is available in a SOT23 and SOT563 package.

**Device Information**(1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TLV62569 | SOT23 (5) | 2.90 mm × 2.80 mm |
| TLV62569P | SOT23 (6) | |
| TLV62569 | SOT563 (6) | 1.60 mm x 1.60 mm |
| TLV62569P | SOT563 (6) | |

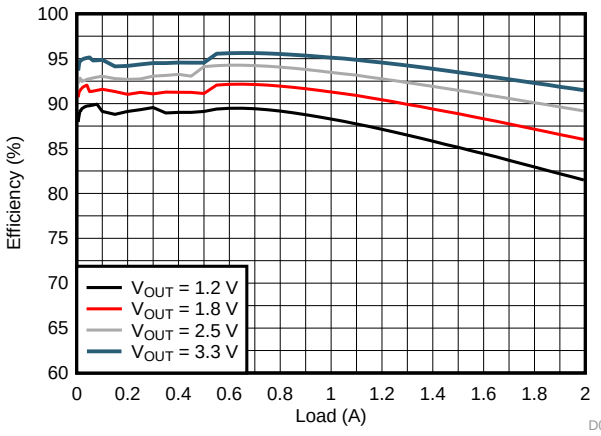
(1) For all available packages, see Mechanical, Packaging, and Orderable Information at the end of the datasheet.

## 4 Simplified Schematic






**Efficiency at 5-V Input Voltage**



# Table of Contents



## 5 Revision History

| DATE | REVISION | NOTES |
|---|---|---|
| December 2016 | * | Initial release. |

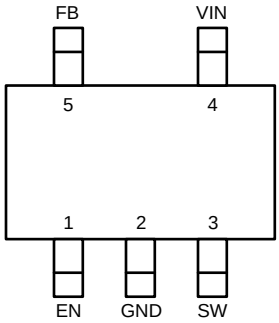
# 6 Device Options

| PART NUMBER (1) | FUNCTION | PACKAGE MARKING | PACKAGE |
|---|---|---|---|
| TLV62569DBV | - | 16AF | SOT23-5 |
| TLV62569PDDC (2) | Power Good | | SOT23-6 |
| TLV62569DRL (2) | - | | SOT563-6 |
| TLV62569PDRL (2) | Power Good | | SOT563-6 |

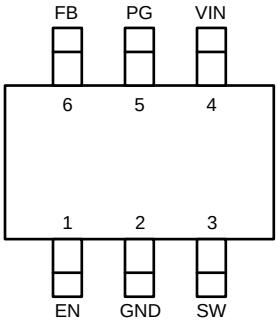
(1) For detailed ordering information, please check *Mechanical, Packaging, and Orderable Information* at the end of this datasheet.
(2) Product preview

# 7 Pin Configuration and Functions

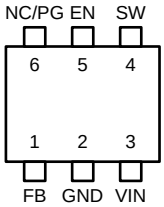
SOT23-5
DBV Package
(Top View)




SOT23-6
DDC Package
(Top View)




SOT563-6
DRL Package
(Top View)




**Pin Functions**

| PIN NUMBER | | | | I/O/PWR | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | SOT23-5 | SOT23-6 | SOT563-6 | | |
| EN | 1 | 1 | 5 | I | Device enable logic input. Logic high enables the device, logic low disables the device and turns it into shutdown. Do not leave floating. |
| GND | 2 | 2 | 2 | PWR | Ground pin. |
| SW | 3 | 3 | 4 | PWR | Switch pin connected to the internal FET switches and inductor terminal. Connect the inductor of the output filter to this pin. |
| VIN | 4 | 4 | 3 | PWR | Power supply voltage input. |
| PG | - | 5 | 6 | O | Power good open drain output pin for TLV62569P. The pull-up resistor should not be connected to any voltage higher than 5.5V. If it's not used, leave the pin floating. |
| FB | 5 | 6 | 1 | I | Feedback pin for the internal control loop. Connect this pin to an external feedback divider. |
| NC | - | - | 6 | O | No connection pin for TLV62569DRL. The pin can be connected to the output or the ground. Or leave it floating. |

# 8 Specifications

## 8.1 Absolute Maximum Ratings

Over operating temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage(2) | VIN, EN, PG | –0.3 | 6 | V |
| | SW (DC) | –0.3 | $V_{IN}$+0.3 | V |
| | SW (AC, less than 10ns)(3) | –3.0 | 9 | V |
| | FB | –0.3 | 5.5 | V |
| Operating junction temperature, $T_J$ | | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and the device is not switching. Functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Normal switching operation

## 8.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±500 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 8.3 Recommended Operating Conditions(1)

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage | 2.5 | | 5.5 | V |
| $V_{OUT}$ | Output voltage | 0.6 | | $V_{IN}$ | V |
| $I_{OUT}$ | Output current | 0 | | 2 | A |
| $T_J$ | Operating junction temperature | –40 | | 125 | °C |
| $I_{SINK\_PG}$ | Sink current at PG pin | | | 1 | mA |

(1) Refer to the *Application and Implementation* section for further information.

## 8.4 Thermal Information

| THERMAL METRIC(1) | | TLV62569 DBV (5 Pins) | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 188.2 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 137.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 41.2 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 31.4 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 40.6 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 8.5 Electrical Characteristics

$V_{IN}$ = 5.0 V, $T_J$ = 25°C, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY** | | | | | | |
| $I_Q$ | Quiescent current into VIN pin | Not switching | | 35 | | uA |
| $I_{SD}$ | Shutdown current into VIN pin | EN = 0 V | | 0.1 | 2 | µA |
| $V_{UVLO}$ | Under voltage lock out | $V_{IN}$ falling | | 2.3 | 2.45 | V |
| | Under voltage lock out hysteresis | | | 100 | | mV |
| $T_{JSD}$ | Thermal shutdown | Junction temperature rising | | 150 | | °C |
| | | Junction temperature falling | | 130 | | |
| **LOGIC INTERFACE** | | | | | | |
| $V_{IH}$ | High-level input voltage at EN pin | 2.5 V ≤ $V_{IN}$ ≤ 5.5 V | 1.2 | 0.95 | | V |
| $V_{IL}$ | Low-level input voltage at EN pin | 2.5 V ≤ $V_{IN}$ ≤ 5.5 V | | 0.85 | 0.4 | V |
| $t_{SS}$ | Soft startup time | | | 800 | | µs |
| $V_{PG}$ | Power good threshold | $V_{FB}$ rising, referenced to $V_{FB}$ nominal | | 95% | | |
| | | $V_{FB}$ falling, referenced to $V_{FB}$ nominal | | 90% | | |
| $V_{PG,OL}$ | Power good low-level output voltage | $I_{SINK}$ = 1 mA | | | 0.4 | V |
| $I_{PG,LKG}$ | Input leakage current into PG pin | $V_{PG}$ = 5.0 V | | 0.01 | | µA |
| $t_{PG,DLY}$ | Power good delay time | $V_{FB}$ falling | | 40 | | µs |
| **OUTPUT** | | | | | | |
| $V_{FB}$ | Feedback regulation voltage | | 0.588 | 0.6 | 0.612 | V |
| $R_{DS(on)}$ | High-side FET on resistance | | | 100 | | mΩ |
| | Low-side FET on resistance | | | 60 | | |
| $I_{LIM}$ | High-side FET current limit | | 3 | | | A |
| $f_{SW}$ | Switching frequency | $V_{OUT}$ = 2.5 V | | 1.5 | | MHz |

## 8.6 Typical Characteristics

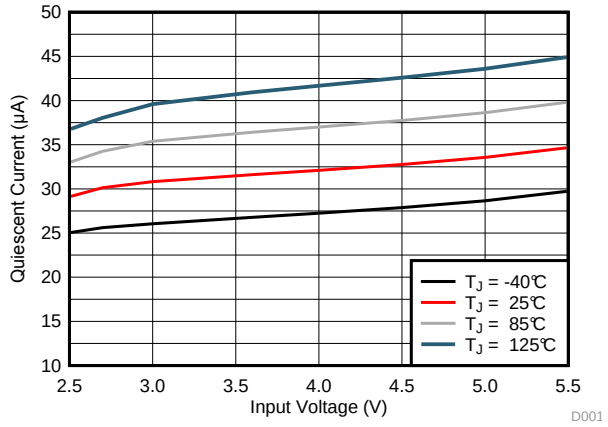



**Figure 1. Quiescent Current vs Input Voltage**

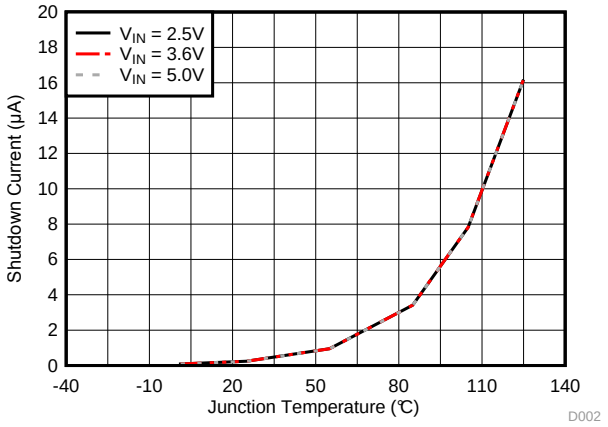



**Figure 2. Shutdown Current vs Junction Temperature**

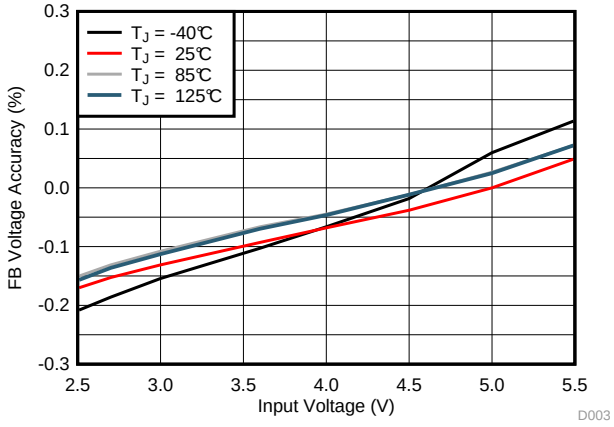



**Figure 3. FB Voltage Accuracy**

# 9 Detailed Description

## 9.1 Overview

The TLV62569 is a high-efficiency synchronous step-down converter. The device operates with an adaptive off time with peak current control scheme. The device operates at typically 1.5-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. Based on the $V_{IN}/V_{OUT}$ ratio, a simple circuit sets the required off time for the low-side MOSFET. It makes the switching frequency relatively constant regardless of the variation of input voltage, output voltage, and load current.

## 9.2 Functional Block Diagrams

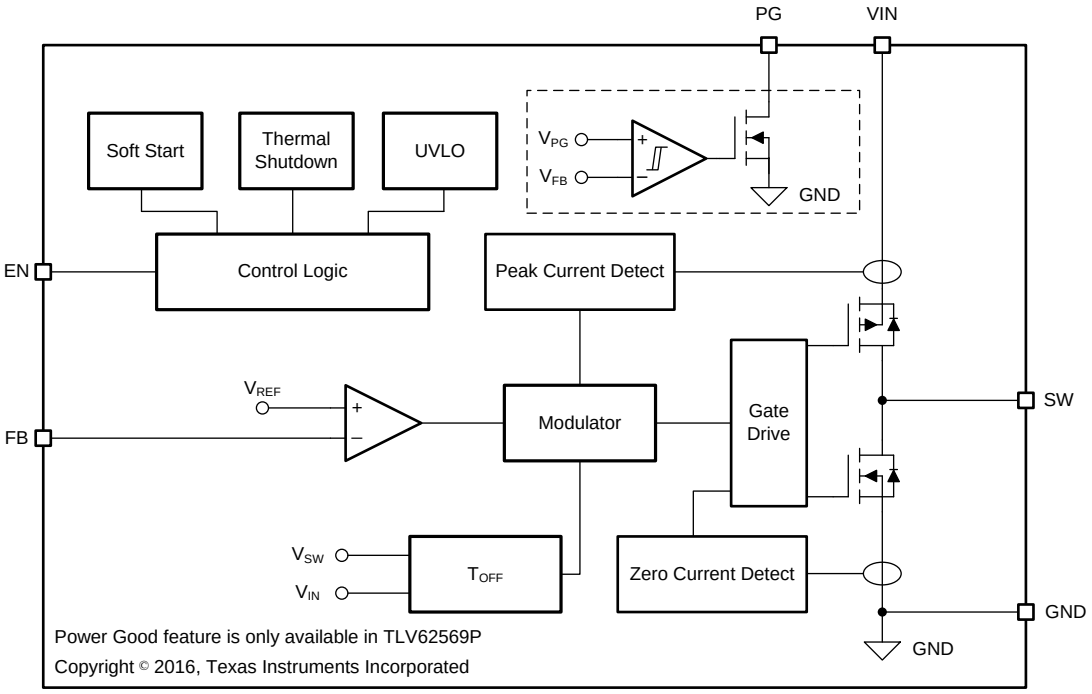



**Figure 4. TLV62569 Functional Block Diagram**

## 9.3 Feature Description

### 9.3.1 Power Save Mode

The device automatically enters Power Save Mode to improve efficiency at light load when the inductor current becomes discontinuous. In Power Save Mode, the converter reduces switching frequency and minimizes current consumption. In Power Save Mode, the output voltage rises slightly above the nominal output voltage. This effect is minimized by increasing the output capacitor.

### 9.3.2 100% Duty Cycle Low Dropout Operation

The device offers a low input-to-output voltage differential by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. The minimum input voltage to maintain output regulation, depending on the load current and output voltage, is calculated as:

$$V_{IN(MIN)} = V_{OUT} + I_{OUT} \times (R_{DS(ON)} + R_L) \quad (1)$$

where

- $R_{DS(ON)}$ = High side FET on-resistance
- $R_L$ = Inductor ohmic resistance (DCR)

## Feature Description (continued)

### 9.3.3 Soft Startup

After enabling the device, internal soft startup circuitry ramps up the output voltage which reaches nominal output voltage during a startup time. This avoids excessive inrush current and creates a smooth output voltage rise slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

The TLV62569 is able to start into a pre-biased output capacitor. The converter starts with the applied bias voltage and ramps the output voltage to its nominal value.

### 9.3.4 Switch Current Limit

The switch current limit prevents the device from high inductor current and drawing excessive current from a battery or input voltage rail. Excessive current might occur with a heavy load or shorted output circuit condition. The TLV62569 adopts the peak current control by sensing the current of the high-side switch. Once the high-side switch current limit is reached, the high-side switch is turned off and low-side switch is turned on to ramp down the inductor current with an adaptive off-time.

### 9.3.5 Under Voltage Lockout

To avoid mis-operation of the device at low input voltages, under voltage lockout is implemented that shuts down the device at voltages lower than $V_{UVLO}$ with $V_{HYS\_UVLO}$ hysteresis.

### 9.3.6 Thermal Shutdown

The device enters thermal shutdown once the junction temperature exceeds the thermal shutdown rising threshold, $T_{JSD}$. Once the junction temperature falls below the falling threshold, the device returns to normal operation automatically.

## 9.4 Device Functional Modes

### 9.4.1 Enabling/Disabling the Device

The device is enabled by setting the EN input to a logic High. Accordingly, a logic Low disables the device. If the device is enabled, the internal power stage starts switching and regulates the output voltage to the set point voltage. The EN input must be terminated and should not be left floating.

### 9.4.2 Power Good

The TLV62569P has a power good output. The PG pin goes high impedance once the output is above 95% of the nominal voltage, and is driven low once the output voltage falls below typically 90% of the nominal voltage. The PG pin is an open-drain output and is specified to sink up to 1 mA. The power good output requires a pull-up resistor connecting to any voltage rail less than 5.5 V. The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used.

**Table 1. PG Pin Logic**

| DEVICE CONDITIONS | | LOGIC STATUS | |
|---|---|---|---|
| | | HIGH Z | LOW |
| Enable | EN = High, $V_{FB} \geq V_{PG}$ | √ | |
| | EN = High, $V_{FB} \leq V_{PG}$ | | √ |
| Shutdown | EN = Low | | √ |
| Thermal Shutdown | $T_J > T_{JSD}$ | | √ |
| UVLO | $1.4\ V < V_{IN} < V_{UVLO}$ | | √ |
| Power Supply Removal | $V_{IN} \leq 1.4\ V$ | √ | |

# 10 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 10.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

## 10.2 Typical Application

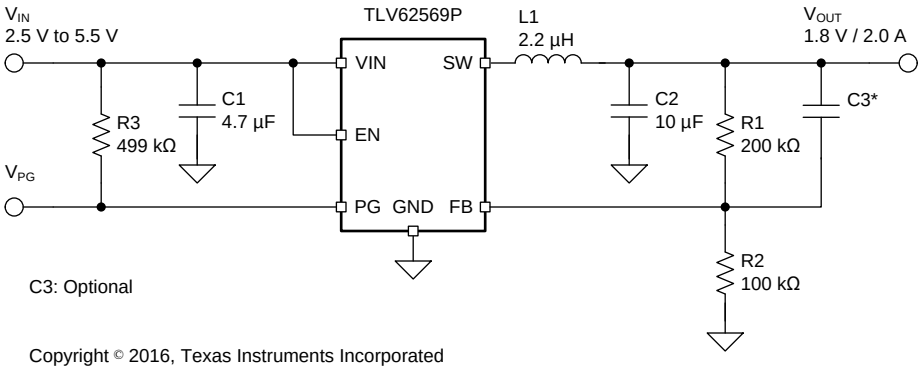



**Figure 5. TLV62569 1.8-V Output Application**

### 10.2.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

**Table 2. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Input voltage | 2.5 V to 5.5 V |
| Output voltage | 1.8 V |
| Maximum output current | 2.0 A |

Table 3 lists the components used for the example.

**Table 3. List of Components**

| REFERENCE | DESCRIPTION | MANUFACTURER(1) |
|---|---|---|
| C1 | 4.7 µF, Ceramic Capacitor, 10 V, X7R, size 0805, GRM21BR71A475KA73L | Murata |
| C2 | 10 µF, Ceramic Capacitor, 10 V, X7R, size 0805, GRM21BR71A106KE51L | Murata |
| L1 | 2.2 µH, Power Inductor, size 4mmx4mm, XAL4020-222ME | Coilcraft |
| R1,R2,R3 | Chip resistor,1%,size 0603 | Std. |
| C3 | Optional, 6.8 pF if it is needed | Std. |

(1) See *Third-party Products Disclaimer*

### 10.2.2 Detailed Design Procedure

#### *10.2.2.1 Setting the Output Voltage*

An external resistor divider is used to set output voltage according to Equation 2.

When sizing R2, in order to achieve low current consumption and acceptable noise sensitivity, use a maximum of 200 kΩ for R2. Larger currents through R2 improve noise sensitivity and output voltage accuracy but increase current consumption.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.6V \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

A feed forward capacitor, C3 improves the loop bandwidth to make a fast transient response (shown in Figure 19). 6.8-pF capacitance is recommended for R2 of 100-kΩ resistance. A more detailed discussion on the optimization for stability vs. transient response can be found in SLVA289.

#### 10.2.2.2 Output Filter Design

The inductor and output capacitor together provide a low-pass filter. To simplify this process, Table 4 outlines possible inductor and capacitor value combinations. Checked cells represent combinations that are proven for stability by simulation and lab test. Further combinations should be checked for each individual application.

**Table 4. Matrix of Output Capacitor and Inductor Combinations**

| $V_{OUT}$ [V] | L [µH](1) | $C_{OUT}$ [µF](2) | | | | |
|---|---|---|---|---|---|---|
| | | 4.7 | 10 | 22 | 2 x 22 | 100 |
| 0.6 ≤ $V_{OUT}$ < 1.2 | 1 | | | | + | |
| | 2.2 | | | | ++(3) | |
| 1.2 ≤ $V_{OUT}$ < 1.8 | 1 | | | + | + | |
| | 2.2 | | | ++(3) | + | |
| 1.8 ≤ $V_{OUT}$ | 1 | | + | + | + | |
| | 2.2 | | ++(3) | + | + | |

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and -30%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by +20% and -50%.
(3) This LC combination is the standard value and recommended for most applications.

#### 10.2.2.3 Inductor Selection

The main parameters for inductor selection is inductor value and then saturation current of the inductor. To calculate the maximum inductor current under static load conditions, Equation 3 is given:

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}}$$

where:

- $I_{OUT,MAX}$ is the maximum output current
- $\Delta I_L$ is the inductor current ripple
- $f_{SW}$ is the switching frequency
- L is the inductor value

(3)

It is recommended to choose a saturation current for the inductor that is approximately 20% to 30% higher than $I_{L,MAX}$. In addition, DC resistance and size should also be taken into account when selecting an appropriate inductor.

#### 10.2.2.4 Input and Output Capacitor Selection

The architecture of the TLV62569 allows use of tiny ceramic-type output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are thus recommended. To keep its resistance up to high frequencies and to achieve narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectric.

The input capacitor is the low impedance energy source for the converter that helps provide stable operation. A low ESR multilayer ceramic capacitor is recommended for best filtering. For most applications, 4.7-µF input capacitance is sufficient; a larger value reduces input voltage ripple.

The TLV62569 is designed to operate with an output capacitor of 10 µF to 47 µF, as outlined in Table 4.

### 10.2.3 Application Performance Curves

$V_{IN}$ = 5 V, $V_{OUT}$ = 1.8 V, L = 2.2 µH, $T_A$ = 25 °C, unless otherwise noted.

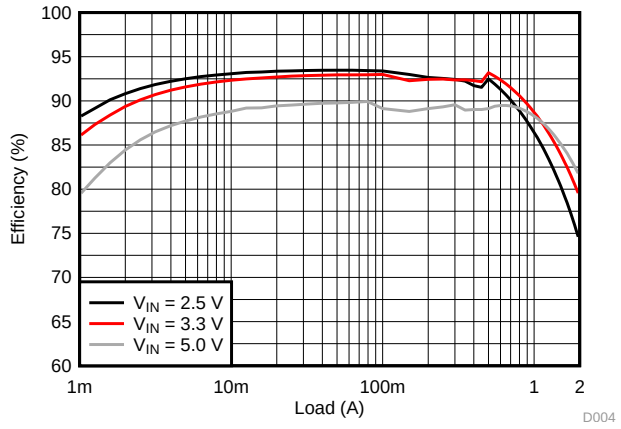



**Figure 6. 1.2-V Output Efficiency**

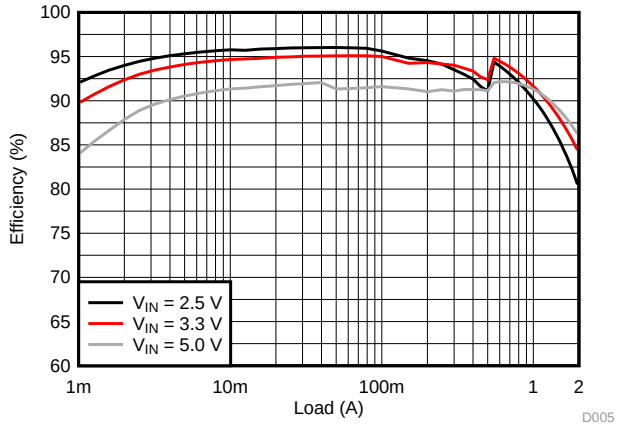



**Figure 7. 1.8-V Output Efficiency**

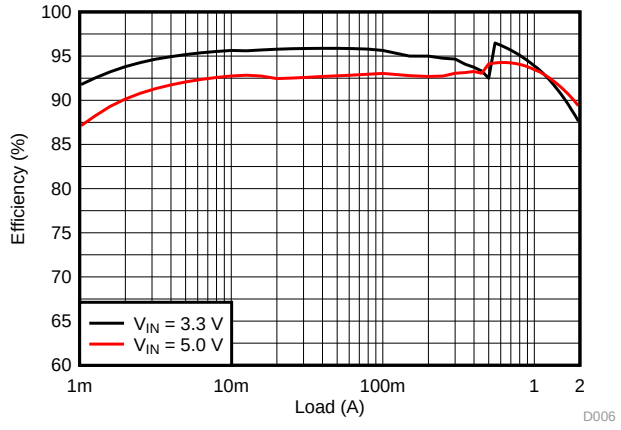



**Figure 8. 2.5-V Output Efficiency**

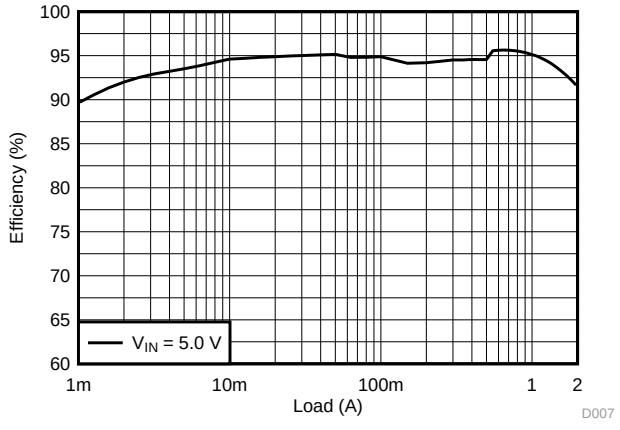
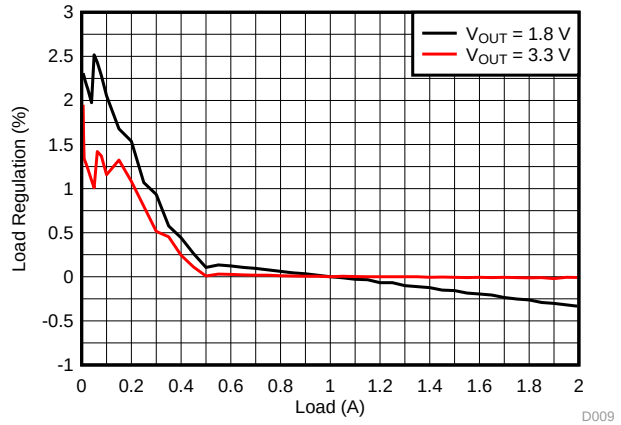
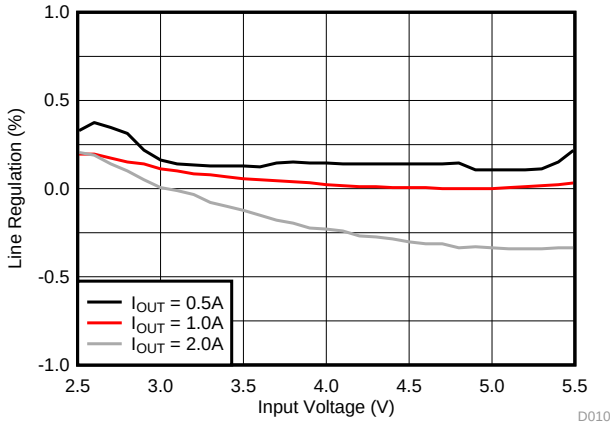



**Figure 9. 3.3-V Output Efficiency**



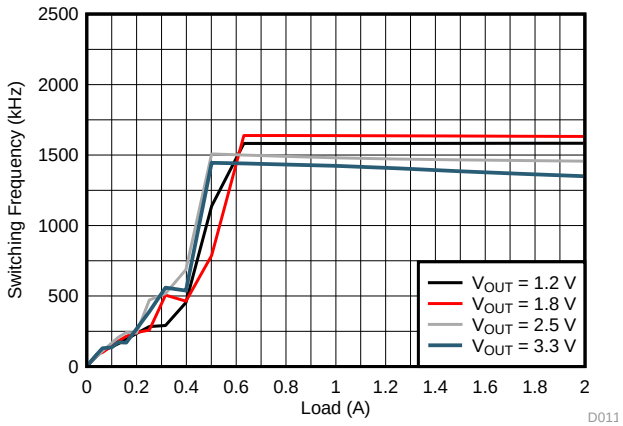

$V_{IN}$ = 5 V

**Figure 10. Load Regulation**



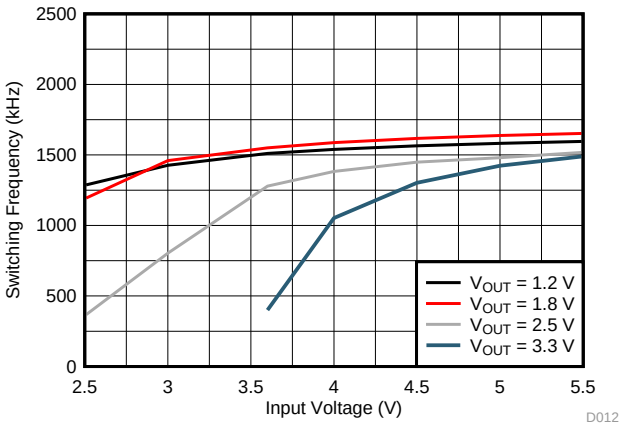

$V_{OUT}$ = 1.8 V

**Figure 11. Line Regulation**



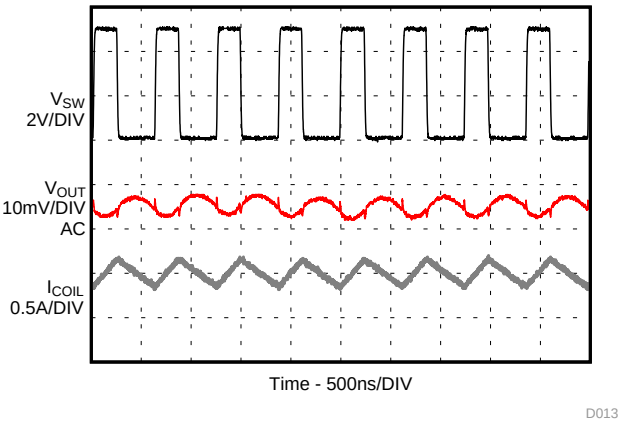

$V_{IN}$ = 5 V

**Figure 12. Switching Frequency vs Load**



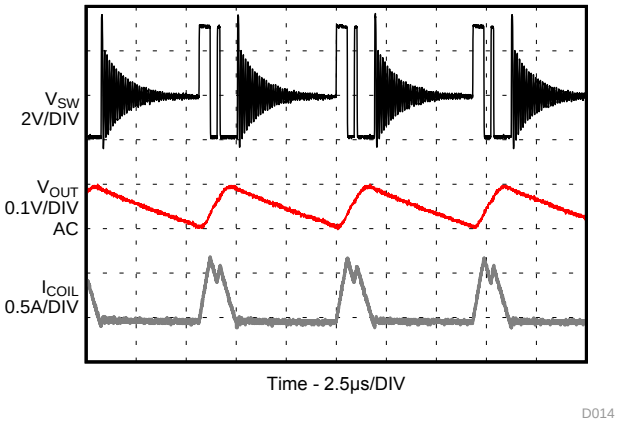

$I_{OUT}$ = 1 A

**Figure 13. Switching Frequency vs Input Voltage**



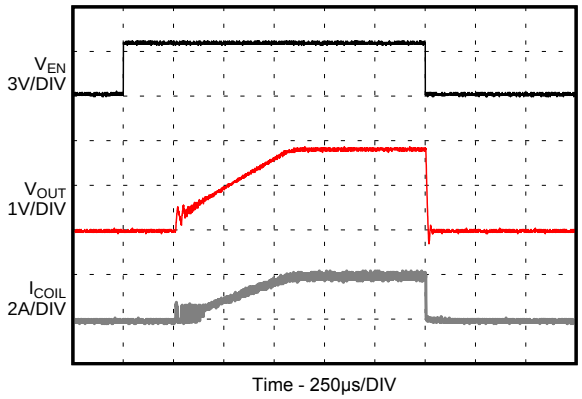

$I_{OUT}$ = 1 A

**Figure 14. PWM Operation**



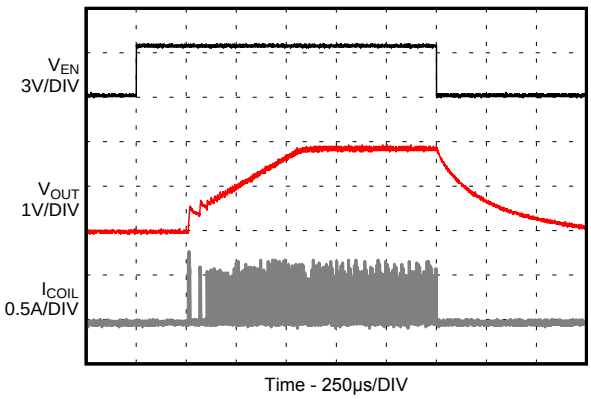

$I_{OUT}$ = 0.1 A

**Figure 15. Power Save Mode Operation**



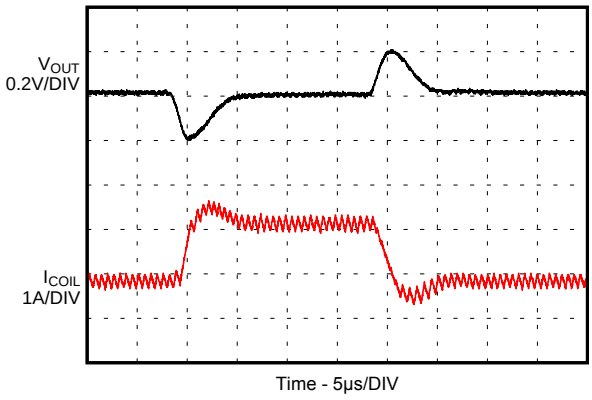

$I_{OUT}$ = 2 A

**Figure 16. Startup and Shutdown with Load**



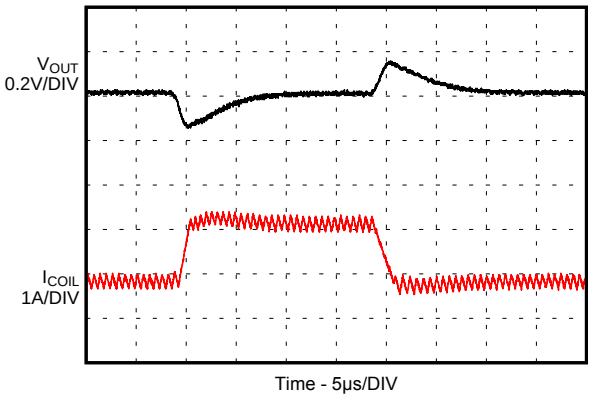

$I_{OUT}$ = 0.1 A

**Figure 17. Startup and Shutdown with Load**




Load Step 0.8 A to 2 A, 1A/µs slew rate

**Figure 18. Load Transient**




Load Step 0.8 A to 2 A, 1A/µs slew rate C3 = 6.8 pF

**Figure 19. Load Transient**

## 11 Power Supply Recommendations

The power supply to the TLV62569 must have a current rating according to the supply voltage, output voltage and output current.

## 12 Layout

### 12.1 Layout Guidelines

The PCB layout is an important step to maintain the high performance of the TLV62569 device.

- The input/output capacitors and the inductor should be placed as close as possible to the IC. This keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.
- The low side of the input and output capacitors must be connected properly to the power GND to avoid a GND potential shift.
- The sense traces connected to FB are signal traces. Special care should be taken to avoid noise being induced. Keep these traces away from SW nodes.
- GND layers might be used for shielding.

## 12.2 Layout Example

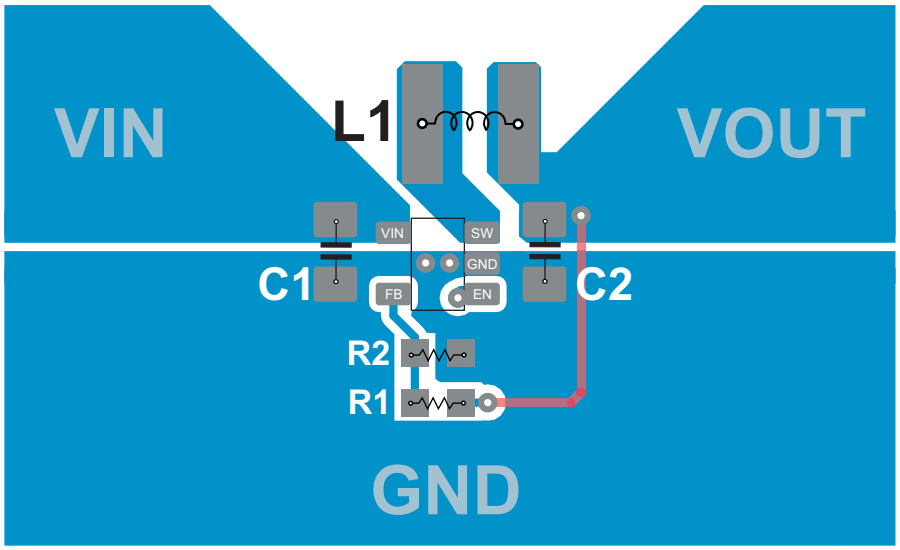



**Figure 20. TLV62569 Layout**

## 12.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: Thermal Characteristics Application Notes SZZA017 and SPRA953.

# 13 Device and Documentation Support

## 13.1 Device Support

### 13.1.1 Third-Party Products Disclaimer

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## 13.2 Documentation Support

### 13.2.1 Related Documentation

*Semiconductor and IC Package Thermal Metrics Application Report* (SPRA953)

*Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs Application Report* (SZZA017)

## 13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 13.5 Trademarks

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## 13.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV62569DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 16AF | Samples |
| TLV62569DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 16AF | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

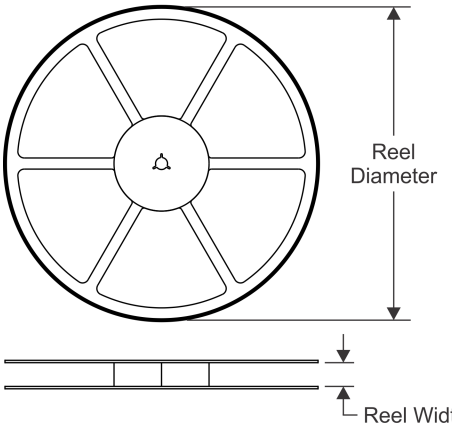
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

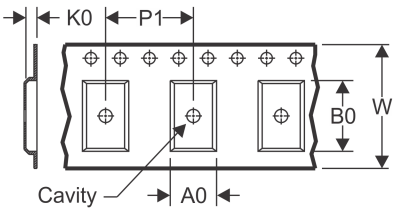
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

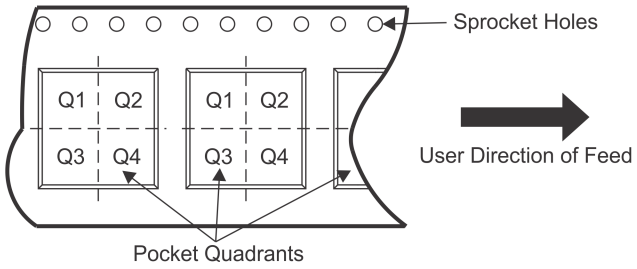



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

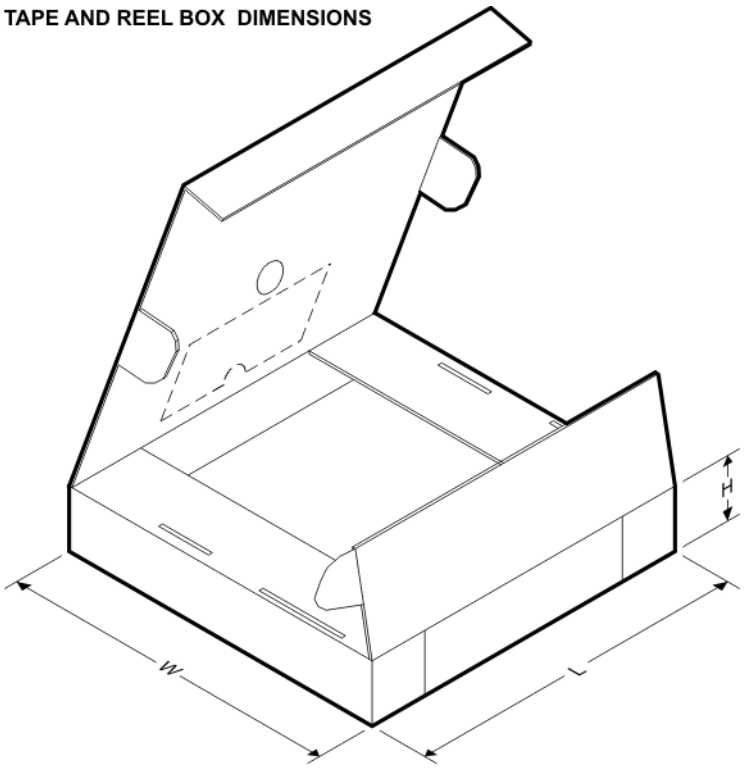
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV62569DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV62569DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

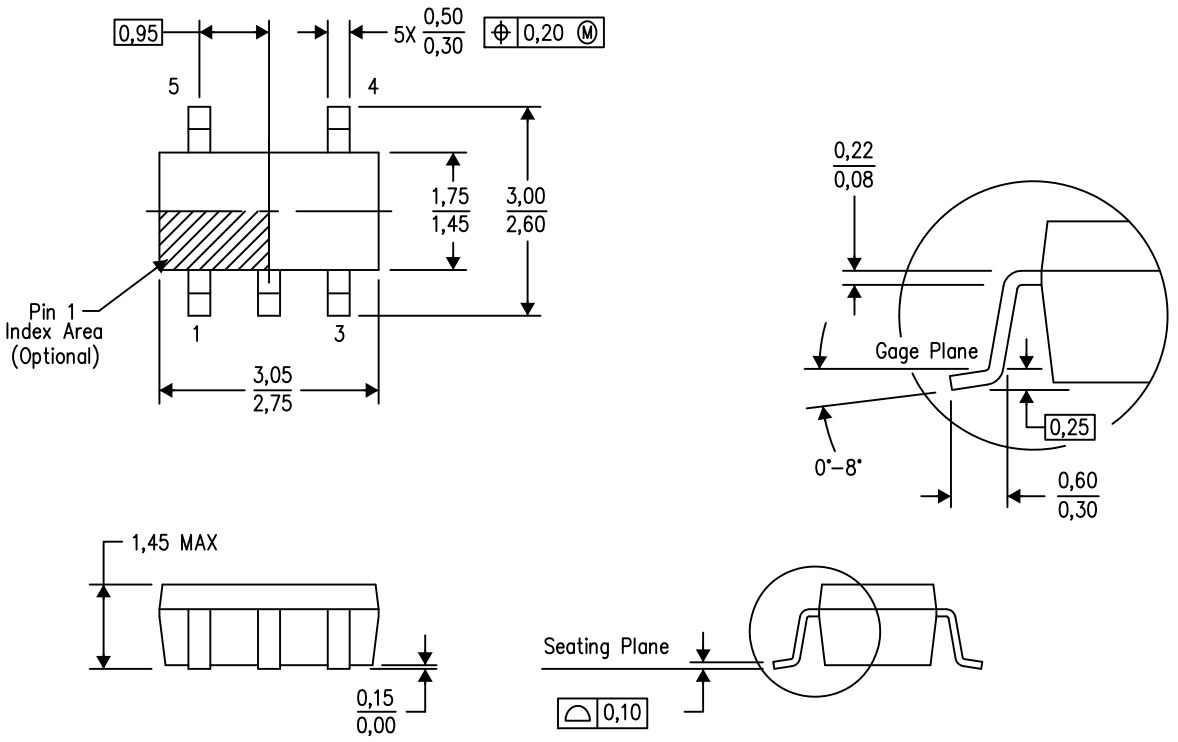
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV62569DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV62569DBVT | SOT-23 | DBV | 5 | 250 | 210.0 | 185.0 | 35.0 |

DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE




4073253–4/N 12/14

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

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