The hardware and software times (199 ms ± 1.32 ms and 11.6 ms ± 9.53 µs respectively) are different because of the large overhead of communication times in the FPGA fabric, single processing of the list from the function call, and low computation time of the modulus operator. The FPGA requires a lot of communication over the AXI bus between PL and PS. The HW operations consists of reading and writing to IP registers whereas in the SW operation, there is virtually no communication overhead (computation stays on PS). FPGAs also benefit from parallel processing. For this task, this was not utilized since each number was tested in sequence. Compounding on this fact, the computation for this task is also very simple and has a low compute time. Since the CPU does not have as much overhead (no AXI bus communication) versus the FPGA, the bulk of time is used for computation and not communication. The CPU user and sys times are 13 ms and 15 µs respectively, and the FPGA user and sys times are 194 ms and 7.93 ms respectively. It can be seen that the CPU has faster computation and communication times.