RF Low Noise Amplifier

Test Vehicle Report

Rev 1.0

Revision History

Rev.No.	History	Draft Date	Designer/Owner
Rev 1.0	Initial Document	09/30/2007	JFKuan / Minghsien Tsai

Contents

General Description

The Low-noise amplifiers (LNAs) are the key components of RF receivers for wireless communications. LNAs must provide enough gain to overcome the noise of subsequent stages. It not only amplifies weak signal received by antenna but also contributes noise as low as possible. The main purpose of this 5.5GHz Single-ended LNA test vehicle is to verify tsmc process based on tsmc recommended design platform by means of checking RF performance and silicon correlation. The recommended design platform includes process design rule, spice model and process design kits (PDK) environment.

Configuration and Feature

- TSMC N65LPGV2 MM/RF MIM with UTM 1.2V/2.5V 1P6M(3X1Z1U) process
- Narrowband amplifier
- Cascode configuration
- Inductive source degeneration input stage
- Single-ended input and output
- Chip area size: 732.7um x 787.4um = 0.576 mm^2
- Center Frequency: 5.5GHz
- Bias current: 7 mA
- Power consumption: 8.4mW

Specification

Item	Spec	Unit
Supply voltage	**1.2**	**V**
Frequency	**5.5**	**GHz**
Gain	**> 15**	**dB**
Noise figure	**< 5**	**dB**
Input return loss	**> 10**	**dB**
Output return loss	**> 10**	**dB**
Isolation	**> 20**	**dB**
P1dB	**> -25**	**dBm**
IIP3	**> -15**	**dBm**
Bias current	**< 10**	**mA**

Schematic

The schematic of LNA is shown as Fig1. The amplifier is single-ended cascode with inductive source degeneration cascode architecture. In order to decrease the Miller effect for good isolation between input and output stage, the cascode amplifier architecture is used. Cascode transistor M_2 is used to reduce the interaction of the tuned output with the tuned input, and to reduce the effect of M_1's *Cgd* (i.e. miller effect). The total node capacitance at the drain of M_2 resonates with inductance L_d both to increase gain at the center frequency and simultaneously to provide an additional level of highly desirable band-pass filtering (i.e. inductive peaking). The C_B capacitor is treated as DC blocking. The value of C_B is chosen to have negligible reactance at the signal frequency, and is sometimes implemented as an off-chip component. The capacitor Cbypass is used to reject DC supply noise. The value of C_B is chosen to have lower reactance at the signal frequency . Most important of all, from Friis equation, the noise performance is dominant by the first stage. In other words, when the gain of first stage is larger, the noise of the subsequent stages is reduced more. These active and passive devices are from PDK

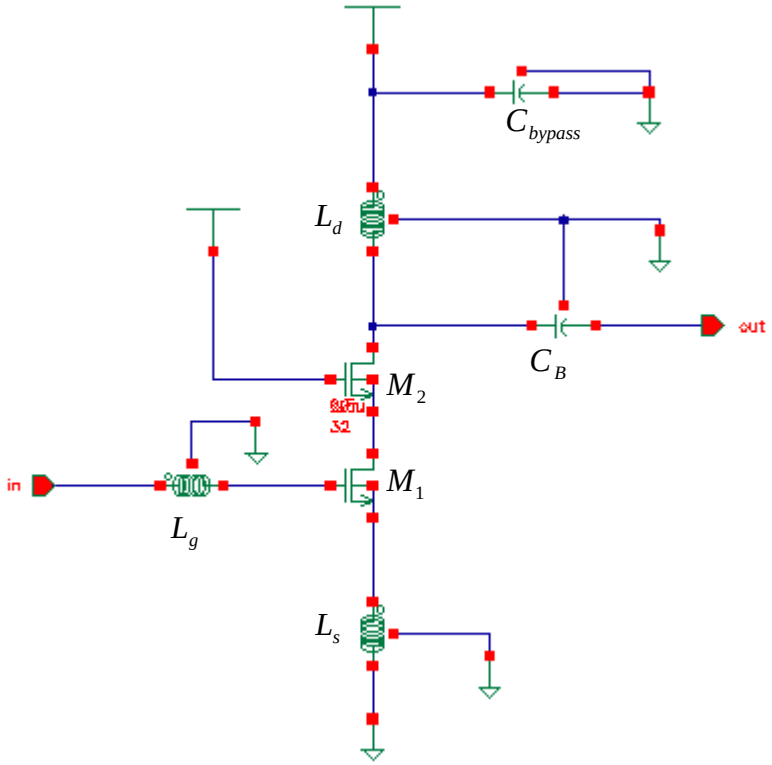


Fig. 1: Narrowband single-ended cascode LNA with inductive source degeneration

Pre-layout Simulation

The main LNA performance check by simulation includes S-parameter, noise figure (NF) and linearity (P1dB, IIP3 ..etc). The simulator is cadence spectre-RF.

- **S-parameter simulation**

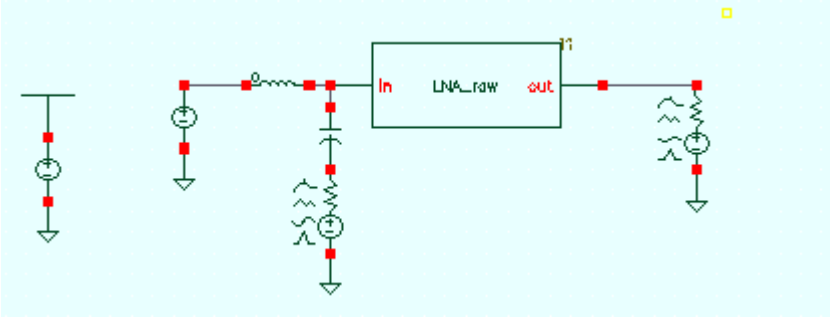


Fig. 2: The schematic of S-parameter test bench

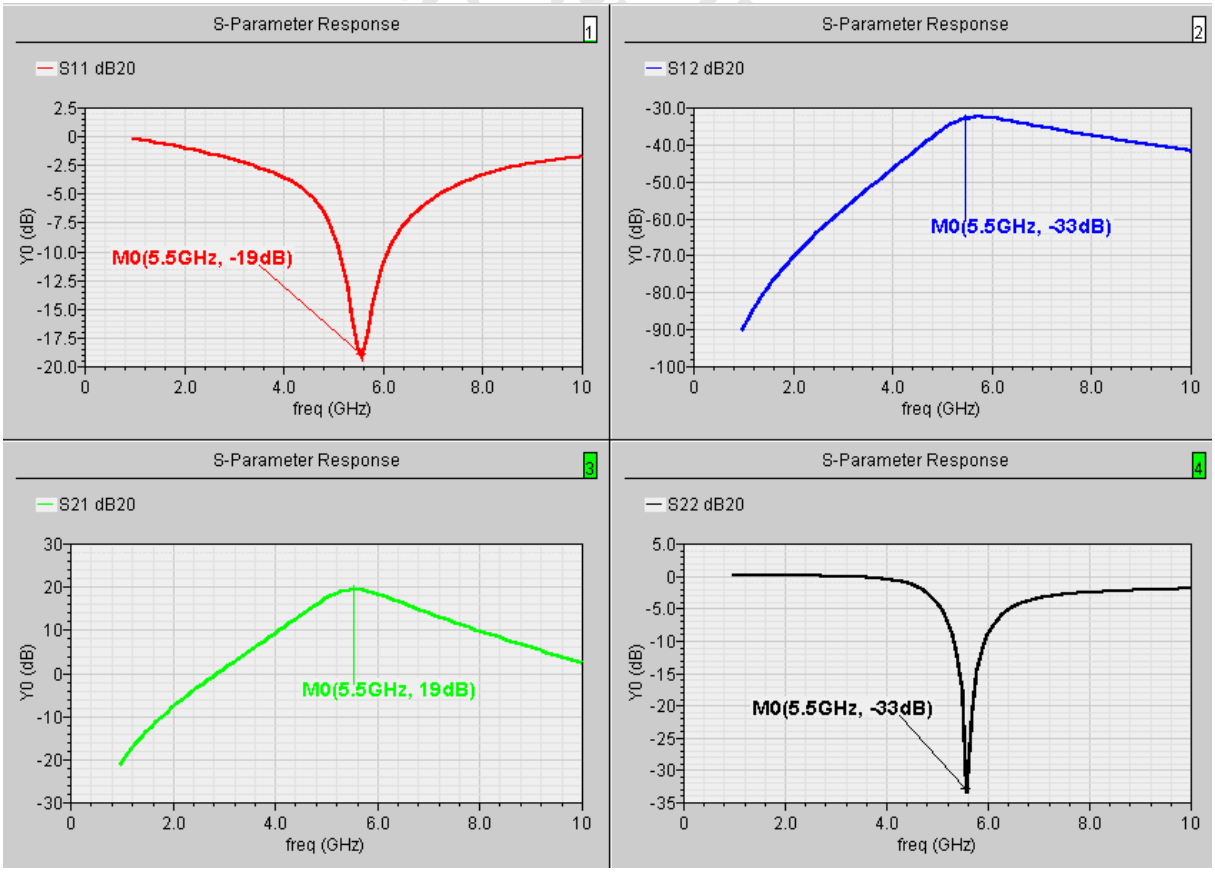


Fig. 3: Separate S-parameters in rectangular form

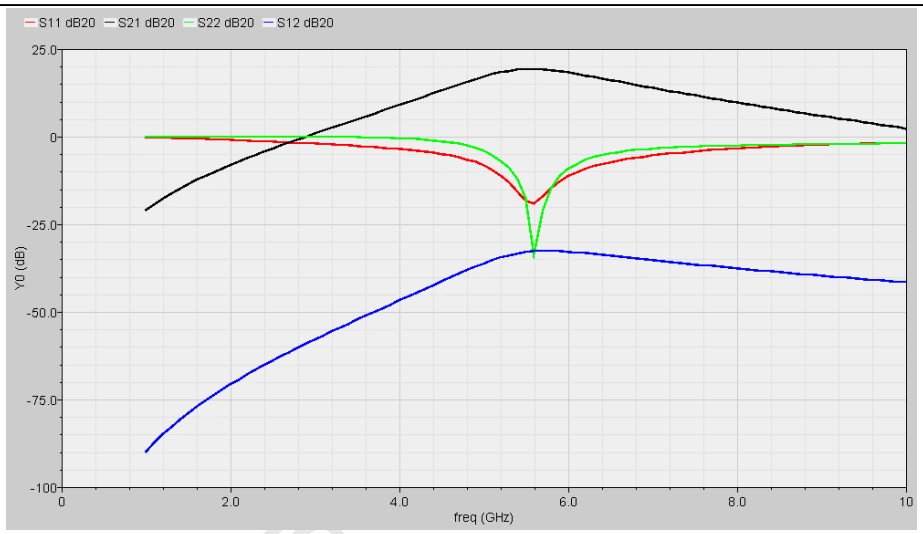
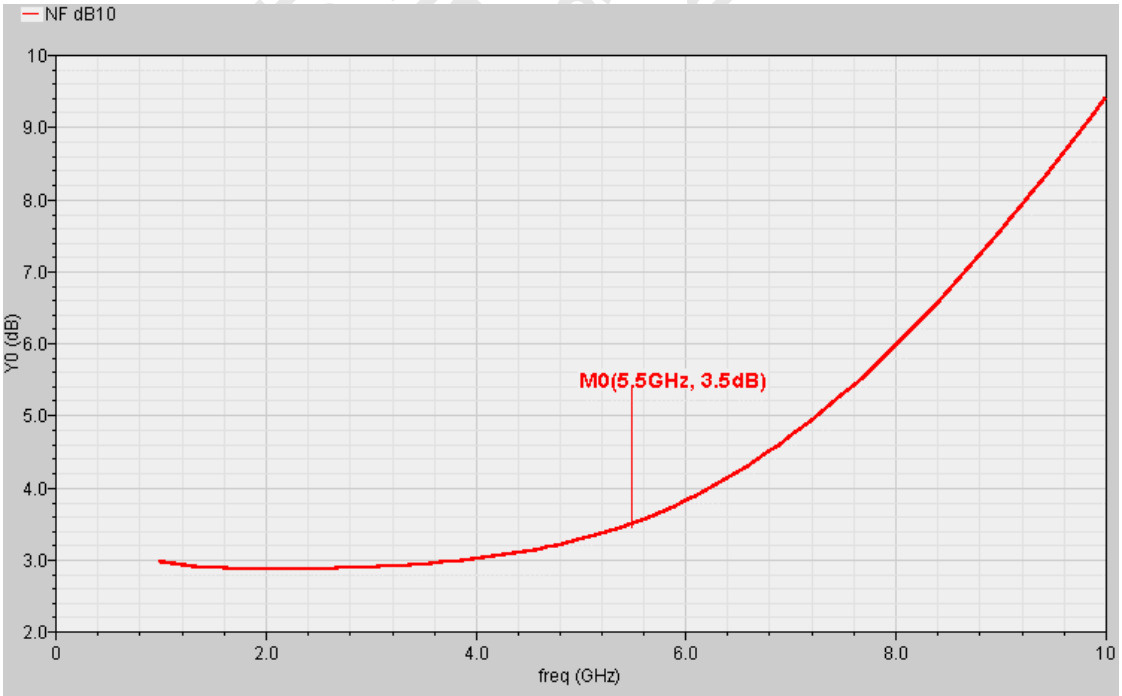


Fig. 4: S-parameters combined in one plot

- **Noise Figure simulation**

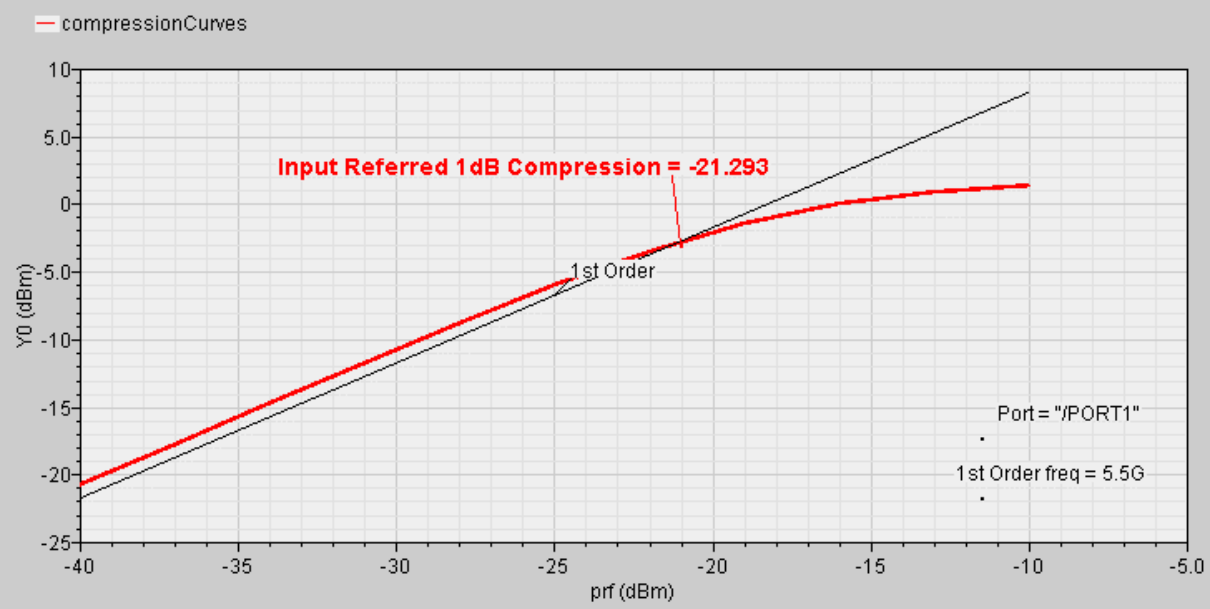
The definition of noise figure: NF=10log [(SNR)in /(SNR)out]

NF=3.5 dB @5.5 GHz



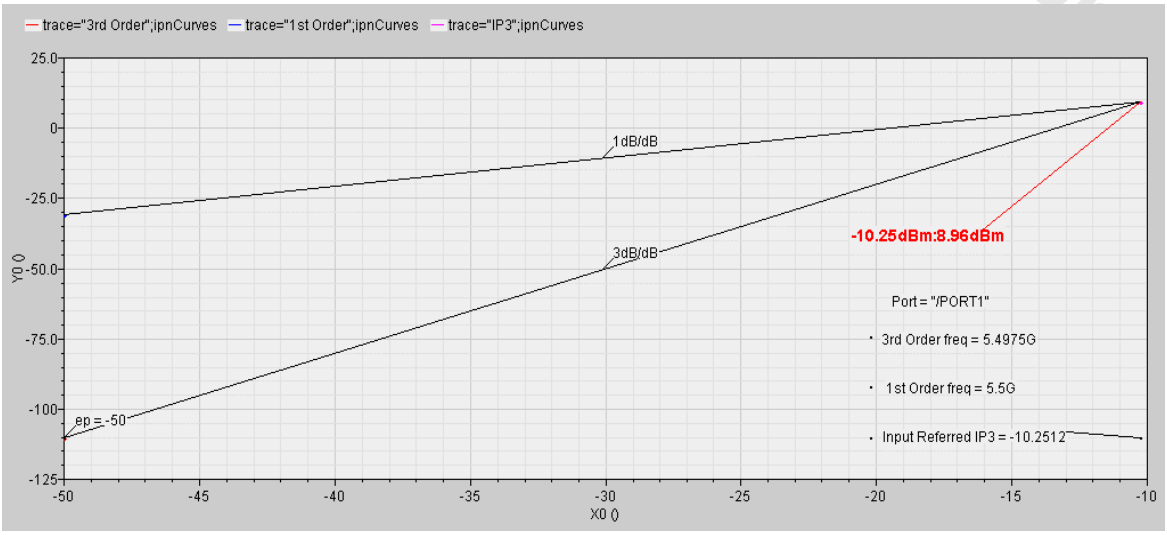
- **Input referred 1dB compression point simulation**

For linear circuits, it is expected that the output signal to be proportional to the input signal. As input signal becomes large, the output signal fails to exhibit this characteristic. The pre-simulation 1 dB compression point is –21.293 dB



- **The input/output third intercept point (IIP3/OIP3) simulation**

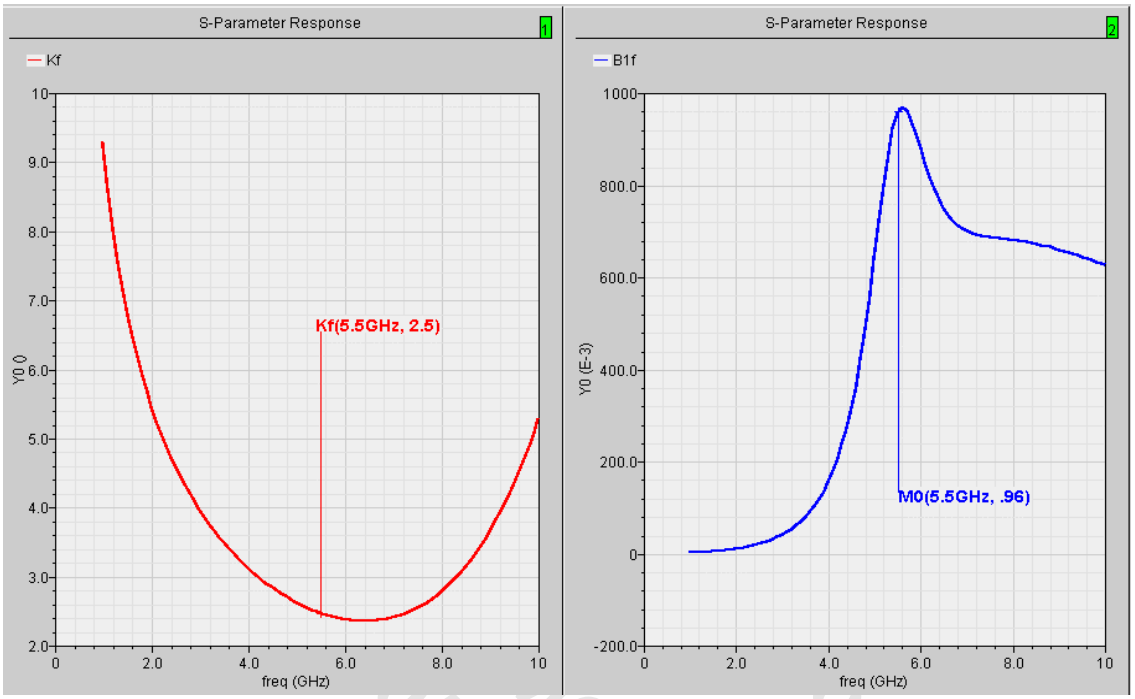
Except for the 1dB compression point, the linearity can also be evaluated by inter-modulations. The IIP3 is measured with two-tone test in which two closely placed signals are injected as input simultaneously. The IP3 is the extrapolation of signal line and the third-order harmonic line. The simulation results of IIP3/OIP3 are –10.25dBm/8.96dBm.



- **Stability simulation check**

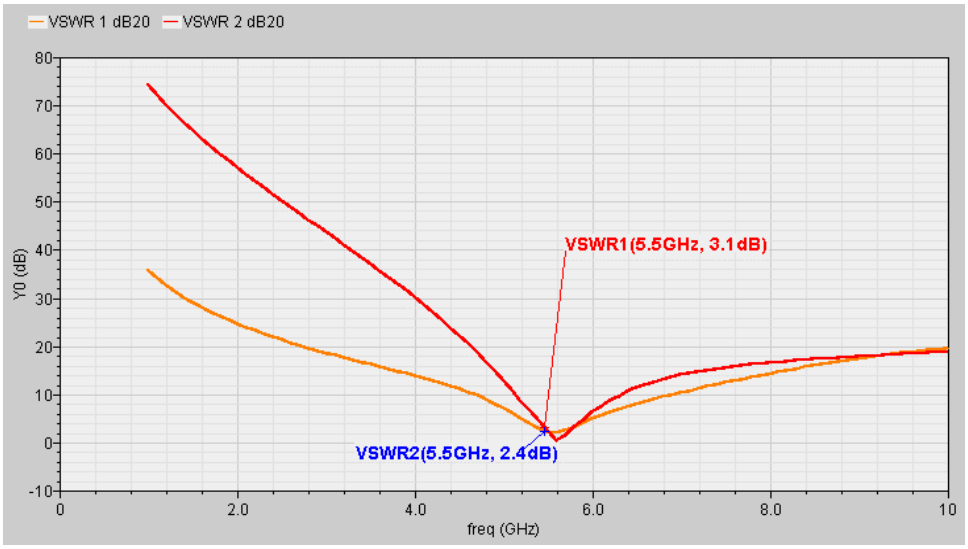
Stability is one of the important issues for LNAs design. If the LNAs are not stable, it will cause oscillation problem. The necessary and sufficient conditions is to check stability factor Kf and Bf.

The simulation results show Kf =2.5 >1; Bf=0.99 >0. This means the LNA is unconditionally stable at operation frequency.



- **Voltage standing wave ratio (VSWR) simulation check**

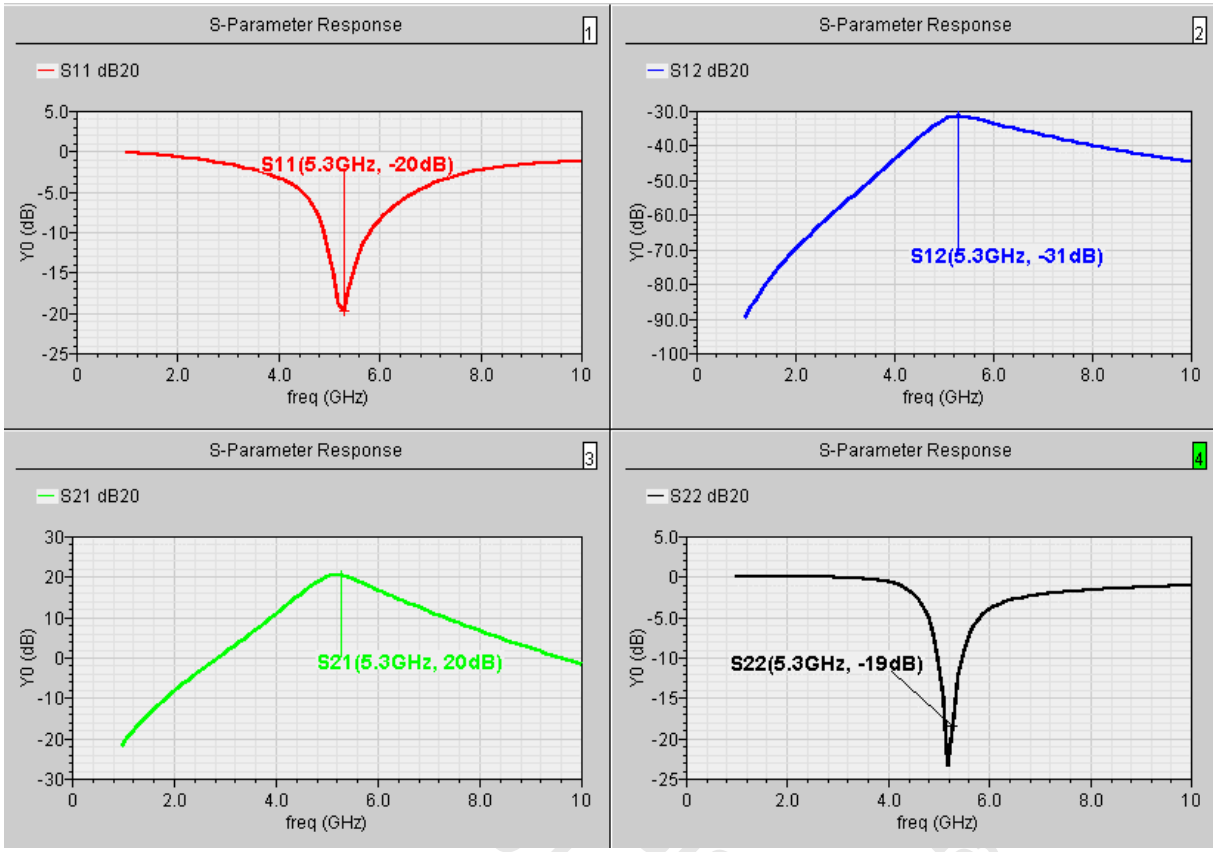
The amplifier design specification often includes the maximum allowable VSWR. The smaller VSWR value is the better performance. The ideal VSWR value is 0 dB.



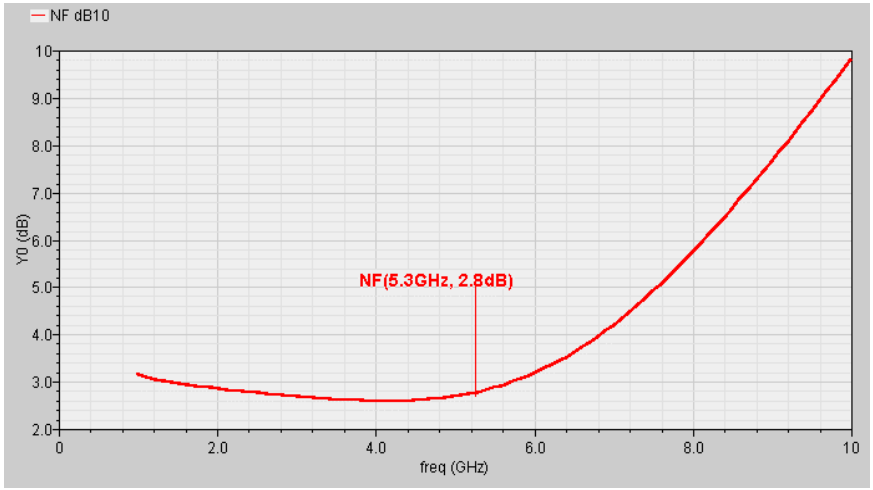
Post-layout Simulation

Based on cadence environment, we use calibre flow to extract RLC parasitic for our post-simulation.

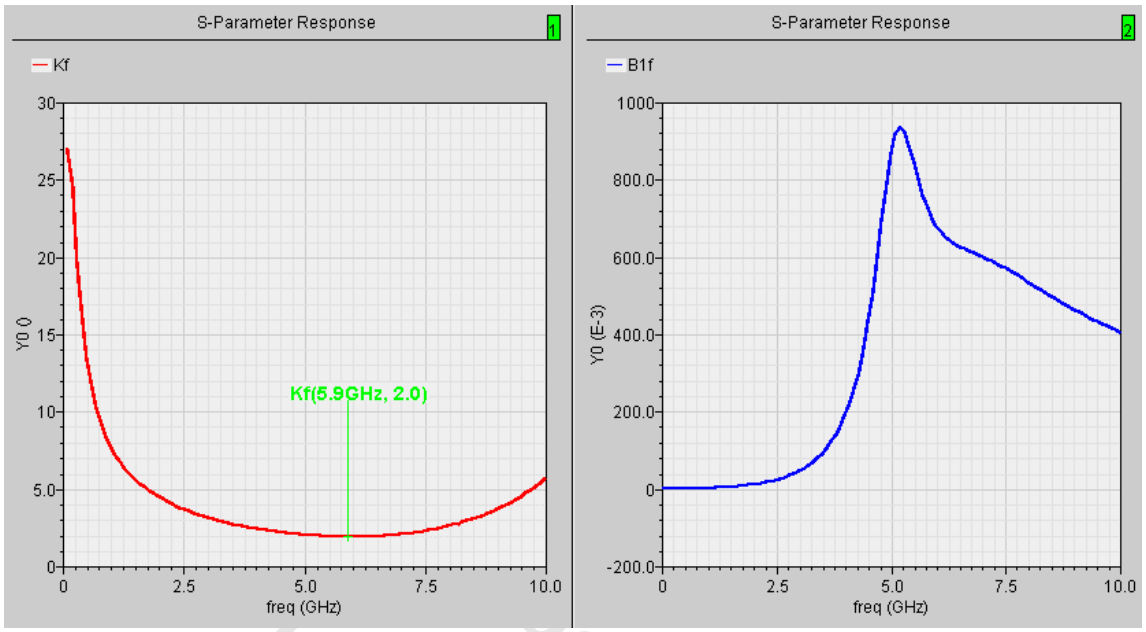
- **S-parameters:** based on S11 impedance matching, the frequency is 5.3GHz



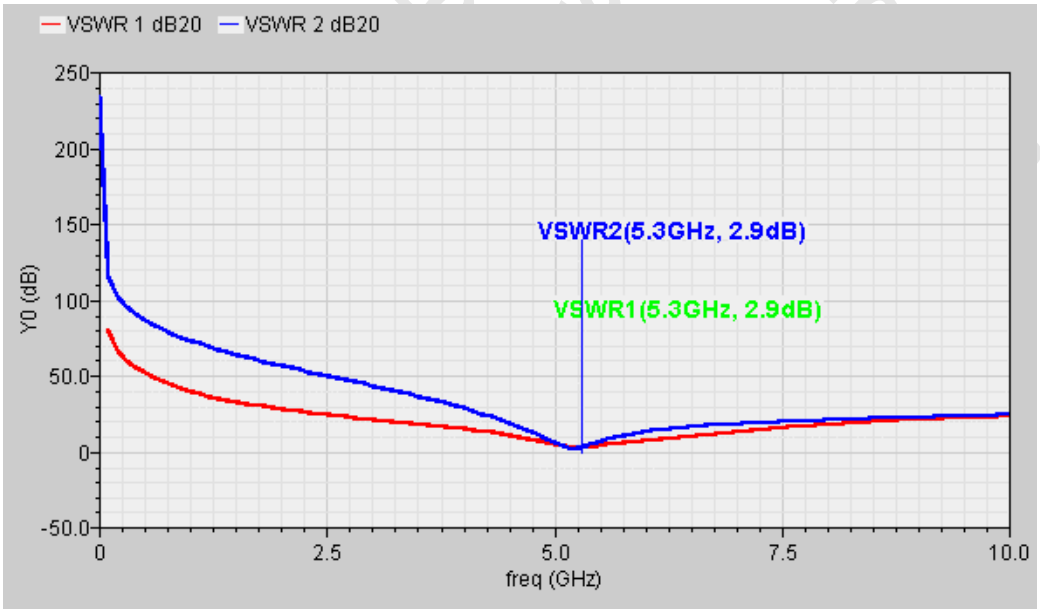
- **Noise Figure :** the post-simulation of NF at 5.3GHz is 2.8 dB



- **Kf & Bf :** The post-simulation results show Kf >1; Bf >0 that the system is unconditionally stable.

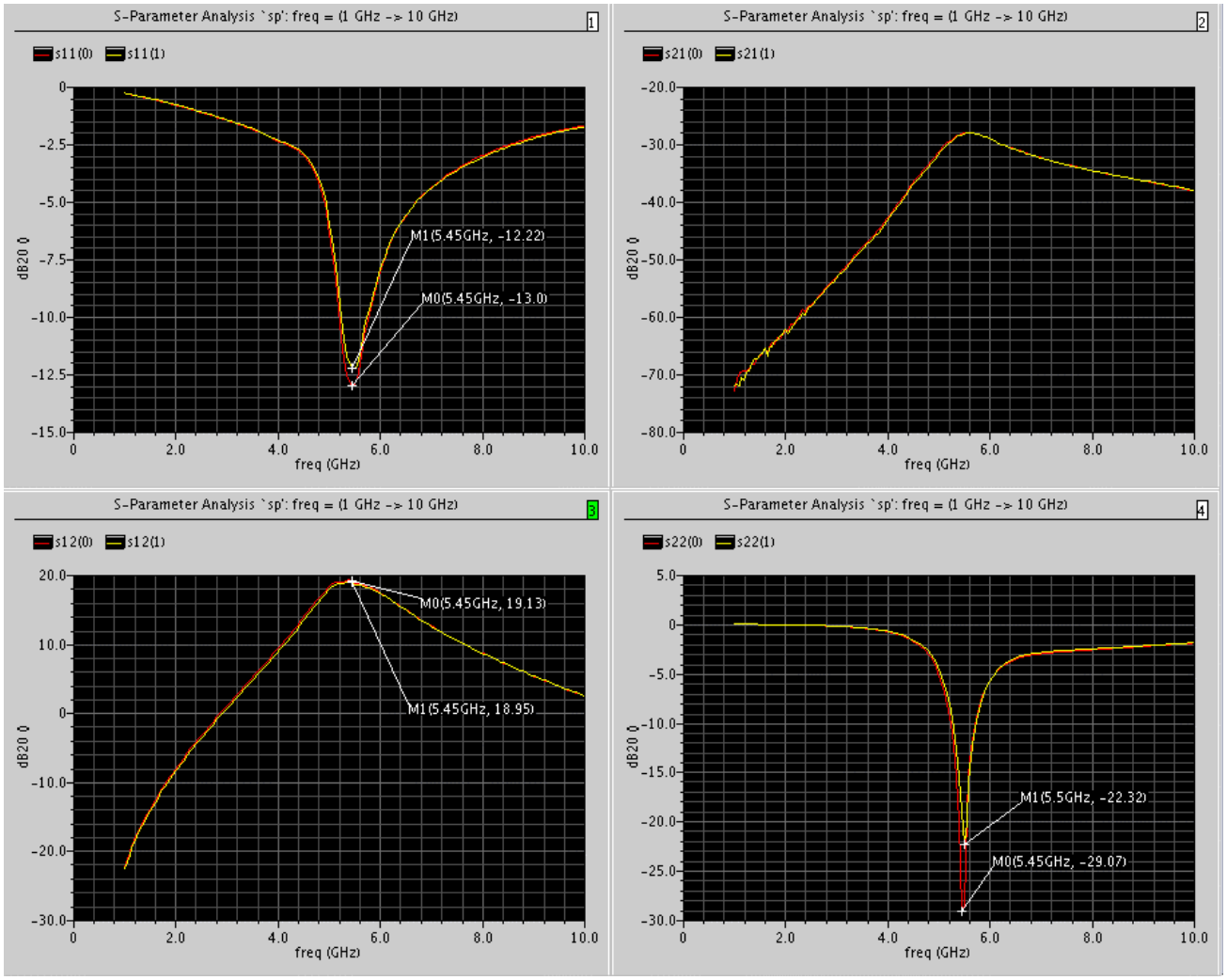


- **VSWR :** The input VSWR and output VSWR are the minimum values at 5.3GHz



Silicon Measurement

The S-parameter silicon measurements are compared with MIM (read line) and MOM (yellow line) splits. The silicon data show close performance between MIM and MOM. For typical MIM case, the input return loss is 13 dB; the isolation S12 is around –30 dB; the gain S21 is around 19 dB, and output return loss is around 22 dB.

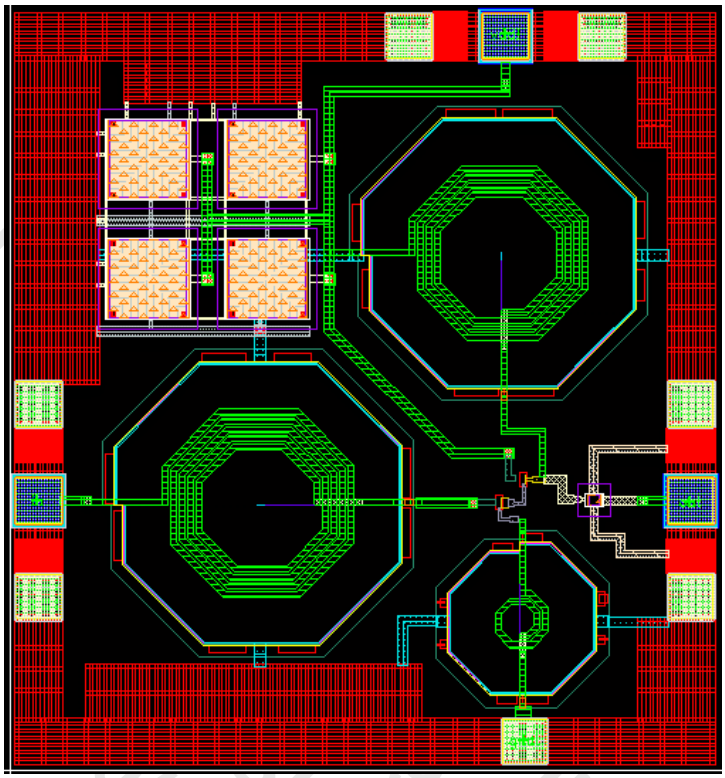


- Simulation and silicon measurement comparison

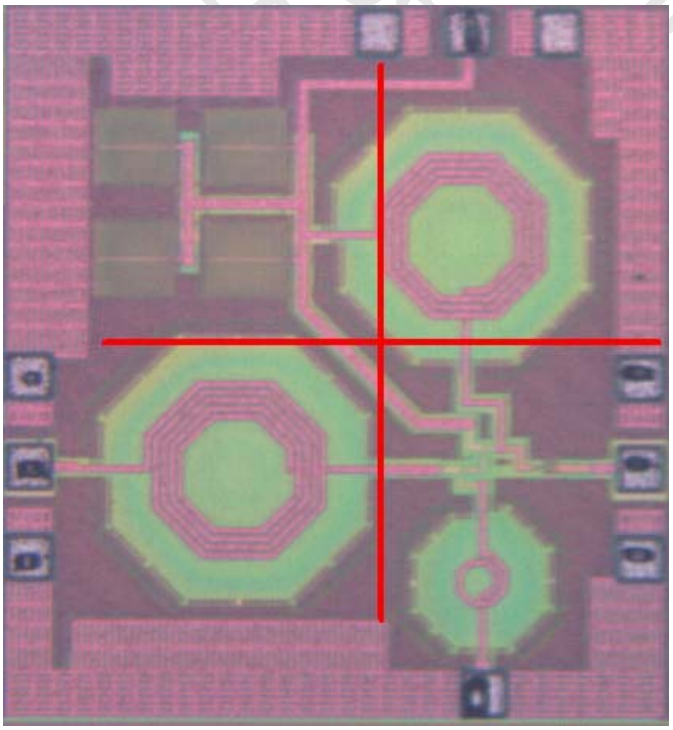
S-parameter	Pre-sim		Post-sim		Measurement	
	Mag.(dB)	freq.(GHz)	Mag.(dB)	freq.(GHz)	Mag.(dB)	freq.(GHz)
S21	19	5.5	20	5.3	19	5.45
S11	-19	5.5	-20	5.3	-13	5.45
S22	-33	5.5	-19	5.3	-30	5.45
S12	-33	5.5	-31	5.3	-30	5.45

GDS and layout

- Layout view in gds



- Photographic on silicon



Special Note

This LNA design flow guideline is to provide reference design flow with correlated to tsmc silicon measurement data. The post-layout simulation is based on RLC extraction but not EM simulation to align with digital/mix-signal design for future SOC co-simulation. It is implemented in this document from pre-simulation, post-simulation procedure and compare to silicon chip measurement results. Because of silicon measurement environment and time constrained, we just to provide s-parameter measurement data first. The noise figure and linearity silicon data like P1dB and IIP3 will be added and packed in future PDK revision. If customers still have any design flow related question, please contact account manager or CAE related people.