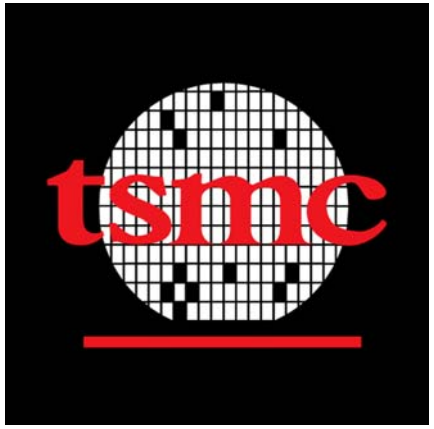


TSMC N65 PDK usage guide:

An introduction on the usage of TSMC process design kits (PDK)

PDK Version: v1.0a Feb .07

TSMCN90RF PDK Usage Guide

Introduction:

- This document describes the TSMC process design kits (PDK) parameterized cell (Pcell) software, which provides a graphical user interface that lets user create parameterized cells for placement in design layout.
- It is assumed that the user is familiar with the development and design of integrated circuits and with the cadence Virtuoso Layout Editor.
- All the information and data contained hereunder constitute TSMC's proprietary and confidential information. Unless TSMC agrees otherwise in writing, you can only use the information contained herein for evaluation purpose. Further, you should treat the information as confidential information and exercise due care to prevent its disclosure to any persons, provided you may disclose it to your employees on a need to know basis in case they agree to similar duty of confidentiality to protect the information herein. You cannot disclose such information to any third party unless TSMC agrees in advance by writing. However, requirements hereunder shall not serve to supersede or change any existing contracts regulating similar issues between you and TSMC.

TSMCN65 PDK Usage Guide

Overview:

- The Symbol Display Information.

  This section describes the symbol display information include four terminal NMOS symble, four terminal PMOS symbol, three terminal NMOS symbol, three terminal PMOS symbol, three terminal npn BJT symbol, three terminal pnp BJT symbol, two terminal diode symbol, two terminal resister symbol, three terminal resister symbol and two terminal varactor symbol.

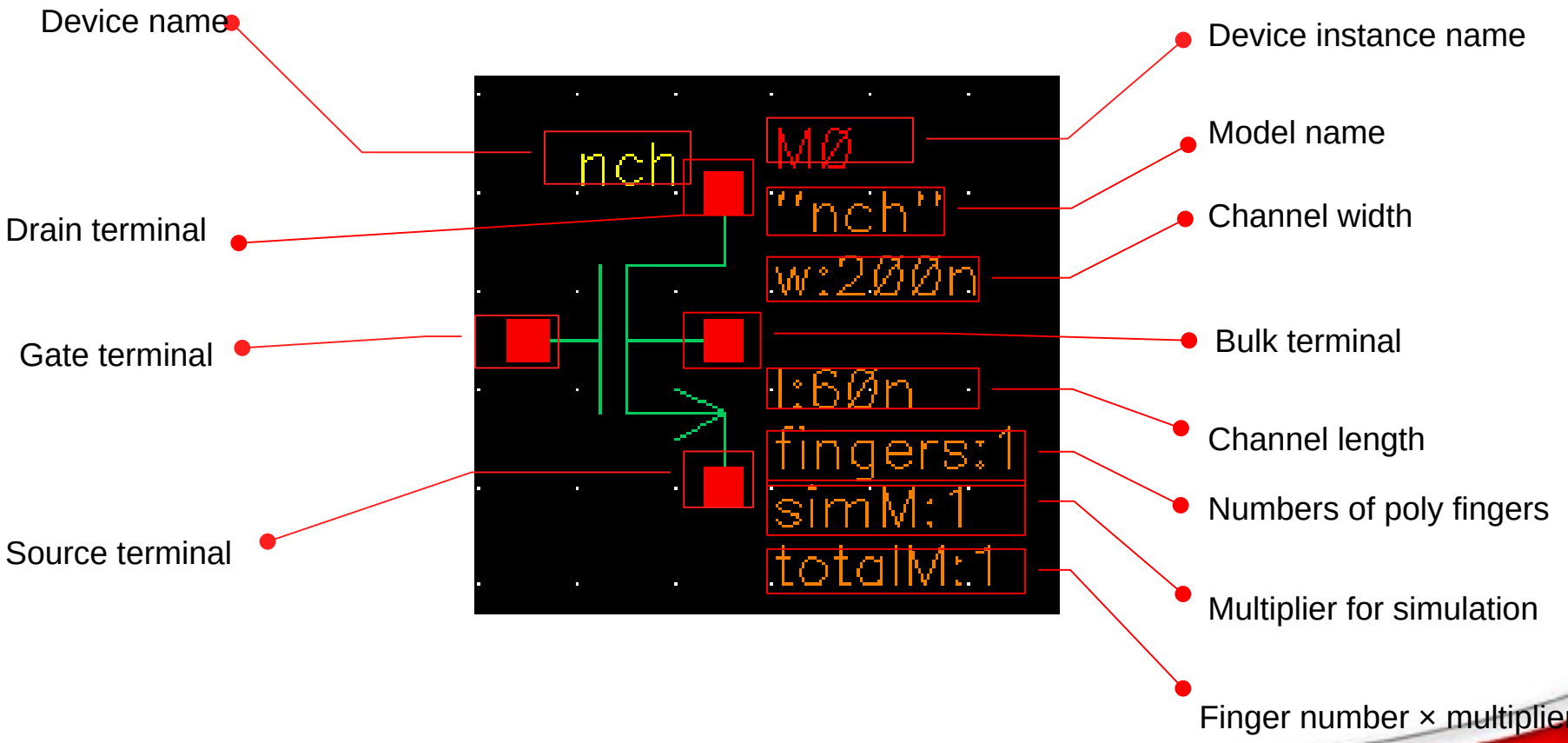
- Device Table

  This section show the total device in this PDK. The user can check the page number in the device table to find out the CDF parameter and Pcell function.

- MOS Parameterized Cell Function Introduction
- BJT Parameterized Cell Function Introduction
- Diode Parameterized Cell Function Introduction
- Resistance Parameterized Cell Function Introduction
- Inductor Parameterized Cell Function Introduction
- Varactor Parameterized Cell Function Introduction
- Capacitor Parameterized Cell Function Introduction
- CDF Parameter Description
- Appendix

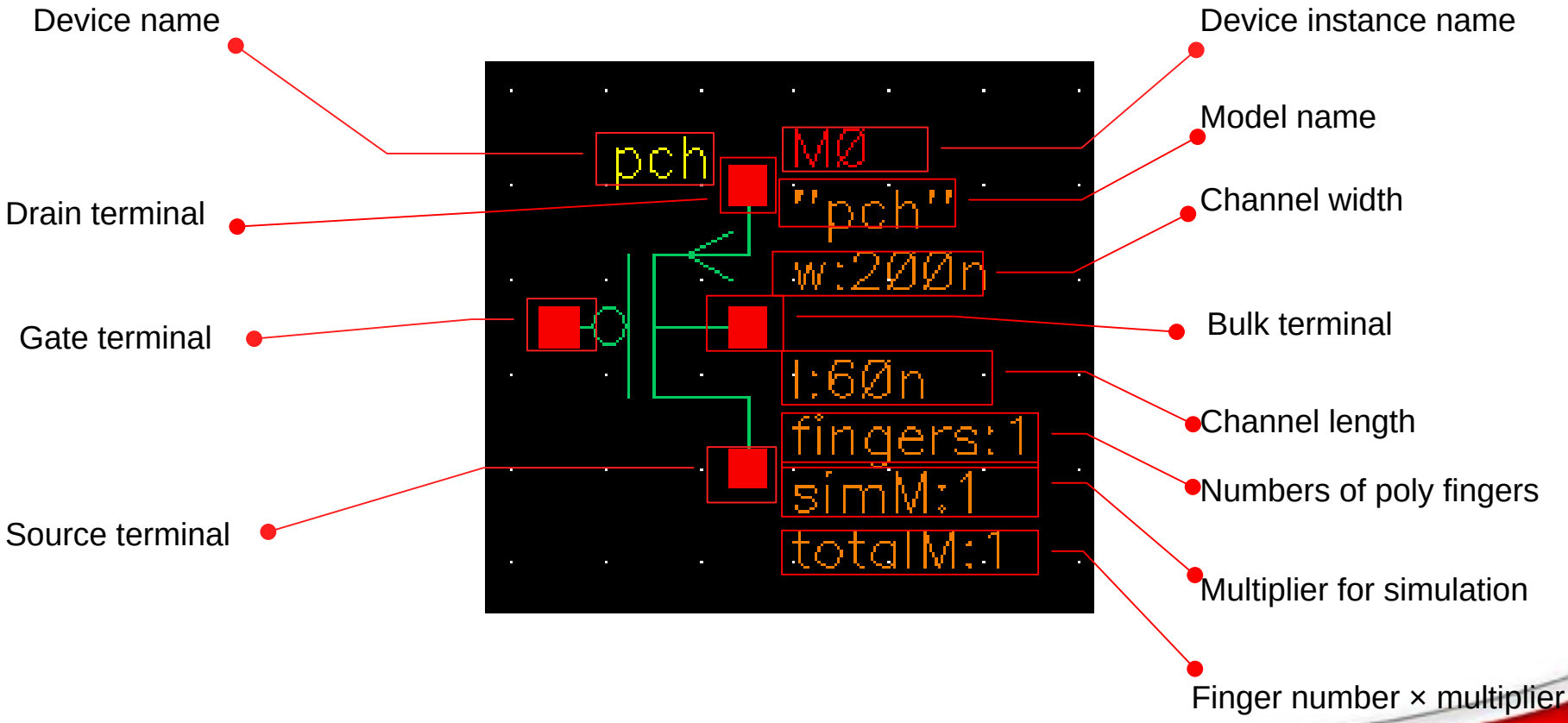
TSMCN65 PDK Usage Guide

- **The Symbol Display Information:**
  - The following figure shows the symbol for a four terminal NMOS:



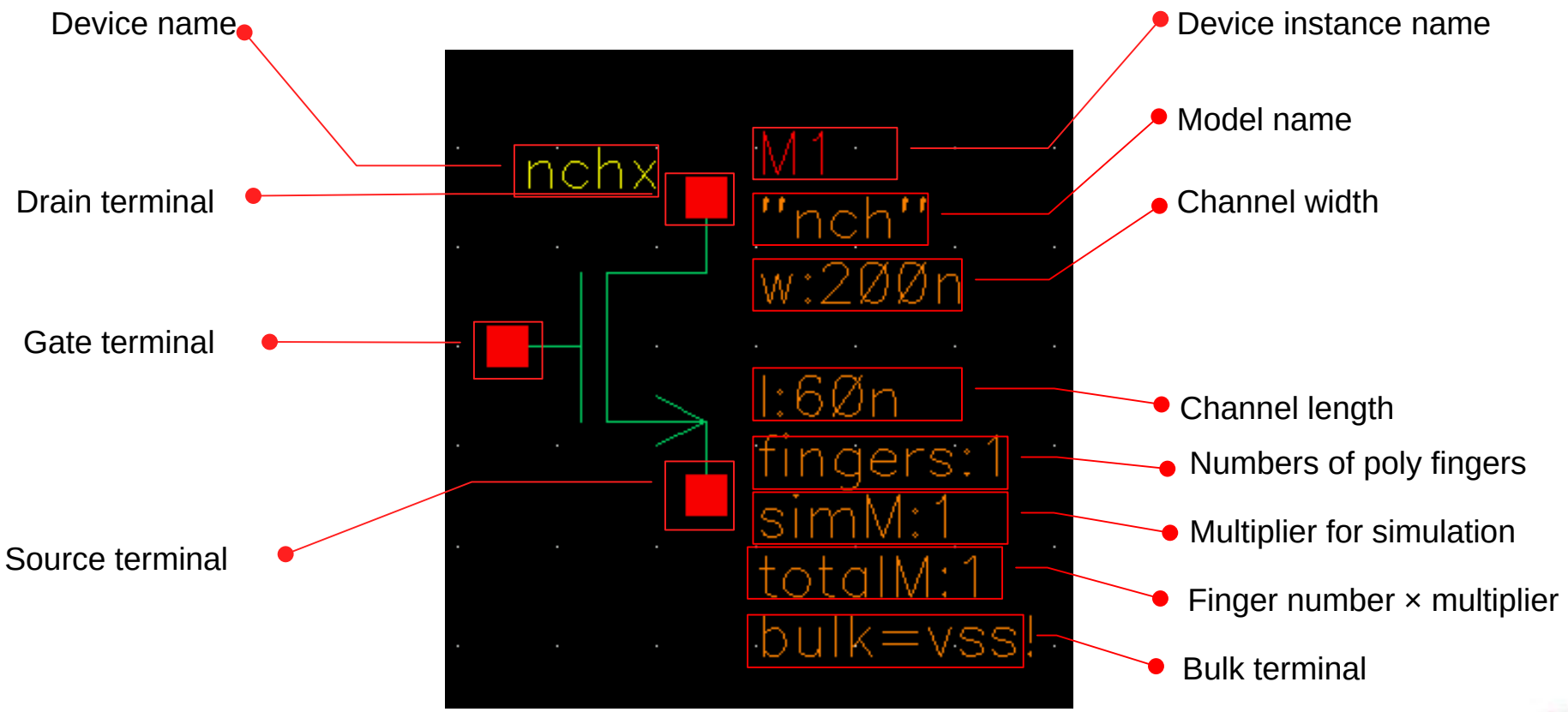
The Symbol Display Information:

- The following figure shows the symbol for a four terminal PMOS:



TSMCN65 PDK Usage Guide

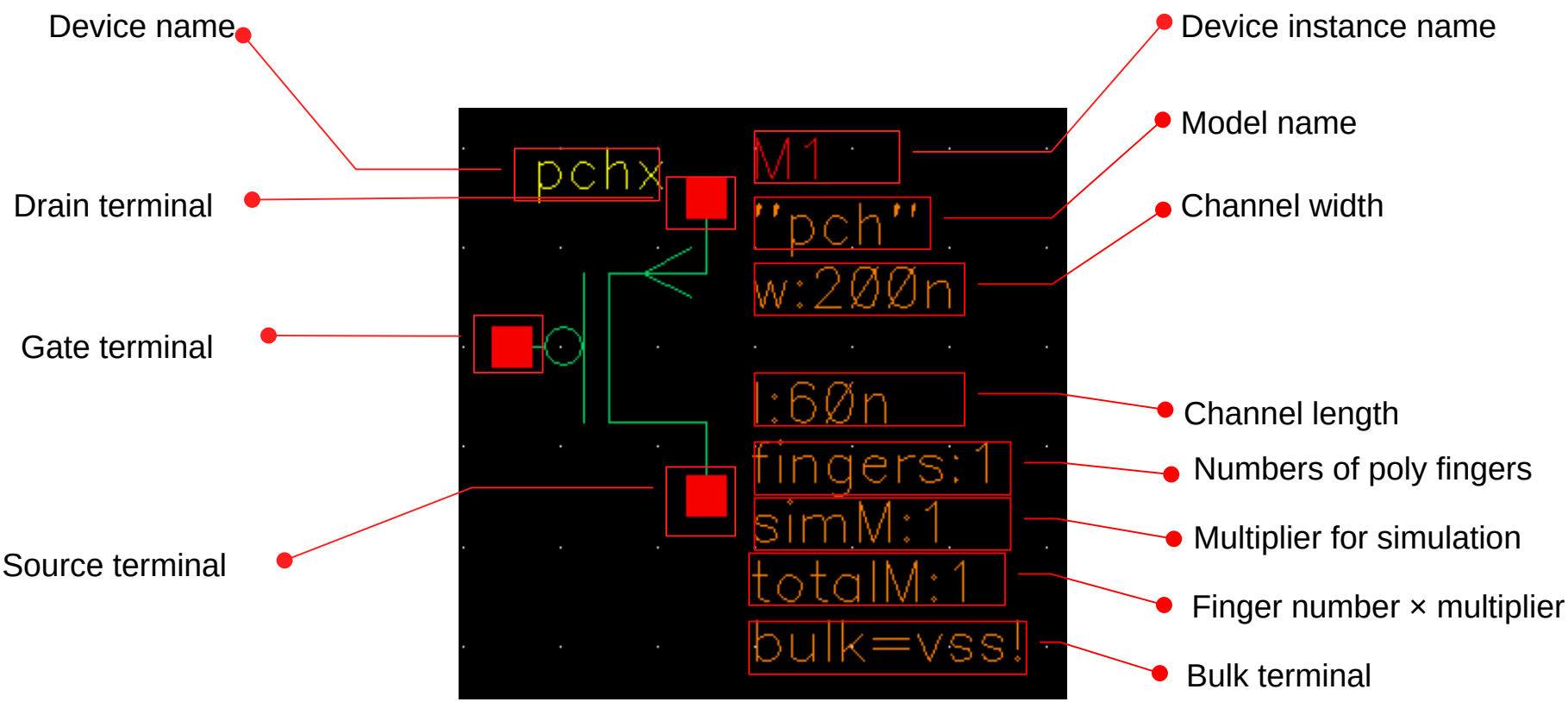
- **The Symbol Display Information:**
  - The following figure shows the symbol for a three terminal NMOS :



TSMCN65 PDK Usage Guide

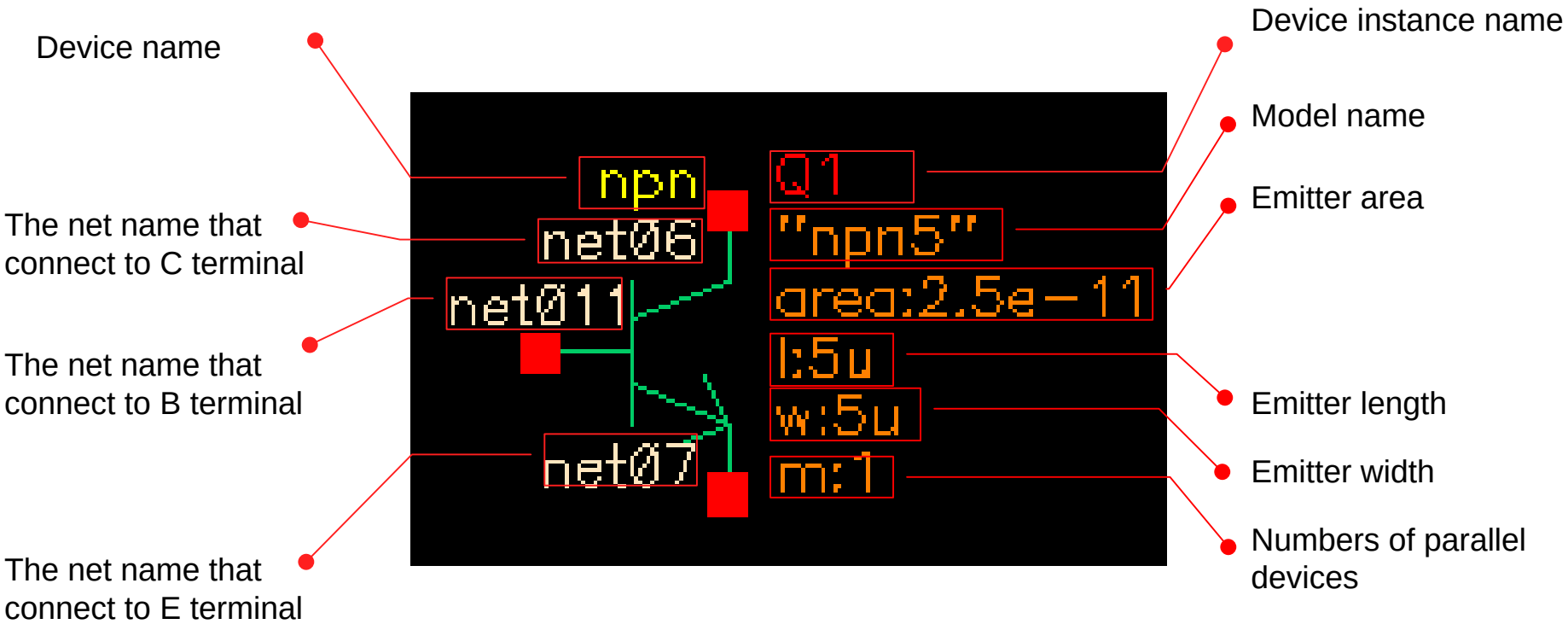
The Symbol Display Information:

- The following figure shows the symbol for a three terminal PMOS :



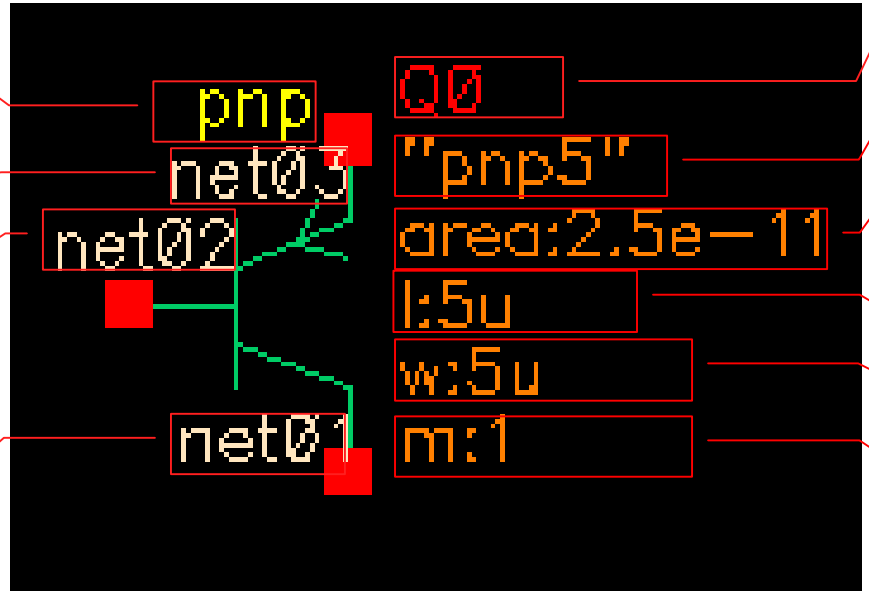
The Symbol Display Information:

- The following figure shows the symbol for a three terminal npn BJT:



TSMCN65 PDK Usage Guide

- **The Symbol Display Information:**
  - The following figure shows the symbol for a three terminal pnp BJT:



Device name

The net name that connect to E terminal

The net name that connect to B terminal

The net name that connect to C terminal

Device instance name

Model name

Emitter area

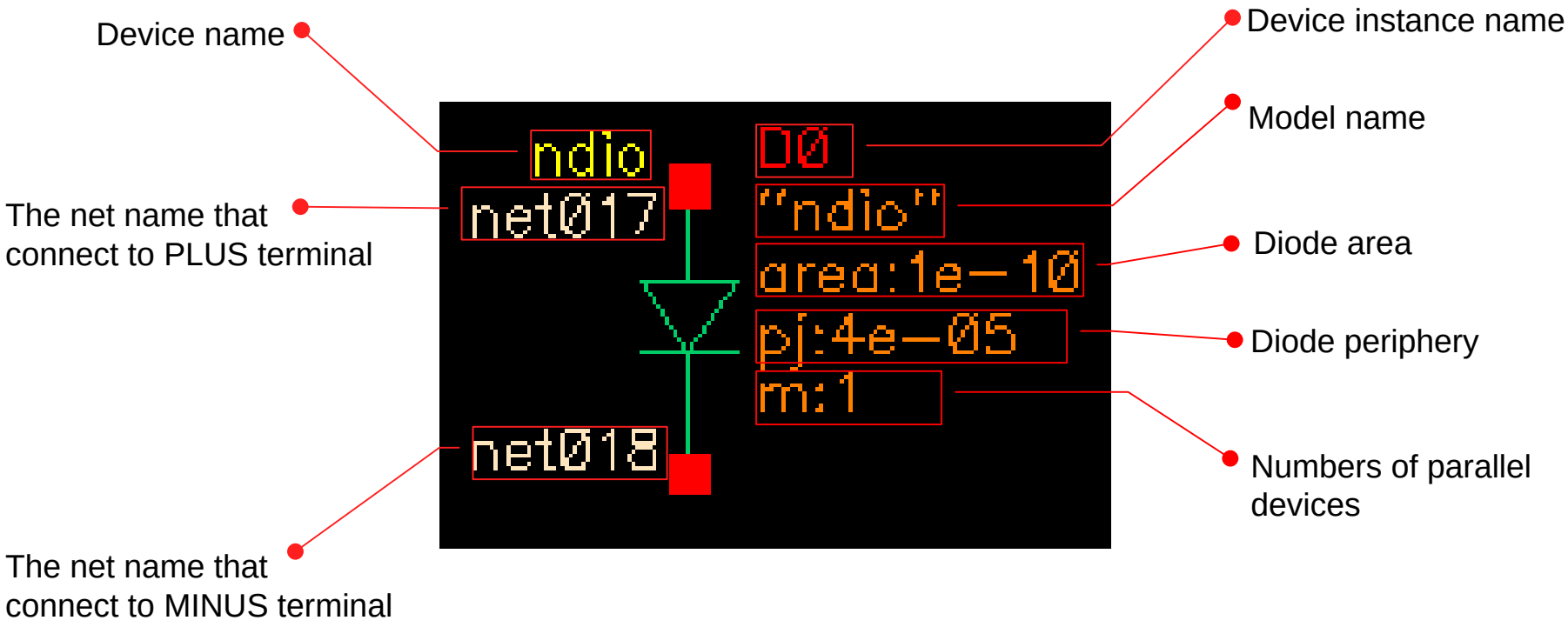
Emitter length

Emitter width

Numbers of parallel devices

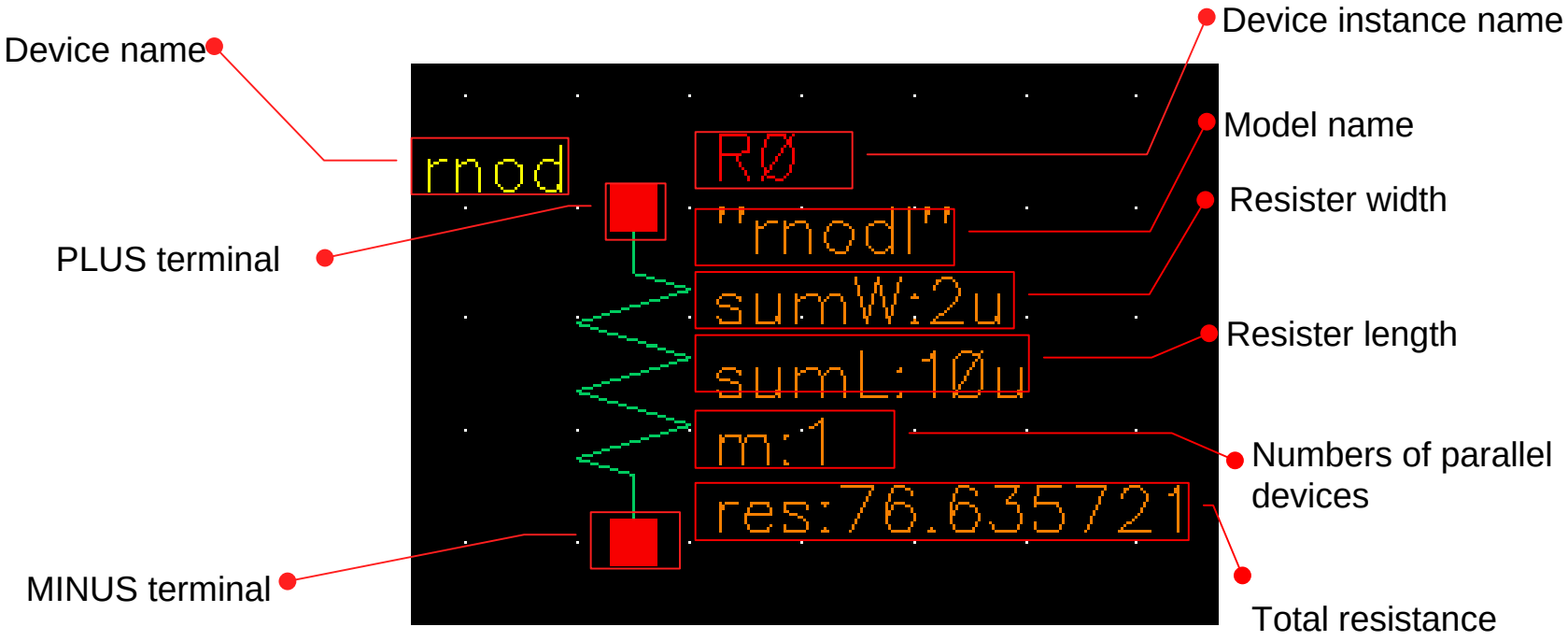
The Symbol Display Information:

- The following figure shows the symbol for a two terminal diode:



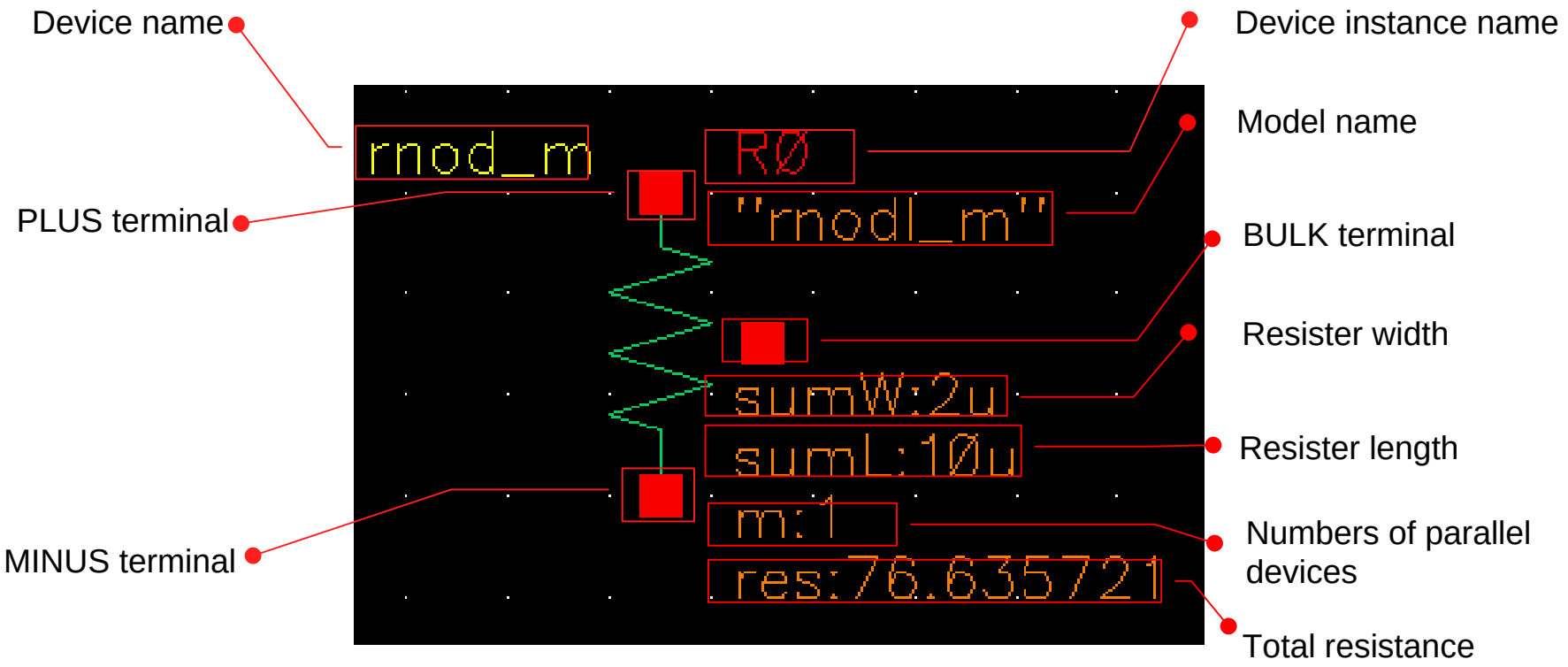
The Symbol Display Information:

- The following figure shows the symbol for a two terminal resister:



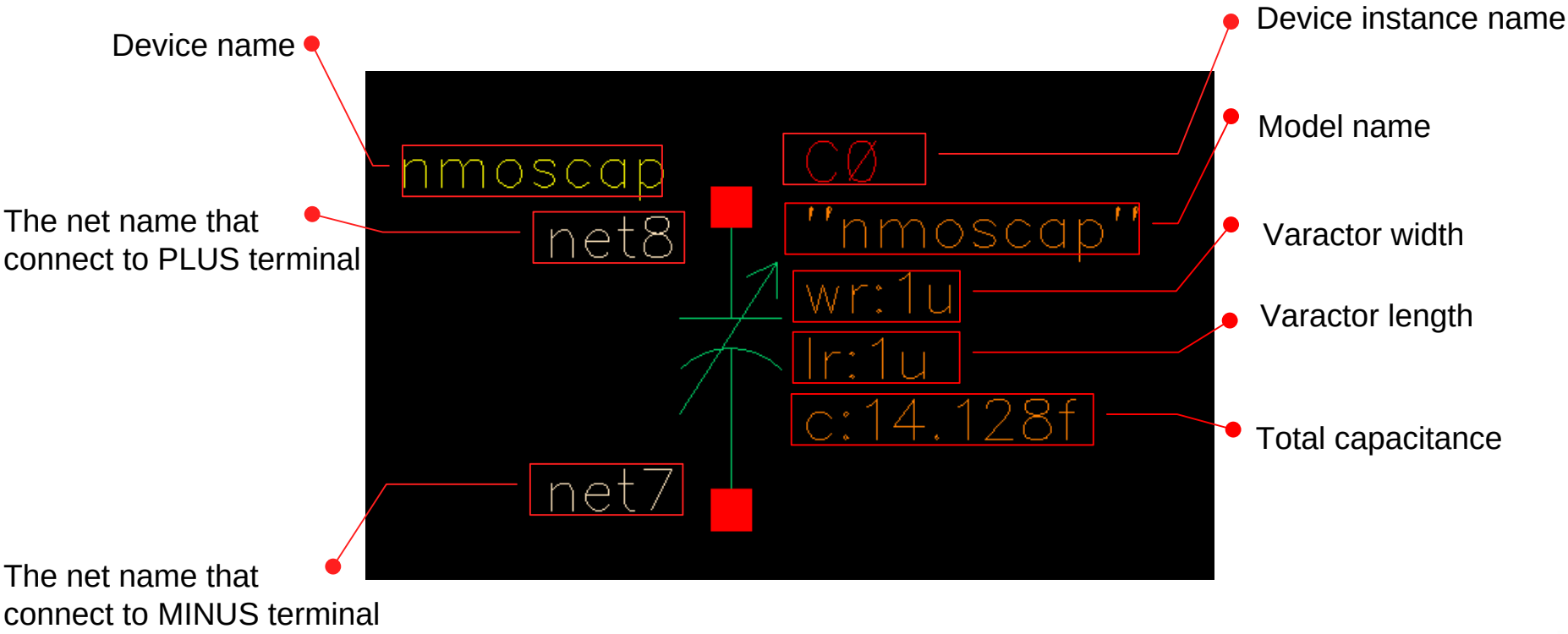
The Symbol Display Information:

- The following figure shows the symbol for a three terminal resister:



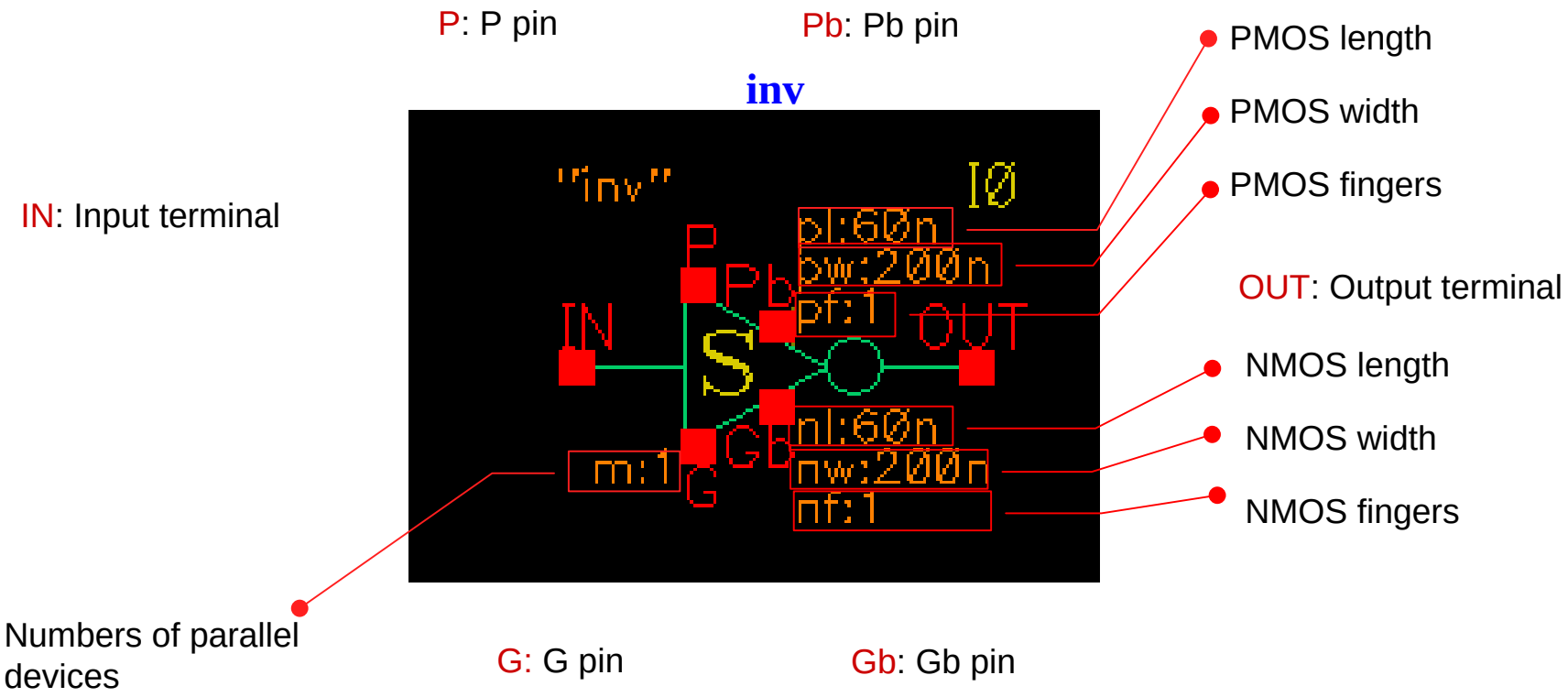
The Symbol Display Information:

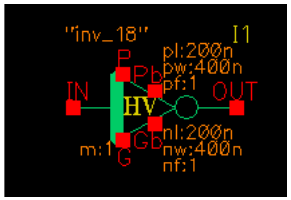
- The following figure shows the symbol for a two terminal varactor:



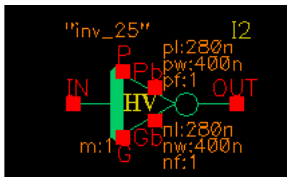
The Symbol Display Information:

- The following figure shows the symbol for a Inverter gate :

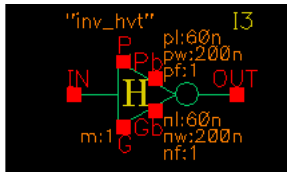




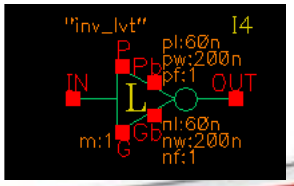
inv_18



inv_25



inv_hvt

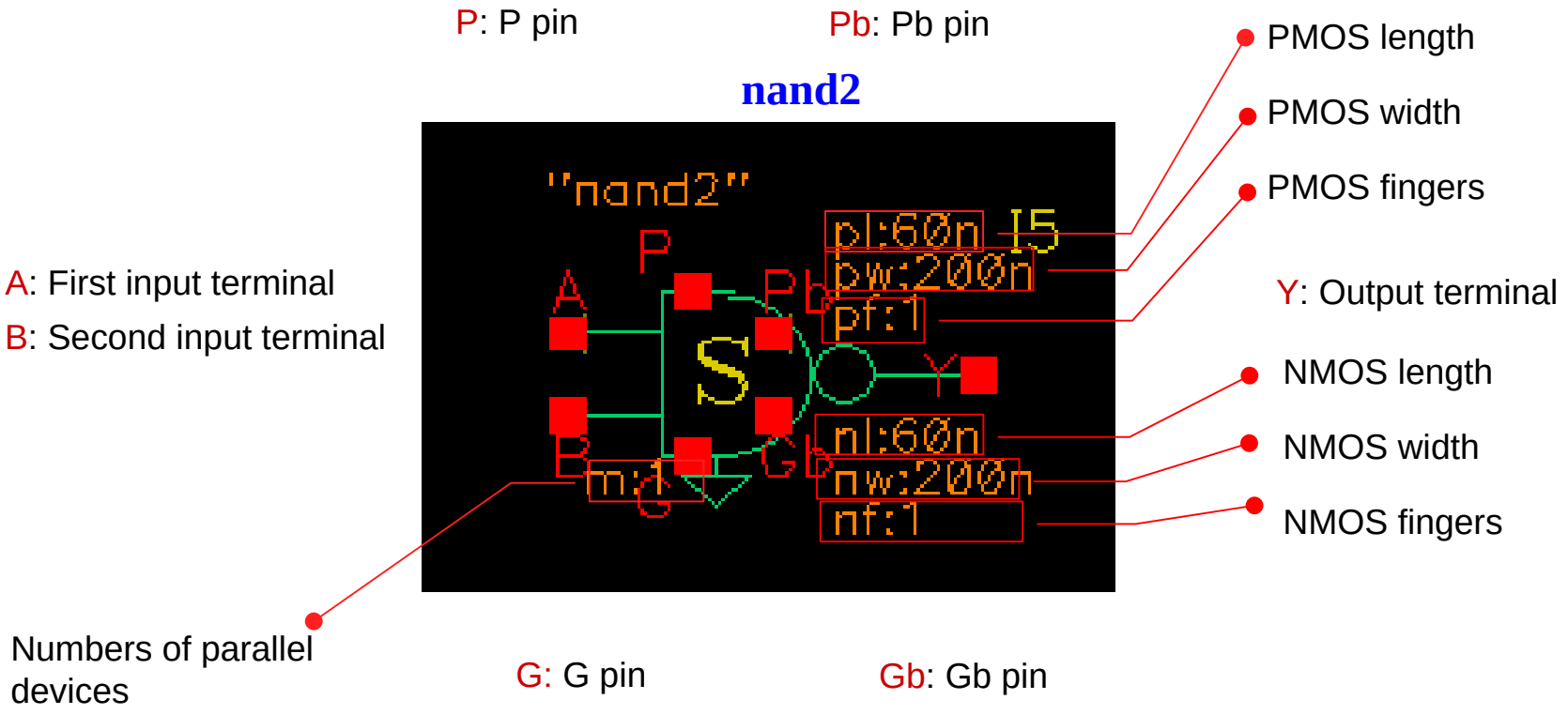


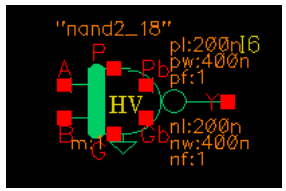
inv_lvt

TSMCN65 PDK Usage Guide

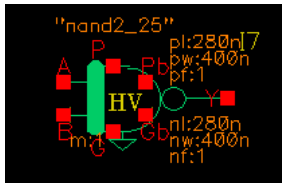
The Symbol Display Information:

- The following figure shows the symbol for a nand-2T gate :

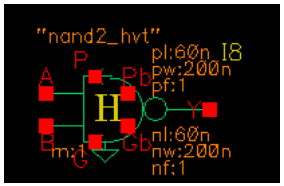




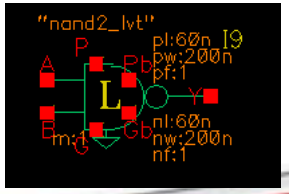
nand_18



nand_25



nand_hvt



nand_lvt

TSMCN65 PDK Usage Guide

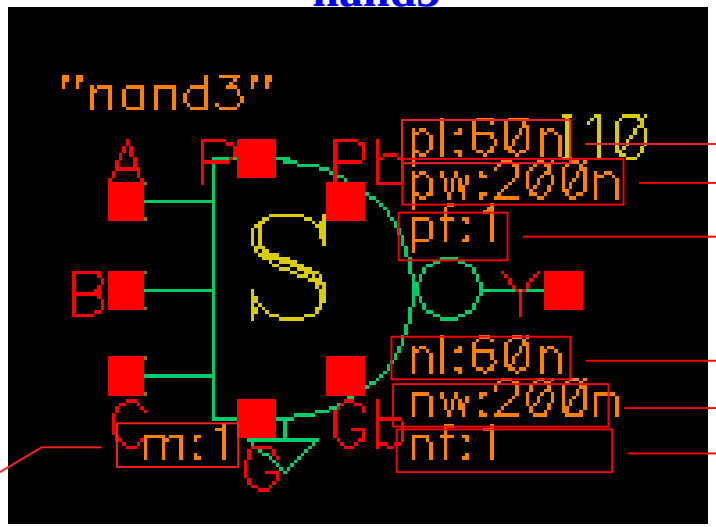
The Symbol Display Information:

- The following figure shows the symbol for a nand-3T gate :

P: P pin

Pb: Pb pin

nand3



PMOS length

PMOS width

PMOS fingers

A: First input terminal

B: Second input terminal

C: Third input terminal

Y: Output terminal

NMOS length

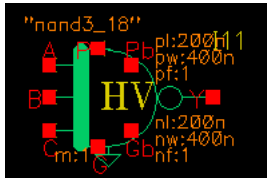
NMOS width

NMOS fingers

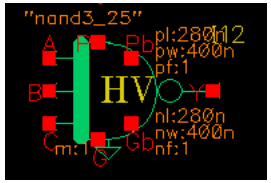
Numbers of parallel devices

G: G pin

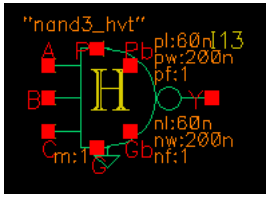
Gb: Gb pin



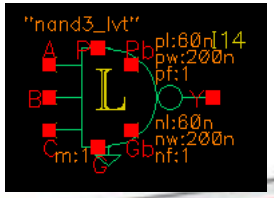
nand3_18



nand3_25



nand3_hvt



nand3_lvt

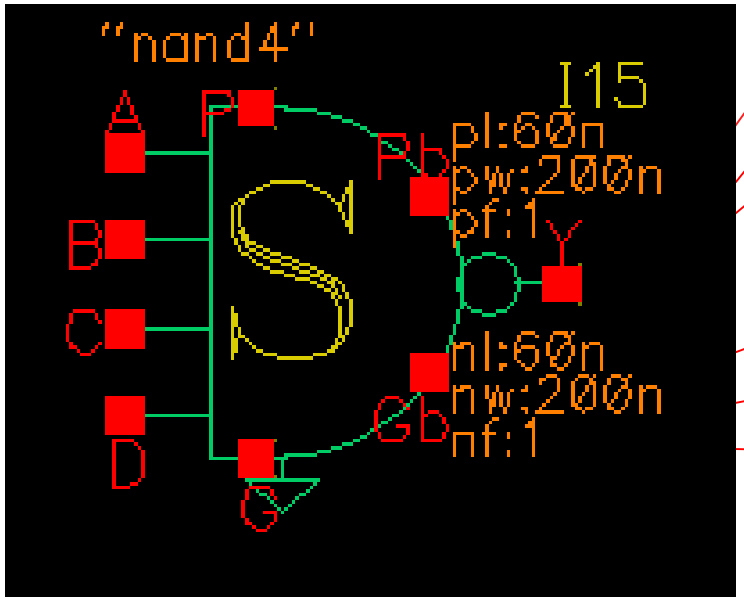
TSMCN65 PDK Usage Guide

- **The Symbol Display Information:**
  - The following figure shows the symbol for a nand-4T gate :

P: P pin

Pb: Pb pin

nand4



A: First input terminal

B: Second input terminal

C: Third input terminal

D: Fourth input terminal

PMOS length

PMOS width

PMOS fingers

Y: Output terminal

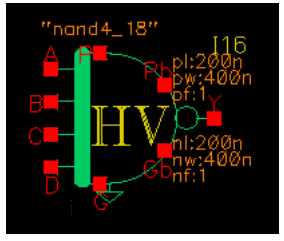
NMOS length

NMOS width

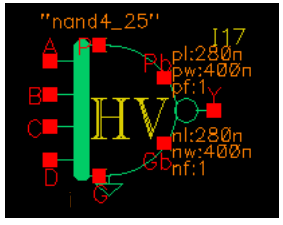
NMOS fingers

G: G pin

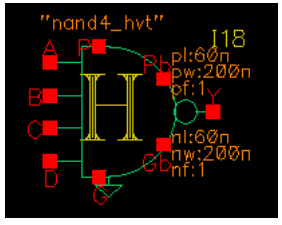
Gb: Gb pin



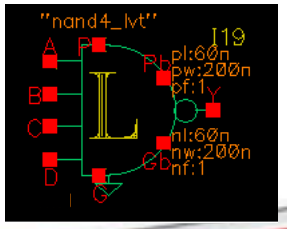
nand4_18



nand4_25



nand4_hvt



nand4_lvt

TSMCN65 PDK Usage Guide

- **The Symbol Display Information:**
  - The following figure shows the symbol for a nor-2T gate :

P: P pin

Pb: Pb pin

PMOS length

PMOS width

PMOS fingers

Y: Output terminal

NMOS length

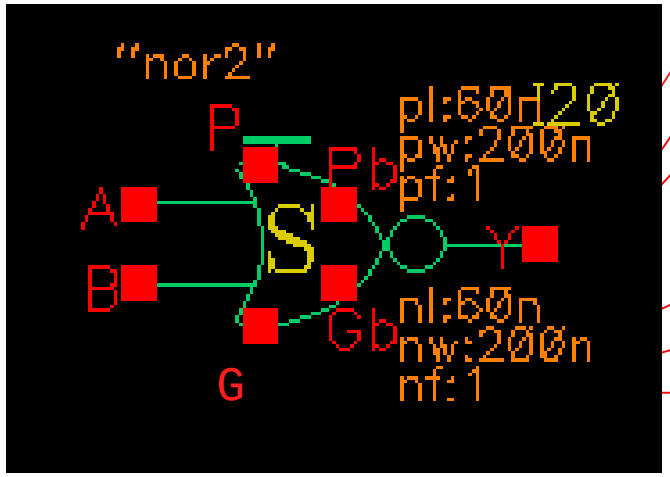
NMOS width

NMOS fingers

A: First input terminal

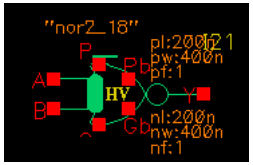
B: Second input terminal

nor2

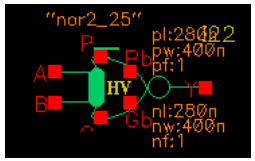


G: G pin

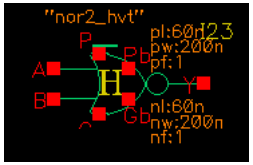
Gb: Gb pin



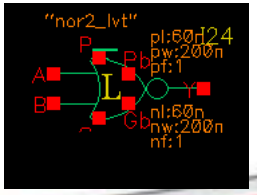
nor2_18



nor2_25



nor2_hvt



nor2_lvt

TSMCN65 PDK Usage Guide

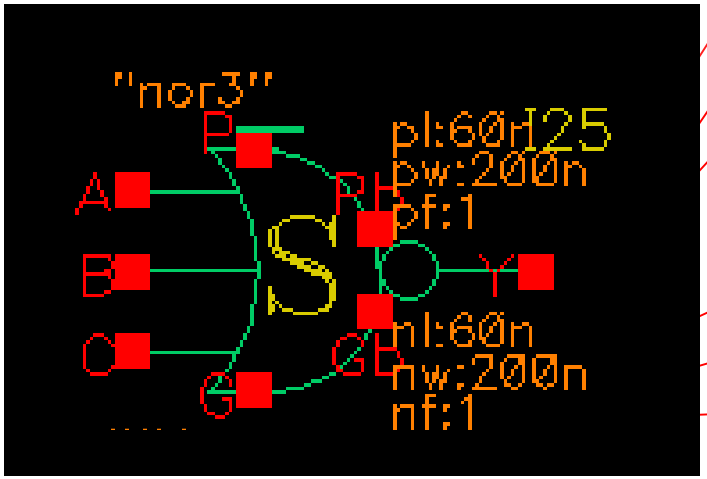
The Symbol Display Information:

- The following figure shows the symbol for a nor-3T gate :

P: P pin

Pb: Pb pin

nor3



PMOS length

PMOS width

PMOS fingers

Y: Output terminal

NMOS length

NMOS width

NMOS fingers

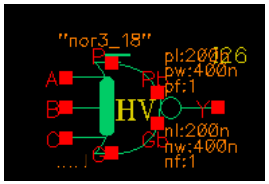
A: First input terminal

B: Second input terminal

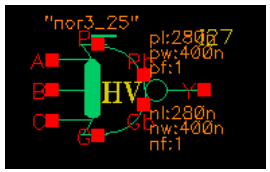
C: Third input terminal

G: G pin

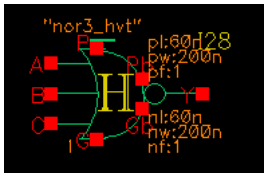
Gb: Gb pin



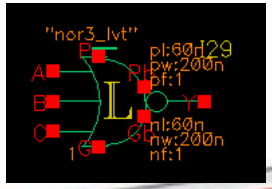
nor3_18



nor3_25



nor3_hvt



nor3_lvt

TSMCN65 PDK Usage Guide

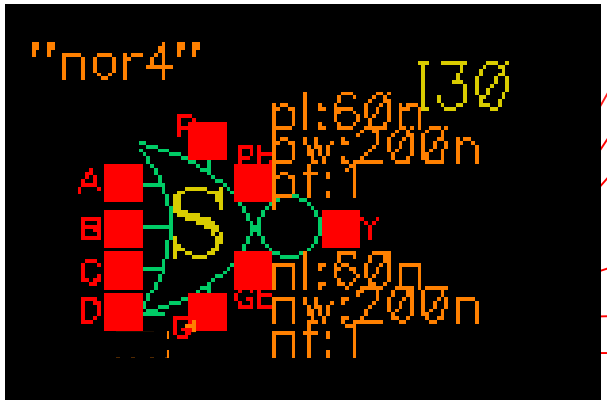
The Symbol Display Information:

- The following figure shows the symbol for a nor-4T gate :

P: P pin

Pb: Pb pin

nor4



PMOS length

PMOS width

PMOS fingers

Y: Output terminal

NMOS length

NMOS width

NMOS fingers

A: First input terminal

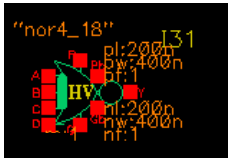
B: Second input terminal

C: Third input terminal

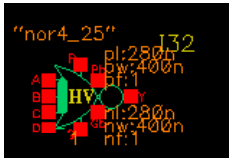
D: Fourth input terminal

G: G pin

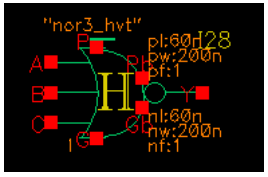
Gb: Gb pin



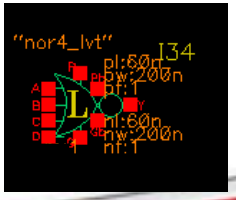
nor4_18



nor4_25



nor4_hvt



nor4_lvt

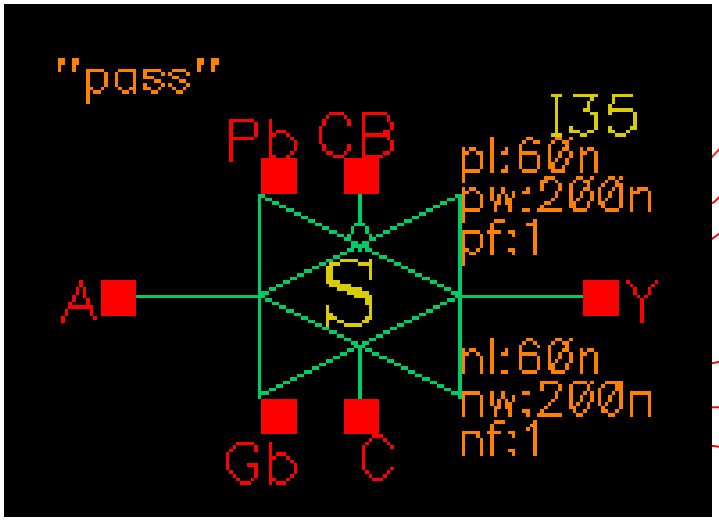
The Symbol Display Information:

- The following figure shows the symbol for a pass gate :

P: P pin

Cb: Cb pin

pass



PMOS length

PMOS width

PMOS fingers

Y: Output terminal

A: First input terminal

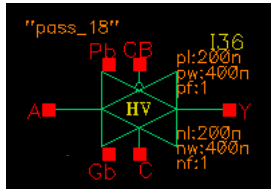
NMOS length

NMOS width

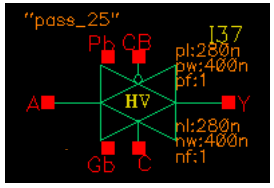
NMOS fingers

G: G pin

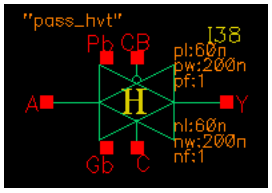
C: C pin



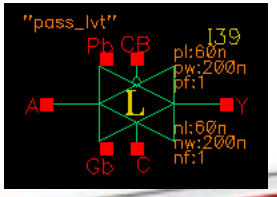
pass_18



pass_25



pass_hvt



pass_lvt

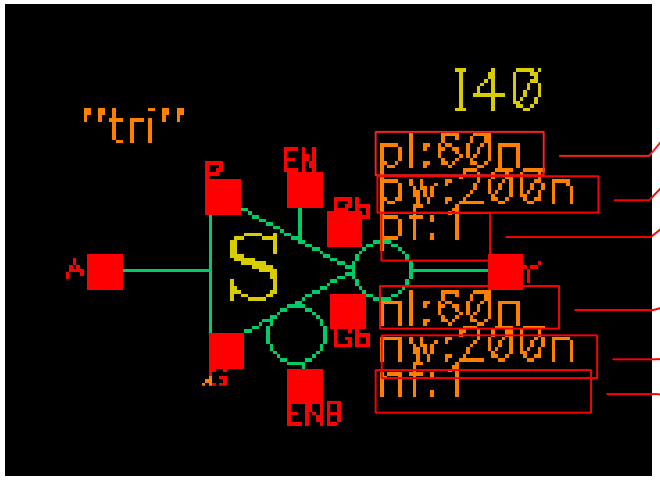
The Symbol Display Information:

- The following figure shows the symbol for a Tri state inverter gate :

P: P pin

Cb: Cb pin

tir



PMOS length

PMOS width

PMOS fingers

Y: Output terminal

A: First input terminal

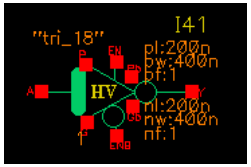
NMOS length

NMOS width

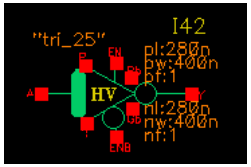
NMOS fingers

G: G pin

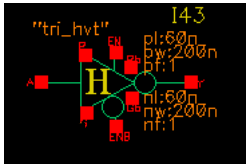
C: C pin



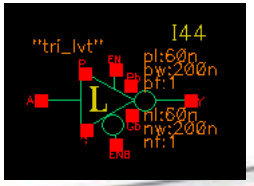
tir_18



tir_25



tir_hvt



tir_lvt

Device Table:

- The devices in this PDK are list as below table:

Categaries	Device
MOS	nch, nch_dnw, nch_18, nch_18_dnw, nch_25, nch_25_dnw, nch33, nch33_dnw, nch_hvt, nch_hvt_dnw, nch_lvt, nch_lvt_dnw,
	nch_mlvt, nch_mlvt_dnw, nch_na, nch_na25, nch_18x, nch_18_dnwx, nch_25_dnwx, nch_33_dnwx, nch_hvt_dnwx,
	nch_lvt_dnwx, nch_mlvt_dnwx, nch_dnwx, nch_nax, nch_na25x, pch, pch_18, pch_25, pch_33, pch_hvt, pch_lvt,
	pch_mlvt, pch_18x, pch_25x, pch_33x, pch_hvtx, pch_lvtx, pch_mlvtx, pchx, nch_25x, nch_33x
MOS_MAC	pch_25_mac, pch_25_macx, pch_33_mac, pch_33_macx, pch_hvt_mac, pch_hvt_macx, pch_lvt_mac, pch_lvt_macx, pch_mac,
	pch_macx, pch_mlvt_mac, pch_mlvt_macx, nch_25_mac, nch_25_macx, nch_33_mac, nch_33_macx, nch_hvt_mac,
	nch_hvt_macx, nch_lvt_mac, nch_lvt_macx, nch_mac, nch_macx, nch_mlvt_mac, nch_mlvt_macx, nch_25_dnw_mac,
	nch_25_dnw_macx, nch_33_dnw_mac, nch_33_dnw_macx, nch_dnw_mac, nch_dnw_macx, nch_hvt_dnw_mac,
	nch_hvt_dnw_macx, nch_lvt_dnw_mac, nch_lvt_dnw_macx, nch_mlvt_dnw_mac, nch_mlvt_dnw_macx
	nch_18_mac, nch_18_macx, nch_18_dnw_mac, nch_18_macx, pch_18_mac, pch_18_macx
MOS_RF	nmos_rf, nmos_rf_25, nmos_rf_hvt, nmos_rf_lvt, nmos_rf_mlvt, nmos_rf_nodnw, nmos_rf_25_nodnw, nmos_rf_hvt_nodnw,
	nmos_lvt_nodnw, nmos_mlvt_nodnw, pmos_rf, pmos_rf_25, pmos_rf_hvt, pmos_rf_lvt, pmos_rf_mlvt, pmos_rf_nw,
	pmos_rf_25_nw, pmos_rf_hvt_nw, pmos_rf_lvt_nw,pmos_rf_mlvt_nw, nmos_rf_18, nmos_rf_18_nodnw, nmos_rf_33,
	nmos_rf_33_nodnw, pmos_rf_18, pmos_rf_18_nw, pmos_rf_33, pmos_rf_33_nw
BJT	pnp, pnp_mis, npn, npn_mis
Diode	ndio, ndio_18, ndio_25, ndio_33, ndio_hvt, ndio_lvt, ndio_mlvt, ndio_na, ndio_na25, nwdio, pwdnw, dnwpsub, dnwpsub,
	ndio_esd, pdio, pdio_18, pdio_25, pdio_33, pdio_hvt, pdio_lvt, pdio_mlvt
Resistor(1)	rm1, rm2, rm3, rm4, rm5, rm6, rm7, rm8, rm9
Resistor(2)	rnod_m, rnodwo,rnodwo_m, rnpoly, rnpoly_m, rnpolywo, rnploywo_m, rnwod, rnwod_m, rnwsti, rnwsti_m, rpod, rpod_m,
	rpod_m, rpodwo, rpodwo_m, rppoly, rppoly_m, rppoly_rf, rppolywo, rppolywo_m, rppolywo_rf

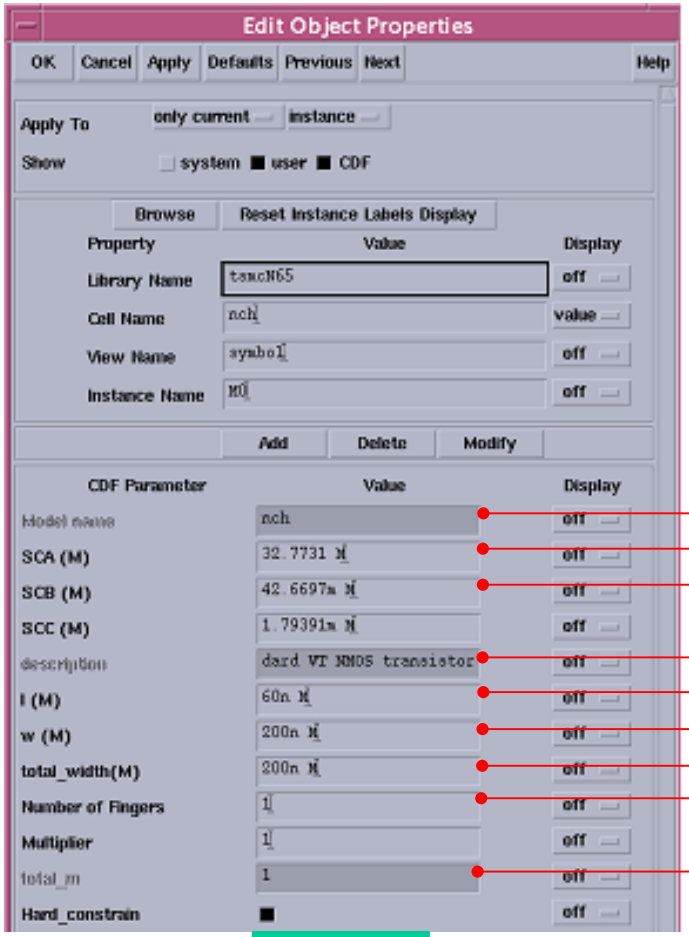
- **Device Table:**

Capacitors	crtmom, crtmom_rf, mimcap, mimcap_um_rf, mimcap_woum_rf, crtmom_mx, mimcap_3t
Varactors	nmoscap, nmoscap_25, moscap_rf, moscap_rf25, moscap_rf_nw, moscap_rf25_nw,
	xjvar, xjvar_nw
Inductors	spiral_std_MU_Z, spiral_sym_MU_Z, spiral_sym_ct_MU_Z, spiral_std_MZA_A, spiral_sym_MZA_A,
	spiral_sym_ct_MZA_A,
Logic Gates	inv, inv_mac, inv_lvt, inv_lvt_mac, inv_hvt, inv_hvt_mac, inv_18, inv_18_mac, inv_25, inv_25_mac, inv_33, inv_33_mac, nand2,
	nand2_mac, nand2_lvt, nand2_lvt_mac, nand2_hvt, nand2_hvt_mac, nand2_18, nand2_18_mac, nand2_25, nand2_25_mac,
	nand2_33, nand2_33_mac, nand3, nand3_mac, nand3_lvt, nand3_lvt_mac,nand3_hvt, nand3_hvt_mac, nand3_18,
	nand3_18_mac, nand3_25, nand3_25_mac, nand3_33, nand3_33_mac, nand4,nand4_mac, nand4_lvt, nand4_lvt_mac,
	nand4_hvt, nand4_hvt_mac, nand4_18, nand4_18_mac, nand4_25, nand4_25_mac, nand4_33, nand4_33_mac, nor2,
	nor2_mac, nor3, nor3_mac, nor3_lvt, nor3_lvt_mac, nor3_hvt, nor3_hvt_mac, nor3_18, nor3_18_mac, nor3_25,
	nor3_25_mac, nar3_33, nar3_33_mac, nor4, nor4_mac, nor4_lvt, nor4_lvt_mac, nor2_lvt, nor2_lvt_mac, nor2_hvt,
	nor2_hvt_mac, nor2_18, nor2_18_mac, nor2_25, nor2_25_mac, nar2_33, nar2_33_mac, nor4_hvt, nor4_hvt_mac, nor4_18,
	nor4_18_mac, nor4_25, nor4_25_mac, nar4_33, nar4_33_mac, tri, tri_mac, tri_lvt, tri_lvt_mac, tri_hvt, tri_hvt_mac, tri_18,
	tri_18_mac, tri_25, tri_25_mac, tri_33, tri_33_mac, pass, pass_mac, pass_lvt, pass_lvt_mac, pass_hvt, pass_hvt_mac,
	pass_18, pass_18_mac, pass_25, pass_25_mac, pass_33, pass_33_mac

TSMCN65 PDK Usage Guide

MOS Parameterized Cell Function Introduction:

- The **schematic** component description format (CDF) parameter in MOS are list as below:



◆**Model name:** Display Model name information.
(These parameters can't be modify in CDF form)

◆**SCA (M):** WPE SCA parameter. - for simulate use

◆**SCB (M):** WPE SCB parameter. - for simulate use

◆**SCC (M):** WPE SCC parameter. - for simulate use

◆**Description:** Display device description.
(These parameters can't be modify in CDF form)

◆**L (M):** Channel length of the device.

◆**W (M):** Channel width of the device.

◆**Total_width(M):** Total channel width of this device, equal to width x fingers.

◆**Number of Fingers_(N):** Numbers of poly fingers.

Check here for more information

◆**Multiplier:** Numbers of parallel MOS device.

Check here for more information

◆**Total_m:** Display numbers of parallel MOS device.
(This parameter can't be modify in CDF form)

◆**Hard_constrain:** This function provides an option to constrain the value for each parameter in this device.

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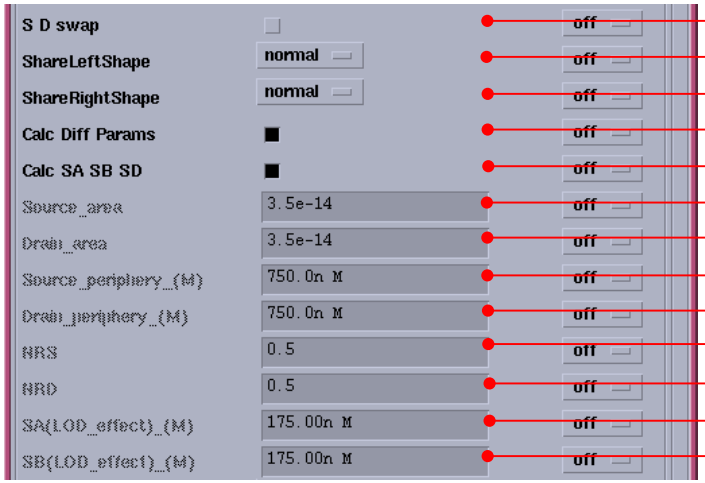
Back to Device Table

MOS Parameterized Cell Function Introduction:

- The **schematic** component description format (CDF) parameter in MOS are list as below:

Front page



◆**S D swap:** Enable this function to swap source and drain terminal.

◆**ShareLeftShape:** (***normal***, ***same***, ***sameExt***, ***small***, ***smallExt***, ***large***, ***largeExt***, ***diff***, ***diffExt***) Preview the left-shape abutment information.

◆**ShareRightShape:** (***normal***, ***same***, ***sameExt***, ***small***, ***smallExt***, ***large***, ***largeExt***, ***diff***, ***diffExt***) Preview the right-shape abutment information.

Check here for more information

◆**Calc Diff Params:** The switch provide to modify simulation parameters.

◆**Calc SA SB SD:** The switch provide to modify simulation SA, SB and SB.

◆**Source_area:** Source area (AS) - for simulate use.

◆**Drain_area:** Drain area (AD) - for simulate use.

◆**Source_periphery:** Source periphery (PS) - for simulate use.

◆**Drain_periphery:** Drain periphery (PD) - for simulate use.

◆**NRS:** Number of squares source resistance – for simulate use.

◆**NRD:** Number of squares drain resistance – for simulate use.

◆**SA(LOD_effect)_(M):** LOD effect parameter – for simulate use.

◆**SA(LOD_effect)_(M):** LOD effect parameter – for simulate use.

Check here for more information

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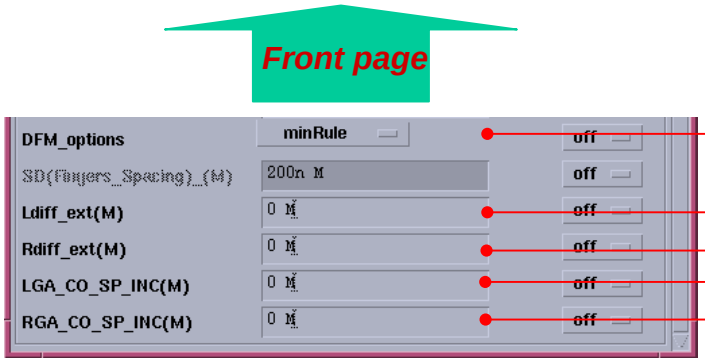
TSMCN65 PDK Usage Guide

MOS Parameterized Cell Function Introduction:

- The **schematic** component description format (CDF) parameter in MOS are list as below:



◆**DFM_options:** (***minRule***, ***DFM***, ***DFM+DRMV11***, ***custom***) This option provide user to select design rule in the layout is follow minimum rule or DFM rule or custom self define.

Check here for more information

◆**SD(Fingers_spacing)_(M):** MOS finger spacing

- for simulate use.

◆**Ldiff_ext:** Increment of left side diffusion.

◆**Rdiff_ext:** Increment of right side diffusion.

◆**LGA_CO_SP_INC(M):** Increment of left side Gate to contact spacing.

◆**RGA_CO_SP_INC(M):** Increment of Right side Gate to contact spacing.

Check here for more information

TSMCN65 PDK Usage Guide

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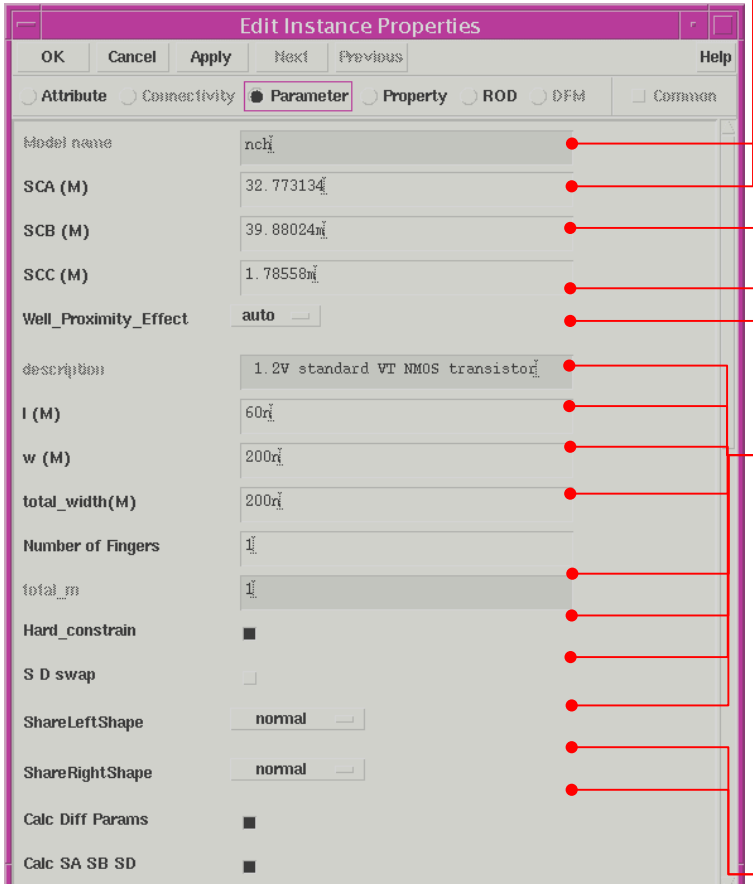
MOS Parameterized Cell Function Introduction:

- The **layout** component description format (CDF) parameter in MOS are list as below:



◆**Model name:** Display Model name information.

◆**SCA (M):** WPE SCA parameter. - for simulate use

◆**SCB (M):** WPE SCB parameter. - for simulate use

◆**SCC (M):** WPE SCC parameter. - for simulate use

◆**Well_Proximity_Effect (M):** Option for WEP - for simulate use
(These are the same parameter that in schematic CDF form)

◆**Description:** Display device description.

◆**L (M):** Channel length of the device.

◆**W (M):** Channel width of the device.

◆**Total_width(M):** Total channel width of this device, equal to width x fingers.

◆**Number of Fingers_(N):** Numbers of poly fingers.

◆**Total_m:** Display numbers of parallel MOS device.

◆**Hard_constrain:** This function provides an option to constrain the value for each parameter in this device.

◆**S D swap:** Enable this function to swap source and drain terminal.

◆**ShareLeftShape:** Display the left-shape abutment information.

◆**ShareRightShape:**Display the right-shape abutment information.
(These are the same parameter that in schematic CDF form)

◆**Calc Diff Params:** The switch provide to modify simulation parameters.

◆**Calc SA SB SD:** The switch provide to modify simulation SA, SB and SB.
(These are the same parameter that in schematic CDF form)

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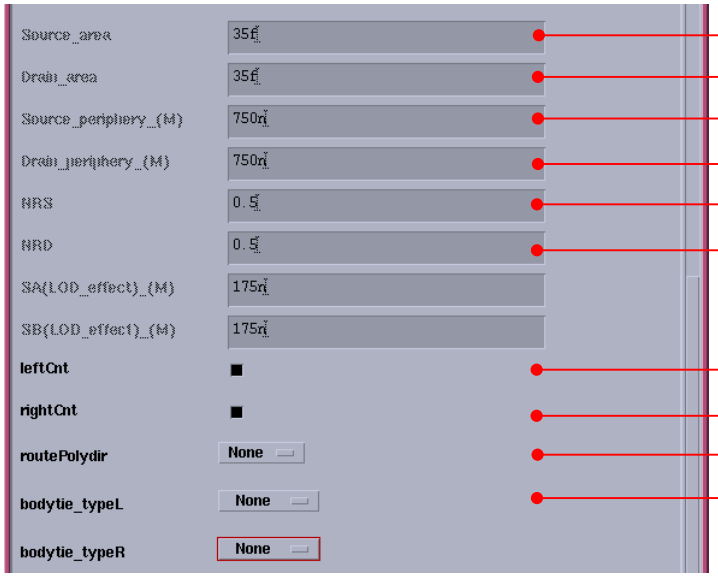
TSMCN65 PDK Usage Guide

MOS Parameterized Cell Function Introduction:

- The **layout** component description format (CDF) parameter in MOS are list as below:

Front page



- **Source_area:** Source area (AS) - for simulate use.
- **Drain_area:** Drain area (AD) - for simulate use.
- **Source_periphery:** Source periphery (PS) - for simulate use.
- **Drain_periphery:** Drain periphery (PD) - for simulate use.
- **NRS:** Number of squares source resistance – for simulate use.
- **NRD:** Number of squares drain resistance – for simulate use.
- **leftCnt:** A option for drawing poly-left diffusion area metal1 connection.
- **RigthCnt:** A option for drawing poly-right diffusion area metal1 connection.

Check here for more information

- **RigthCnt:** A option for drawing inter-poly diffusion metal1 connection.

The function only appears when Number of fingers_(N) > 1

- **routePolydir:**(***None***, ***Top***, ***Bottom***, ***Both***) A option for drawing poly gate connection.

The function only appears when Number of fingers_(N) > 1

Check here for more information

- **route_Source_Drain:**(***Source***, ***Drain***, ***Both***) A option for drawing source and drain connection.

The function only appears when Number of fingers_(N) > 1

Check here for more information

- **bodytie_typeL:** (***None***, ***Integred***, ***Detached***) A option for drawing body connection.
- **bodytie_typeR:** (***None***, ***Integred***, ***Detached***) A option for drawing body connection.

Check here for more information

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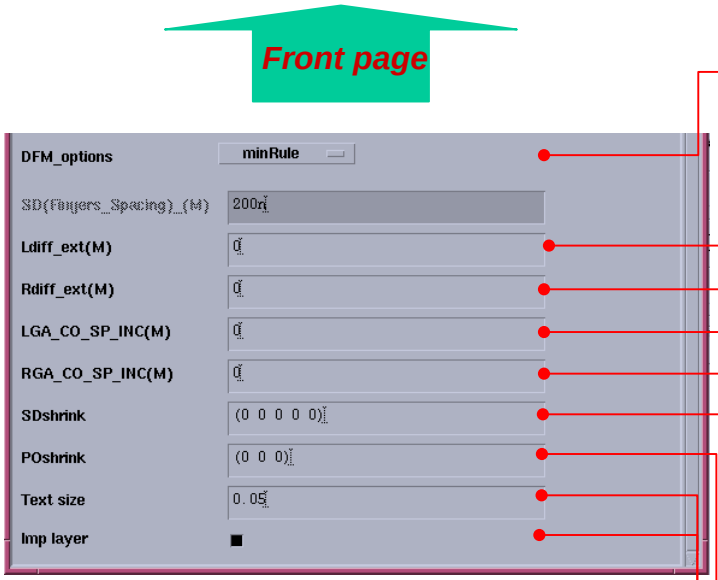
MOS Parameterized Cell function Introduction:

- The **layout** component description format (CDF) parameter in MOS are list as below:



◆**DFM_options:** (***minRule***, ***DFM***, ***DFM+DRMV11***, ***custom***)
This option provide user to select design rule in the layout is follow minimum rule or DFM rule or custom self define.
(This is the same parameter that in schematic CDF form)

◆**fingers_SP_INC(M):** The function is provided to modify poly gate space.
The function only appears when Number of fingers_(N) > 1
Check here for more information

◆**Ldiff_ext:** Increment of left side diffusion.

◆**Rdiff_ext:** Increment of right side diffusion.

◆**LGA_CO_SP_INC(M):** Increment of left side Gate to contact spacing.

◆**RGA_CO_SP_INC(M):** Increment of Right side Gate to contact spacing.
(These are the same parameter that in schematic CDF form)

◆**SDshrink:** The function is provided to modify the metal dimension on source or drain area.
Check here for more information

◆**POshrink:** The function provide a option for well implant.
Check here for more information

◆**Text size:** The function can modify the font value in layout view.

◆**Imp layer:** The function provide a option for well implant.

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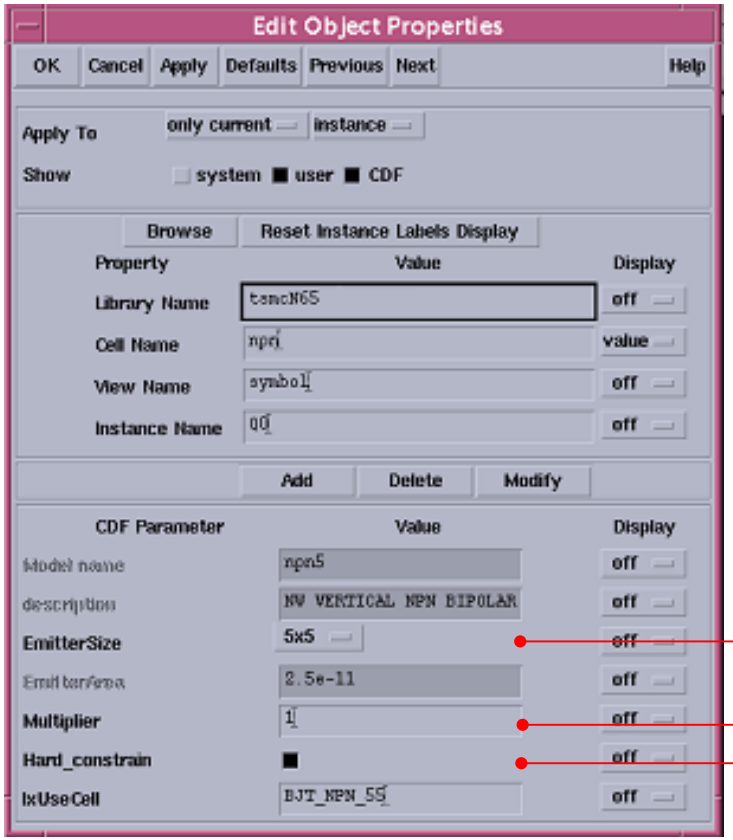
BJT Parameterized Cell Function Introduction:

- The **schematic** component description format (CDF) parameter in BJT are list as below:



◆**Model name:** Display model name information.

◆**Description:** Display device description.
(These parameter can't be modify in CDF form)

◆**EmitterSize:** (***2X2***, ***5X5***, ***10X10***) Select the bjt dimension in design layout.
Check here for more information

◆**EmitterArea:** Display the bjt emitter area.
(This parameter can't be modify in CDF form)

◆**Multiplier:** Numbers of parallel MOS device.
Check here for more information

◆**Hard_constrain:** This function provides an option to constrain the value for each parameter in this device.

◆**IxUseCell:** Display the layout cell name.
(This parameter can't be modify in CDF form)

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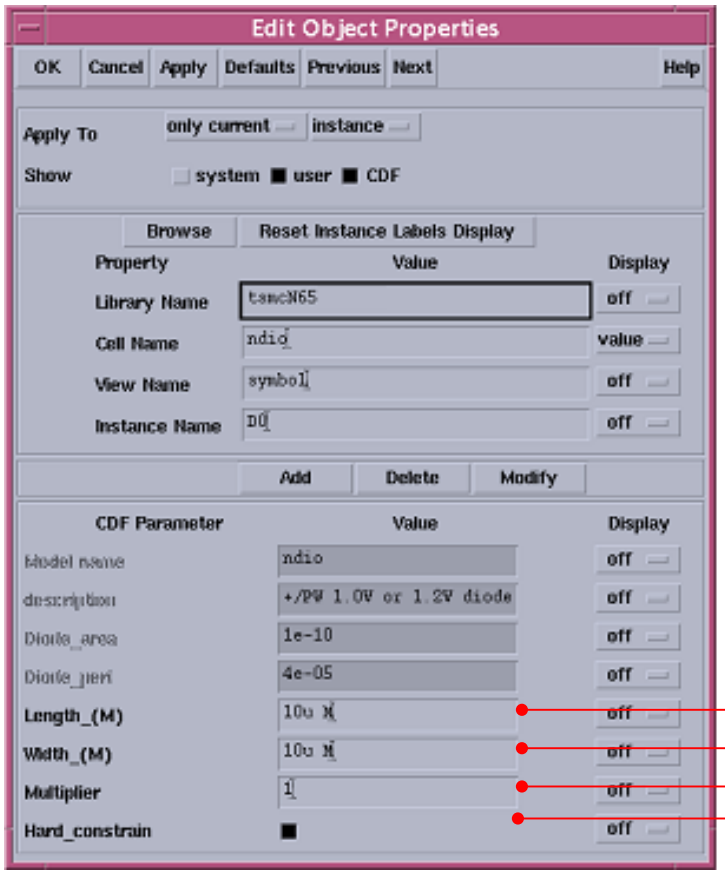
TSMCN65 PDK Usage Guide

Diode Parameterized Cell Function Introduction:

- The **schematic** component description format (CDF) parameter in Diode are list as below:



- **Model name:** Display model name information.
- **Description:** Display device description.
- **Diode_area:** Display the diode area.
- **Diode peri:** Display the diode periphery.

(These parameter can't be modify in CDF form)

- **Length_(M):** Junction length of the device.
- **Width_(M):** Junction Width of the device.
- **Multiplier:** Numbers of parallel Diode device.

Check here for more information

- **Hard_constrain:** This function provides an option to constrain the value for each parameter in this device.

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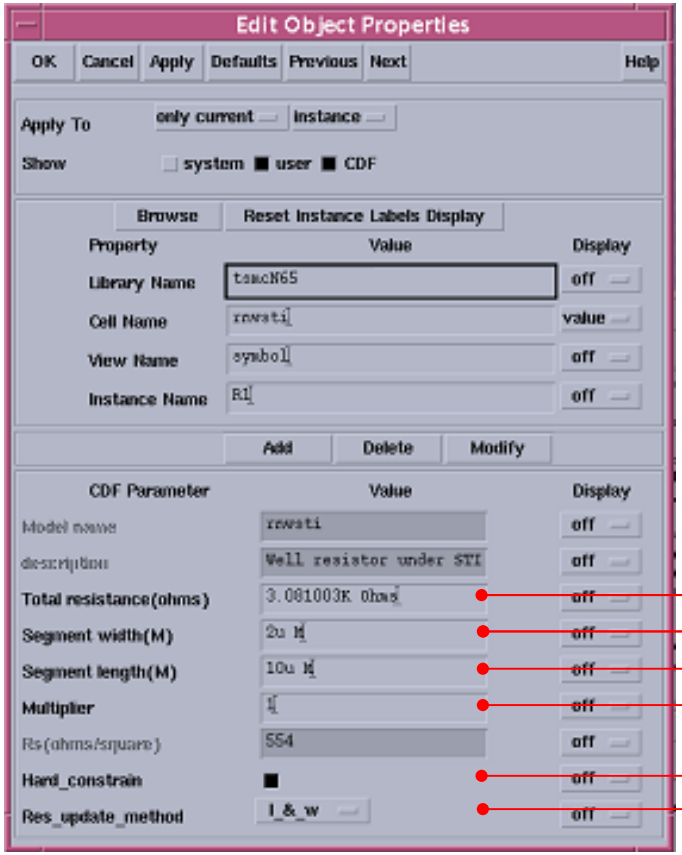
TSMCN65 PDK Usage Guide

Resistance (1) Parameterized Cell Function Introduction:

- The **schematic** component description format (CDF) parameter in resistance are list as below:



◆**Model name:** Display model name information.

◆**Description:** Display device description.

(These parameter can't be modify in CDF form)

◆**Total resistance(ohms):** Device resistance value.

◆**Segment width(M):** Device segment width.

◆**Segment length(M):** Device segment length.

Check here for more information

◆**Multiplier:** Numbers of parallel Diode device.

Check here for more information

◆**Rs(ohms/square):** Display the device Rs value.

(This parameter can't be modify in CDF form)

◆**Hard_constrain:** This function provides an option to constrain the value for each parameter in this device.

◆**Res_update_method:** (***l_&_W***, ***Res_&_W***) Res update method, please review segment width and segment length function.

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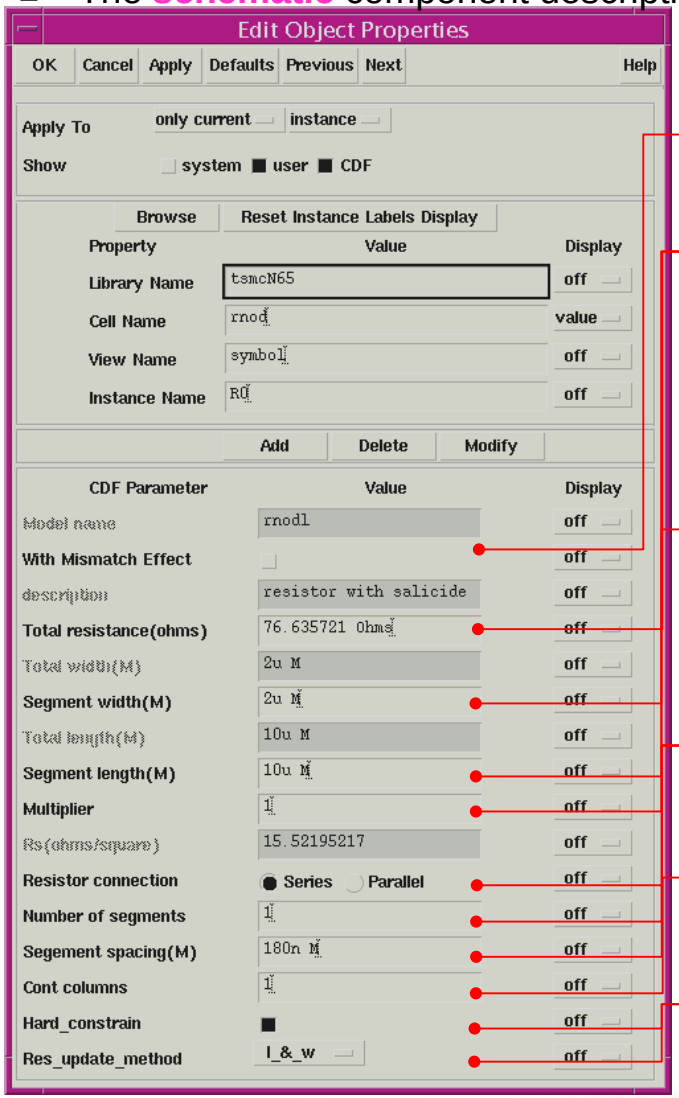
Resistance(2) Parameterized Cell Function Introduction:

- The schematic component description format (CDF) parameter in resistance are list as below:



- **Model name:** Display model name information.
- **Description:** Display device description.
- **With Mismatch Effect:** Option for run mismatch effect
- **Total resistance(ohms):** Device resistance value.
- **Segment width(M):** Device segment width.
- **Segment length(M):** Device segment length.

Check here for more information

- **Total width(M):** Display the device segment width.
- **Total length(M):** Display the device segment length.
- (These parameter can't be modify in CDF form)
- **Multiplier:** Numbers of parallel Diode device.

Check here for more information

- **Rs(ohms/square):** Display the device Rs value.

(This parameter can't be modify in CDF form)

- **Resistor connection:** Device resistance value.
- **Number of segment:** Device segment width.
- **Segment spacing(M):** Device segment length.

Check here for more information

- **Cont columns:** Device contact columns number.

Check here for more information

- **Hard_constrain:** This function provides an option to constrain the value for each parameter in this device.
- **Res_update_method:** (***l_&_W***, ***Res_&_W***) Res update method, please review segment width and segment length function.

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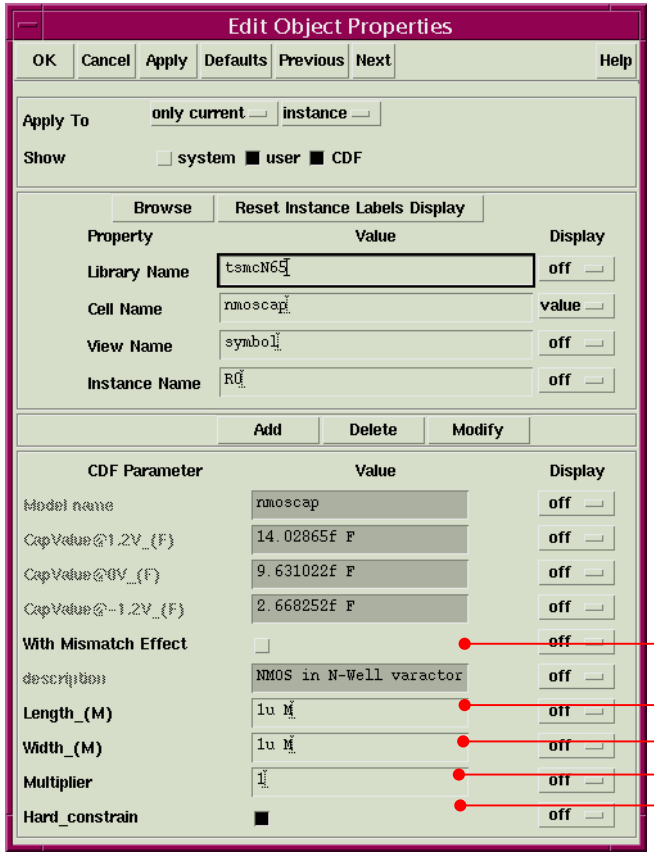
TSMCN65 PDK Usage Guide

Varactor Parameterized Cell Function Introduction:

- The **schematic** component description format (CDF) parameter in varactor are list as below:



◆**Model name:** Display model name information.

◆**Description:** Display device description.

(These parameter can't be modify in CDF form)

◆**CapValue@1.2V(F):** Device capacitance information.

◆**CapValue@0V(F):** Device capacitance information.

◆**CapValue@-1.2V(F):** Device capacitance information.

(These parameter can't be modify in CDF form)

◆**With Mismatch Effect:** Option for run mismatch effect

◆**Width(M):** Device width.

◆**Length(M):** Device length.

◆**Multiplier:** Numbers of parallel Varactor device.

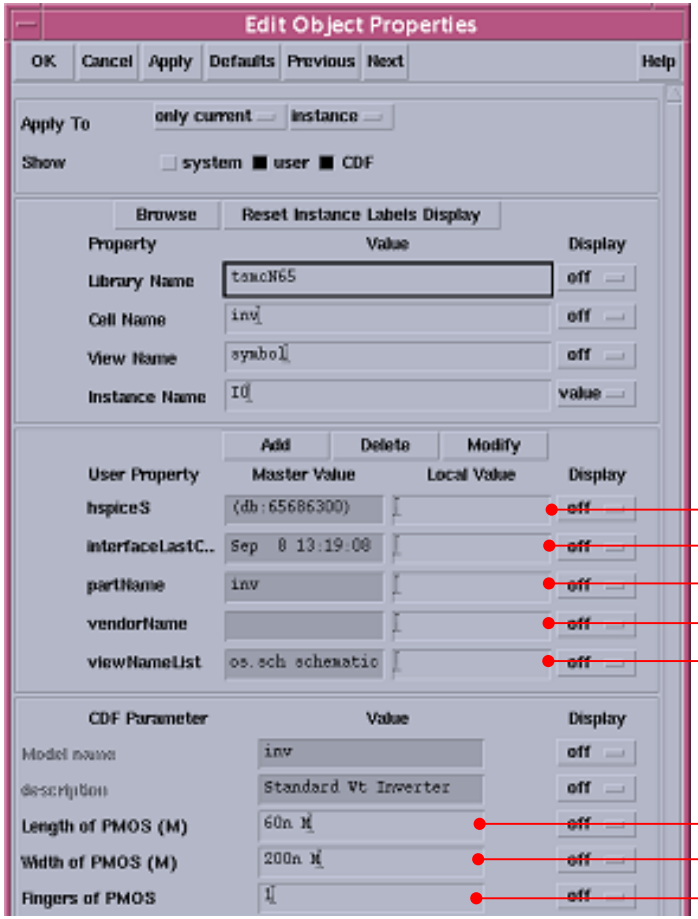
Check here for more information

◆**Hard_constrain:** This function provides an option to constrain the value for each parameter in this device.

Back to Device Table

LogicGate Parameterized Cell Function Introduction:

- The **schematic** component description format (CDF) parameter in inverter are list as below:



- ◆**HspiceS:** Display model name information.
- ◆**InterfaceLastC..:** Display device description.
- ◆**partName:** Display device description.
- ◆**vendorName:** Display device description.
- ◆**viewNameList:** Display device description.

(Cell information)

- ◆**Model name:** Display model name information.
- ◆**Description:** Display device description.

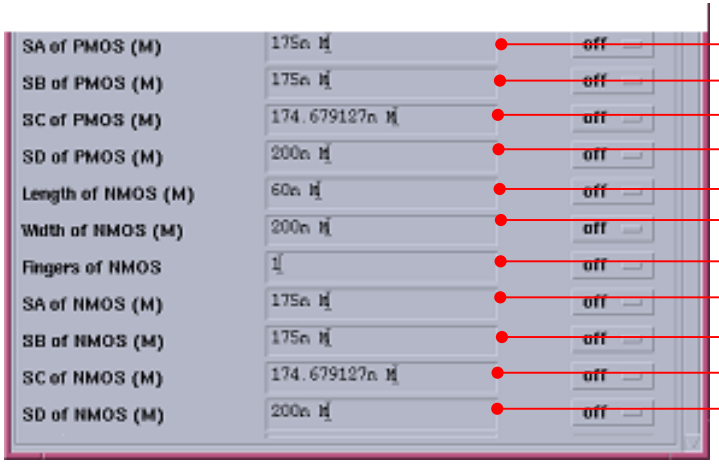
(These parameter can't be modify in CDF form)

- ◆**Length of PMOS(M):** All pmos length.
- ◆**Width of PMOS(M):** All pmos width.
- ◆**Fingers of PMOS(M):** All pmos fingsers.

Back to Device Table

LogicGate Parameterized Cell Function Introduction:

- The **schematic** component description format (CDF) parameter in varactor are list as below:



- **SA of PMOS(M):** All pmos SA.
- **SB of PMOS(M):** All pmos SB. .
- **SC of PMOS(M):** All pmos SC.
- **SD of PMOS(M):** All pmos SD.
- **Length of NMOS(M):** All nmos length.
- **Width of NMOS(M):** All nmos width.
- **Fingers of NMOS(M):** All nmos fingsers.
- **SA of NMOS(M):** All nmos SA.
- **SB of NMOS(M):** All nmos SB. .
- **SC of NMOS(M):** All nmos SC.
- **SD of NMOS(M):** All nmos SD.

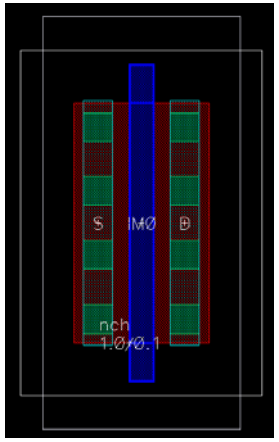
Back to Device Table

CDF Parameter Description

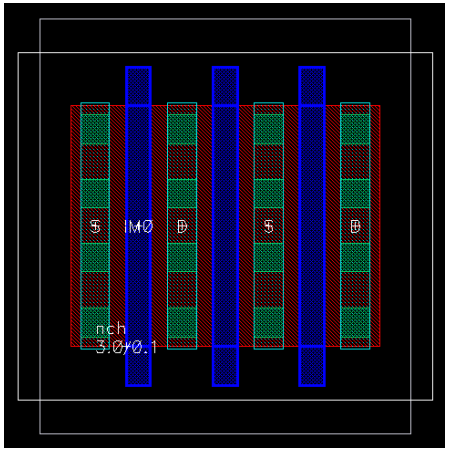
TSMCN65 PDK Usage Guide

- **The function of Number of Fingers_(N)**
  - This parameter provide user to increment the poly finger numbers.

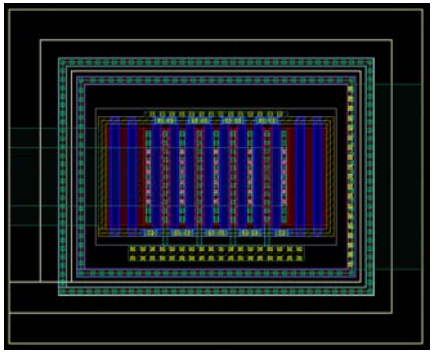
Number of Fingers_(N)=1



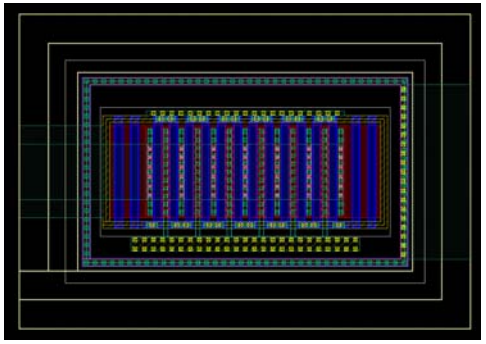
Number of Fingers_(N) =3



Number of Fingers_(N)=8



Number of Fingers_(N) =12

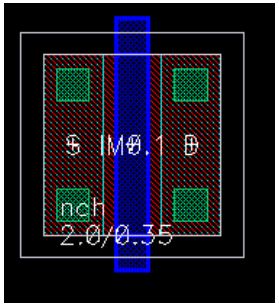


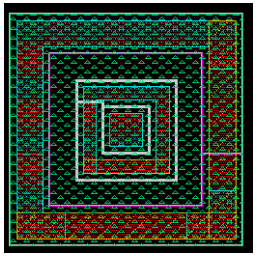
Check here to back to MOS

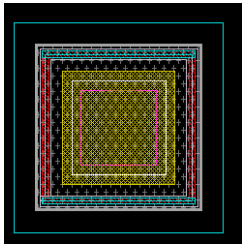
The function of Multiplier

- This parameter provide user to increment the parallel device.

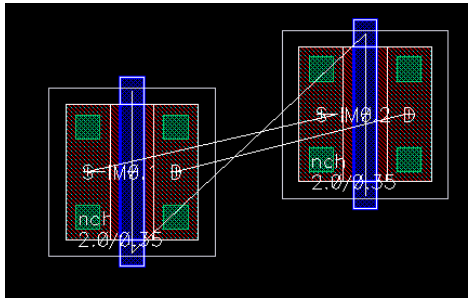
Multiplier = 1

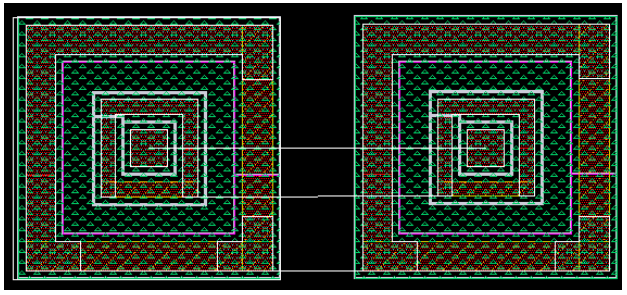


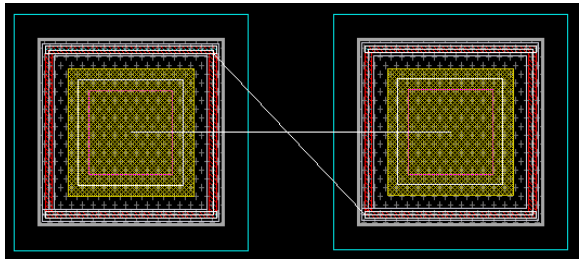




Multiplier = 2



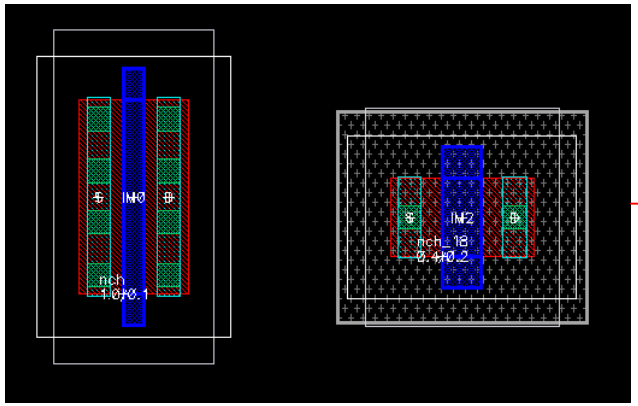




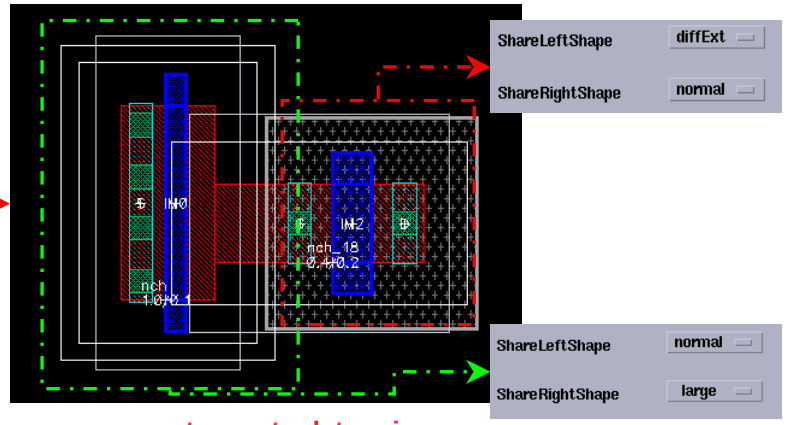
Check here to back to MOS
Check here to back to BJT
Check here to back to Diode
Check here to back to Resistance(1)
Check here to back to Resistance(2)
Check here to back to Varactor

The function of ShareLeftShape and ShareRightShape

- These functions provide user to preview the device difference before and after abutment. When the user abuts the devices in layout view, system will auto determine the abutment type of the both device. These two function can be selected to preview the layout but they can't be used to determine abutment type. Please check ***Appendix A*** for the details

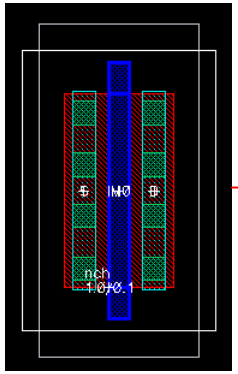


Abut the two device in the layout view

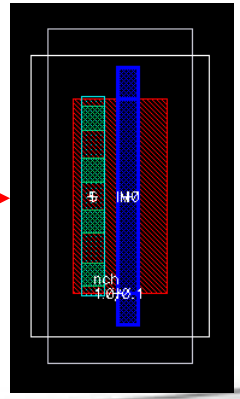


system auto determine

User select for review only



Change the ShareRightShape to ***large***

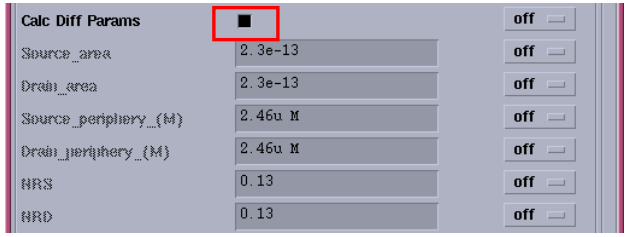


Check here to back to MOS

The function of Calc Diff Params and Calc SA SB SD

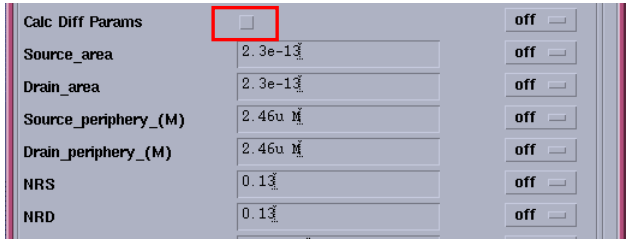
- It's a switch for input simulation parameter that include area of source (AS), area of drain (AD), periphery of source (PS), periphery of drain (PD), number of squares source resistance (NRS), number of squares drain resistance (NRD) and LOD effect parameter- SA , SB and SD. Modify those parameters only influence simulation conditions, the design layout will not have any different.

Calc Diff Params is enable



Parameters can't be modify

Calc Diff Params is disable



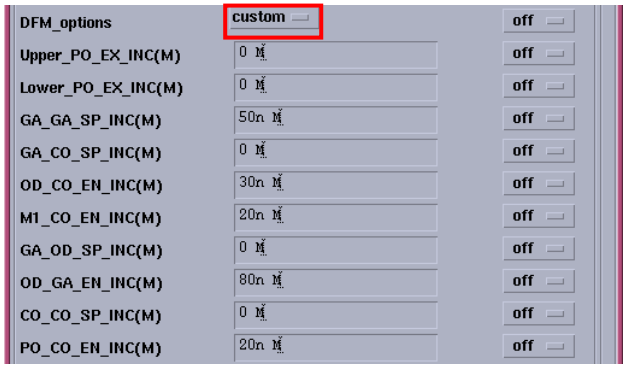
Parameters can be modify

Check here to back to MOS

The function of DFM_options

- This option provides user to select design rule in the layout is follow minimum rule or DFM rule[1] or custom self define. When User selects the ***custom*** selection, the input spaces appear below the DFM_options. ***DFM*** option will check PO.EX.1, PO.EN.1.R, PO.EN.2.R and PO.EN.3.R rule.

DFM_options = *custom*



CDF parameter V.S Design Rule number comparison table

CDF Parameter	TSMC N65 Design Rule
Upper_PO_EX_INC(M)	PO.EX.1
Lower_PO_EX_INC(M)	PO.EX.1
GA_GA_SP_INC(M)	PO.S.11.R
GA_CO_SP_INC(M)	CO.EN.3.R
OD_CO_EN_INC(M)	CO.EN.1.R
M1_CO_EN_INC(M)	M1.EN.1.R
GA_OD_SP_INC(M)	PO.S.5.R
OD_GA_EN_INC(M)	PO.EX.2.R
CO_CO_SP_INC(M)	-
PO_CO_EN_INC(M)	CO.EN.3.R
NW_GA_SP_INC(M)	PO.EN.1.R PO.EN.3.R
OD2_GA_EN_INC(M)	PO.EN.2.R

Design rule document number:T-N65-CL-DR-001

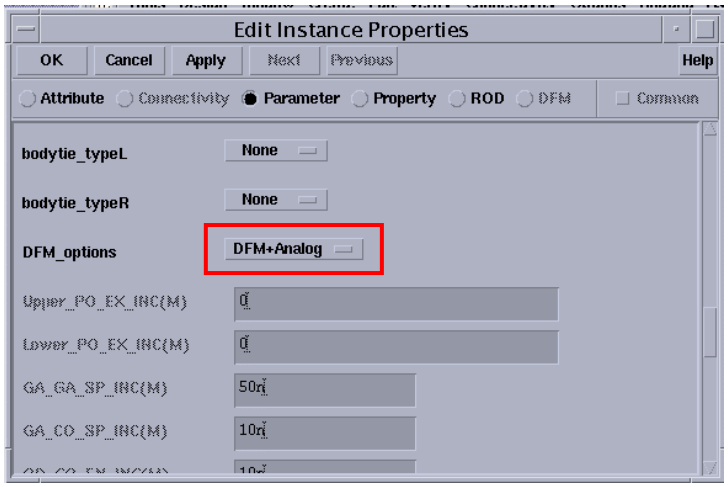
Check here to back to MOS

[1] Design For Manufacturing (DFM) rule is a recommendation rule that TSMC provide customer to minimized process variation and yield benefit. For the details, please review TSMC 65NM CMOS Design RULE.

The function of DFM_options

- This option provides user to select design rule in the layout is follow minimum rule or DFM rule[1] or custom self define. When User selects the ***custom*** selection, the input spaces appear below the DFM_options. The ***DFM+Analog*** will check PO.EN.1m, PO.EN.2m, PO.EN.3m.

DFM_options = *DFM+Analog*



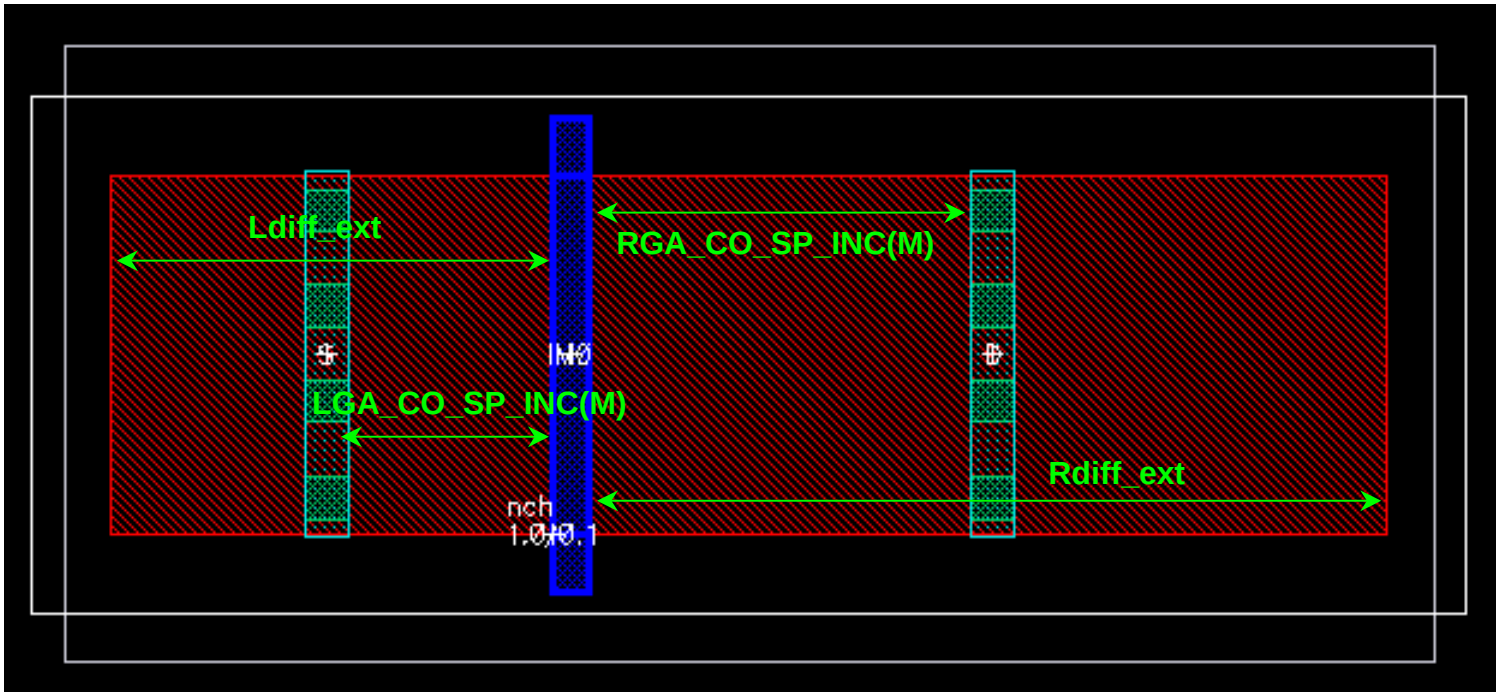
DFM+Analog option check the following rules:

PO.EN.1m >= 1.0um
PO.EN.2m >= 2.0um
PO.EN.3m >= 1.5um

Check here to back to MOS

[1] Design For Manufacturing (DFM) rule is a recommendation rule that TSMC provide customer to minimized process variation and yield benefit. For the details, please review TSMC 65NM CMOS Design RULE.

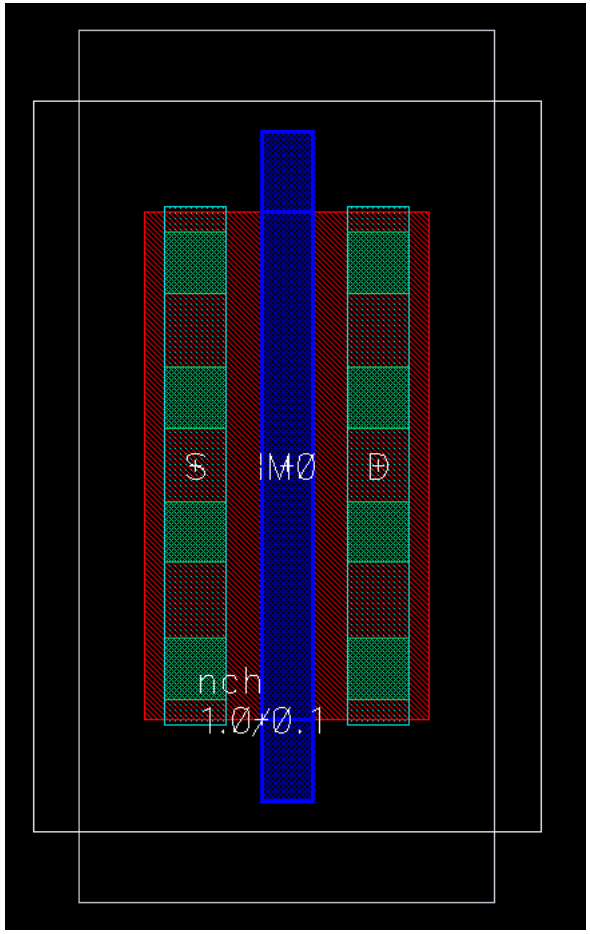
- **The function of Ldiff_ext, Rdiff_ext, LGA_CO_SP_INC(M) and RGA_CO_SP_INC(M)**
  - Those function provide user to increment the area of left and right diffusion and the space form contact to poly.



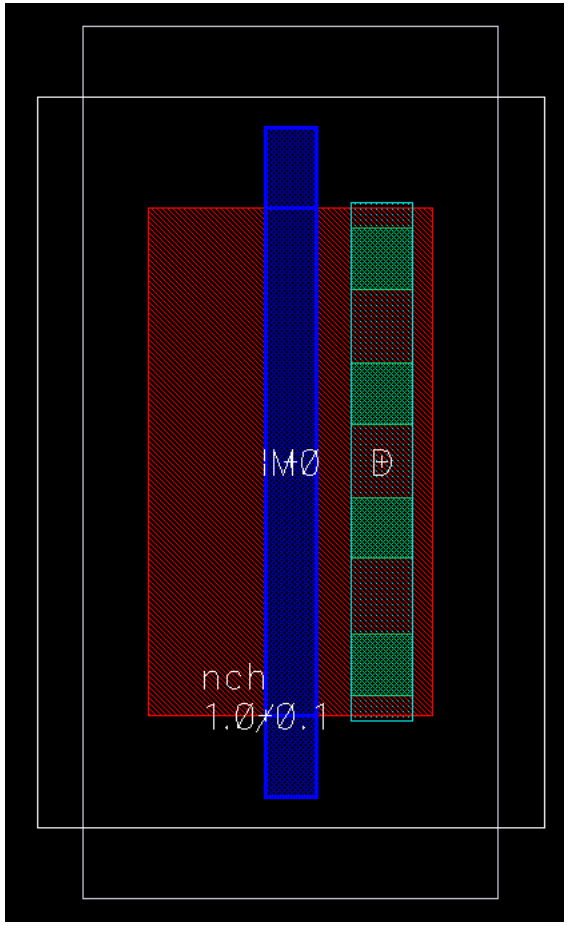
Check here to back to MOS

- **The function of leftCnt, RightCnt**
  - The function provide a option for drawing poly-left (right) diffusion area metal1 connect

leftCnt is enable



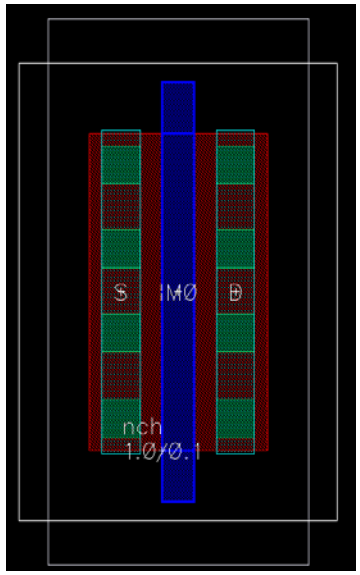
leftCnt is Disable



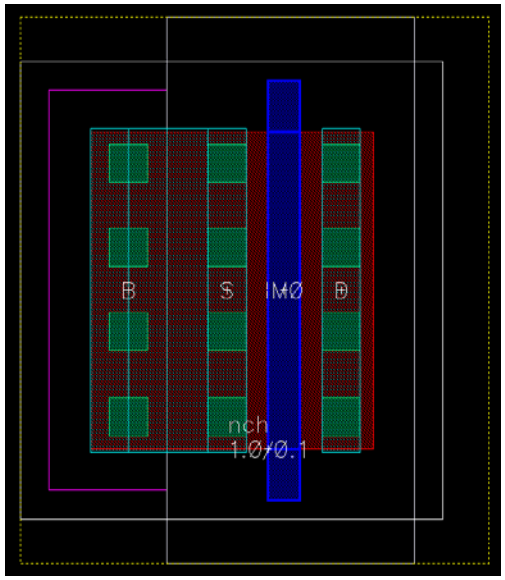
Check here to back to MOS

- **The function of bodytie_typeL and bodytie_typeR**
  - The function provide a option for drawing body connection at the device left (bodytie_typeL) or device right (bodytie_typeR).

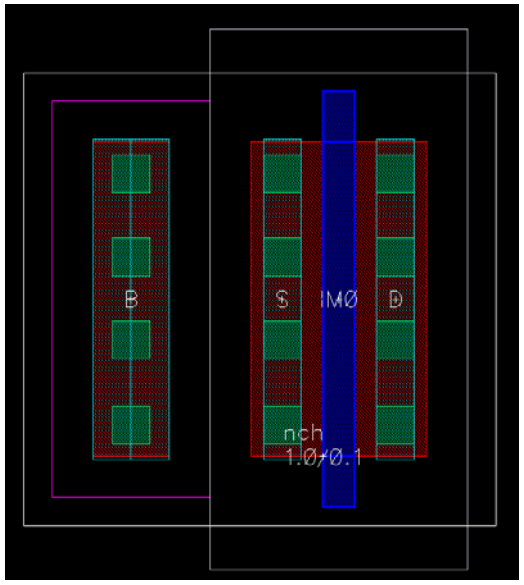
bodytie_typeL is *None*



bodytie_typeL is *Integred*



bodytie_typeL is *Detached*



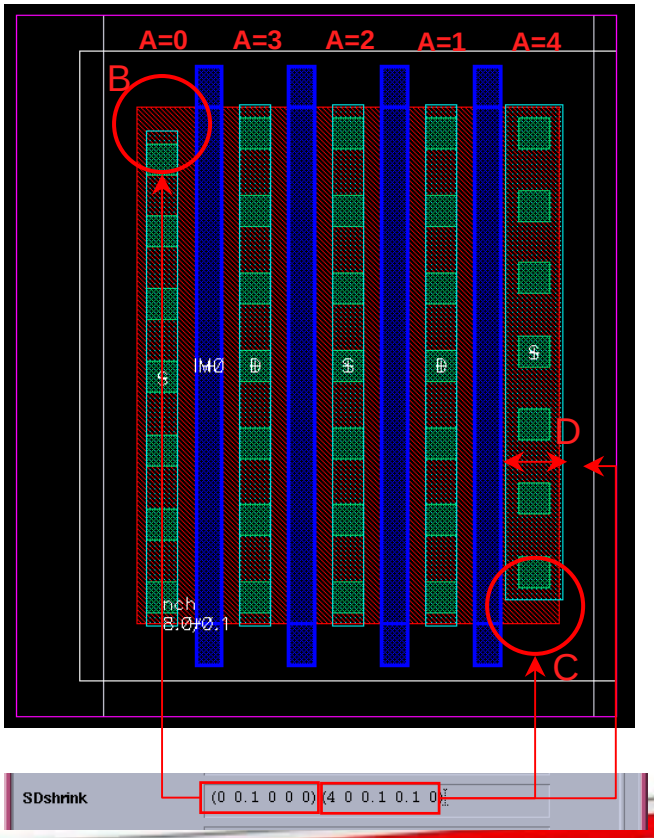
Check here to back to MOS

The function of SDshrink

- The function is provided to modify the metal dimension on source or drain area. It's a list include five numbers. The first number is used to decide which metal user want to modify. The second number is used to shrink the dimension of the metal top. The third number is used to shrink the dimension of the metal bottom. The fourth number is used to extend the dimension of the metal left and right. The fifth number is used to increment the contact space in the metal. The number of these five numbers must be positive and the unit is micrometer.

(A B C D E)

A:select metal
B:metal Top shrink
C:metal bottom shrink
D:metal side shrink
E:contact space increment



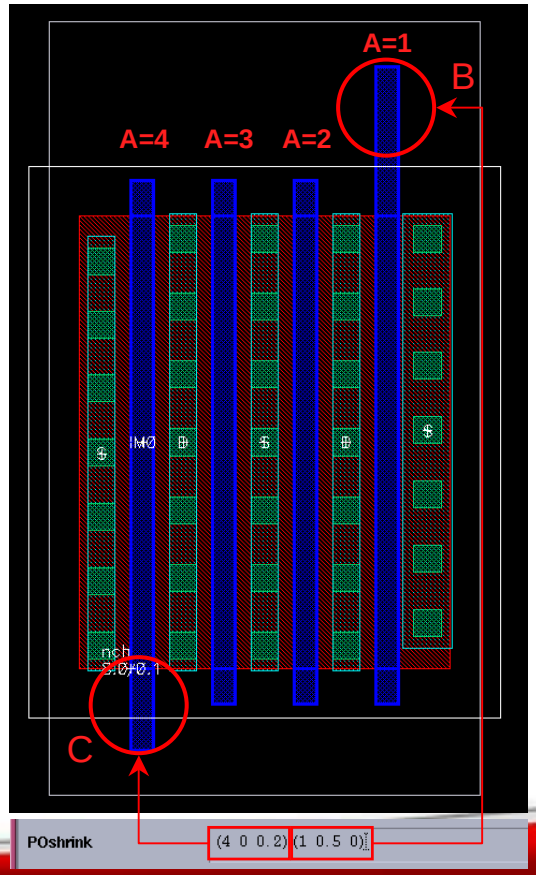
Check here to back to MOS

The function of POshrink

- The function is provided to modify the poly gate dimension. It's a list include three numbers. The first number is used to decide which metal user want to modify. The second number is used to shrink the dimension of the poly gate top. The third number is used to shrink the dimension of the poly gate bottom. The number of these three numbers must be positive and the unit is micrometer.

(A B C)

A:select poly gate
B:poly gate top shrink
C:poly gate bottom shrink

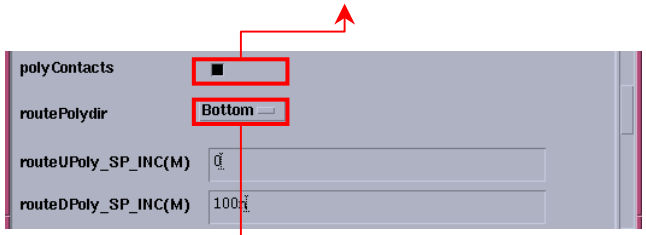


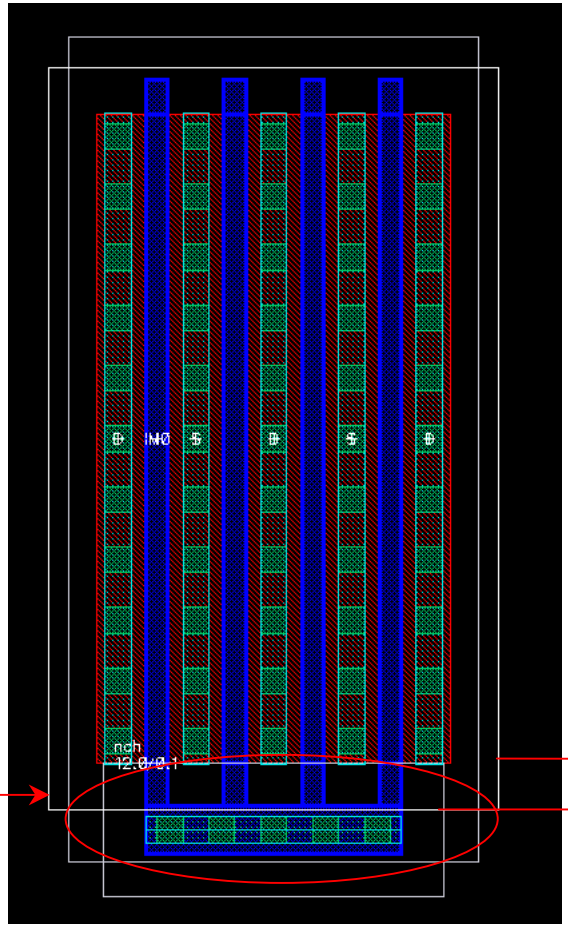
Check here to back to MOS

The function of routePolydir

- The function is provided to drawing poly gate connection. The space of poly gate connection to the diffusion area can be modify by routeUPoly_SP_INC(M) and routeDPoly_SP_INC(M) [2].

The **poly Contacts** will appear when **routPolydir** doesn't None. It is an option to draw contact on the poly gate.





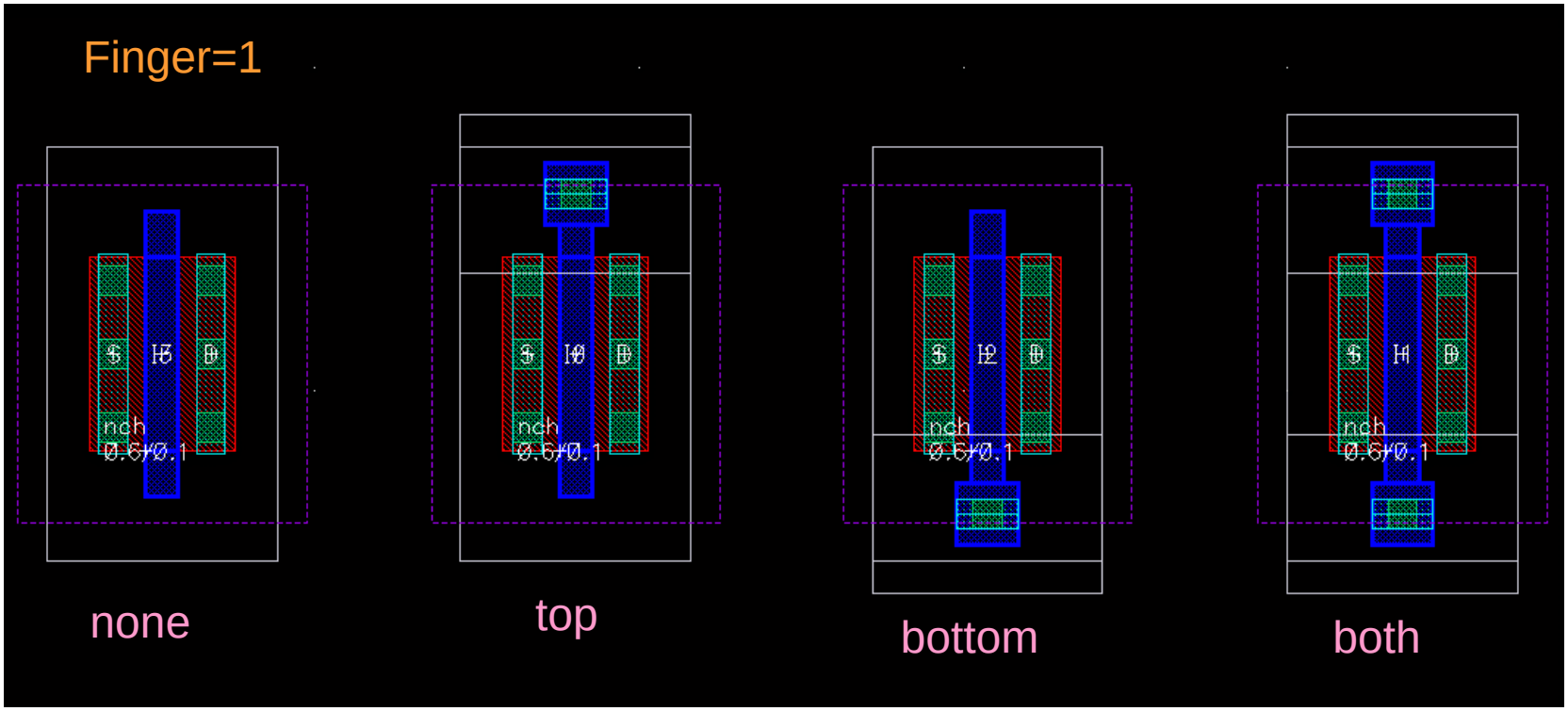
PO.S.6(design rule)
+ routeDPoly_SP_INC

Check here to back to MOS

[2] The routeUPoly_SP_INC(M) and routeDPoly_SP_INC(M) only appear when routePolydir doesn't ***None.***

The function of routePolydir

- The function is suggest to use in multi-finger. If customer use only one finger and turn on the routePolydir none/top/bottom/both direction. It will shows the following layout.



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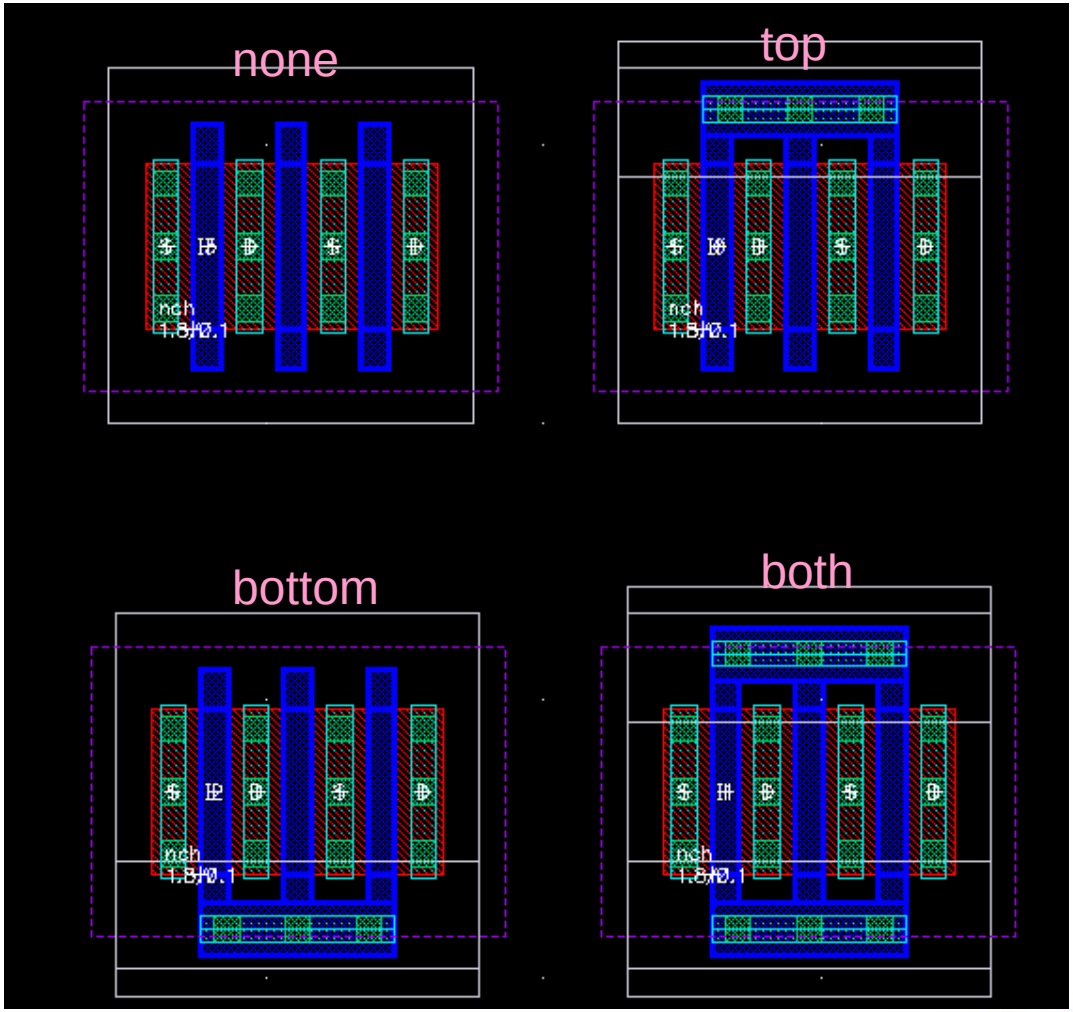
The function of routePolydir

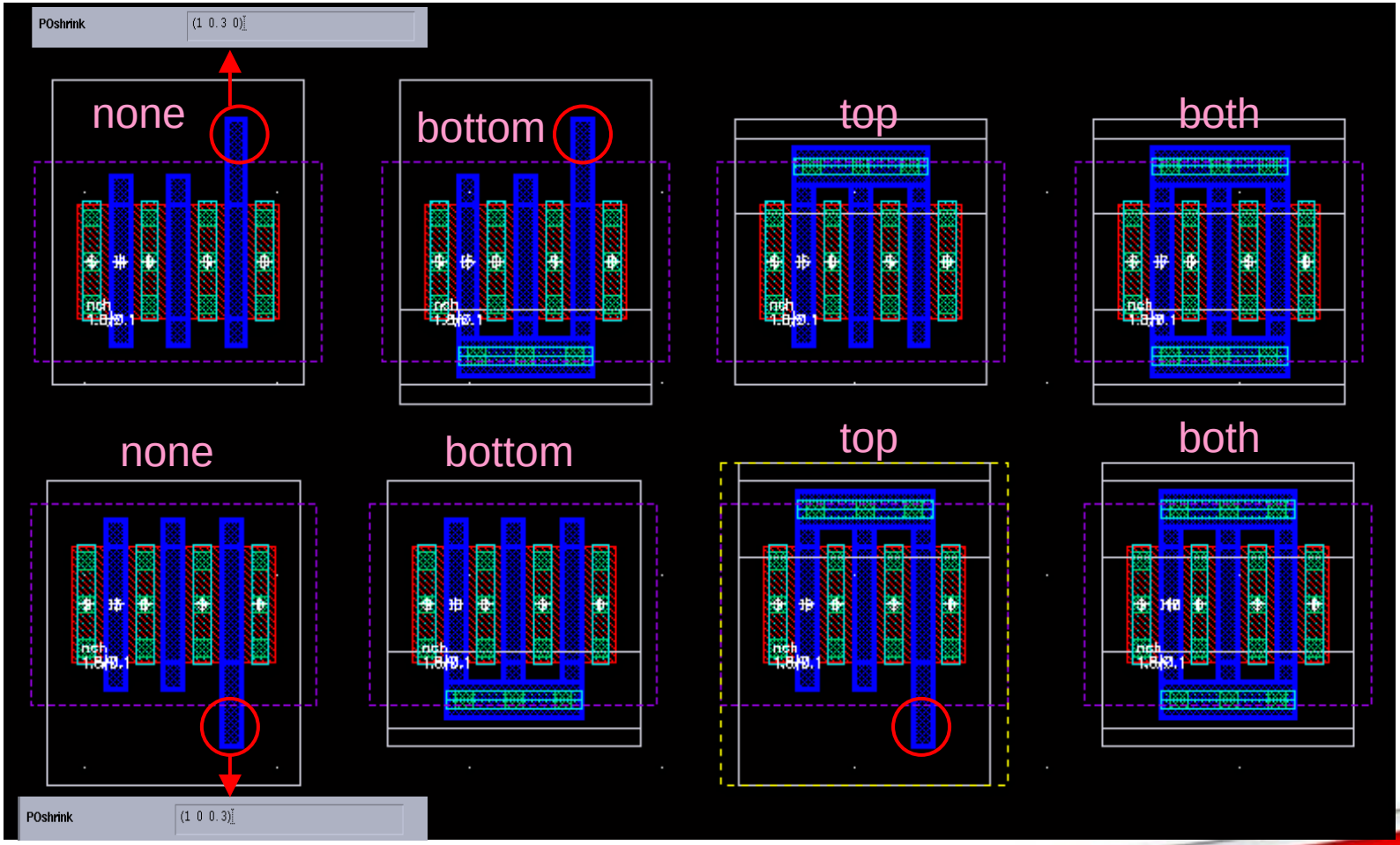
- Finger number=3. If customer use finger number=3 and turn on the routePolydir none/top/bottom/both direction. It will shows the following layout.

Finger=3



TSMCN65 PDK Usage Guide

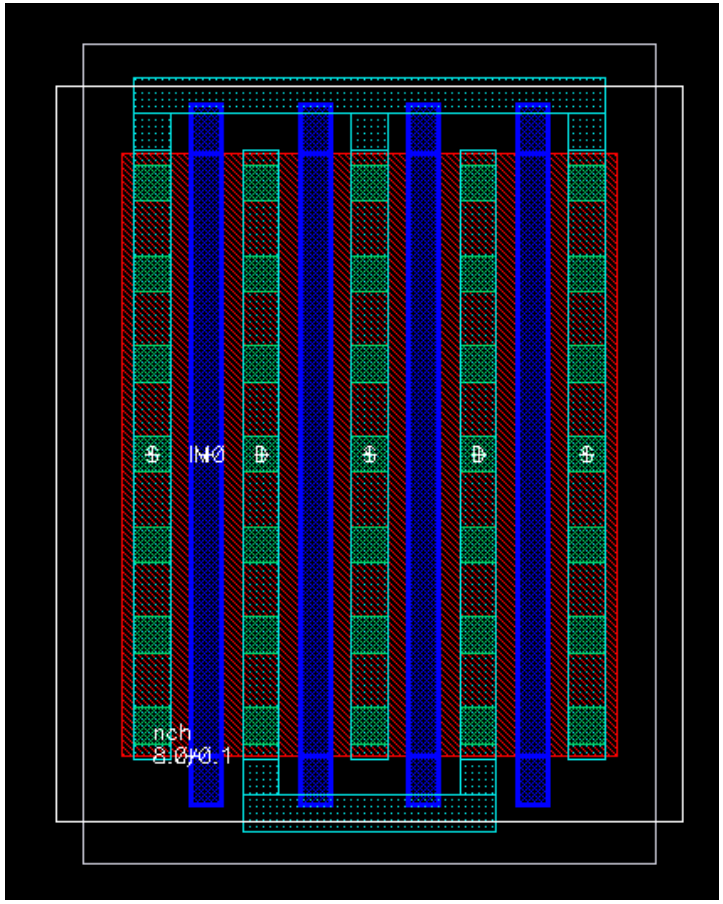
- **The function of routePolydir**
  - Finger number=3. Customer use finger number=3 and turn on the routePolydir none/top/bottom/both direction. At the same time customer uses Poshrink option as following : Finger=3



The function of route_Source_Drain

- The function is provided to drawing source and drain connection.

route_Source_Drain is *Both*

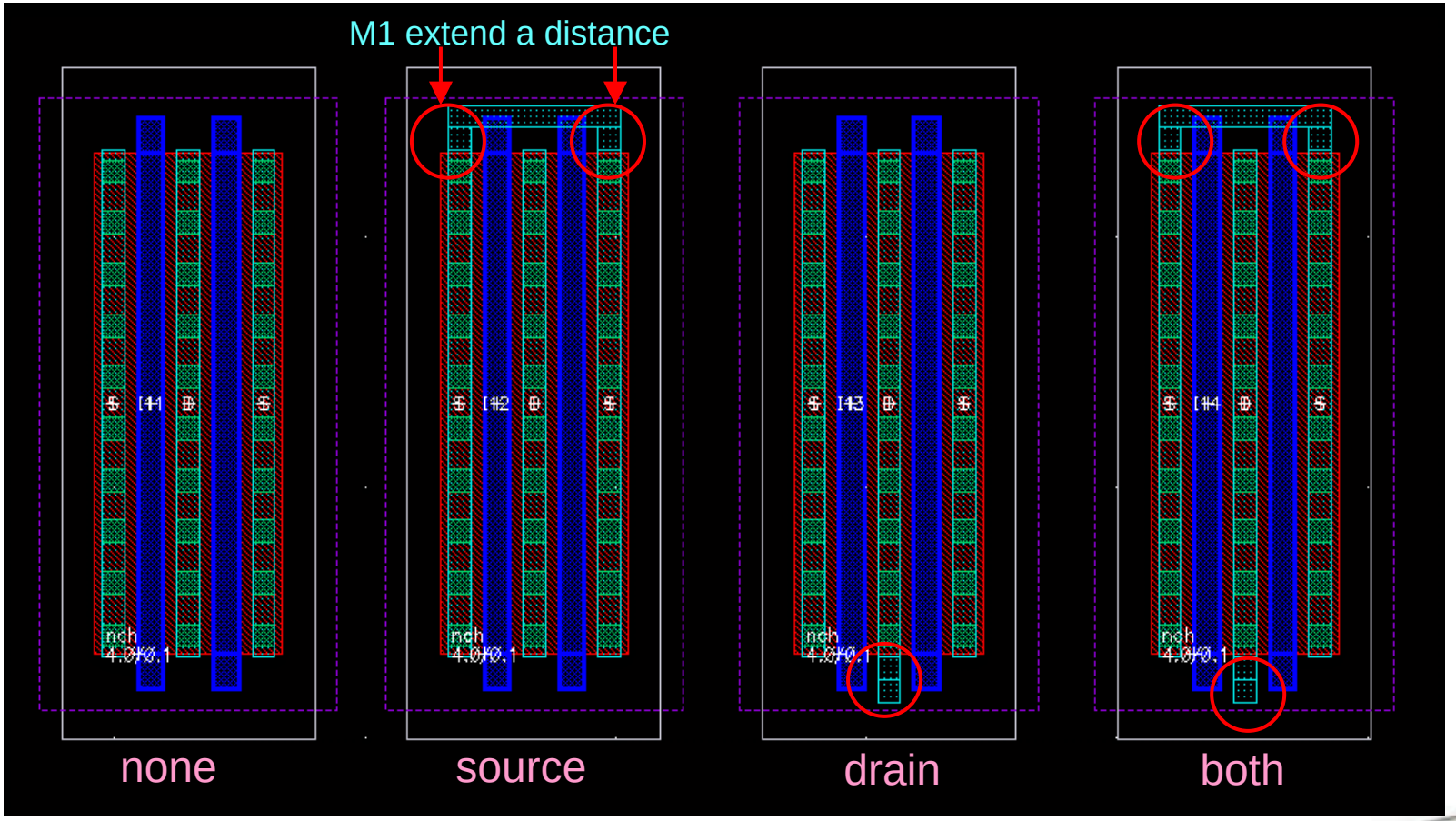


Check here to back to MOS

TSMCN65 PDK Usage Guide

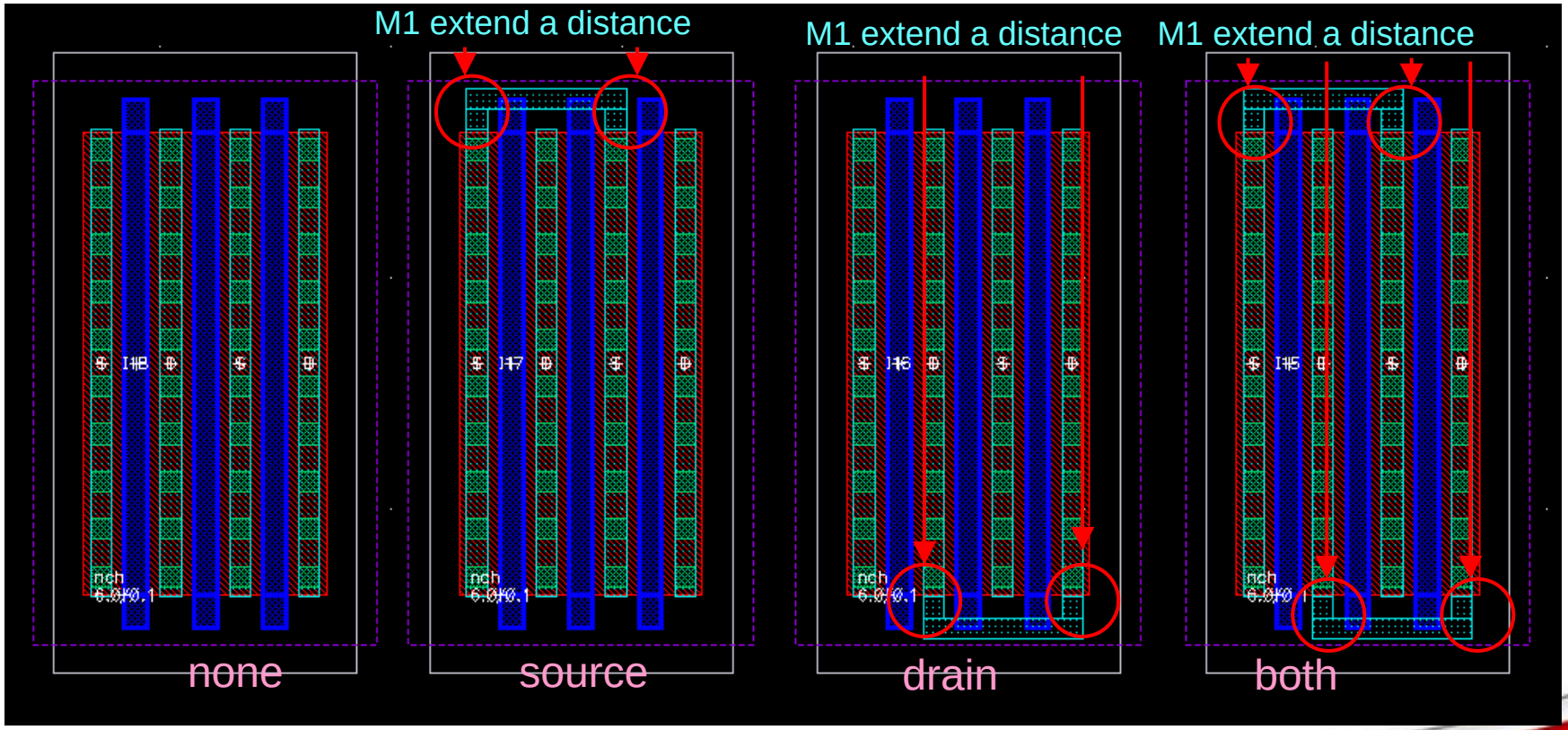
The function of route_Source_Drain

- The function is provided to drawing source and drain connection(it happens to nf >1). User need to pay attention for the following case Nf=2; it means the mos has two source and one drain. If you turn on this function your source-drain metal layer will extend a distance.



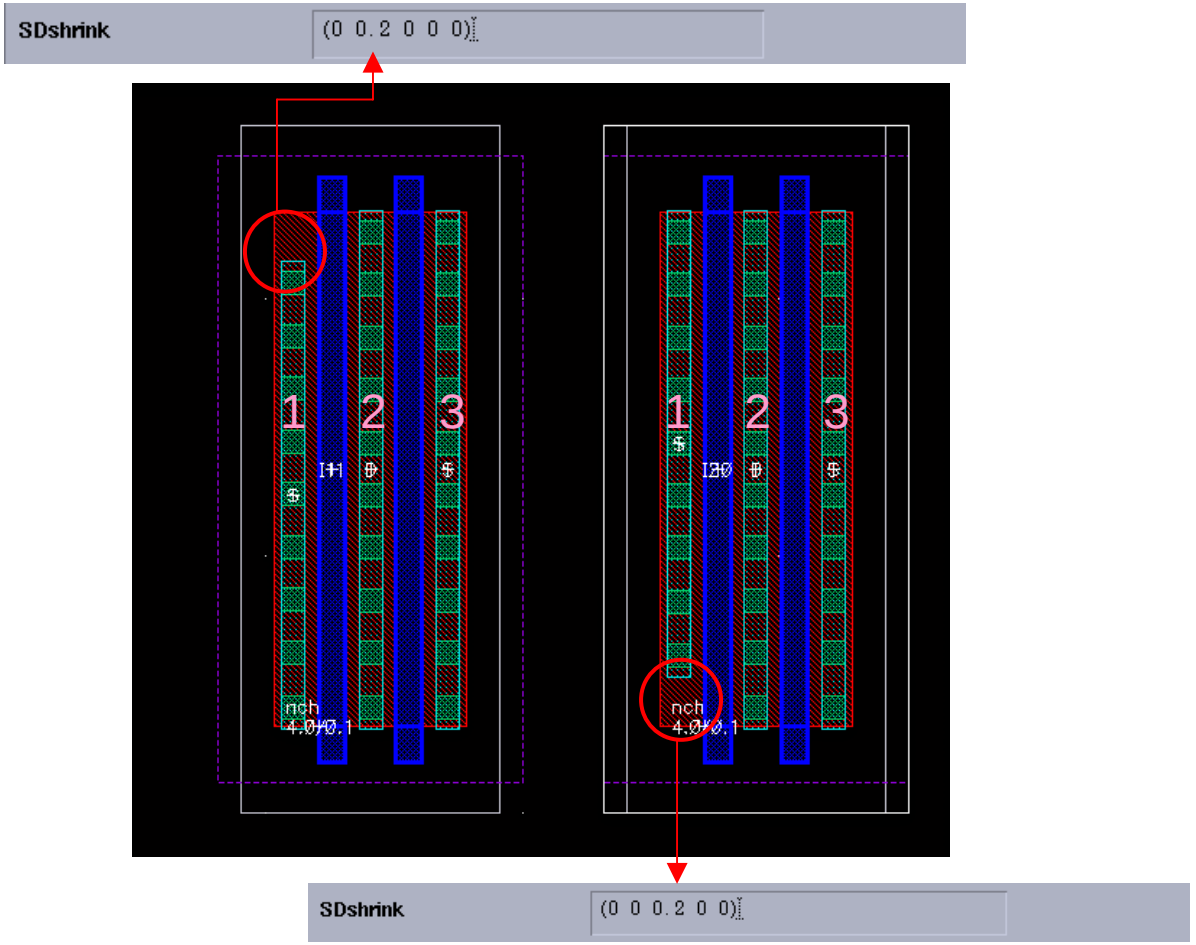
TSMCN65 PDK Usage Guide

- **The function of route_Source_Drain**
  - The function is provided to drawing source and drain connection(it happens to nf >1). User need to pay attention for the following case Nf=3; it means the mos has two source and one drain. If you turn on this function your source-drain metal layer will extend a distance.



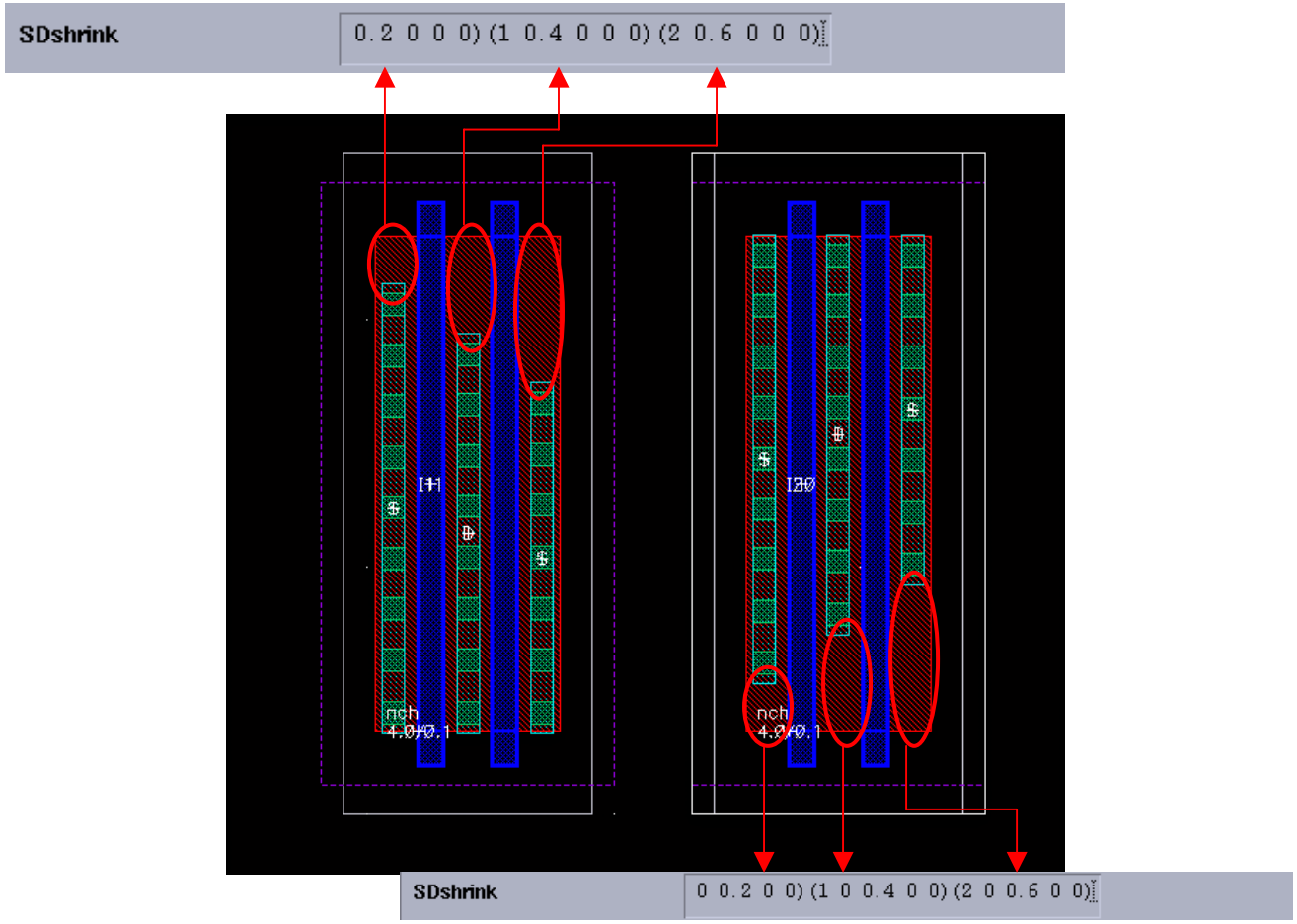
The function of route_Source_Drain

- The function is provided to drawing source and drain connection(it happens to nf >1). User set SD shrink function, the mos layout will shrink the length as following.



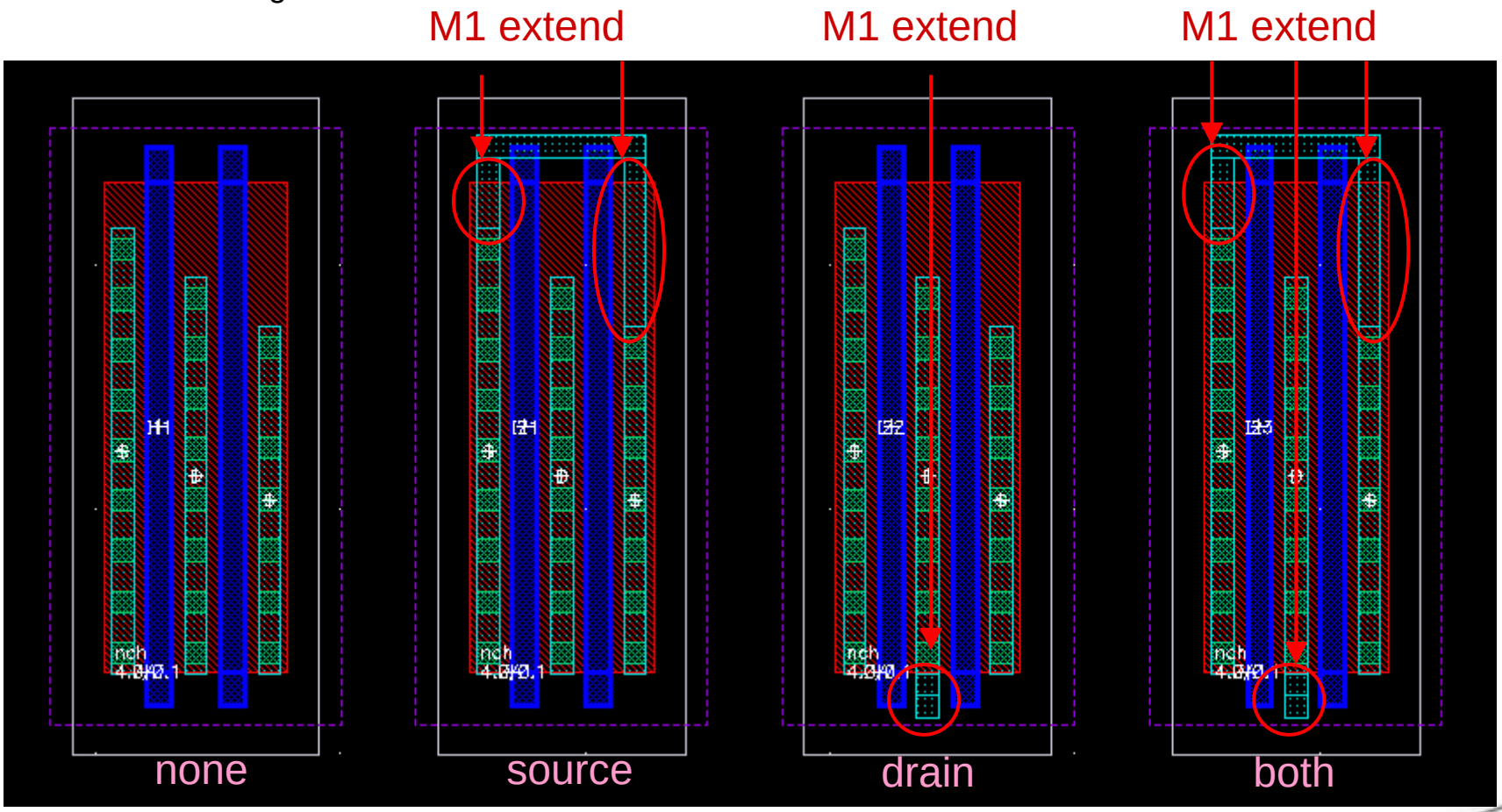
The function of route_Source_Drain

- The function is provided to drawing source and drain connection(it happens to nf >1). User set SD shrink function, the mos layout will shrink the length as following.



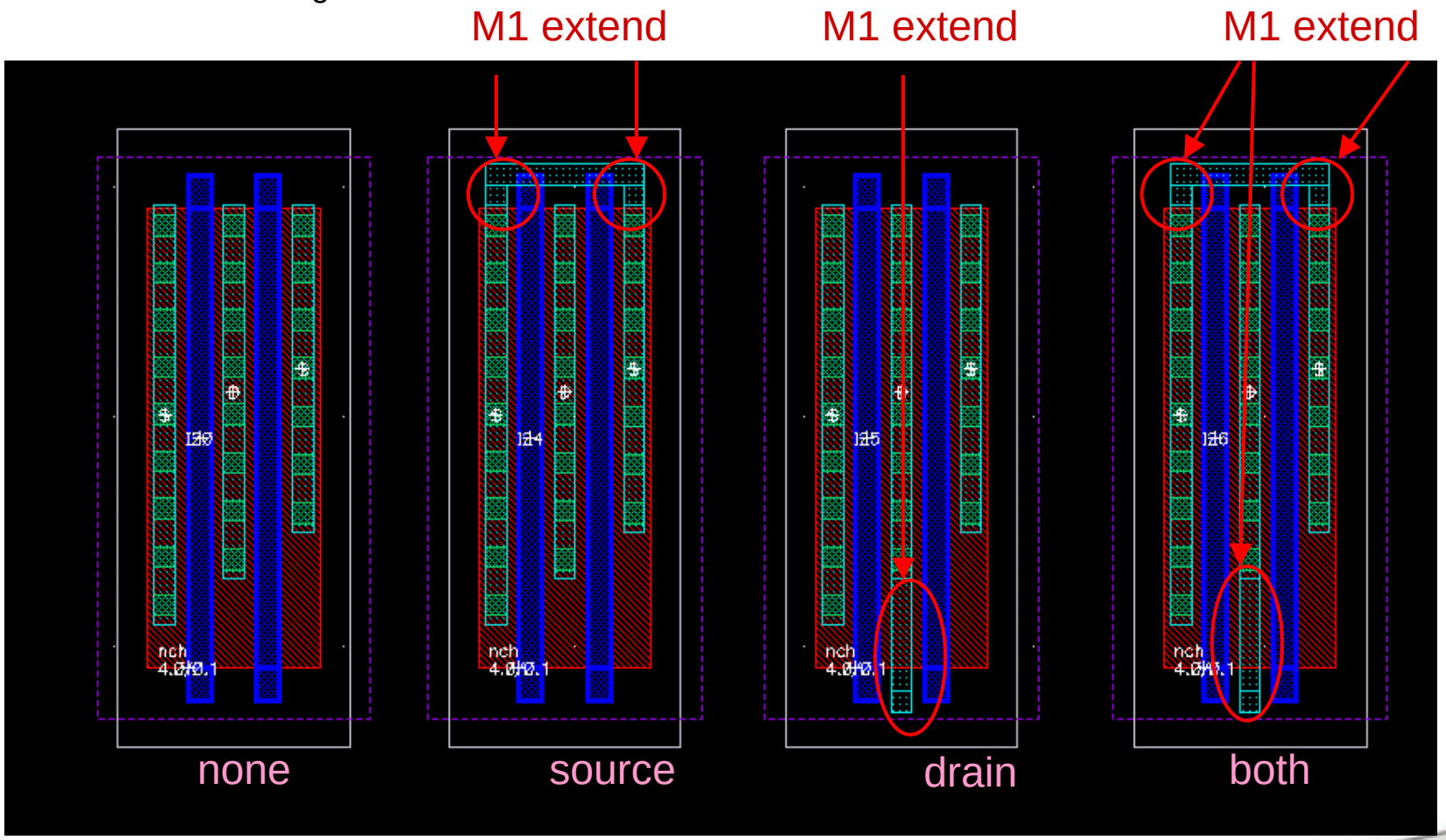
The function of route_Source_Drain

- The function is provided to drawing source and drain connection(it happens to nf >1). User set SD shrink function+route_source_drain, the mos layout will shrink the length as following.



TSMCN65 PDK Usage Guide

- **The function of route_Source_Drain**
  - The function is provided to drawing source and drain connection(it happens to nf >1). User set SD shrink function+route_source_drain, the mos layout will shrink the length as following.

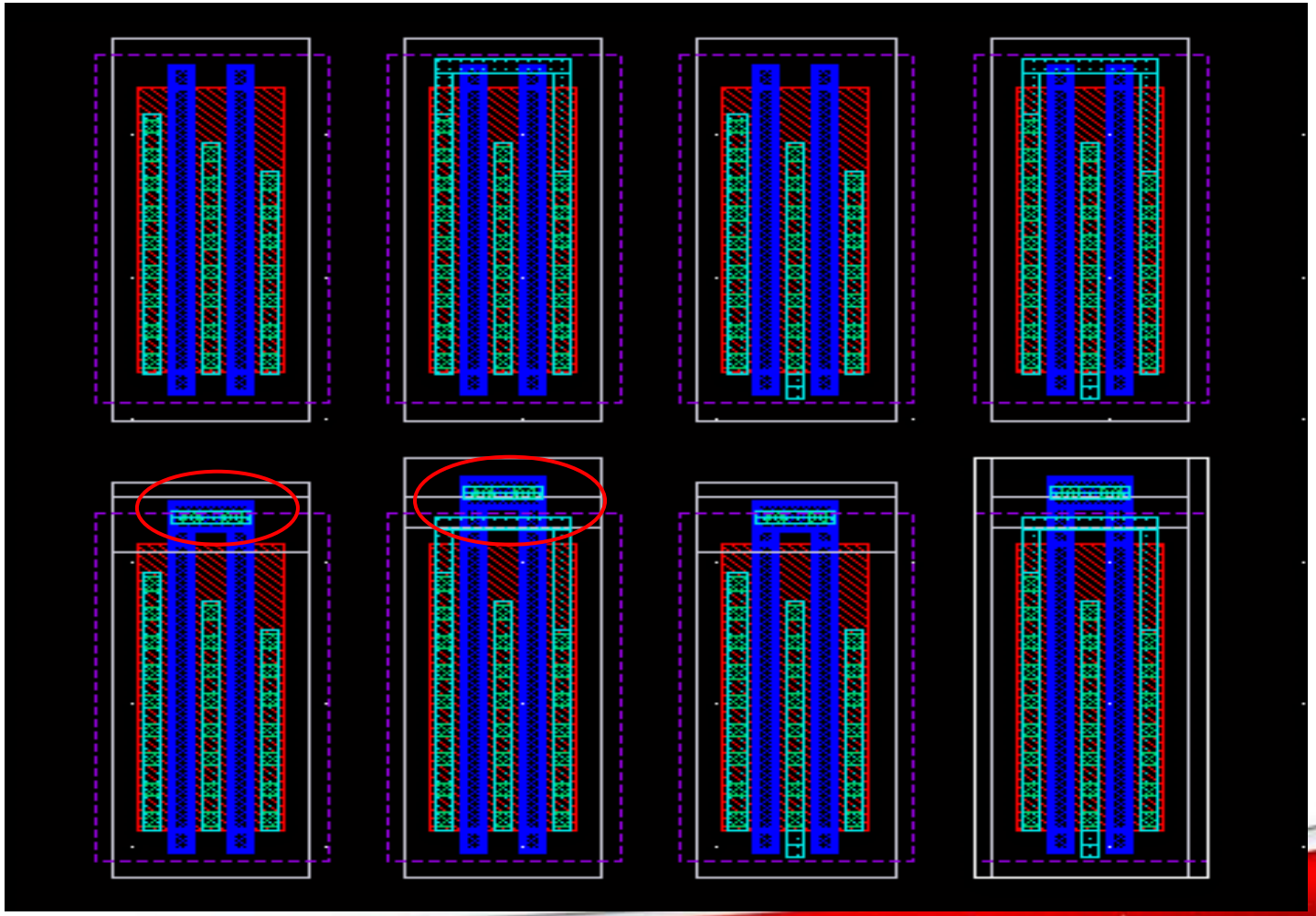


The function of route_Source_Drain

- The function is provided to drawing source and drain connection(it happens to nf >1). User set SD shrink function+route_source_drain+routePolydir, the mos layout will shrink the length as following.Note with SD route, the poly will extend more length than none SD route.

routePolydir:NONE

routePolydir:TOP

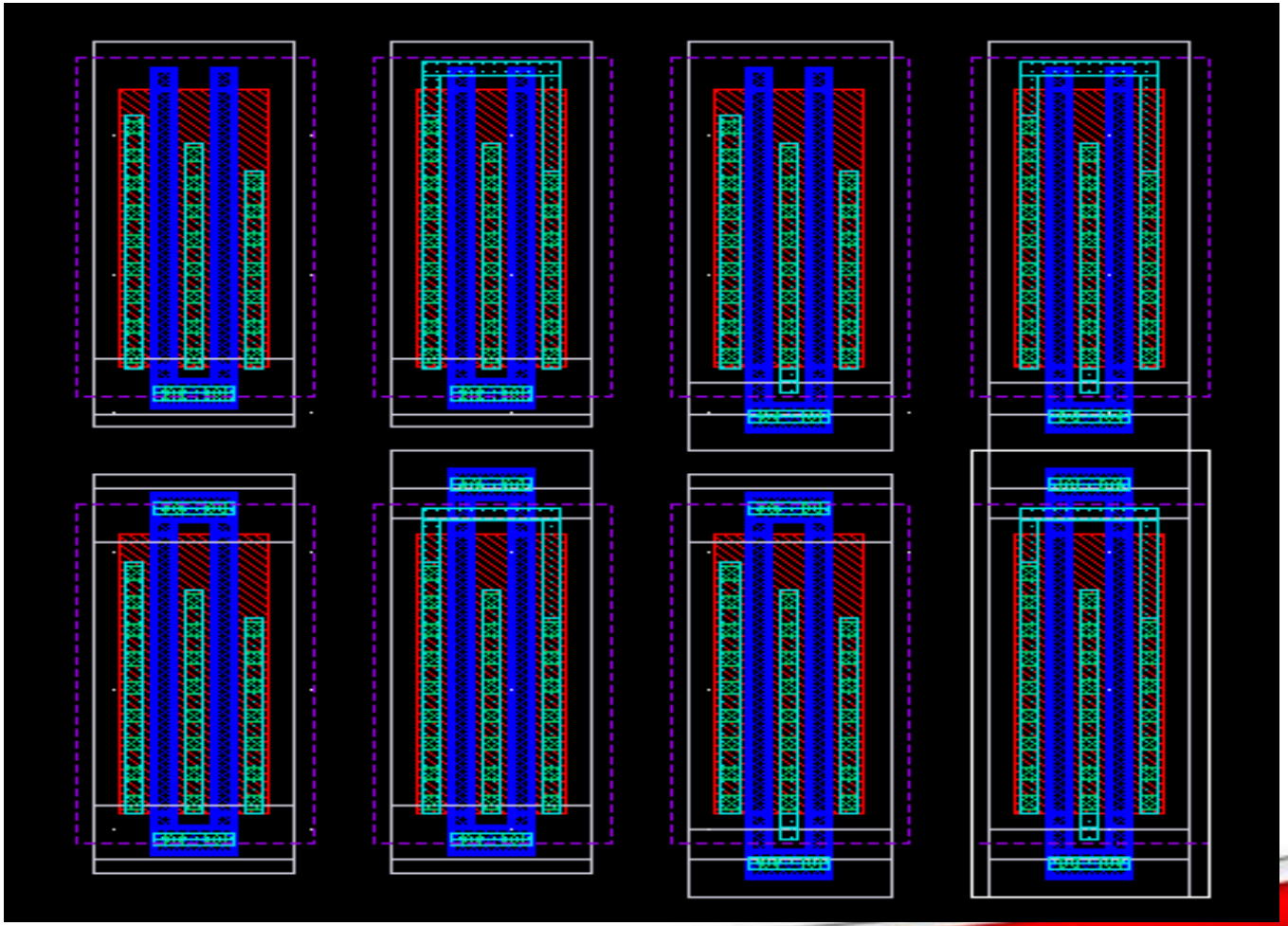


The function of route_Source_Drain

- The function is provided to drawing source and drain connection(it happens to nf >1). User set SD shrink function+route_source_drain+routePolydir, the mos layout will shrink the length as following.Note with SD route, the poly will extend more length than none SD route.

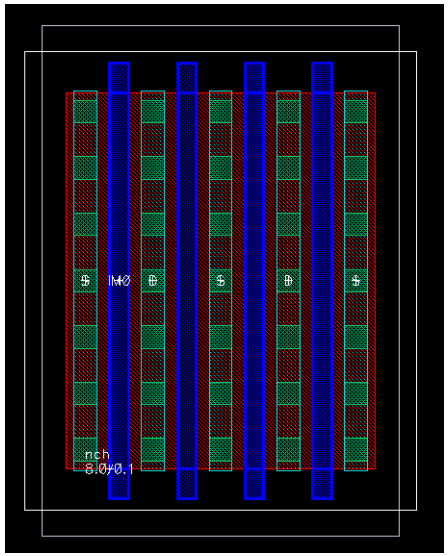
routePolydir:Bottom

routePolydir:Both

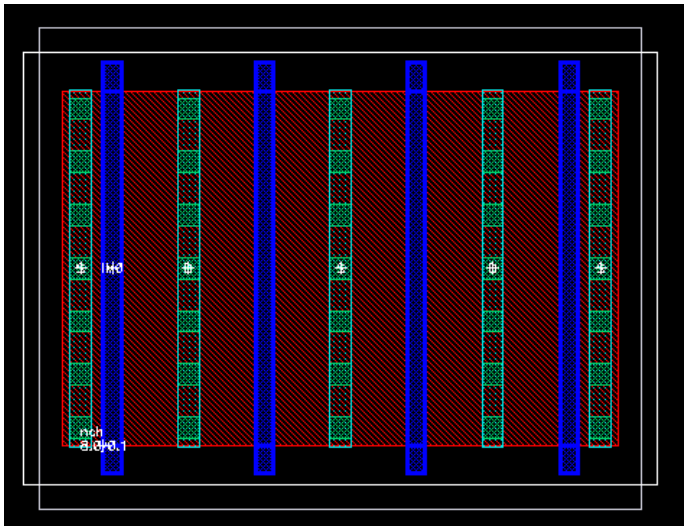


- **The function of fingers_SP_INC(M)**
  - The function provide user to modify poly gate space. Fingers_SP_INC(M) is a increase value, it's not a distance between poly gate.

fingers_SP_INC(M) = 0



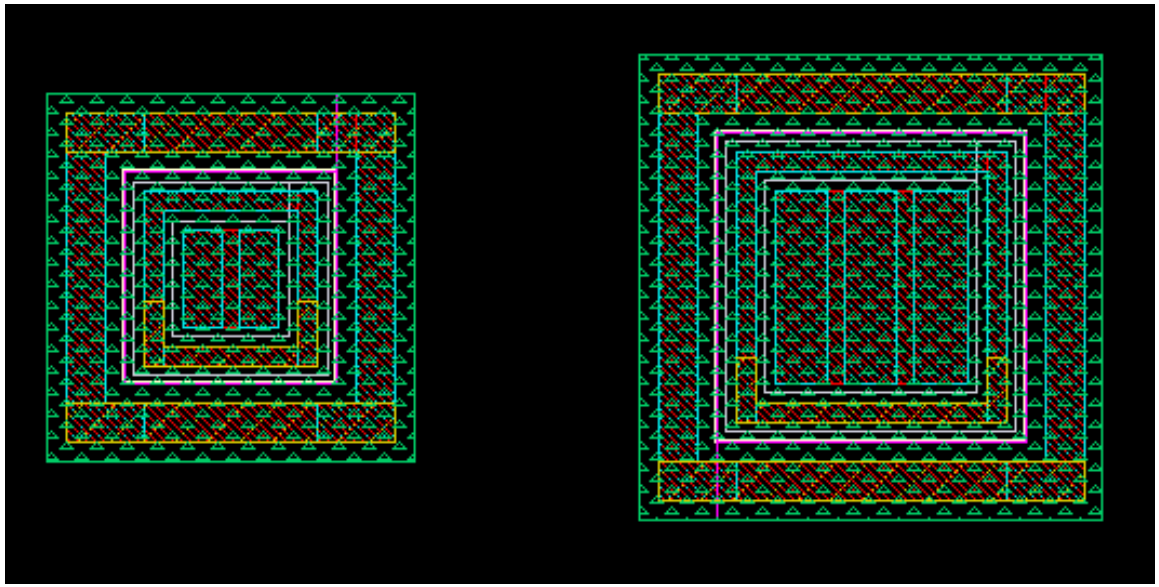
fingers_SP_INC(M) = 0.5



Check here to back to MOS

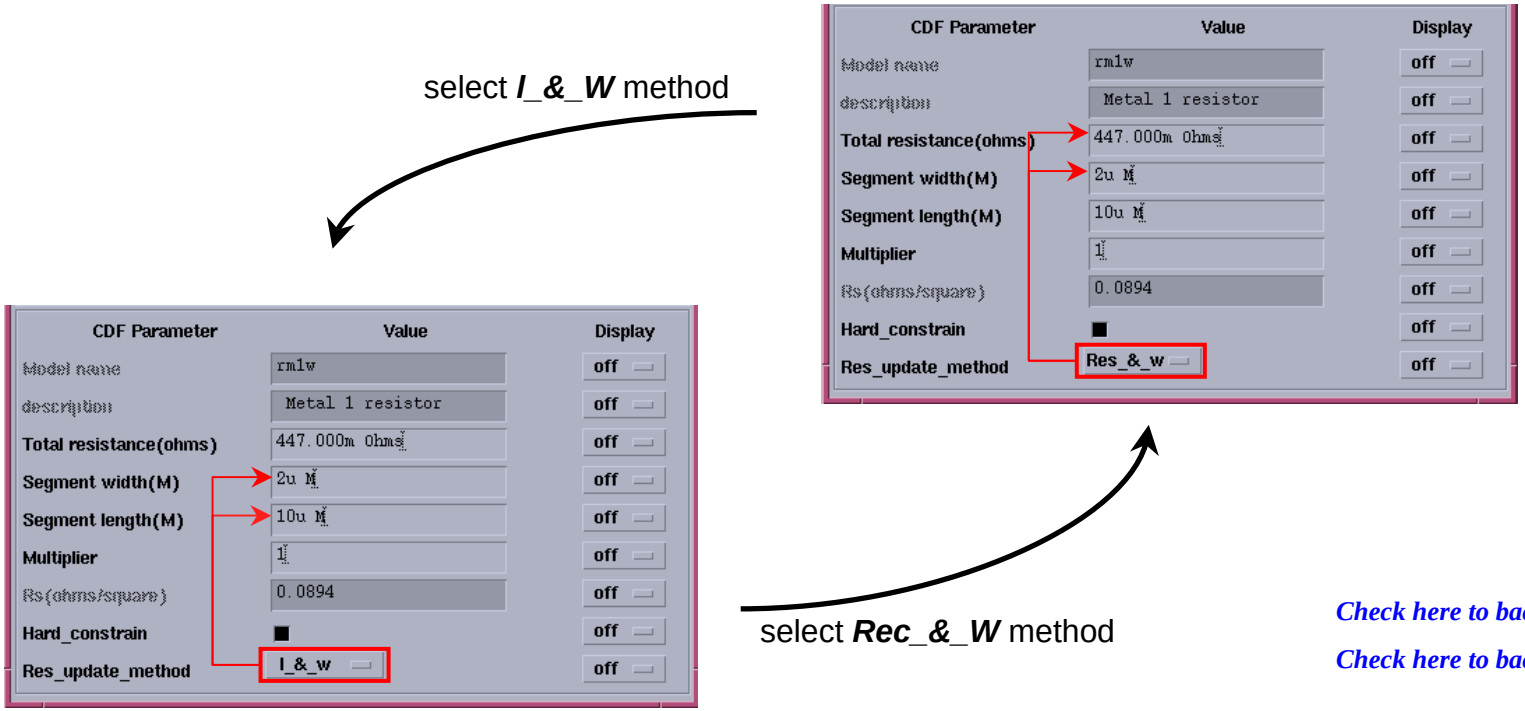
- **The function of BJT_type**
  - There are three dimension of pnp and npn are provided in this PDK, user can use this function to choose those device layout.

BJT_type = 5X5 **BJT_type = 10X10**



Check here to back to BJT

- **The function of Total resistance(ohms), Segment width(M), Segment length(M) and Res_update_method**
  - In the resistance cell, we provide user two kinds of input method – ***I_&_W*** and ***Rec_&_W*** to modify the device resistance. When the user select ***I_&_W*** method, the input parameter will be segment length(M) and segment width(M), the other one is total resistance(ohms) and segment width(M).

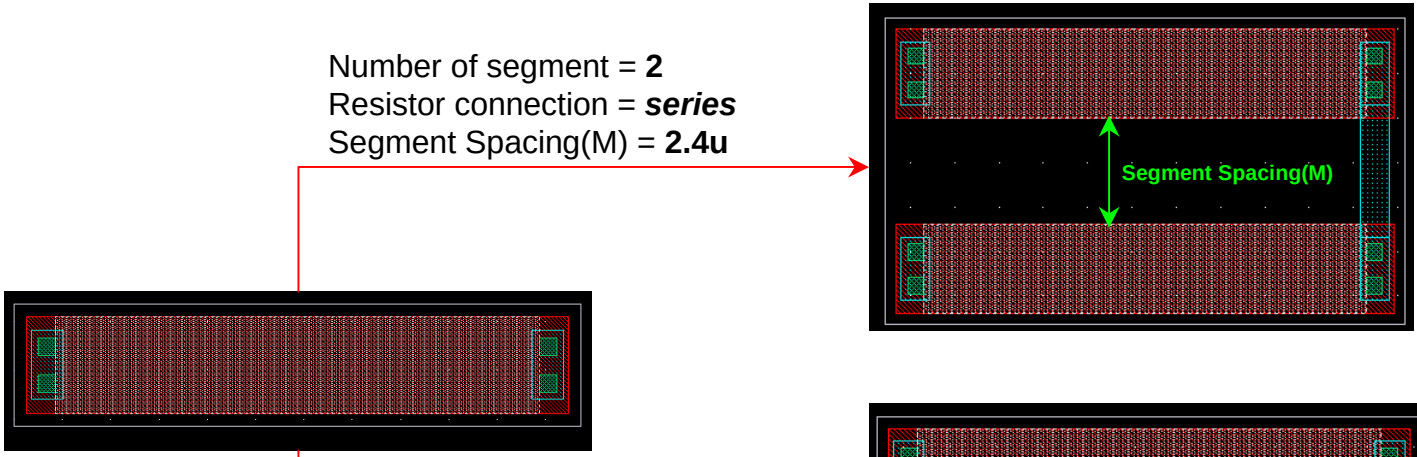


Check here to back to Resistance(1)

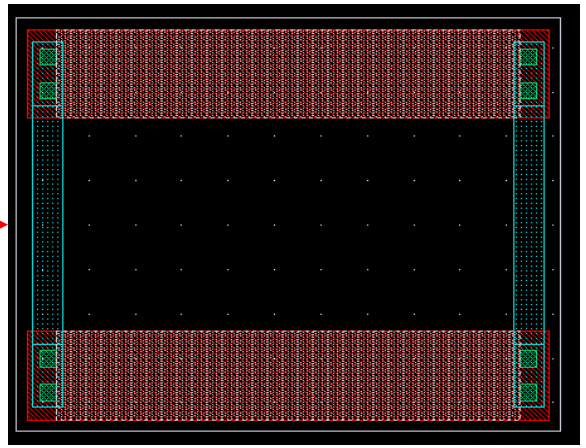
Check here to back to Resistance(2)

- **The function of Resistor connection, Number of segment, Segment spacing(M)**
  - Number of segment provide user a function to Increment the number of segment resistance, user can use Resistor connection and Segment spacing(M) to modify connection type – ***series*** or ***parallel*** and segment spacing.

Number of segment = **2**
Resistor connection = ***series***
Segment Spacing(M) = **2.4u**



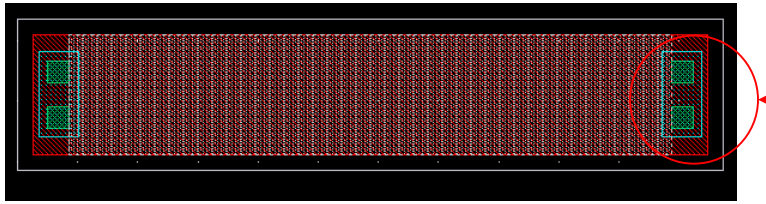
Number of segment = **2**
Resistor connection = ***parallel***
Segment Spacing(M) = **4.8u**



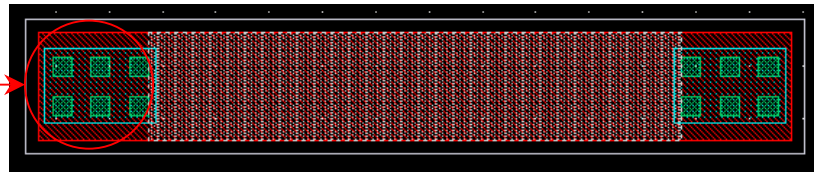
Check here to back to Resistance(2)

- **The function of Cont columns**
  - This function provide user to modify the contact columns.

Cont columns= 1

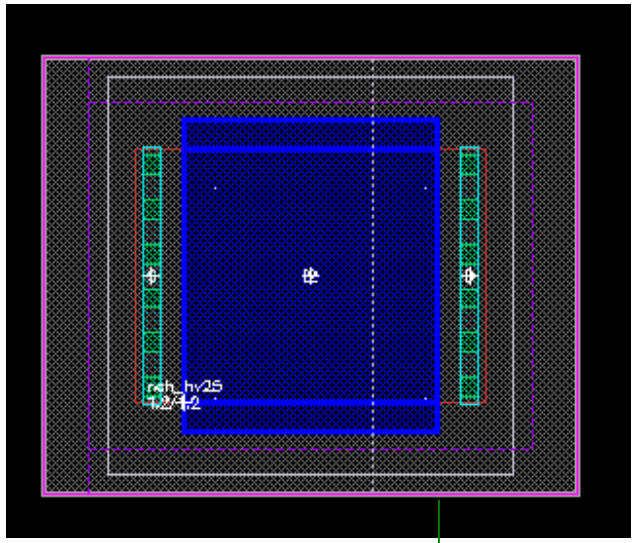


Cont columns= 3

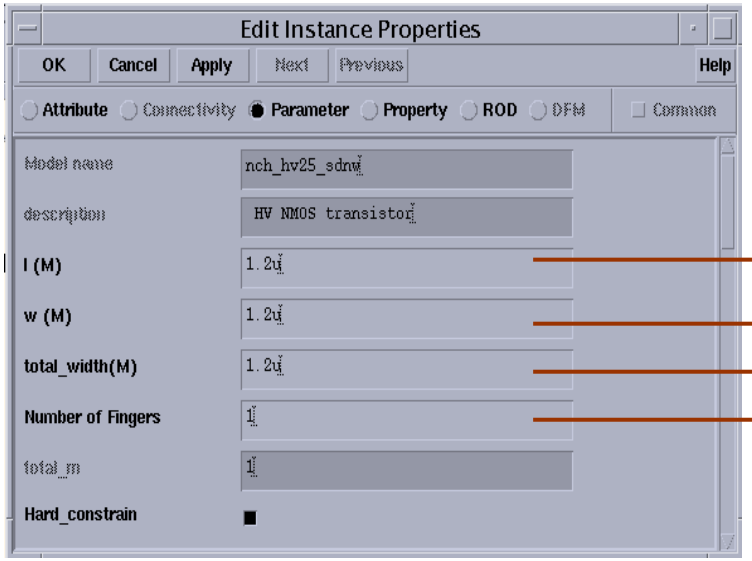


Check here to back to Resistance(2)

- **The function of HVMOS (nch_hv25/pch_hv25)**
  - This function provide user to modify the device layout

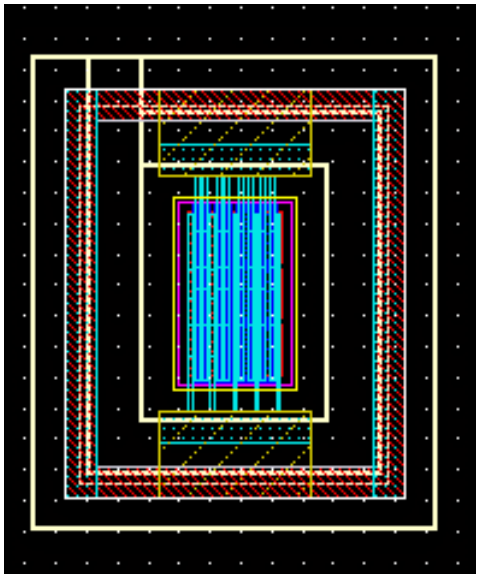


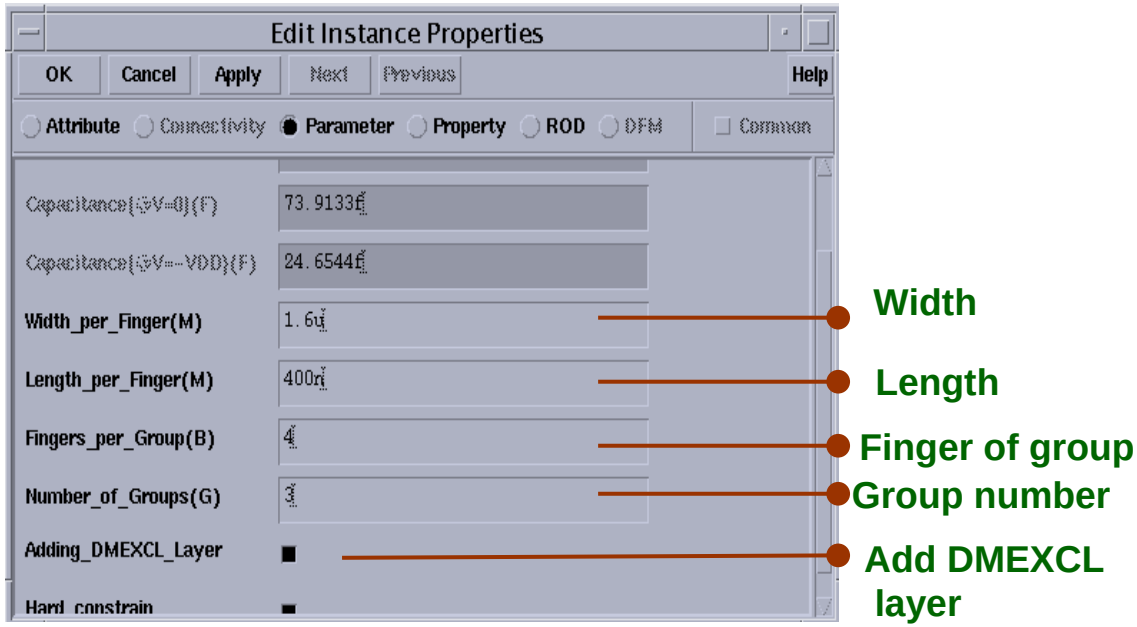
HVD (n_a)



- Length
- Width
- Total_width
- NF

- **The function of PMOSCAP_RF**
  - This function provide user to modify the device layout





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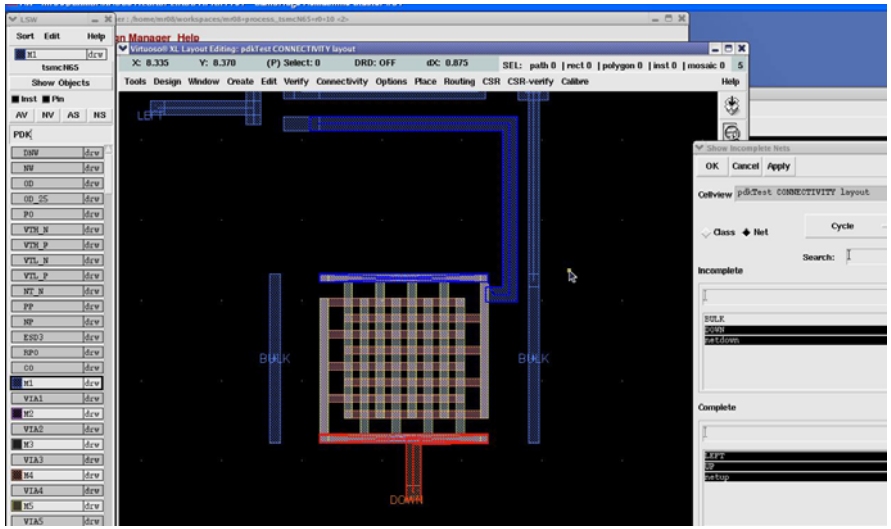
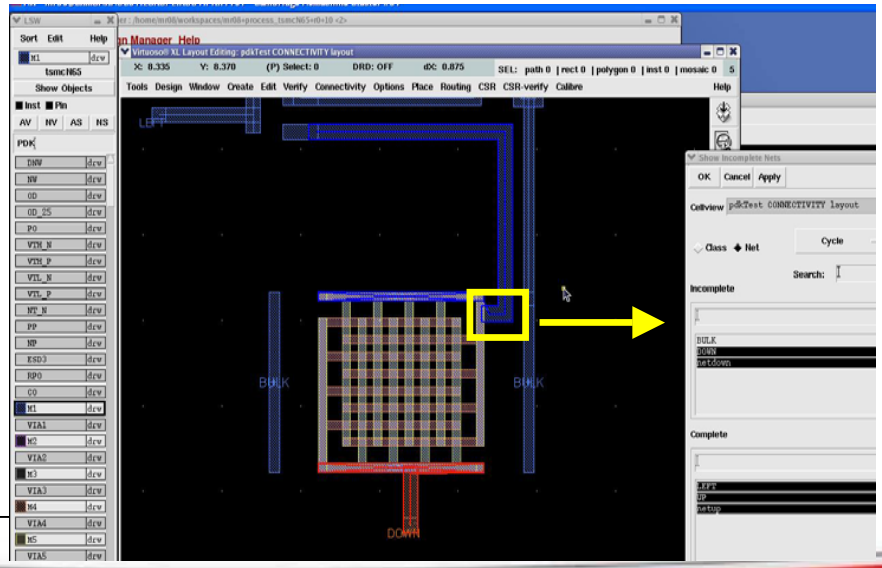
- **The function of CRTMOM**



1. No problem to add different metal layer connection flexibility.
2. Allow right&left side for connection but need to consider improper metal routing caused additional parasitic capacitances.



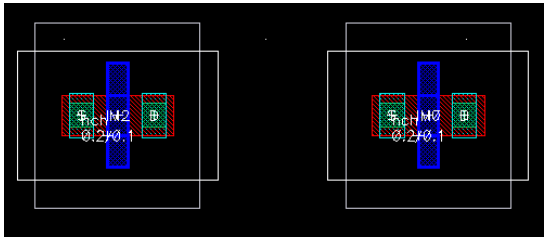
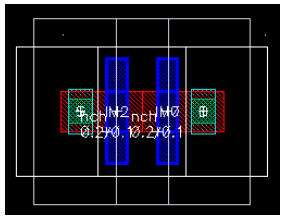
Extra Parasitic devices will be extracted in yellow mark region. Need to consider very careful.

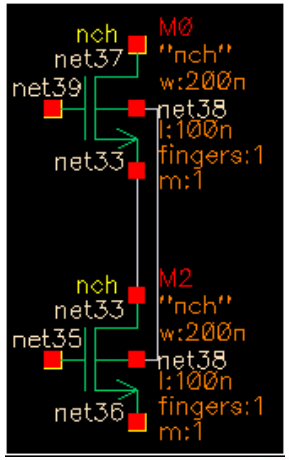
TSMC don't recommend this kind connection.

Appendix

Appendix A - Abutment

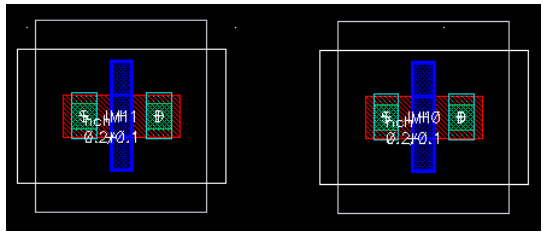
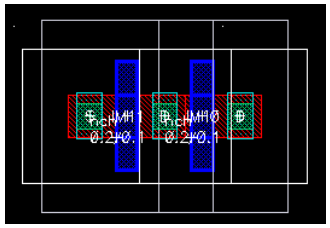
- To make the user understand this function, we describe more details and examples about abutment in this section. There are two point about this function is important, first this function only support MOS device in this PDK, second there are the same type MOS (ex: nch and nch_18, pch and pch_25) can be abutted only.
- When user abut two device, the terminal B must connects certainly in the layout view so it must be connected to the same net in the schematic view.
- The system will auto determine abutment type of the both device. User can't modify abutment type.
- The same devices abut case as show in below :(Case Ⅰ)

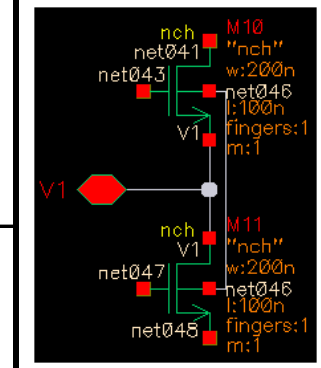
Device	nch (W=0.2u)	nch (W=0.2u)	The view in schematic
Abutment type	ShareLeftShape: normal ShareRightShape: same	ShareLeftShape: same ShareRightShape: normal	
Before Abutment			
After Abutment			



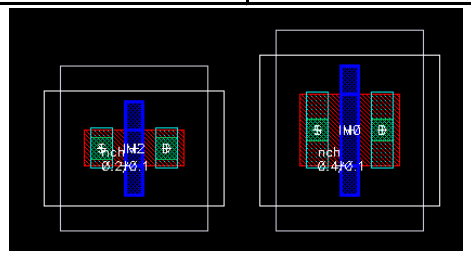
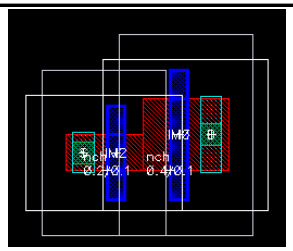
Check here to back to ShareLeftShape

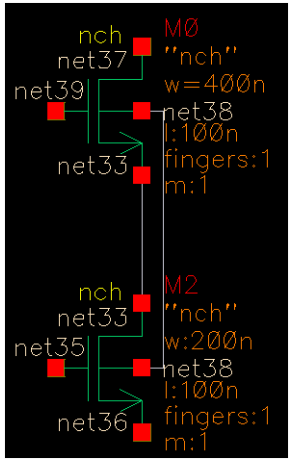
- Abutment ability lets you overlap two MOS, to create a connection between two sets of shapes overlapping each other. The two sets of shapes must include pins connected to the same net. (Case Ⅱ)

Device	nch (W=0.2u)	nch (W=0.2u)	The view in schematic
Abutment type	ShareRightShape largeExt ShareLeftShape normal	ShareLeftShape sameExt ShareRightShape normal	
Before Abutment			
After Abutment			

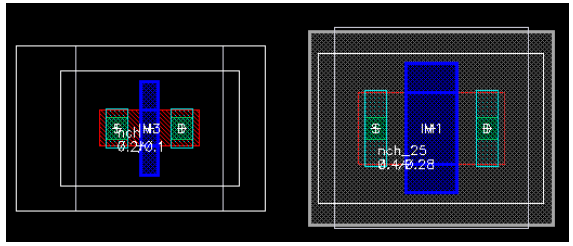
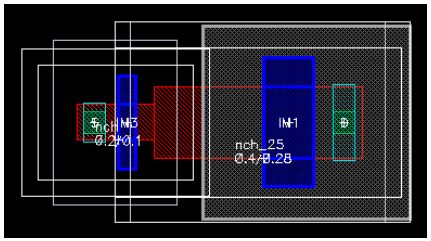


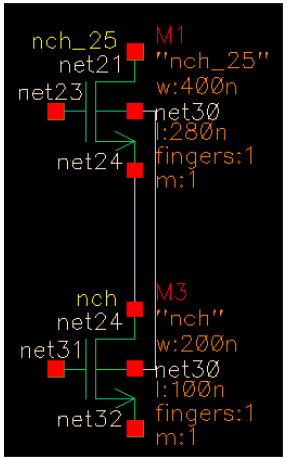
- This case show out the different width device have been abutted. (Case Ⅲ)

Device	nch (W=0.2u)	nch (W=0.4u)	The view in schematic
Abutment type	ShareLeftShape: normal ShareRightShape: small	ShareLeftShape: large ShareRightShape: normal	
Before Abutment			
After Abutment			



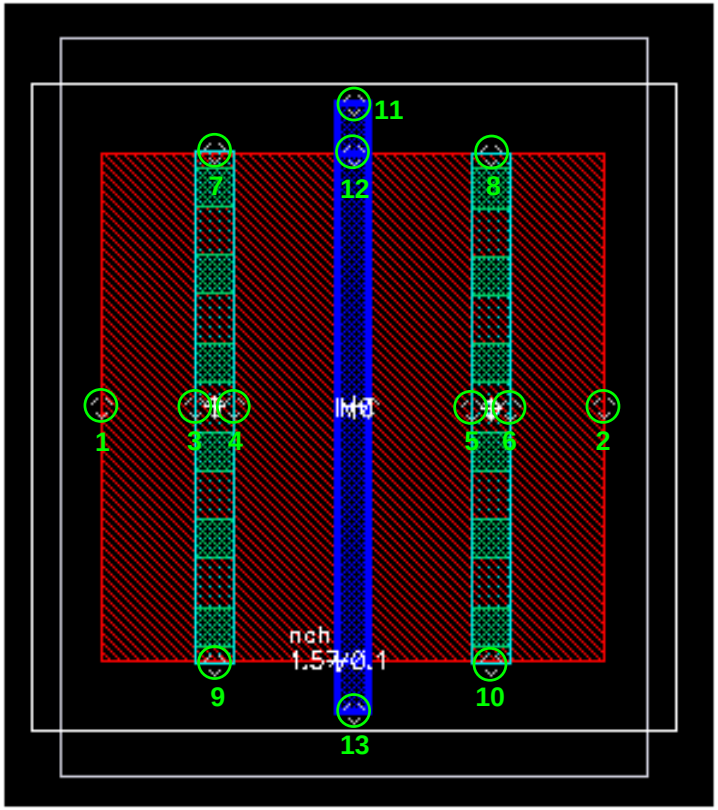
- This case show out that the same type MOS also can be abutted. (Case Ⅳ)

Device	nch (W=0.2u)	nch_25 (W=0.4u)	The view in schematic
Abutment type	ShareLeftShape: normal ShareRightShape: small	ShareLeftShape: diff ShareRightShape: normal	
Before Abutment			
After Abutment			



Appendix B – Stretch Handles

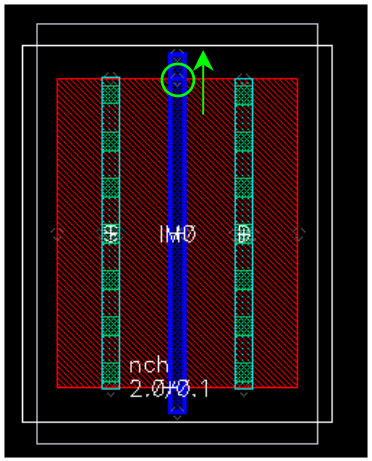
- This function lets user graphically change the value of those parameter for Pcell instances after user place them. The only one device MOS is a stretchable Pcell in this PDK.
- The system default is not show out the stretch handles, user must be enable the function manually. (Direct: in the layout view Options → Display option → Stretch Handles)



Stretch Handles number	Stretch direction
1	← →
2	← →
3, 5	←
4, 6	→
7, 8	↓
9, 10	↑
11	↑
13	↓
12	↑ ↓

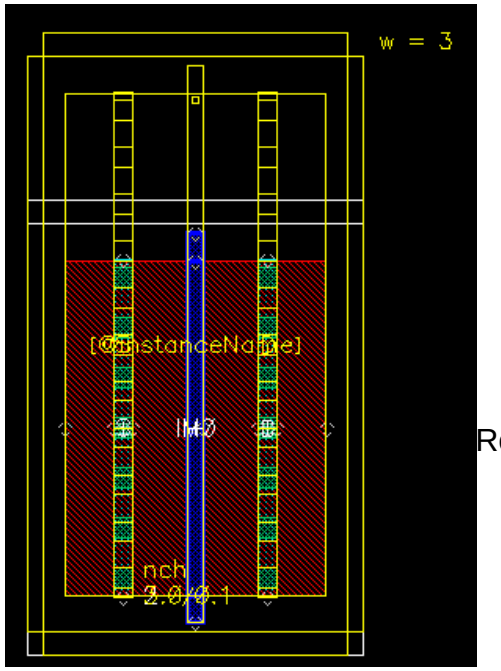
- A example to show out the stretch case when the user stretch the handle 12.

Width = 2.0u



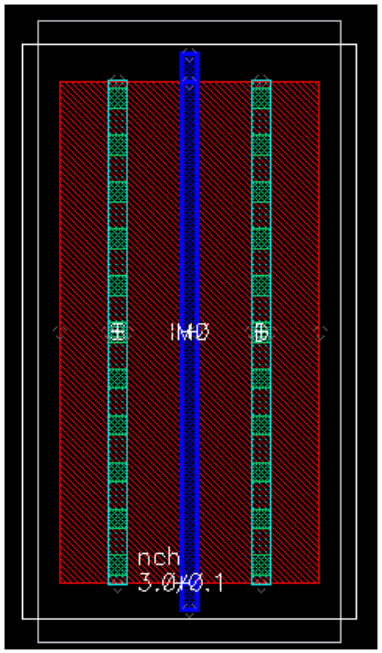
Select handle 11 and move up the handle.

Width = 2.0u →3.0u



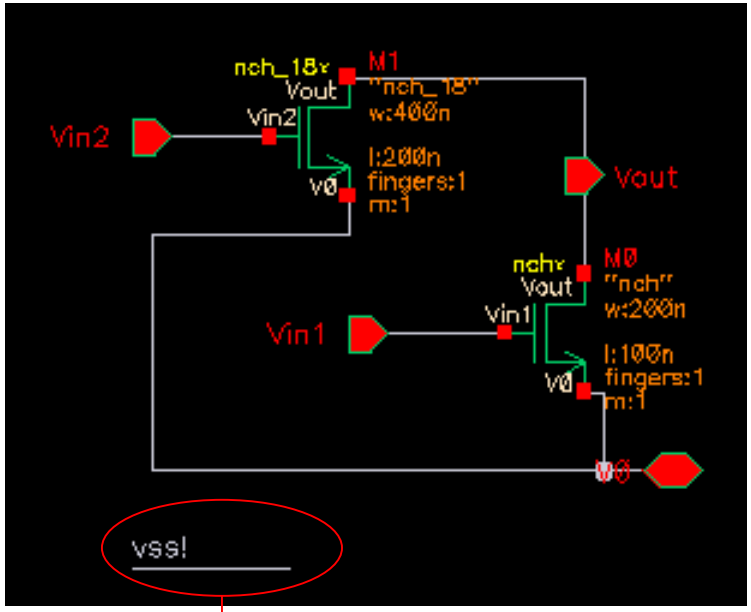
Release the handle

Width = 3.0u



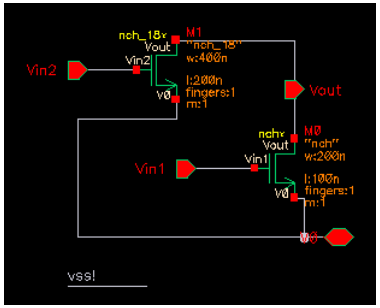
Appendix C – The three terminal MOS substrate pin

- In three terminal MOS, we create a parameter for substrate pin. The pin name is vss_sub in NMOS and vdd_sub in PMOS. When user instances the three terminal MOS, all of the devices substrate terminal will connect to vss_sub or vdd_sub. User doesn't need to draw the wire to link the device. In the hierarchy structure, user can add a parameter in CDF form to assign the substrate terminal name.

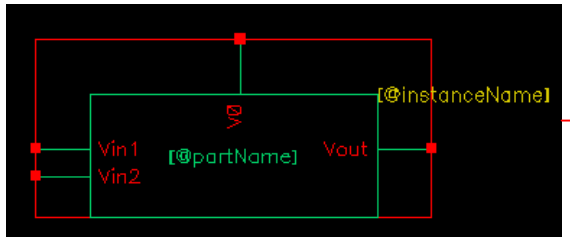


When user instances the nchx and nch_18x (three terminal MOS), all of the devices substrate terminal will connect to vss_sub (VSS!)

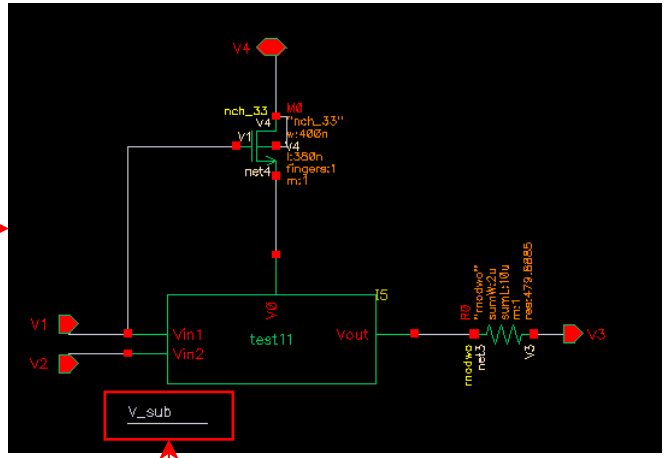
- In the hierarchy structure, user can add a parameter in CDF form to assign the substrate terminal name.

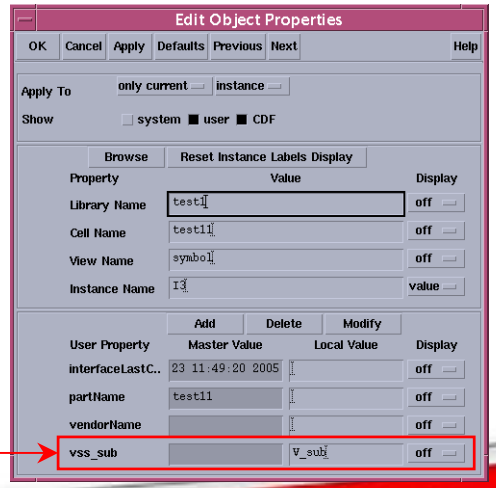


Create cellview to build up the symbol



Instance the symbol to other schematic view and assign the vss_sub to V_sub





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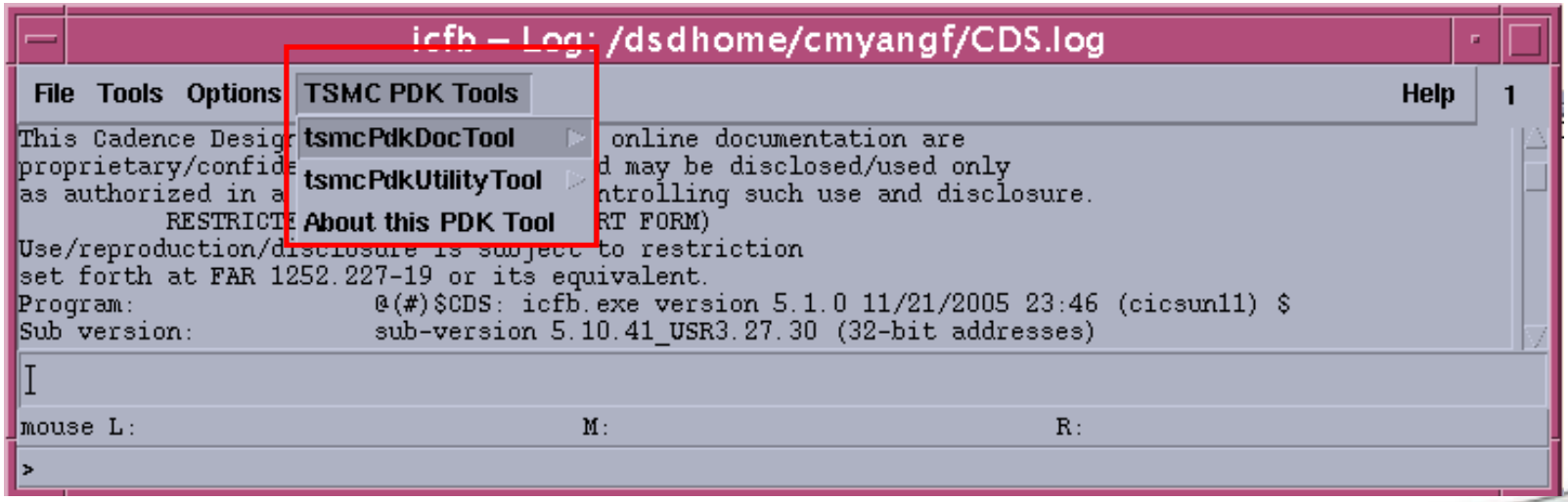
- **Appendix D – TSMC Utility**
  - **tsmcPdkDocTool**
    - tsmcPdkDocumentViewer
  - **tsmcPdkToolAbout**
  - **tsmcPdkUtilityTool**
    - tsmcPdkFC_set
    - tsmcPdkDFMset
    - tsmcPdkUpdateCDF
    - tsmcPdkChangeOD
    - tsmcPdkZoomIn
    - tsmcPdkLVL
    - tsmcPdkFileViewer



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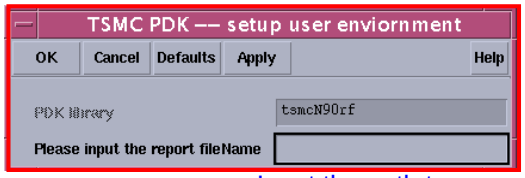
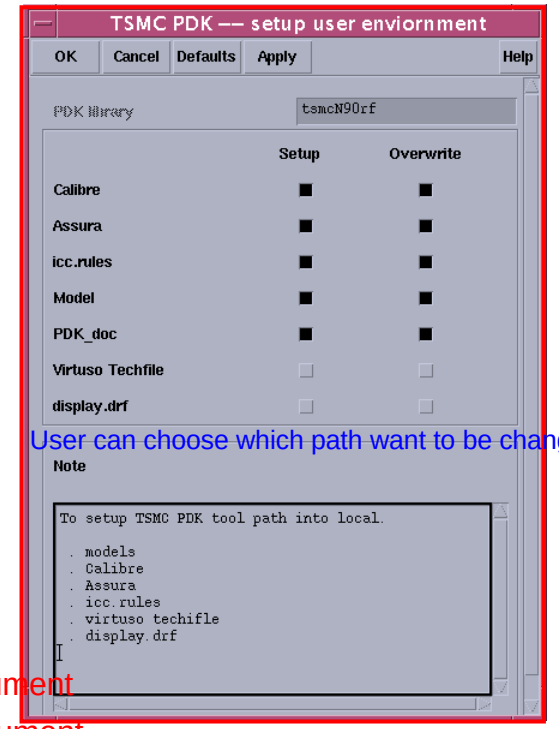
- **tsmcPdkDocTool :**
  - Sometimes TSMC PDK user will use symbolic link to use the PDK, user will encounter a problem - documents and technology file path missing. TSMC provide tsmcPdkDocumentView function to solve this problem. The function will re-connect the document directory and replace the default path setup.



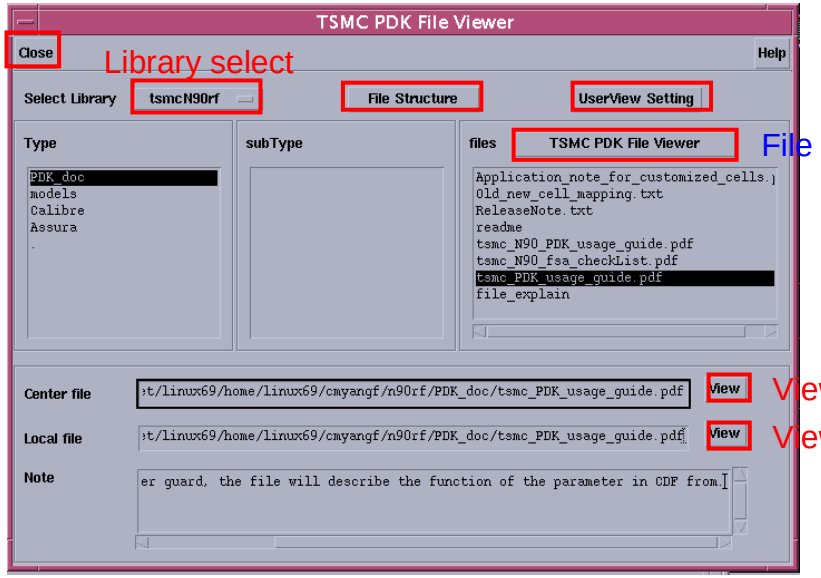
Input the path to save setup report



User can choose which path want to be change

Close window

Library select

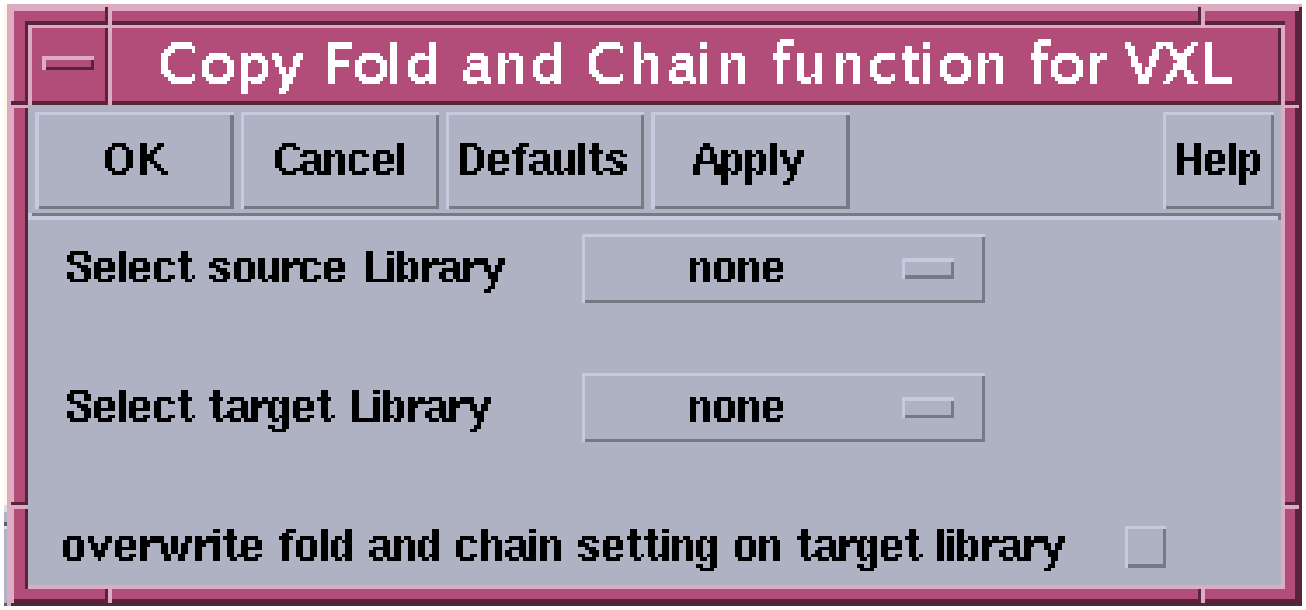


File Browser

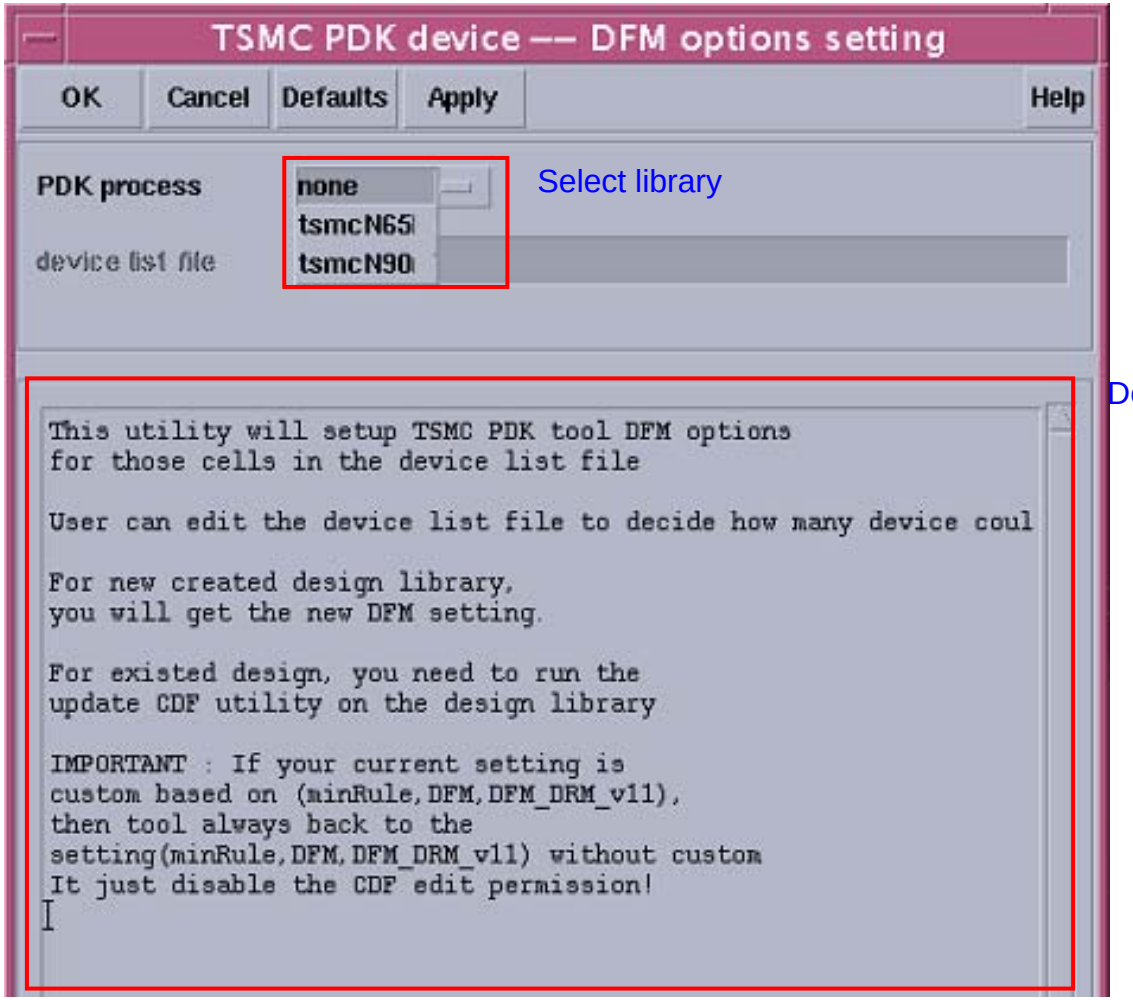
View PDK document

View Local document

- **tsmcPdkUtilityTool :**
  - The function of tsmcPdkFC_set is a utility function fold and chain.



- **tsmcPdkUtilityTool :**
  - The function of tsmcPdkDFMset will set the pcell to mimRule or DFM or DFM_DRMv11 or custom setup.



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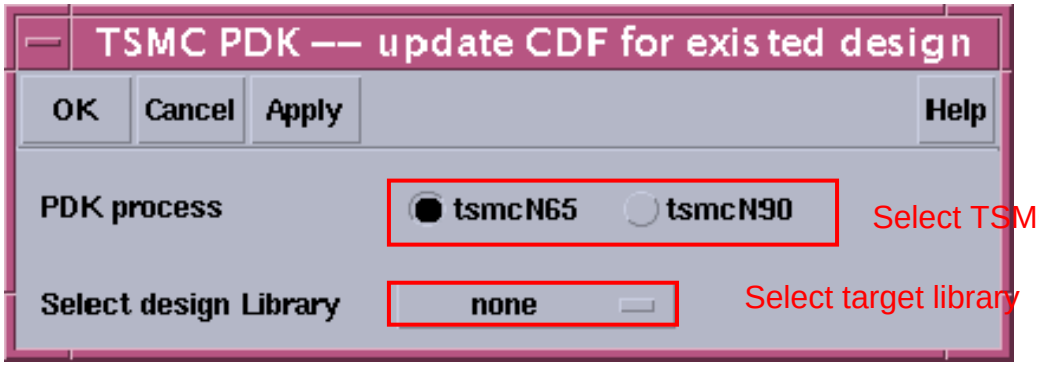
- **tsmcPdkUtilityTool :**
  - The function of tsmcPdkUpdateCDF will run TSMC CDF parameter update utility.



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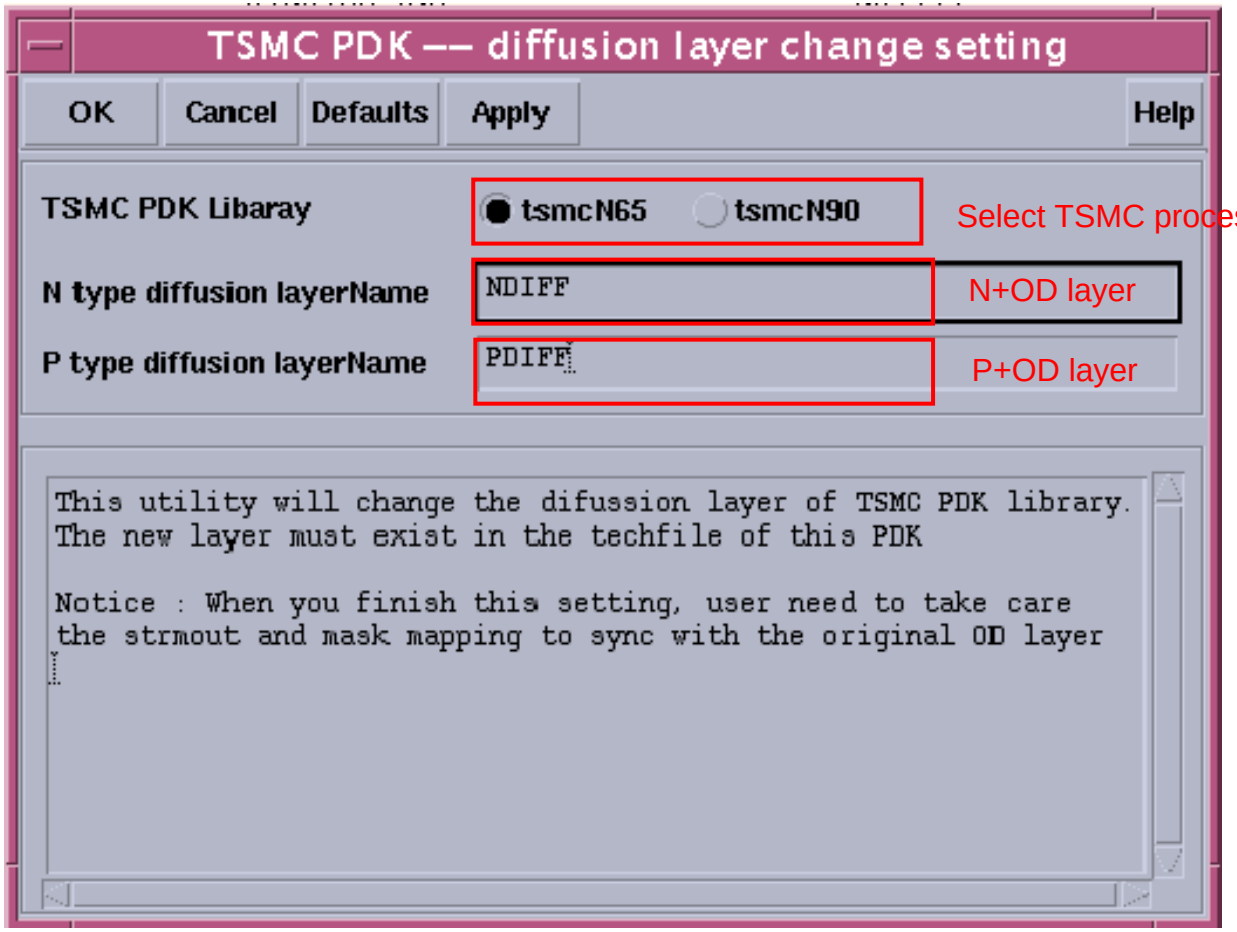
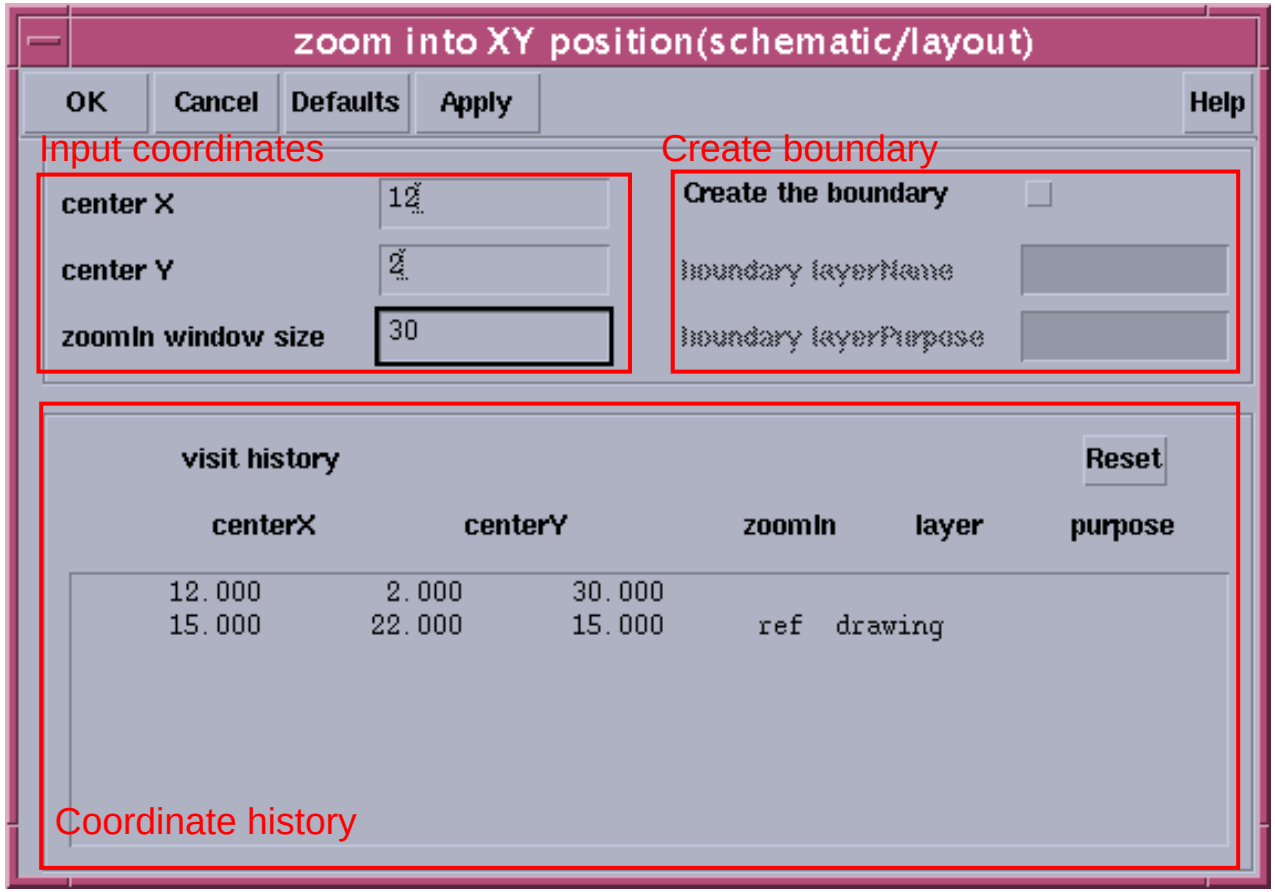
- **tsmcPdkUtilityTool :**
  - The function of tsmcPdkChangeOD will change the N+OD and P+OD layer.



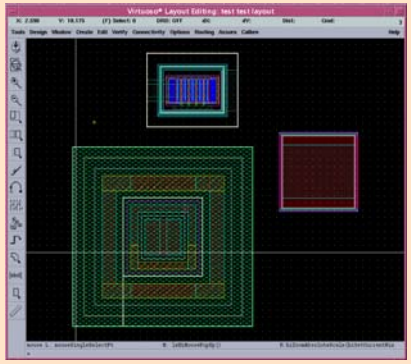
- **tsmcPdkUtilityTool :**
  - The function of tsmcPdkZoomIn is a utility to help user easy to find the layout.



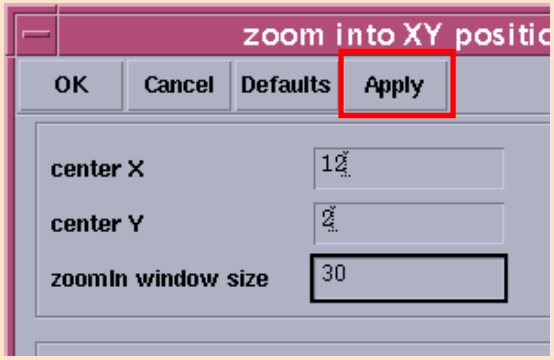
TSMCN65 PDK Usage Guide

Way1

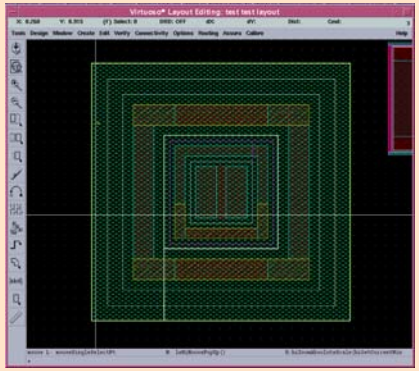
Select layout window



input coordinates and check Apply

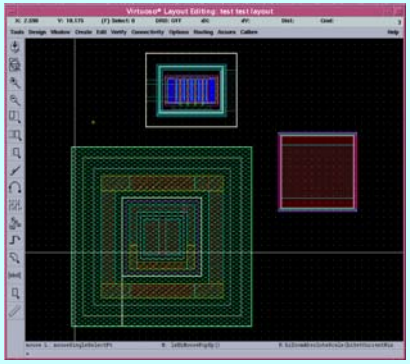


Window zoom in

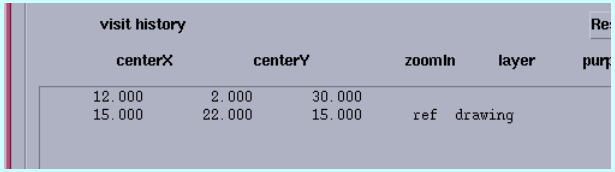


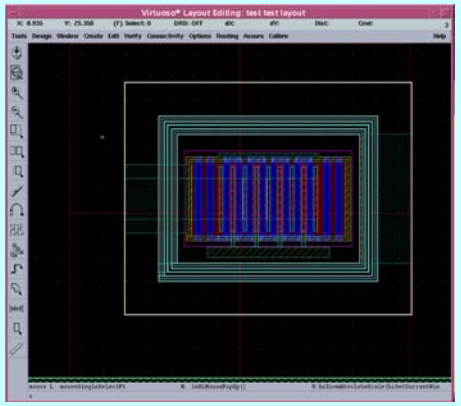
Way2

Select layout window



Double check coordinate history

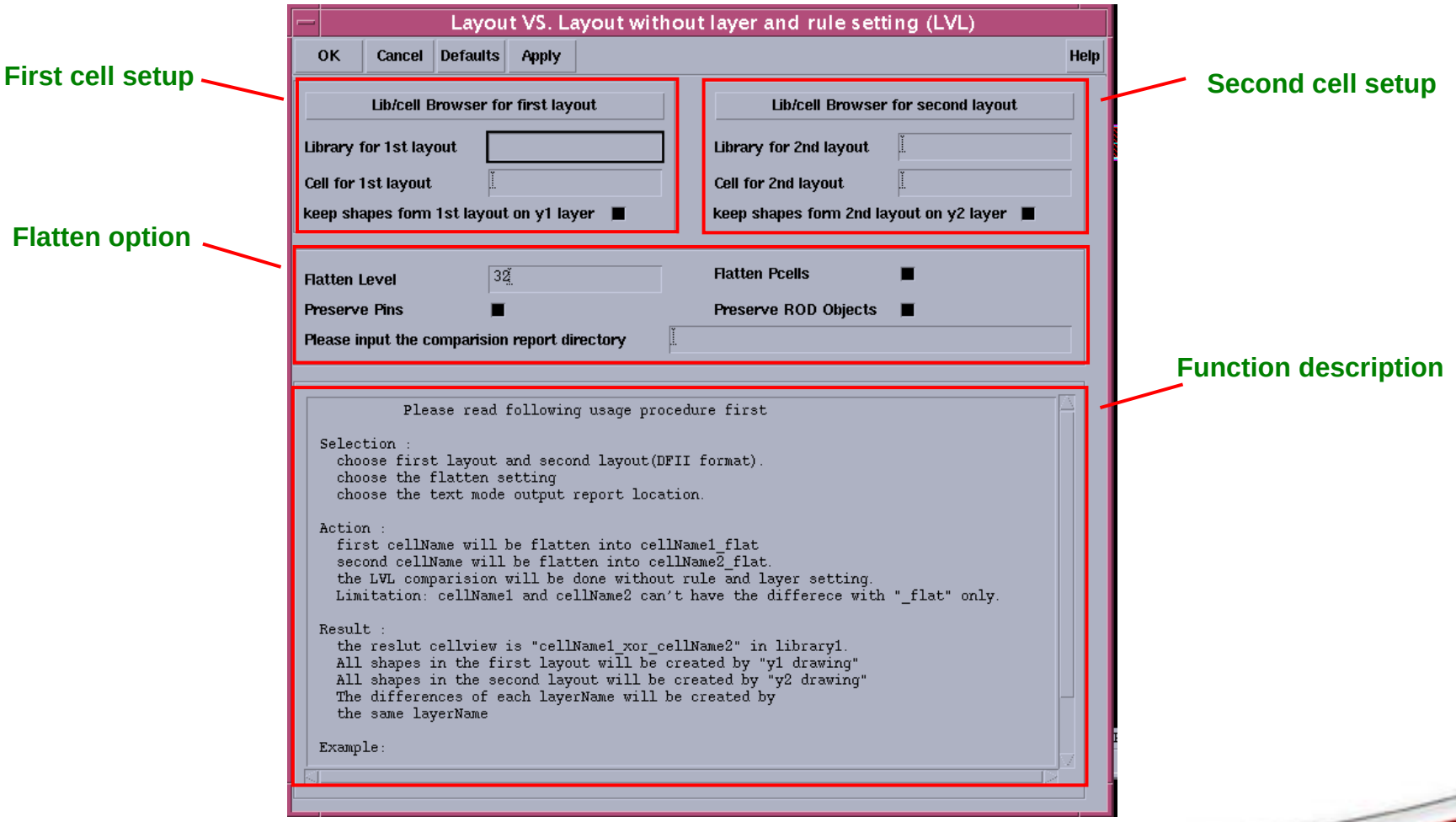




TSMCN65 PDK Usage Guide

tsmcPdkUtilityTool :

- tsmcPdkLVL utility:

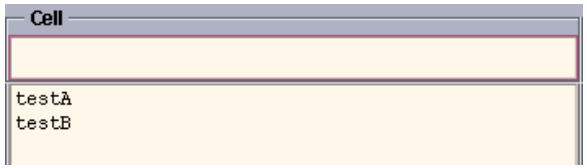


TSMCN65 PDK Usage Guide

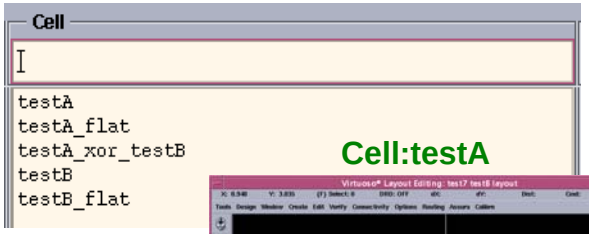
tsmcPdkUtilityTool :

- tsmcPdkLVL utility:

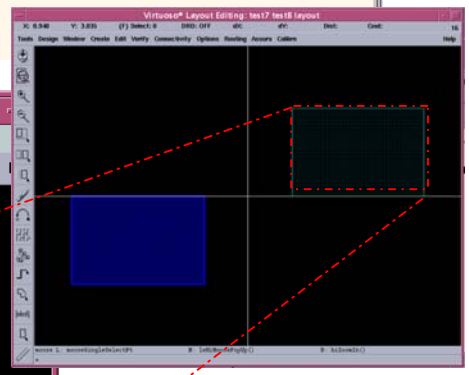
Before LVL



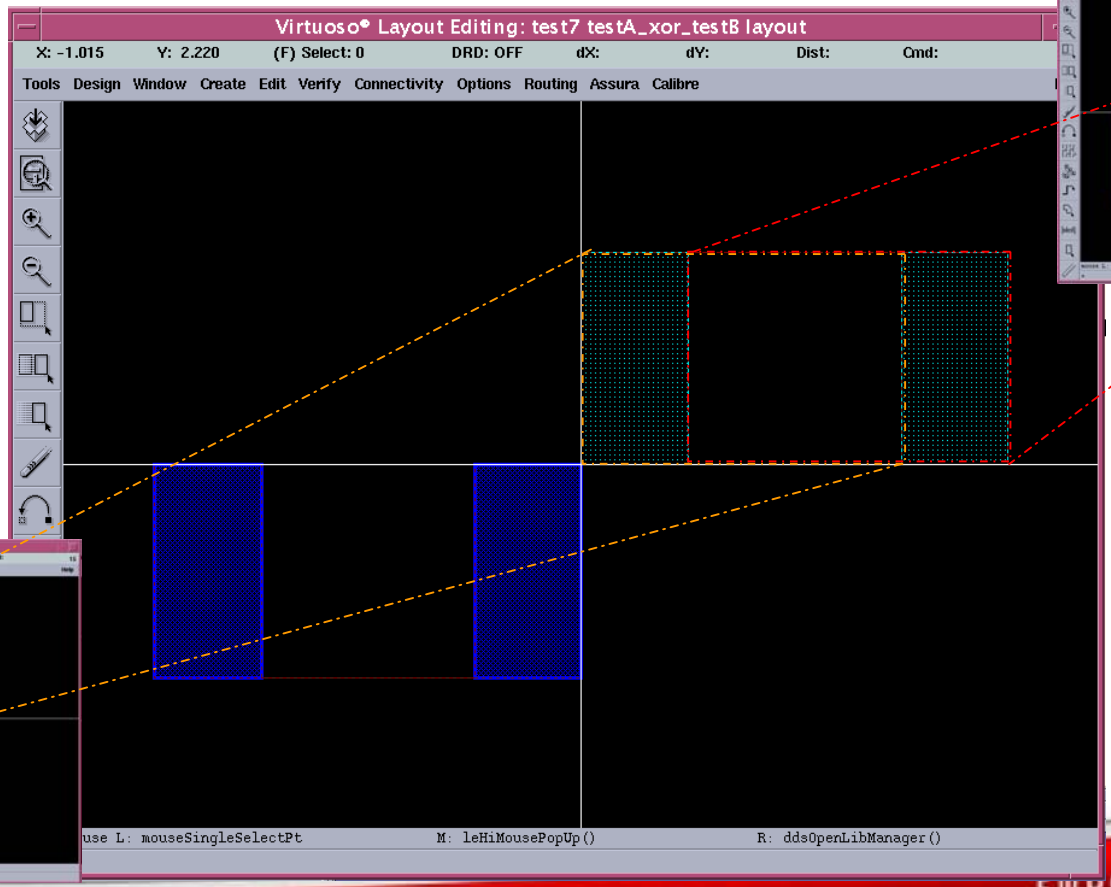
After LVL



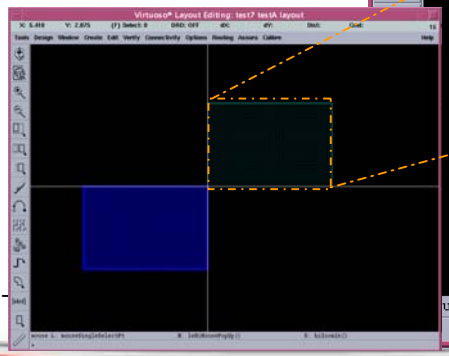
Cell:testA



Cell:testA_xor_testB



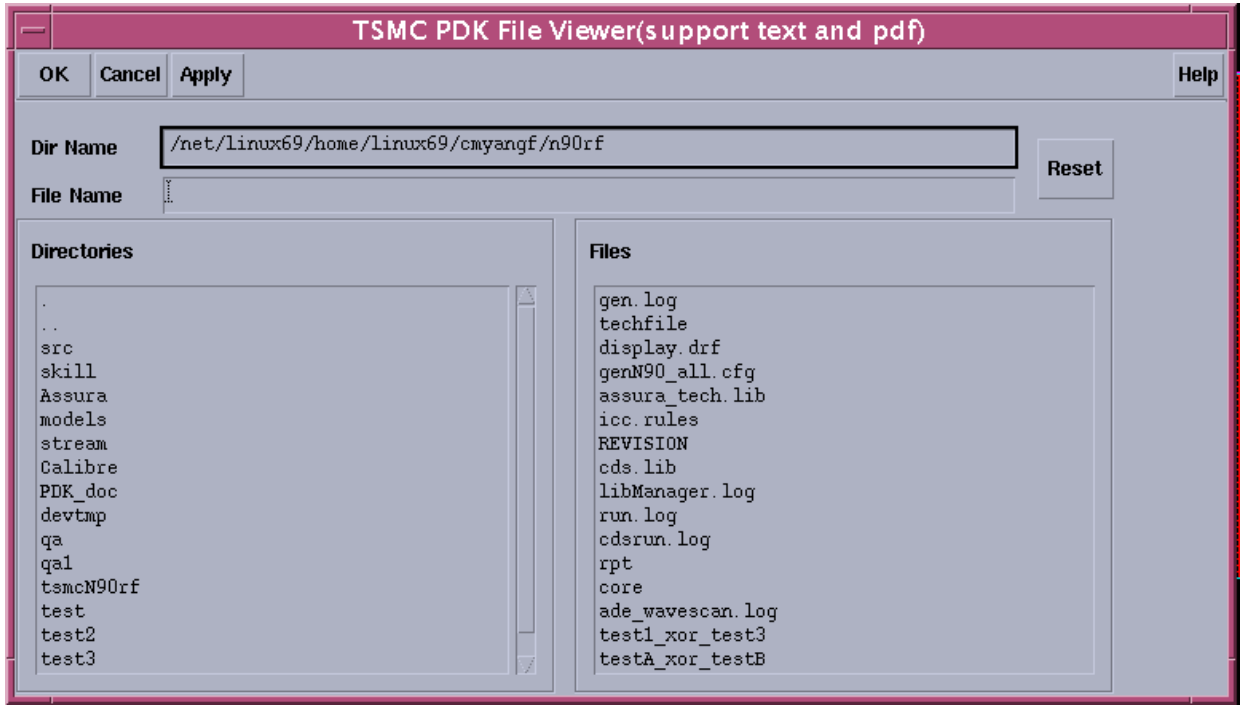
Cell:testB



TSMCN65 PDK Usage Guide

tsmcPdkUtilityTool :

- tsmcPdkFileViewer – TSMC file browser tool, user can easily find the file they needs.



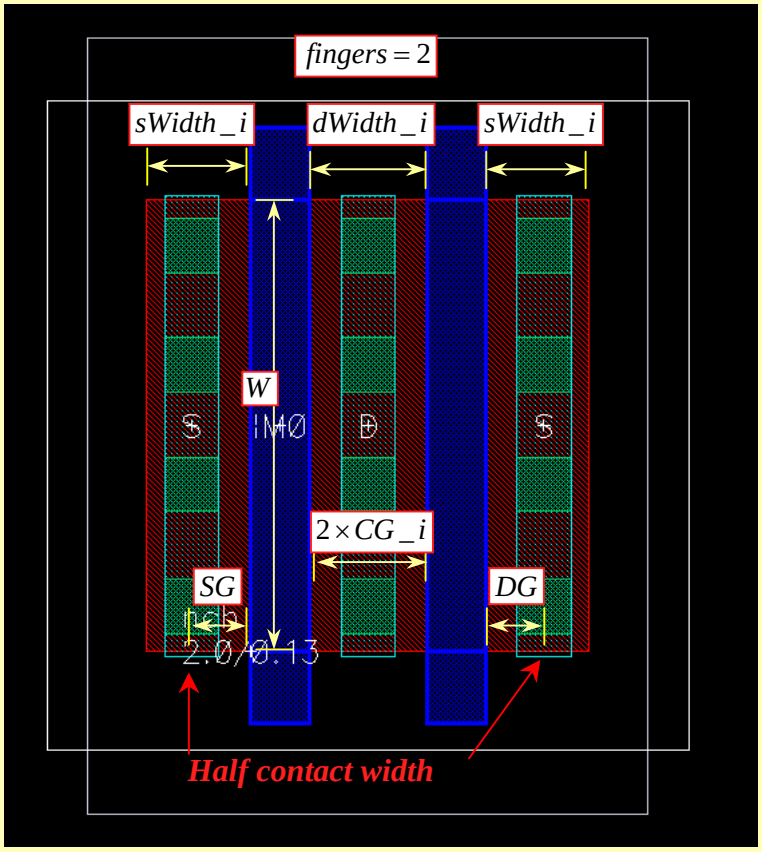
- **tsmcPdkToolAbout :**

Appendix E – AS AD PS PD NRS NRD methodology

- In this section, we will description that the PDK how to calculate as, ad, ps, pd, nrs and nrd.

Case I

• Normal MOS with multi fingers



$$S_{Area\_total} = \sum_{i=1} sWidth\_i \times w \qquad AS = S_{Area\_total} / fingers$$

$$S_{Peri\_total} = \sum_{i=1} (sWidth\_i + w \times N_s) \times 2 \qquad PS = S_{Peri\_total} / fingers$$

$$D_{Area\_total} = \sum_{i=1} dWidth\_i \times w \qquad AD = D_{Area\_total} / fingers$$

$$D_{Peri\_total} = \sum_{i=1} (dWidth\_i + w \times N_d) \times 2 \qquad PD = D_{Peri\_total} / fingers$$

N_s : Number of Source N_d : Number of Drain

$$NRS = (\sum_{i=1} CG\_i\_s + SG\_s + DG\_s) / fingers / w$$

$$NRD = (\sum_{i=1} CG\_i\_d + SG\_d + DG\_d) / fingers / w$$

CG_i_d : CG_i in Drain diffusion area

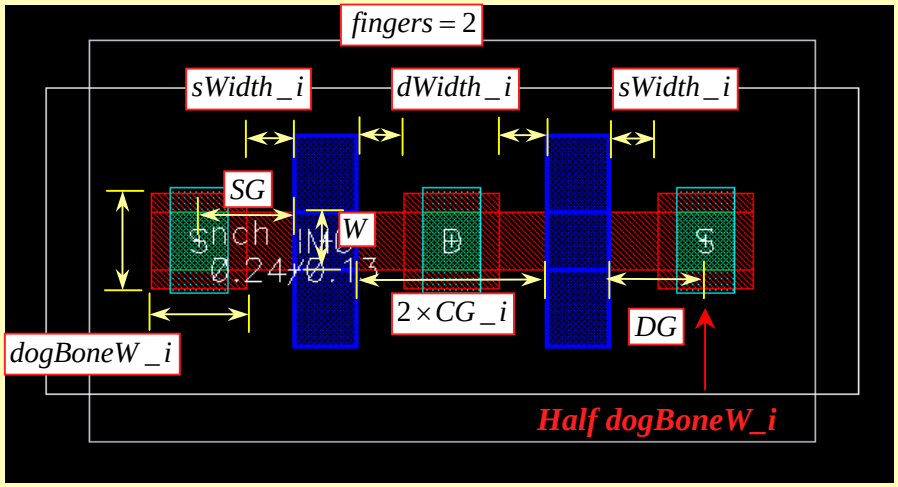
CG_i_s : CG_i in Source diffusion area

$SG\_d(SG\_s)$: SG in Drain(Source) diffusion area

$DG\_d(DG\_s)$: DG in Drain(Source) diffusion area

Case II

- ***Dog Bone MOS with multi fingers***



$$S_{Area\_total} = \sum_{i=1} sWidth\_i \times w + dogBoneW\_i \times dogBoneW\_i \times N_s$$

$$D_{Area\_total} = \sum_{i=1} dWidth\_i \times w + dogBoneW\_i \times dogBoneW\_i \times N_d$$

$$S_{Peri\_total} = \sum_{i=1} sWidth\_i \times 2 + dogBoneW\_i \times 4 \times N_s$$

$$D_{Peri\_total} = \sum_{i=1} dWidth\_i \times 2 + dogBoneW\_i \times 4 \times N_d$$

N_s : Number of Source N_d : Number of Drain

$$AS = S_{Area\_total} / fingers$$

$$PS = S_{Peri\_total} / fingers$$

$$AD = D_{Area\_total} / fingers$$

$$PD = D_{Peri\_total} / fingers$$

$$NRS = (\sum_{i=1} CG\_i\_s + SG\_s + DG\_s) / fingers / w$$

$$NRD = (\sum_{i=1} CG\_i\_d + SG\_d + DG\_d) / fingers / w$$

CG_i_d : CG_i in Drain diffusion area

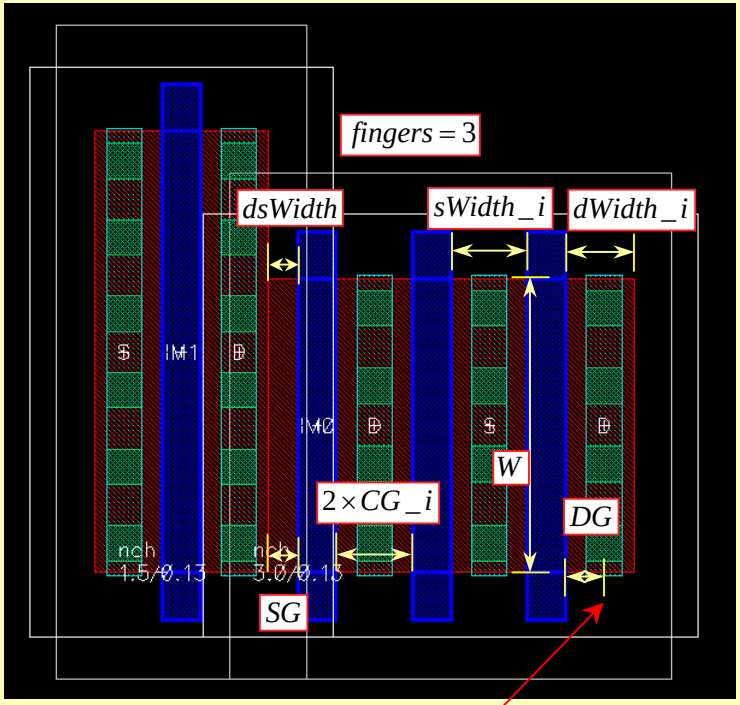
CG_i_s : CG_i in Source diffusion area

$SG\_d(SG\_s)$: SG in Drain(Source) diffusion area

$DG\_d(DG\_s)$: DG in Drain(Source) diffusion area

Case III

- ***Normal MOS with multi fingers after abut***



Half contact width

$$S_{Area\_total} = (\sum_{i=1} sWidth\_i + dsWidth) \times w$$

$$S_{Peri\_total} = (\sum_{i=1} sWidth\_i + dsWidth + w \times N_s) \times 2$$

$$D_{Area\_total} = (\sum_{i=1} dWidth\_i + ddWidth) \times w$$

$$D_{Peri\_total} = (\sum_{i=1} dWidth\_i + ddWidth + w \times N_d) \times 2$$

N_s : Number of Source N_d : Number of Drain

$AS = S_{Area\_total} / fingers$ $PS = S_{Peri\_total} / fingers$

$AD = D_{Area\_total} / fingers$ $PD = D_{Peri\_total} / fingers$

$$NRS = (\sum_{i=1} CG\_i\_s + SG\_s + DG\_s) / fingers / w$$

$$NRD = (\sum_{i=1} CG\_i\_d + SG\_d + DG\_d) / fingers / w$$

CG_i_d : CG_i in Drain diffusion area

CG_i_s : CG_i in Source diffusion area

$SG\_d(SG\_s)$: SG in Drain(Source) diffusion area

$DG\_d(DG\_s)$: DG in Drain(Source) diffusion area

Appendix F – SA SB SD methodology

- In this section, we will description that the PDK how to calculate sa and sb.

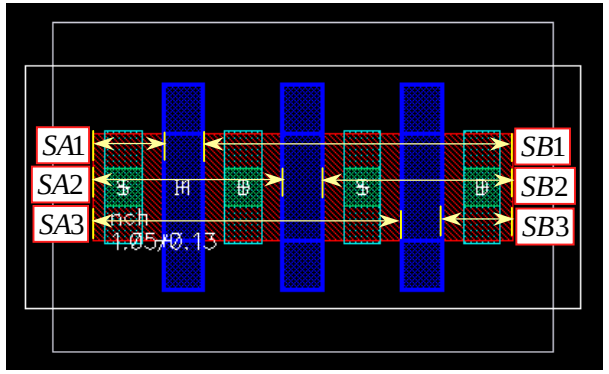
- For post-layout simulation (netlists extracted from the layout):

  Treat each finger of devices as an independent MOS. And thus PDK assigns different SA/SB to each independent MOS. So the netlist will look like (if finger_number=3):

m1 d g s b w=channel width l =channel length SA=SA1 SB=SB1

m2 d g s b w=channel width l =channel length SA=SA2 SB=SB2

m3 d g s b w=channel width l =channel length SA=SA3 SB=SB3



- For pre-layout simultation (netlists estimated from schematic diagram):

  PDK sets m=finger_number, SA=SA, SB=SB and SD=SD. So the netlist will look like

  m0 d g s b w=channel width l =channel length m=1 SA=SA SB=SB SD=SD

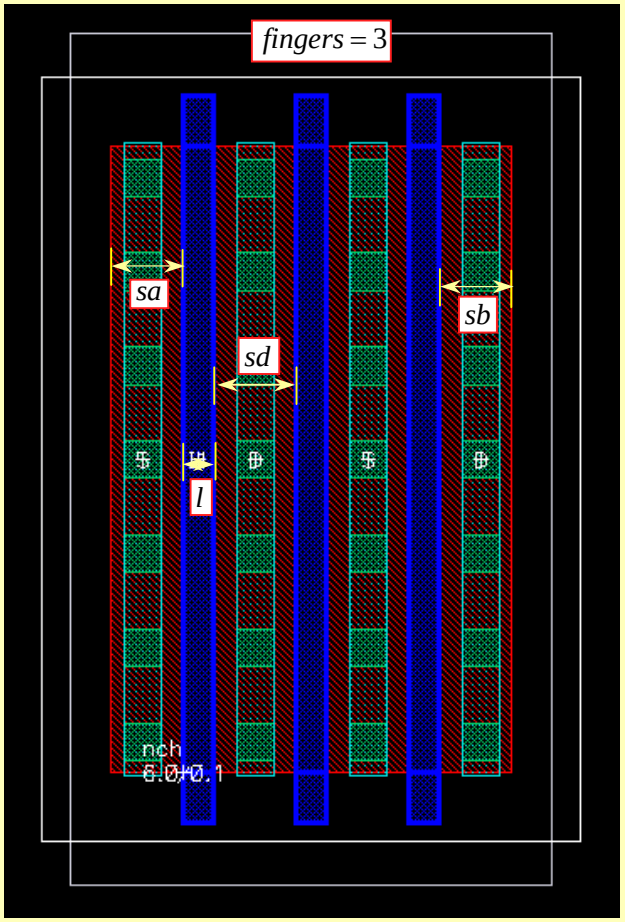
  Please refer next two page to understand the SA, SB and SD in layout

TSMCN65 PDK Usage Guide

- In this page, we will description that the PDK how to calculate SA, SB and SD.

Case I

• Normal MOS with multi fingers



SA = sa : *In the netlist, SA equal to sa*

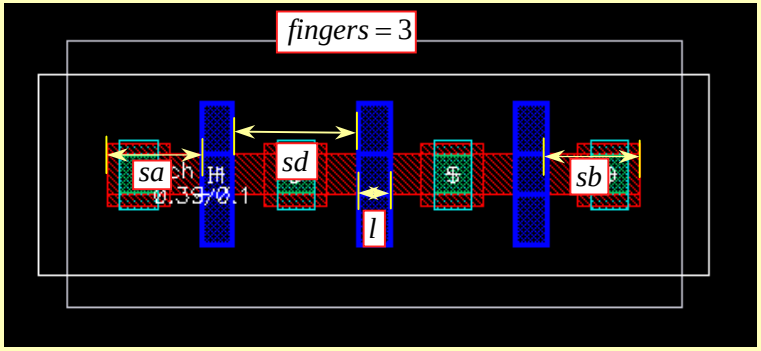
SB = sb : *In the netlist, SB equal to sb*

SB = sd : *In the netlist, SB equal to sd*

- In this page, we will description that the PDK how to calculate SA, SB and SD.

Case II

- ***Dog Bone MOS with multi fingers***



SA = sa : *In the netlist, SA equal to sa*

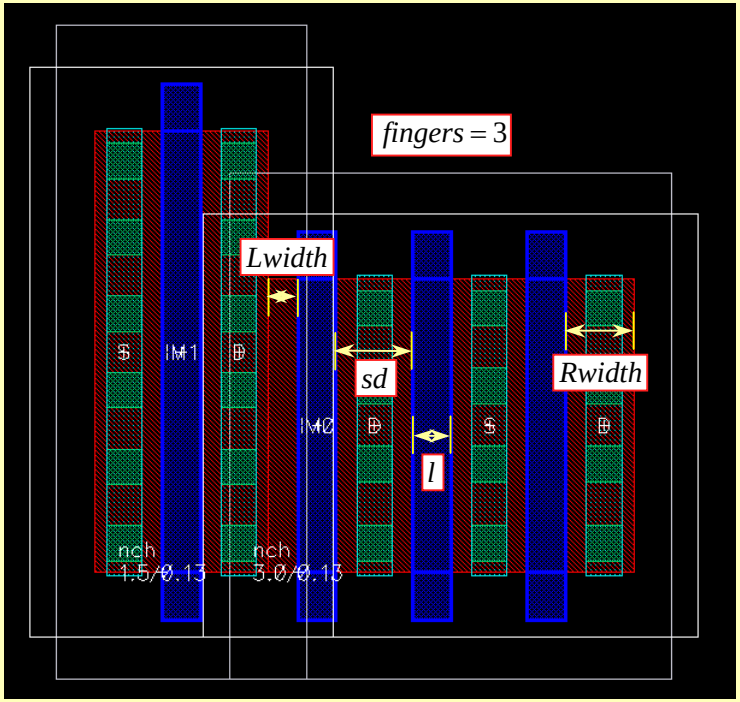
SB = sb : *In the netlist, SB equal to sb*

SB = sd : *In the netlist, SB equal to sd*

- In this page, we will description that the PDK how to calculate SAeff and SBeff.

Case III

- ***Normal MOS with multi fingers after abut***



$$Sum1_i = 1/(Lwidth + i \times (sd + l) + 0.5 \times l)$$

$$SAeff = fingers / \sum_{i=0}^{fingers-1} Sum1_i - 0.5 \times l$$

$$Sum2_i = 1/(Rwidth + i \times (sd + l) + 0.5 \times l)$$

$$SBeff = fingers / \sum_{i=0}^{fingers-1} Sum2_i - 0.5 \times l$$

$$SAeff = SAeff$$

$$SBeff = SBeff$$

$SA = SAeff$: *In the netlist, SA equal to SAeff*

$SB = SBeff$: *In the netlist, SB equal to SBeff*

$SA = sa$: *In the netlist, SA equal to sa*

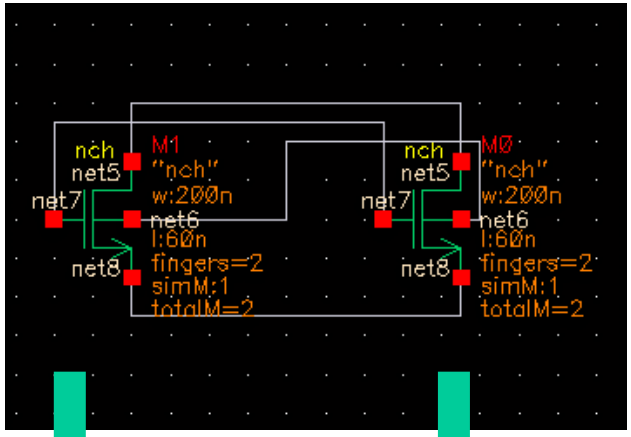
$SB = sb$: *In the netlist, SB equal to sb*

$SB = sd$: *In the netlist, SB equal to sd*

TSMCN65 PDK Usage Guide

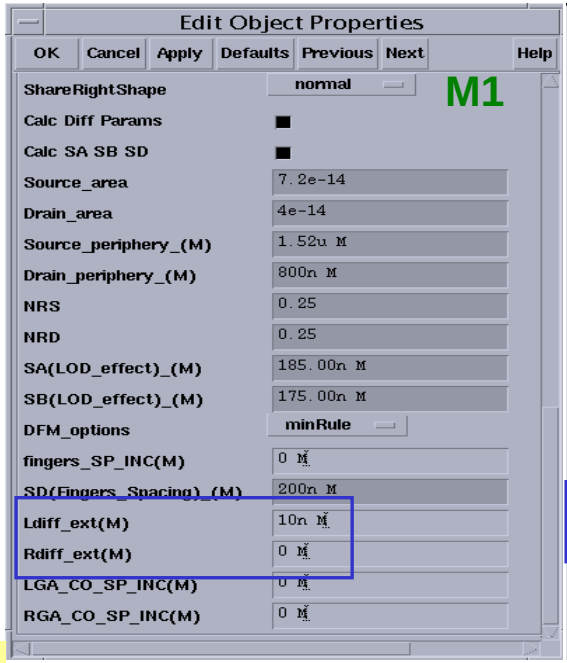
Appendix G – Multiple devices Abutment methodology

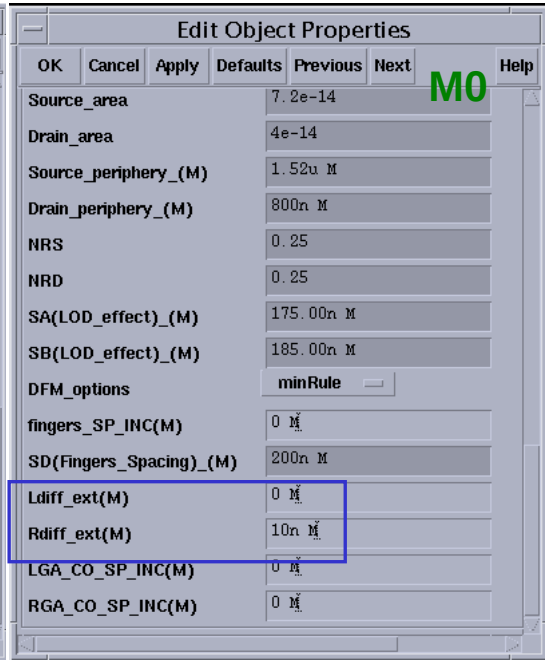
- In this section, we will describe that the PDK how to use multiple devices abutment with Ldiff_ext and Rdiff_ext

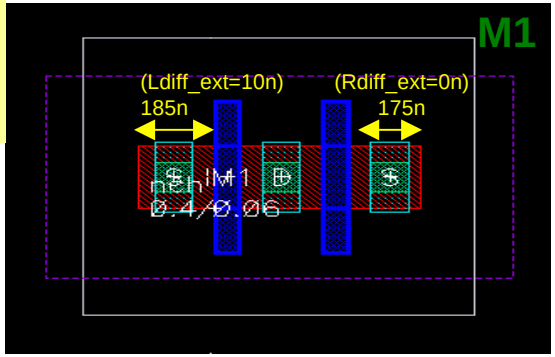


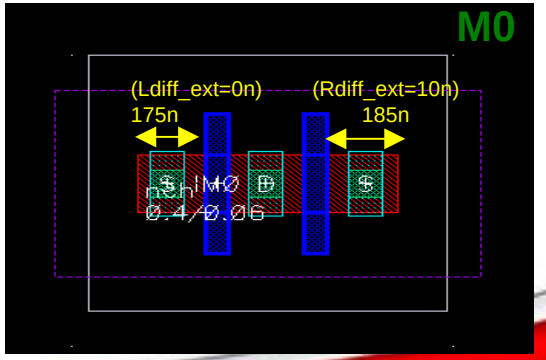
M1:
Ldiff_ext(M):10n
Rdiff_ext(M): 0n

M0:
Ldiff_ext(M): 0n
Rdiff_ext(M):10n

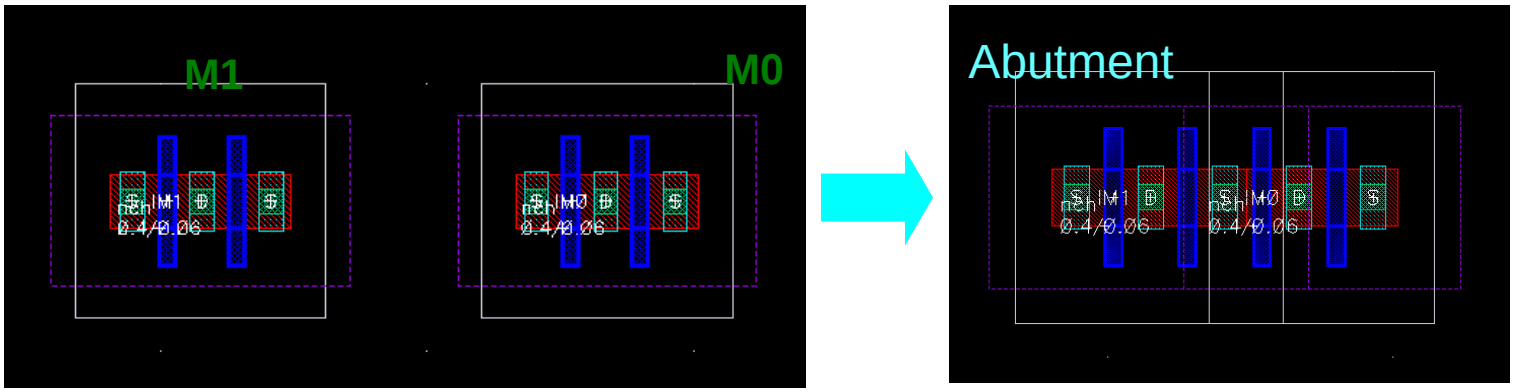


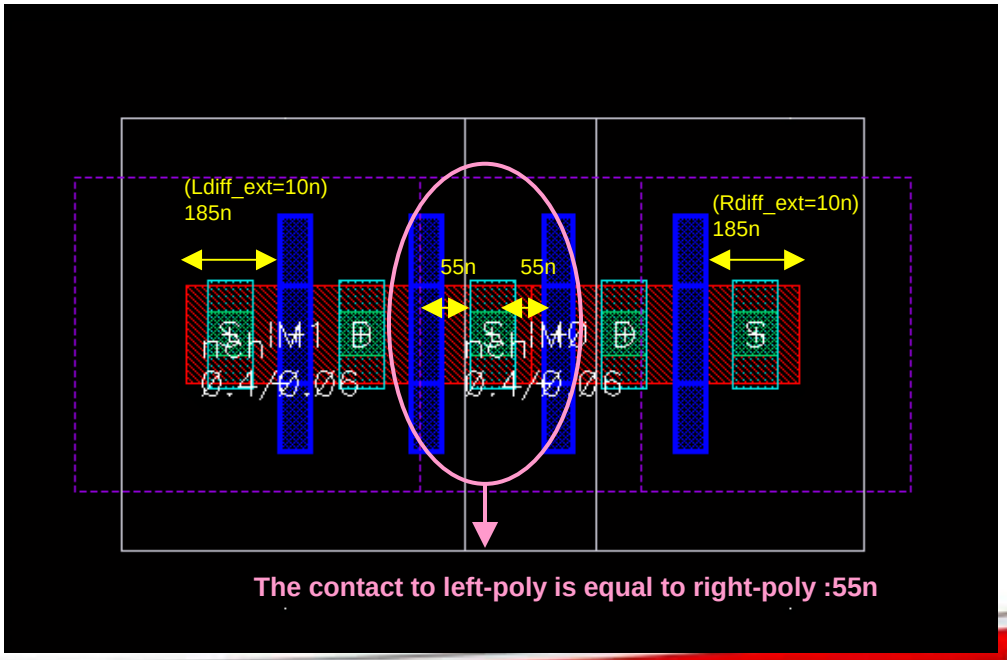






■use multiple devices abutment with Ldiff_ext and Rdiff_ext

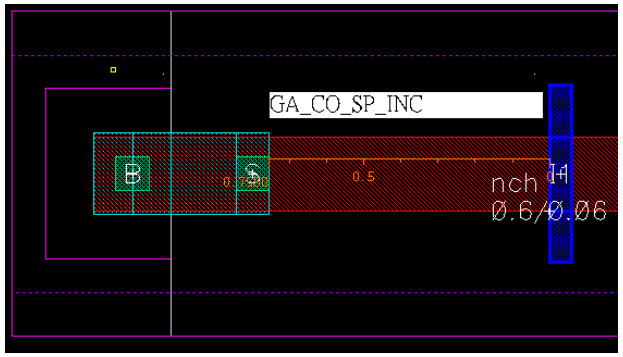




Appendix H – MOS pcell usage GA_CO_SP_INC

- Function introduction

  - GA_CO_SP_INC : Add gate to contact spacing for DFM
    - Real spacing = GA_CO_SP_INC + Original spacing

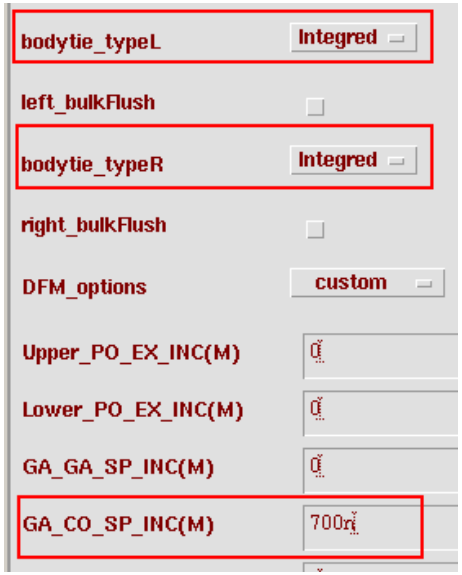


  - Ldiff_ext : extend left-hand side OD
  - Rdiff_ext : extend right-hand side OD

Appendix H – MOS pcell usage GA_CO_SP_INC

- Problem description

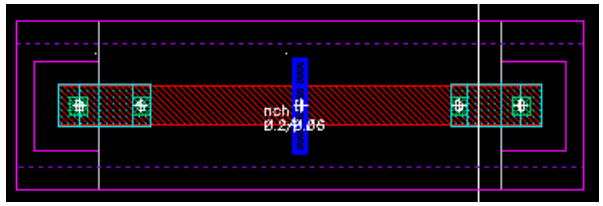
  - Mos pcell
    - When turning on bodytie as integred and set GA_CO_SP_INC to 700n, mos pcell will fail.

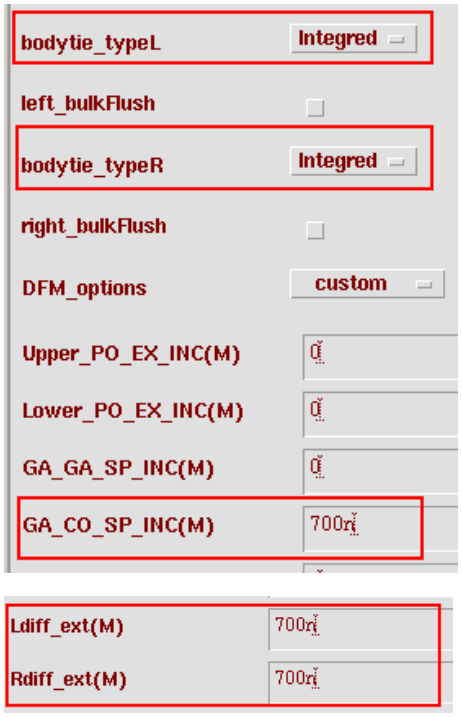


Appendix H – MOS pcell usage GA_CO_SP_INC

- Problem solution

  - **Correct usage method :**
    - Before setting GA_CO_SP_INC, Ldiff and Rdiff should extend first.
    - Let contacts have space to insert or contact will over-extend.





Appendix H – Sdshrink and Poly Gate position

- Routing method : M1 will extend if route_source_drain option set to “both”.