N65LP 2.4GHz RF LC-tank VCO Process Vehicle Report

Process: N65LPGV2
TM#: TMT501, TMT504
Designer: RFDP/SDP/tsmc
Report Date: August 31, 2007
Version: Preliminary 0.1v

Contents

1. Introduction

This design guide of N65LP 2.4GHz LC-tank VCO is for process vehicle purpose to verify design flow from process, spice model, PDK, circuit and silicon measurement. The meaning is from frond-end of circuit to back-end overall flows verification in tsmc N65LP process technology. In this design guide, we start from VCO core circuit, output buffer design, especially in frequency tuning, phase noise, current and output power circuit simulation. Second, we had done back-end flow in GDS layout, parasitic capacitance extraction and post-simulation. Finally, the silicon measurement is compare to all of design procedure in pre-simulation and post-simulation results.

2. Specification

(1) LC-VCO DC Specification

Item	Parameter	Condition	MIN.	TYP	MAX	Unit
Vdd	VCO core Supply Voltage			1.2		V
Vd25_buf	Buffer Supply Voltage			2.5		V
VIL	Logic low for control signal				0.2VDD	V
VIH	Logic high for control voltage		0.8VDD			V
Ivdd	VCO core current consumption	TT, 25C		1		mA
Ivd25_buf	Buffer current consumption	TT, 25C		16		mA

(2) LC-VCO AC Specification

Item	Parameter	Condition	MIN.	TYP	MAX	Unit
Fout	VCO Output frequency		2300	2400	2600	MHz
PN	Phase noise @1MHz offset			110		dBc/Hz
Kvco	VCO gain			100		MHz/V
Vout	Output Swing	Single-end		0.5		Vpp
Cload	Output Load Drive @buffer			1		pF
Rout	Output impedance			50		ohm

3. Schematic

This design has used a complementary cross-coupled LC-tank VCO structure to provide negative resistance to sustain VCO oscillation. The device is 1.2v core device, 3X1Z1U metal scheme of inductor, MIM capacitor of ac coupling application and varactor for tunable of frequency output. Figure 1 shows the VCO core schematic.

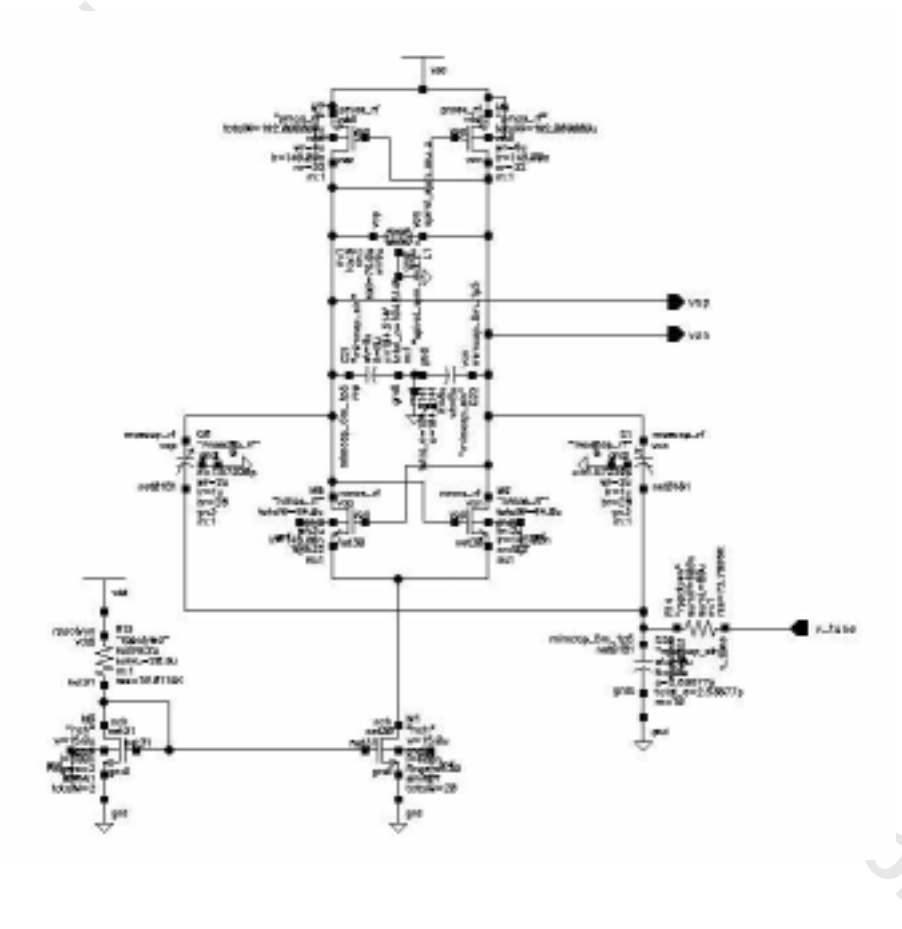


Fig. 1 LC-tank VCO

TSMC PDK Inductor Finder:

The LC-tank VCO generally consists of an LC tank and a negative resistance circuit. And the quality factor (Q) of LC-tank is one of main parameters that affect phase noise. In modern CMOS process, the dominant factor of the quality factor of an LC-tank is the inductor.

In the TSMC PDK, there is a function to search suitable inductor.

<i> Choose inductor and select Edit -> properties

<ii> Press Finder item and fill in the design spec.

Design Frequency ; L value ; available L value ; minimum Q factor ; inductor area

<iii>Press FIND

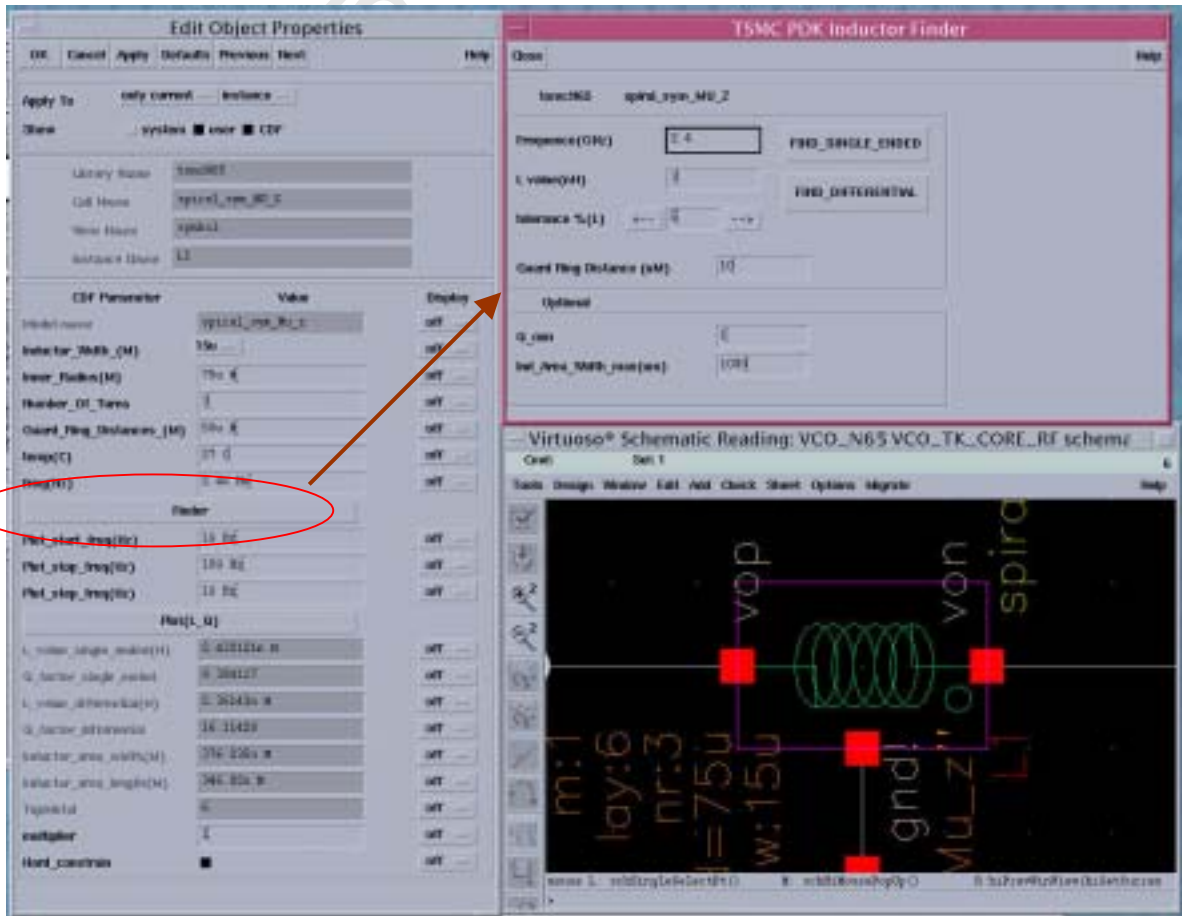


Fig. 2 TSMC PDK Inductor Finder

As shown in Fig3, after searching inductor, each parameter of inductor is listed and can be trade off with the design spec. When the suitable inductor is chosen, the graph of inductance and quality factor will pop out after pressing LQ preview item.

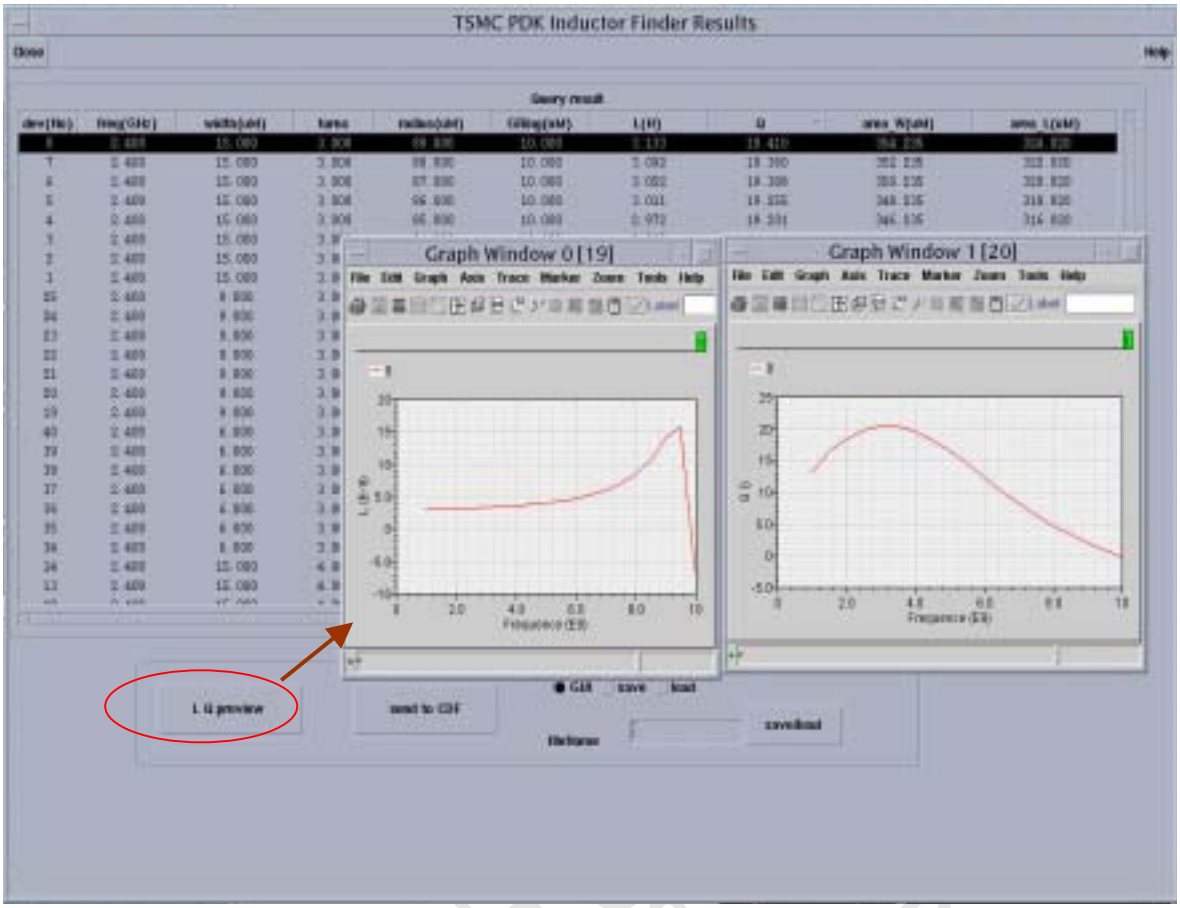


Fig. 3 TSMC PDK Inductor Finder results

The output buffer has used 2.5V device and driving external 50-Ohm load of design. This output buffer is a differential pair with AC coupling input, self-bias DC circuit and differential output. And, it provides 300mVp-p(single) output swing. Figure 4 shows output buffer design. Power supply for the output buffer is 2.5V and the current consumption is 16mA.

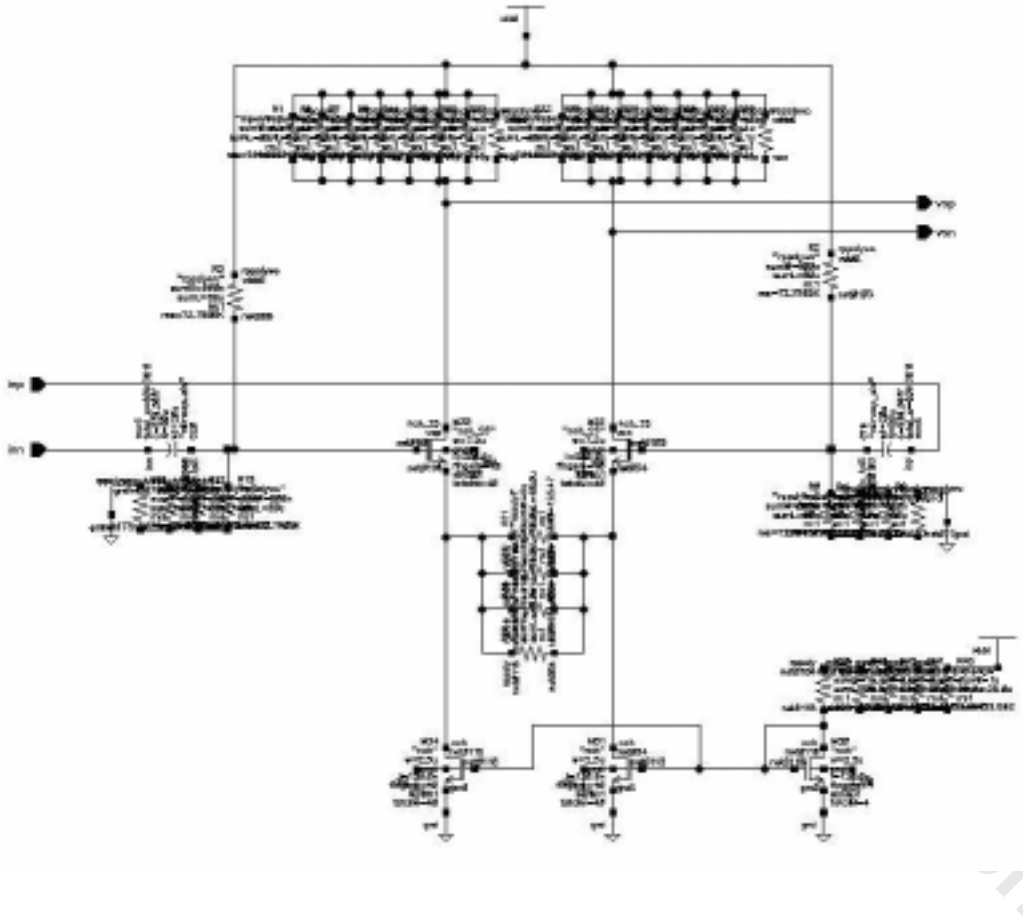


Fig 4 VCO output buffer

4. Pre-Simulation

The VCO target frequency, tuning range and phase noise are key performance of VCO design. Simulation of those parameters can be done by PSS and pnoise simulation in cadence spectreRF. And this design also need to consider the corner effect in VCO performance. The following of setting figure is for PSS, pnoise and corner simulation.

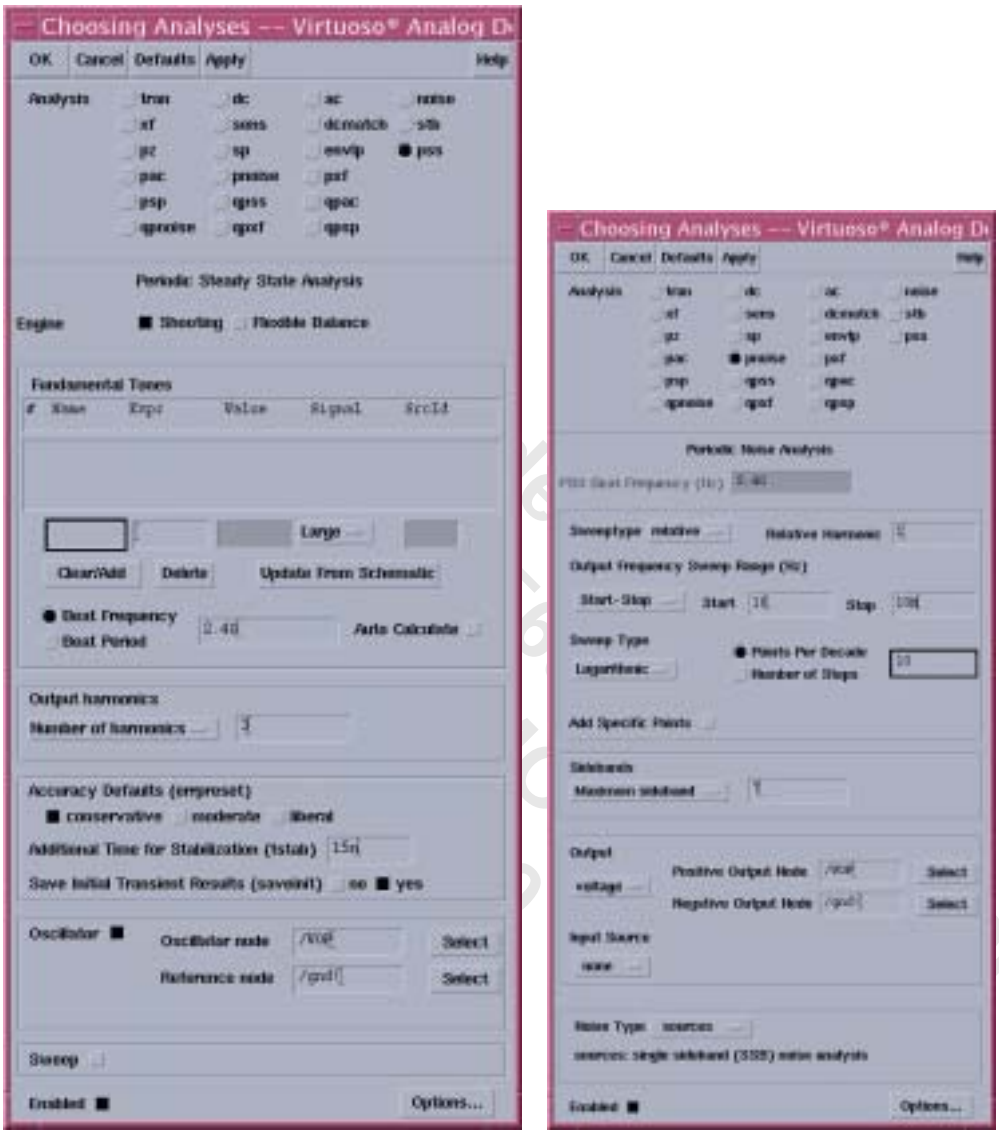


Fig 6 PSS and pnoise setting in cadence ADE environment

Corner simulation setup procedure: ADE Tools ----> corner

load xxx.pcf from pdk models path.

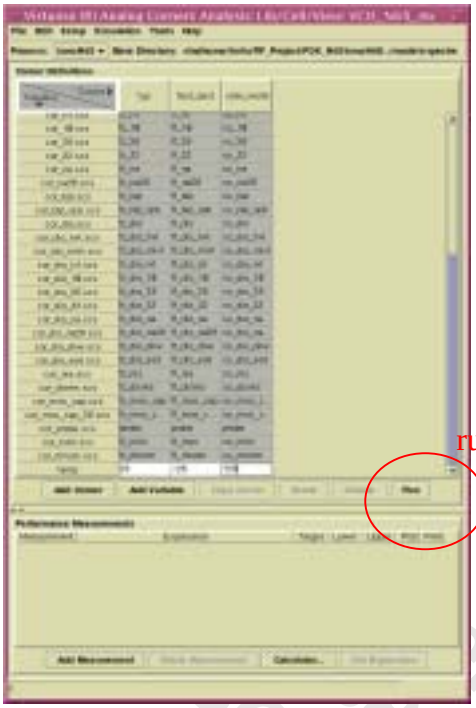


Fig 7 Corner setting

1) Tuning Frequency

This is VCO output frequency vs. tuning voltage. The output frequency is from 2.3GHz to 3GHz. That is related varator capacitor tuning selection with inductor value to define frequency range.

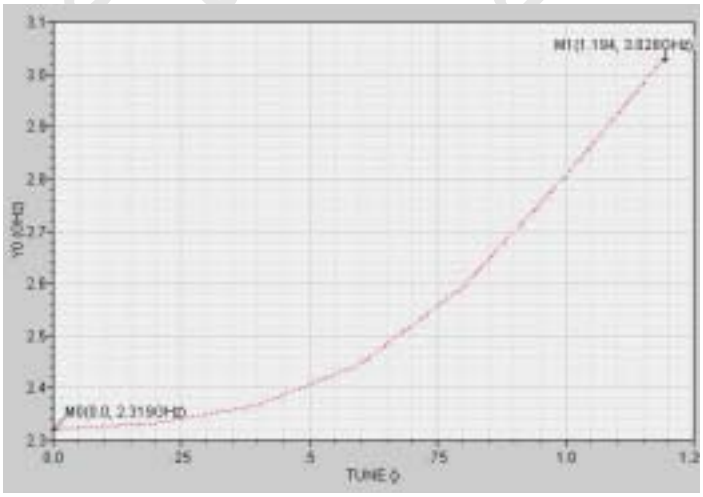
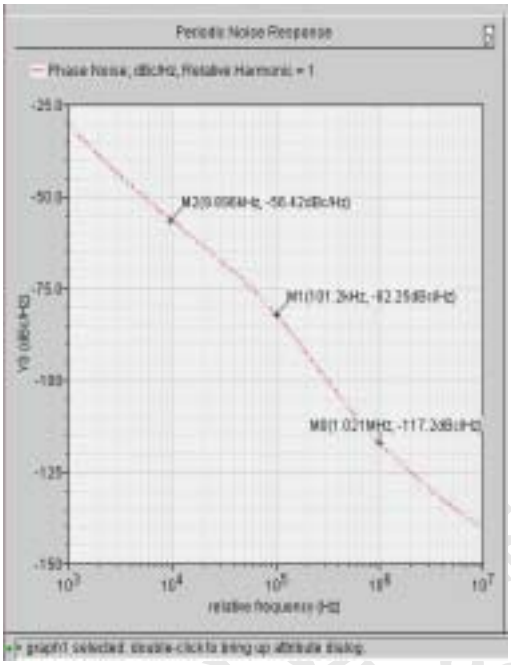


Fig 8 frequency tuning range

2) Phase Noise

In following figure, phase noise of VCO is shown at different offset frequencies with respect to center frequency. They are –82dBc/Hz and -117dBc/Hz at 100KHz, 1MHz offset frequency, respectively.



Offset Freq.	Pre-sim (dBc/Hz)
1K	-30
10K	-56.4
100K	-82.2
1M	-117
10M	-140

Fig 9 phase noise

3) Transient Signal

This diagram shows VCO core output transient signal and swing. The output swing is 400mV.

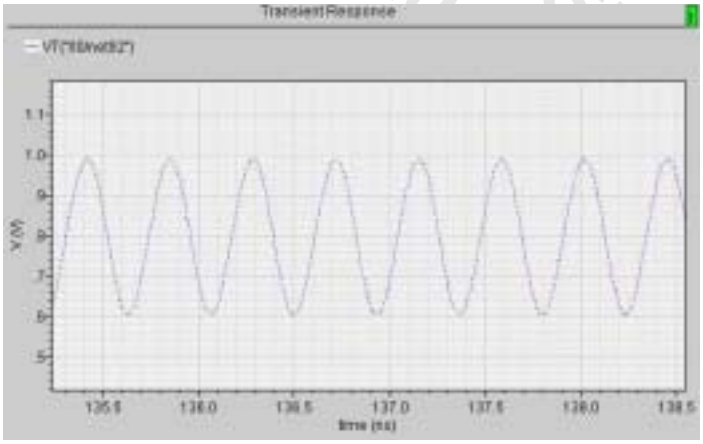


Fig 10 transient signal

5. Extraction Flow

The purpose of this section is to show parasitic extraction flow. A 2.4G complementary cross-coupled VCO is presented to go through the whole extraction flow. There are two ways for RLC extraction flow. One is Calibre extraction simulation and the other is Assura extraction simulation.

A.) Calibre Extraction Flow

1. Calibre Demo Environment

1.1 PDK version

PDK version：

CRN65LP_PDK_1.1a_official_2007_05_31_all_12v25v3x1z1u

Please copy below directory to local directory

CRN65LP_PDK_1.1a_official_2007_05_31_all_12v25v3x1z1u/Calibre

1.2 Extraction rule file

Please download rule deck with specific metal scheme from EDW system

(Need to request from PDK team)

For this case, rule deck file : RC_xCalibre_crn65lp_1p6m_3X1Z1U_alrdl_typical_v1.0.tar

The setup is as follows :

<i> Untar and include the file “crn65lp_1p06m+alrdl_typical.res” into rules

<ii> Include the file “rules” into “/local directory/…/…/Calibre/rcx/calibre.rcx”

<iii> The new caliber.rcx has used for RLC extraction

Note: To avoid double count

** calibre.rcx need to be added** LAYOUT CASE YES

LVS COMPARE CASE NAMES

PEX IDEAL XCELL YES

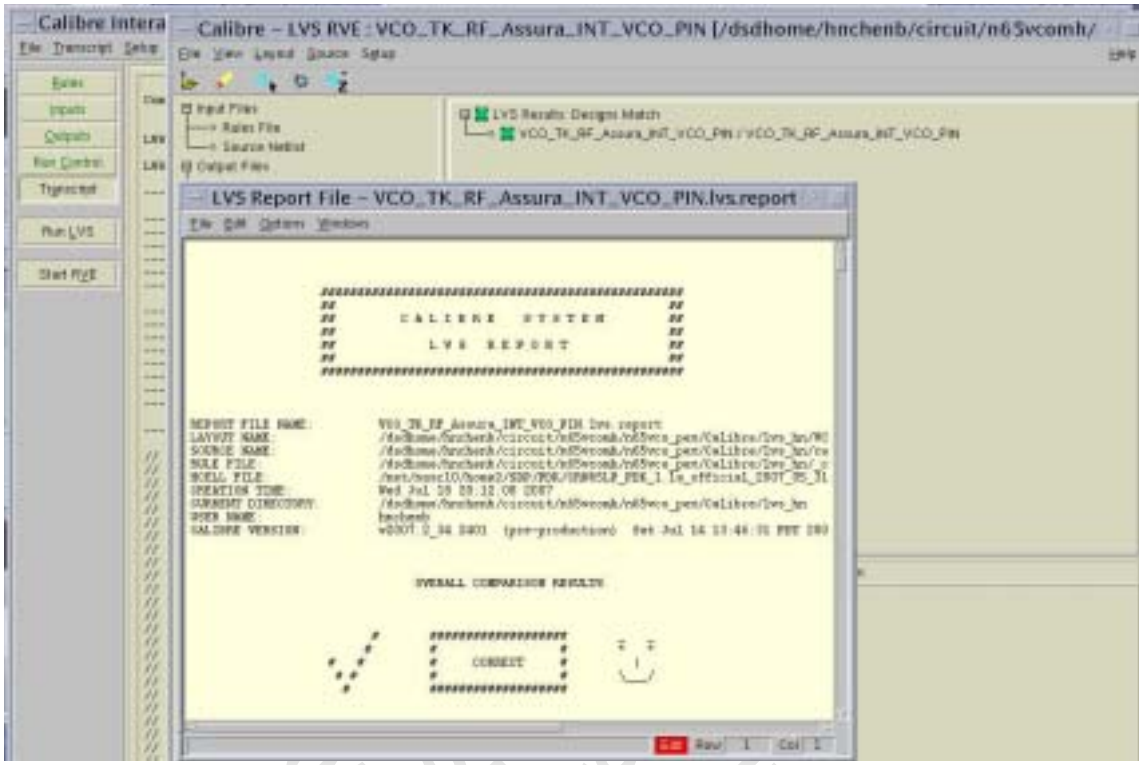
where the three lines was added manually

2. Setup Calibre PEX step-by-step

2.1 Run LVS and check LVS clean

LVS： from layout view， pull down **caliber** menu and press **Run LVS**；

LVS result should look like



2.2 Run Calibre PEX

PEX： from layout view， pull down **caliber** menu and press **Run PEX**；

Setp1. Rules :

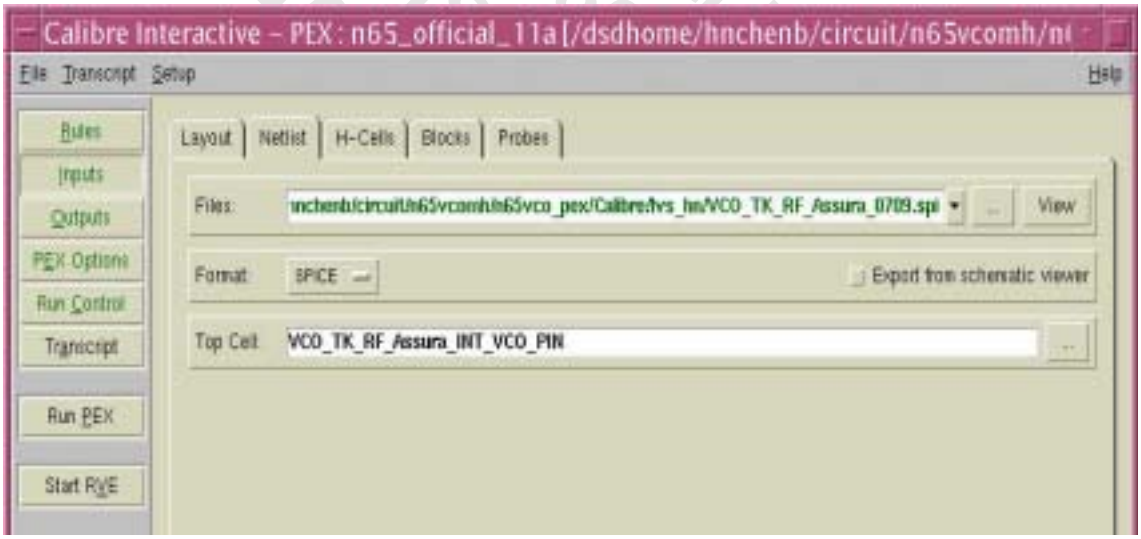
a.) Choose your run directory

Setp2. Inputs

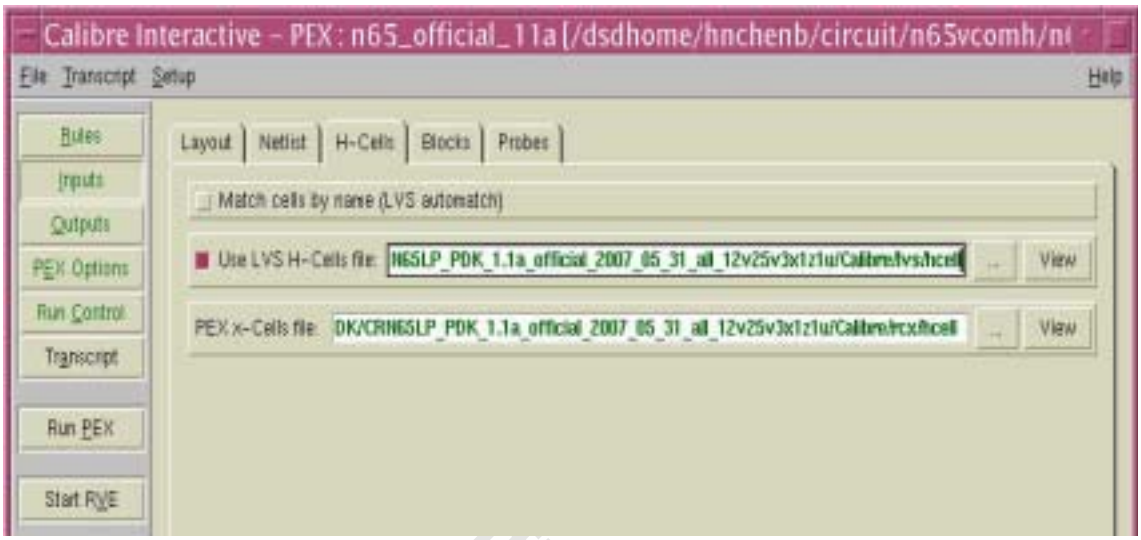
a.) **Disable** the Export from layout viewer box if you already have GDS file.

Or **enable** it to make sure the new update GDS file

b.) **Choose** the correct netlist



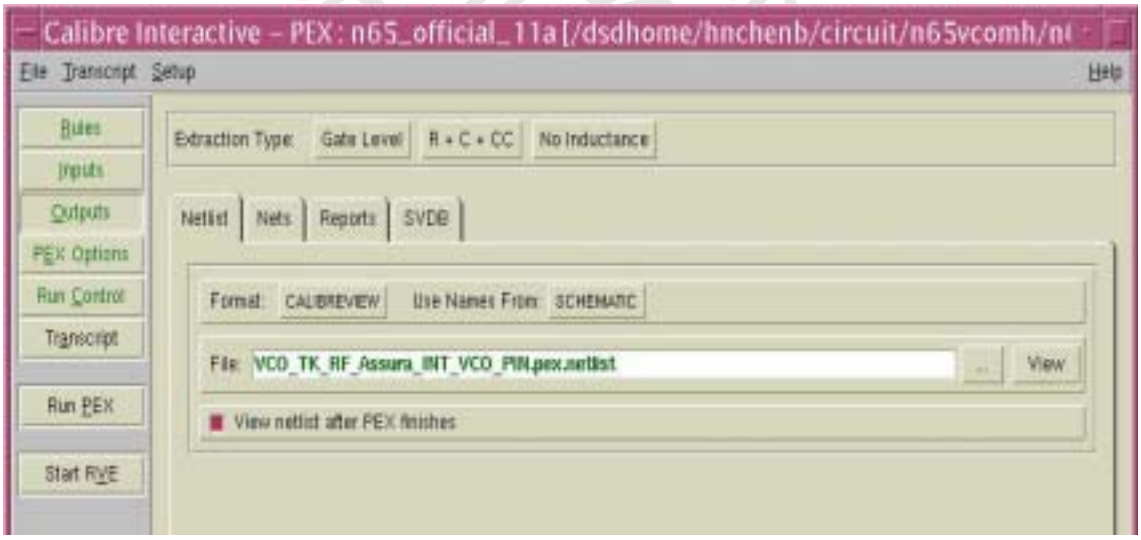
c.) Please **enable** H-cell file with the Gate level output



Setp3. Outputs

a.) Select the **Gate level** type to avoid double counting inside RF device.

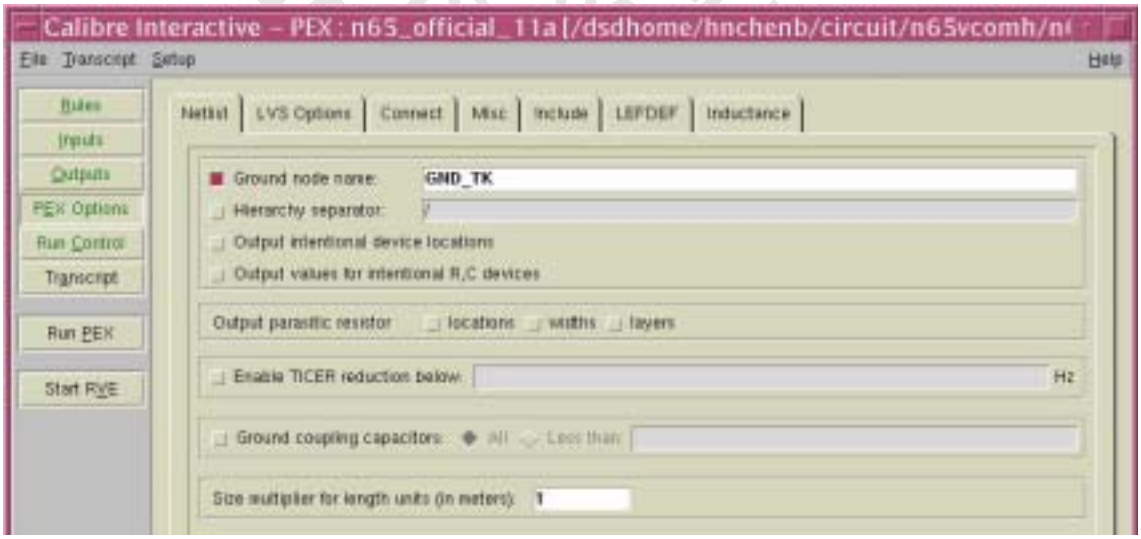
b.) Choose **CALIBRE VIEW** output format



d.) If you want to extract some specified net, choose **Specified Nets**.

Setp4. PEX Options

a.) **Disable** Ground coupling capacitor for accuracy guarantee

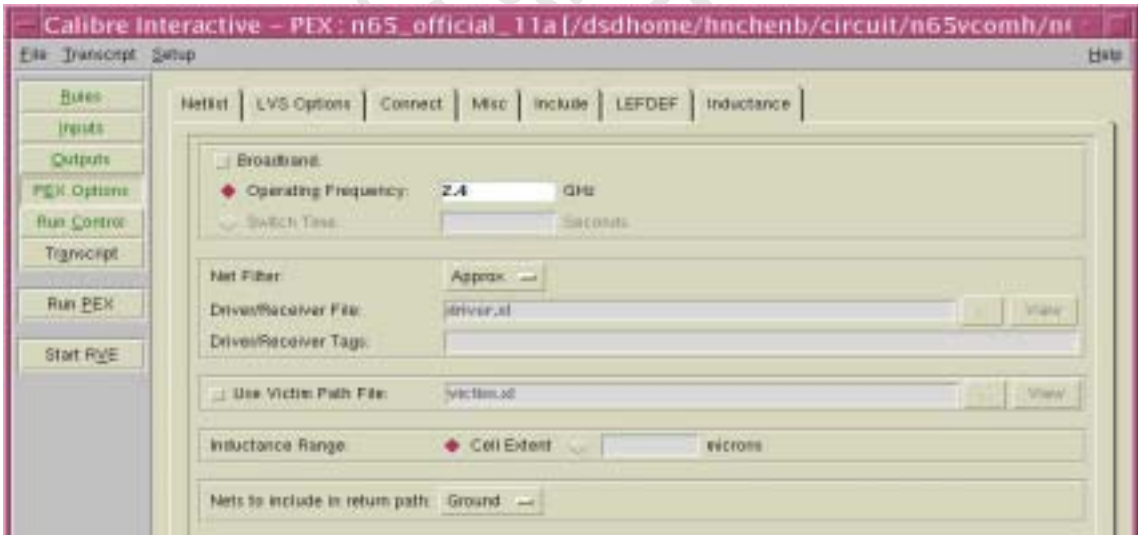


b.) Recognize gates should be chosen **none**

c.) **Enable** Output looped resistance to RC netlist for accuracy guarantee

Parasitics to output to RC netlist should be chosen **All**

c.) Fill in the operating Frequency



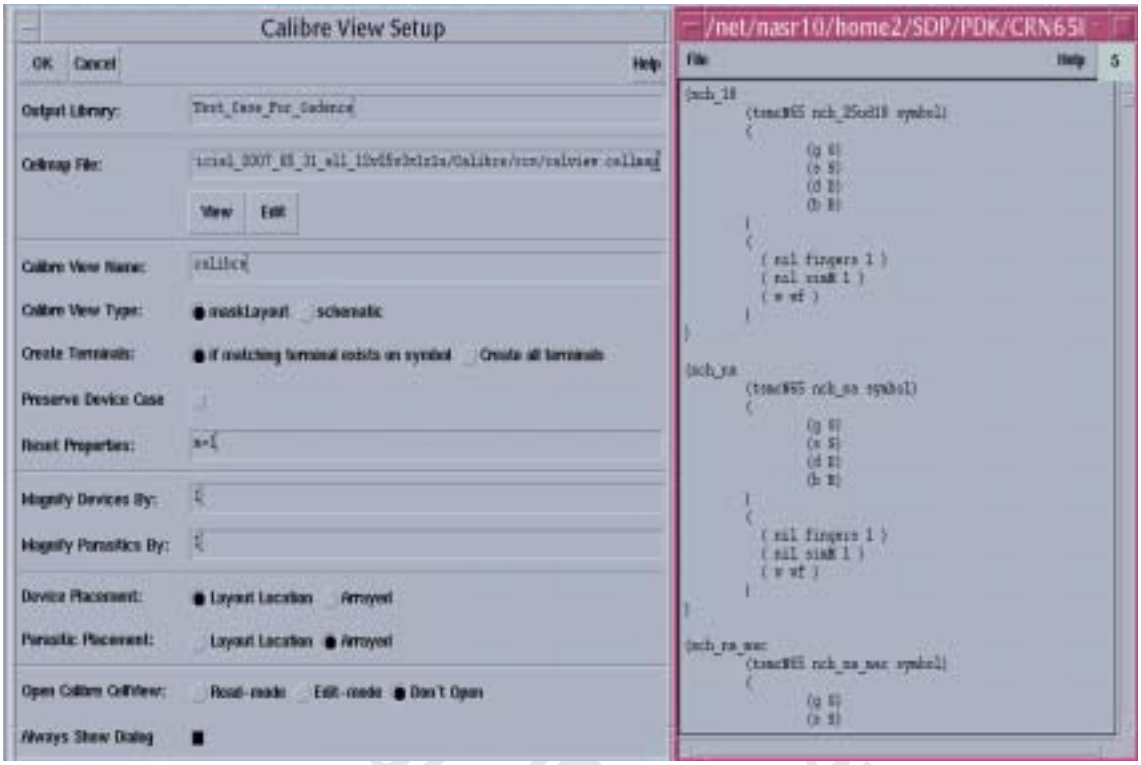
Setp5. Run PEX

After PEX Run

a.) Remember to check correctness of Cell map File

b.) Fill in view name and click OK of the Caliber View

PEX result should look like



B.) Assura Extraction Flow

1. Assura Demo Environment

1.1 PDK version

PDK version：

CRN65LP_PDK_1.1a_official_2007_05_31_all_12v25v3x1z1u

Please copy below directory to local directory

CRN65LP_PDK_1.1a_official_2007_05_31_all_12v25v3x1z1u/Assura

1.2 Extraction rule file

Please download rule deck with specific metal scheme from EDW system

(Need to request from PDK team)

For this case, rule deck file : RC_Assura_crn65lp_1p06m+alrdl_typical.tar

The setup is as follows :

<i> Untar and place them into “/local directory/…/…/Assura/lvs_rcx”

<ii>Note: To avoid double count

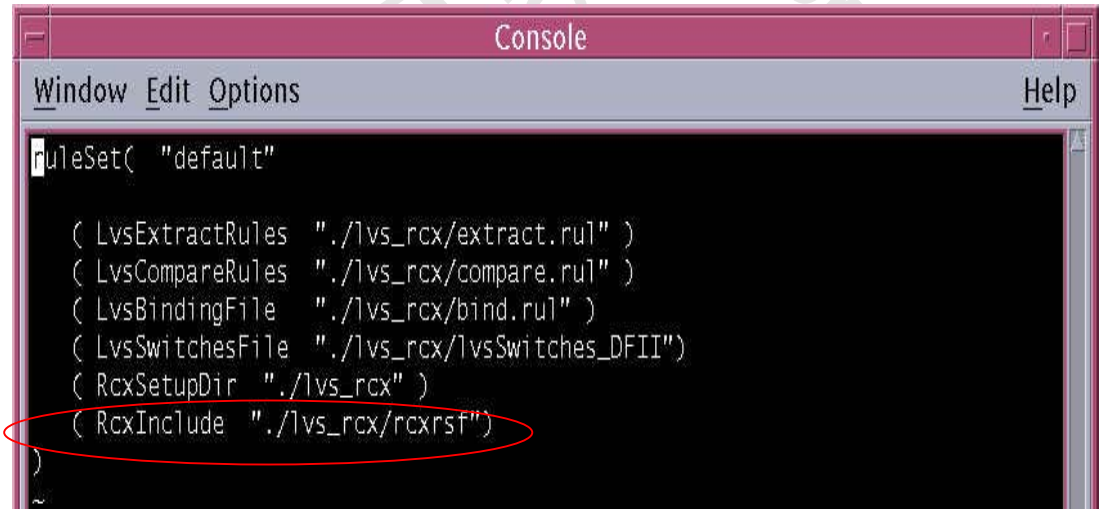
Add new option into

a.) “/local directory/…/…/Assura/techRuleSets”

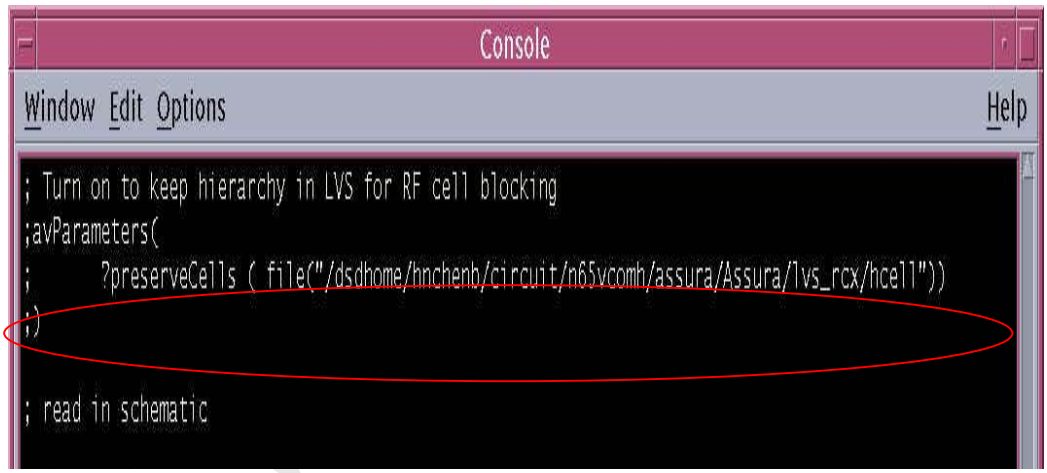
b.) “/local directory/…/… /Assura/lvs_rcx/compare.rul “

c.) “/local directory/…/… /Assura/lvs_rcx/rcxrsf “

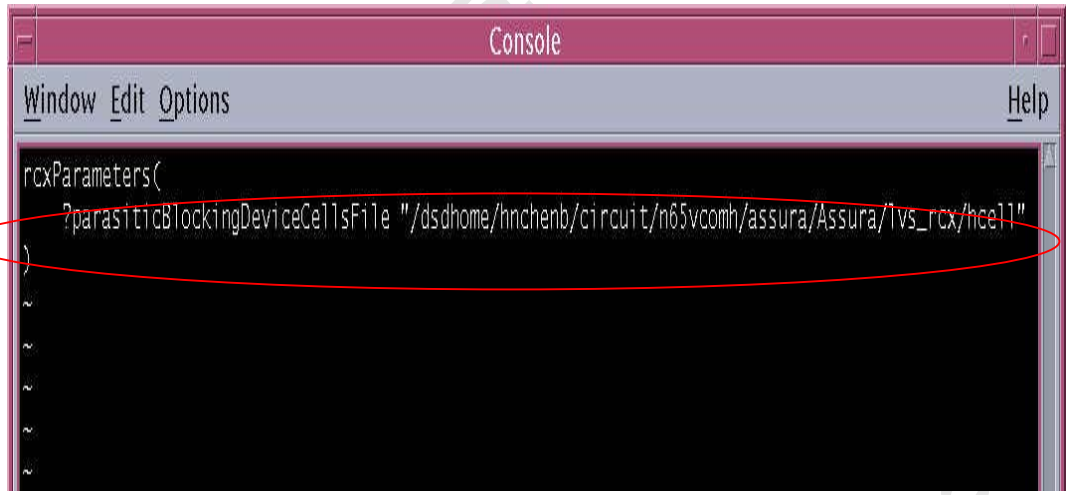
a.) Add RcxInclude into techRuleSets



b.) Add hcell path into compare.rul



c.) Add hcell path into rcxrsf

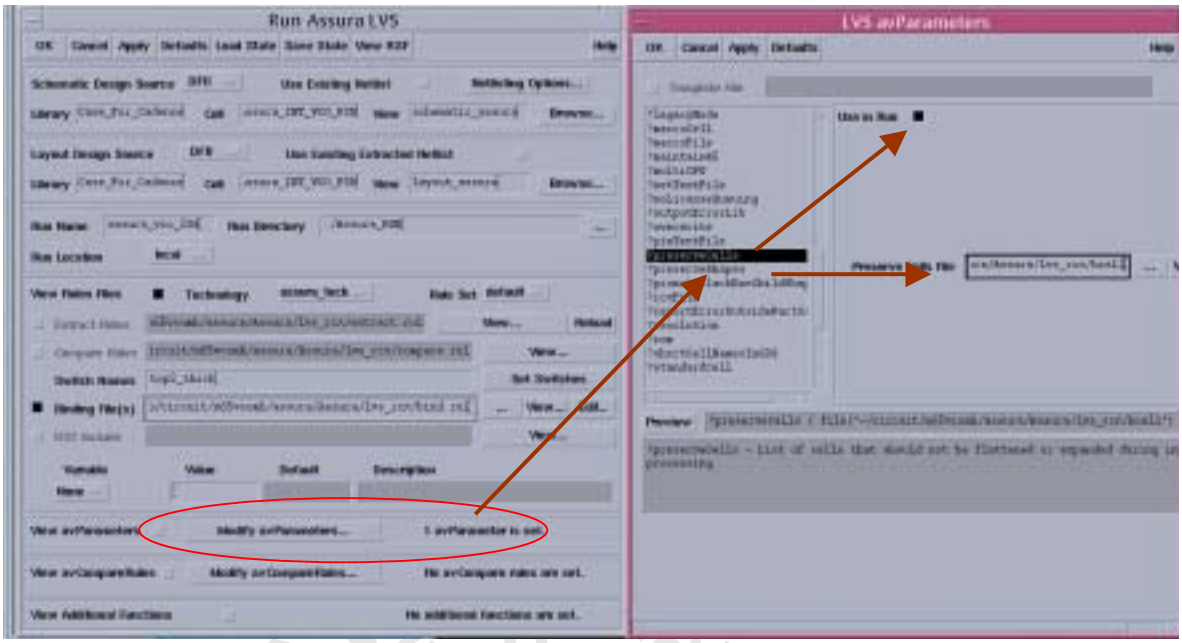


2. Setup Assura RCX step-by-step

2.1 Enable PreserveCells

a.) Choose Modify avParametersSelect

b.) Select ?preserveCells and choose hcell path



2.2 Run LVS and check LVS clean

LVS： from layout view， pull down **Assura** menu and press **Run LVS**；

LVS result should look like

2.3 Run Assura RCX

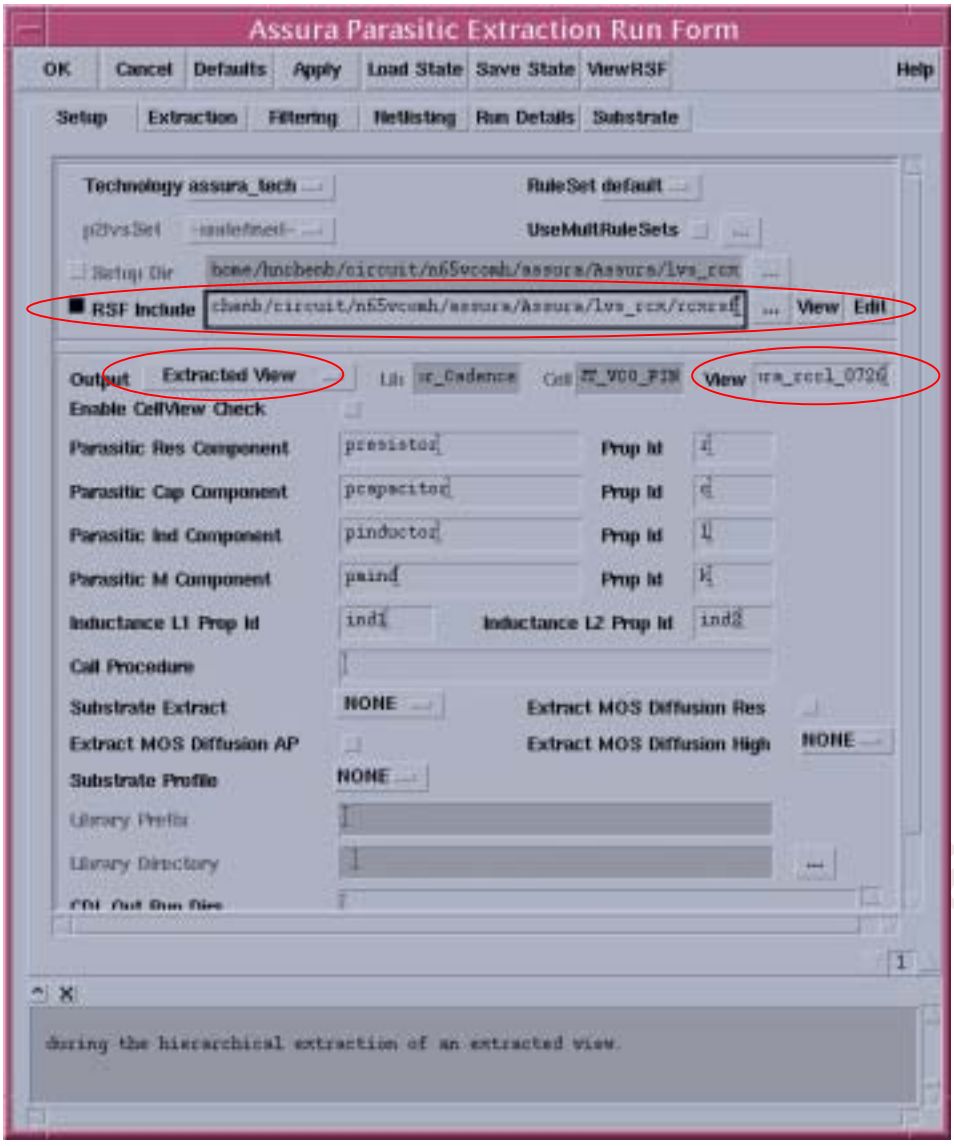
RCX： from layout view， pull down **Assura** menu and press **Run RCX**；

Setp1. Setup

a.) RSF file should be enabling

b.) Please choose Extracted View output format

c.) Fill in Extracted View name



Setp2. Extraction

a.) Choose Extraction Mode: RC ; RLC ; RLCK ; R Only ; C Only

b.) Set Max fracture length

c.) Select cap Extraction Mode **"coupled"** for C extraction accuracy guarantee

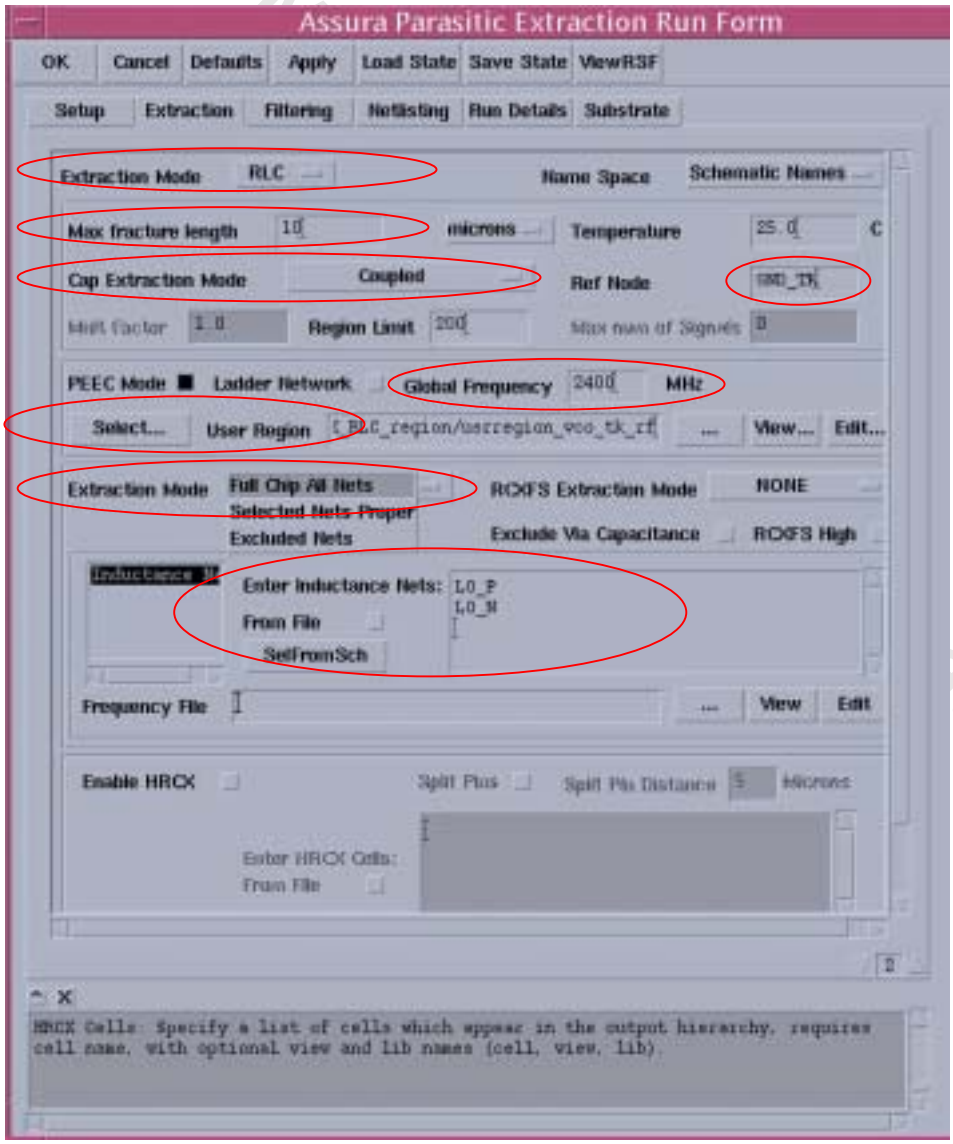
d.) Select extracted region (will be described in the following)

e.) Choose Extraction Mode: Full chips All Nets ; Selected Nets ; Excluded Nets

f.) Select the net that required inductance extraction from schematic

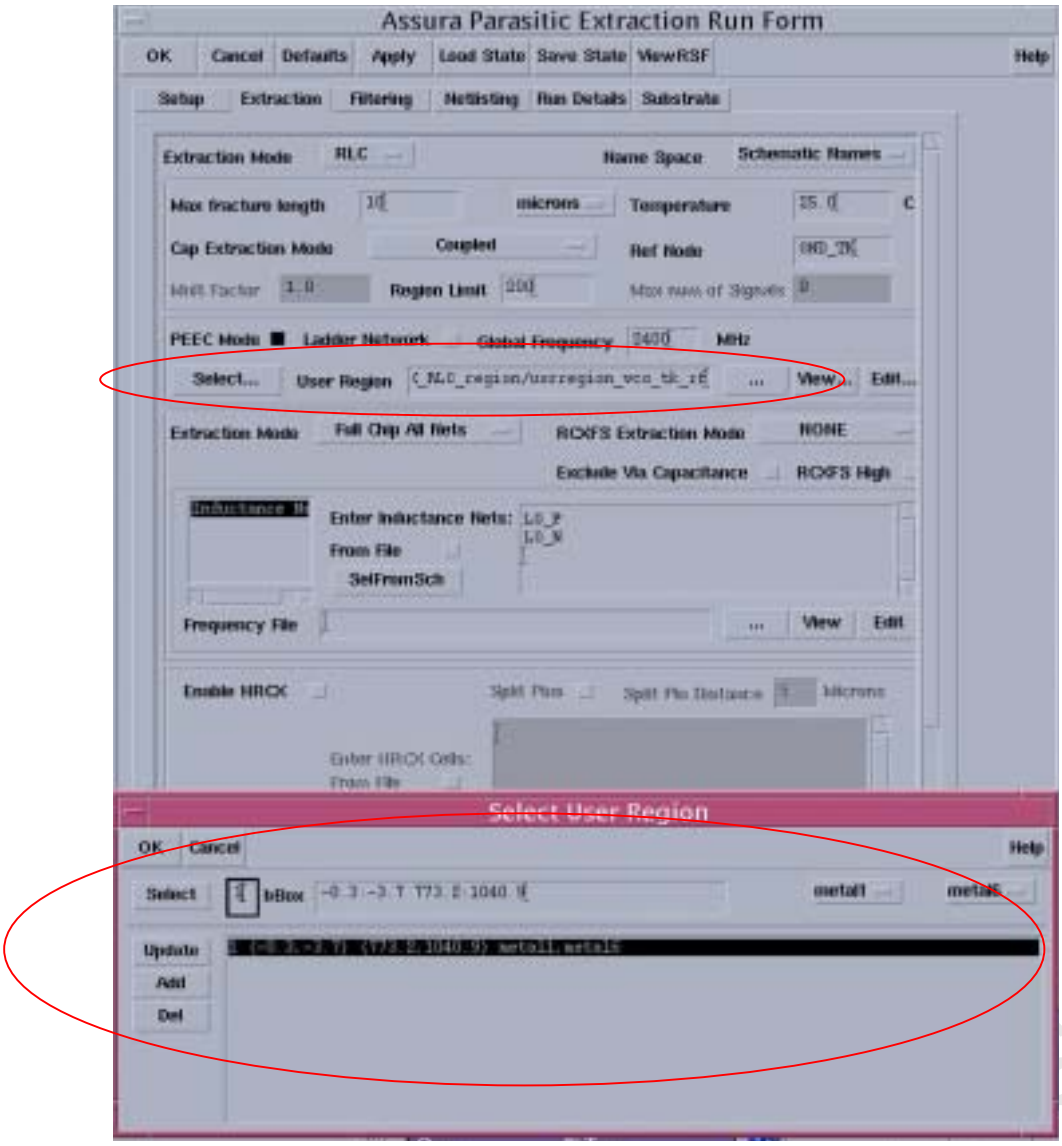
g.) Fill in Ref node name (It's usually "gnd!")

h.) Fill in Global Frequency



d.) Select extracted region

Edit the layout region and the layers used in the layout

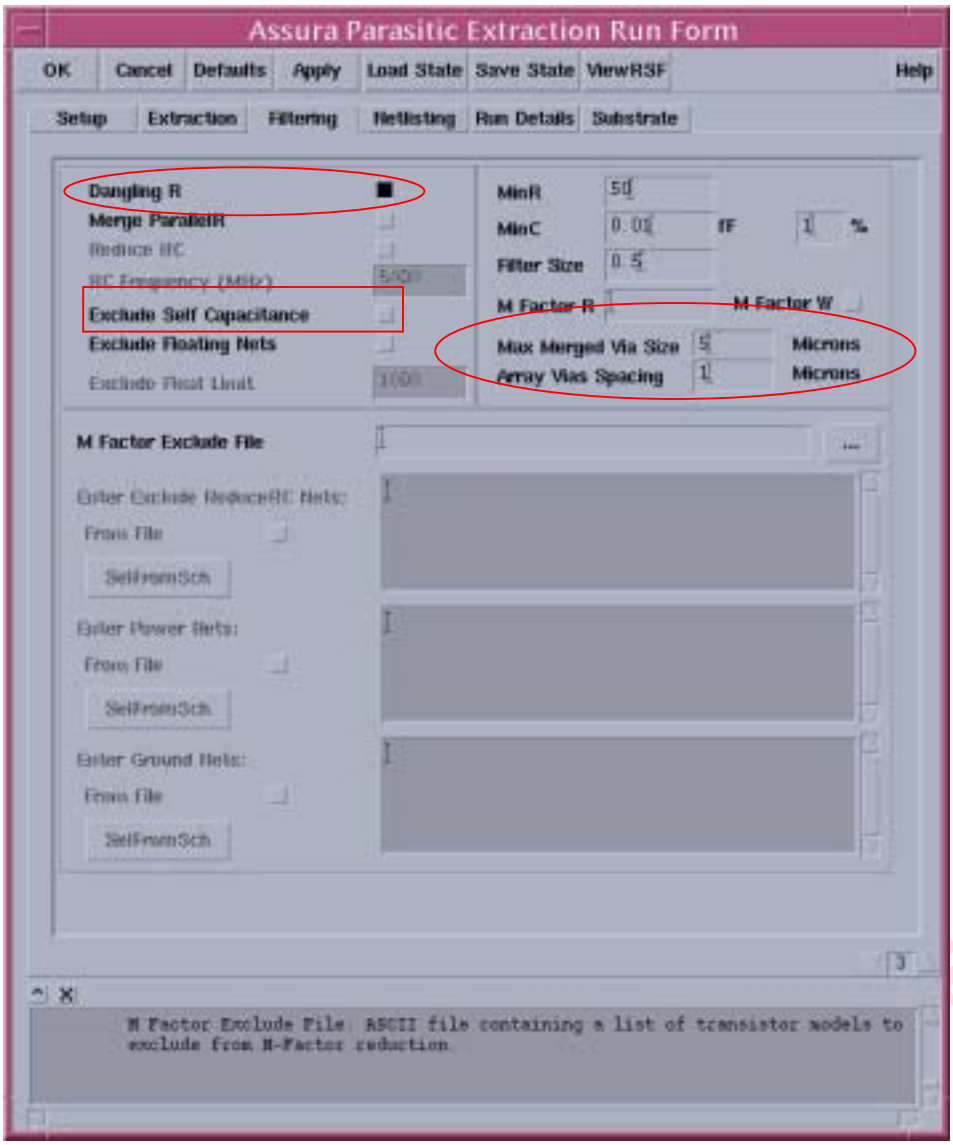


Setp3. Filtering

a.) **Disable** Exclude Self Capacitance for accuracy guarantee

b.) **Enable** Dangling R

c.) Set Via parasitic resistor merging policy



Setp5. Run RCX

RCX result should look like

6. Simulation vs. Silicon Measurement

This is post-simulation with measurement results, and samples were from TMT501 and TMT504. From these results, it had same of frequency results between shuttle measurements. To compare pre-simulation and silicon measurement results, there has just below 5% difference.

1. Calibre RCCL mode and RCC mode

1.1 Frequency tuning range

This is pre-simulation, post-simulation and silicon measurement result.

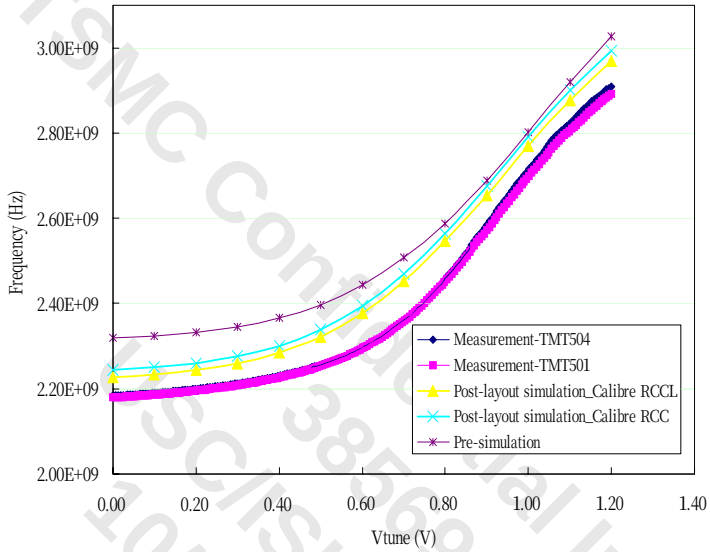


Fig 11 Pre-sim, post-sim vs. measurement

1.2 Phase Noise

This is phase noise pre-simulation and silicon measurement data. Please see the fig 13 and summary table. They have close of noise results between pre-simulation and measurement.

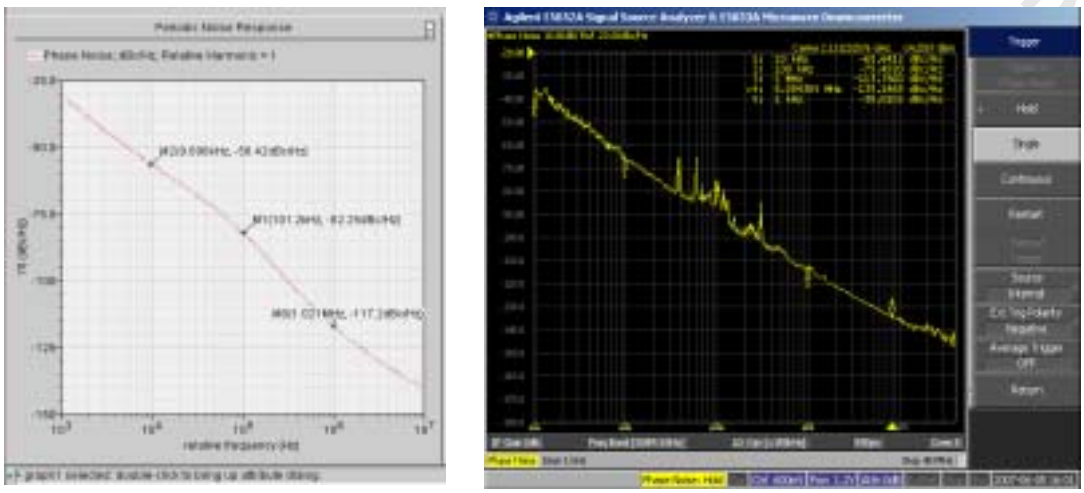
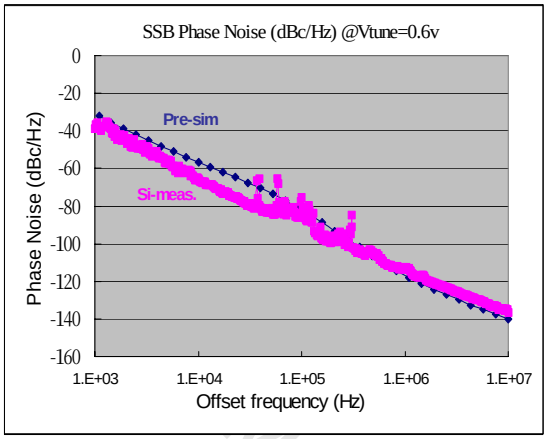
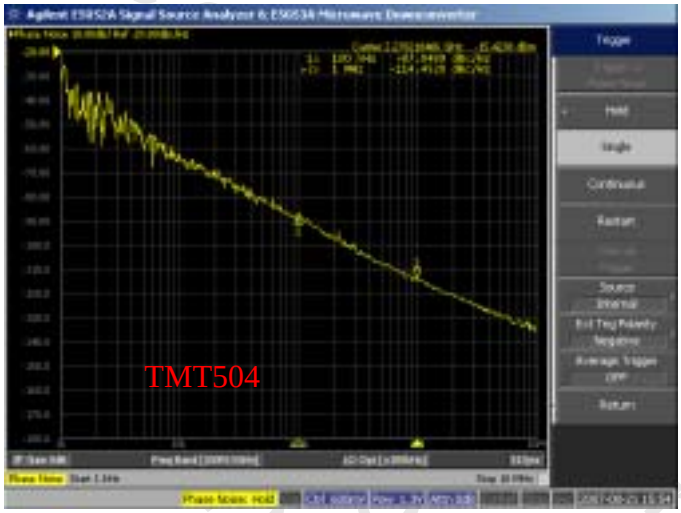


Fig 12 phase noise



Offset Freq.	Pre-sim (dBc/Hz)	Si Meas. TMT501 (dBc/Hz)	Si Meas. TMT504 (dBc/Hz)
1K	-30	-39	-32
10K	-56.4	-65.6	-65
100K	-82.2	-75.5	-87.05
1M	-117	-113.35	-114.45
10M	-140	-137	-135

Fig 13 Phase noise summary tables



1.3 Output Power

Output power post-sim and silicon measurement results.

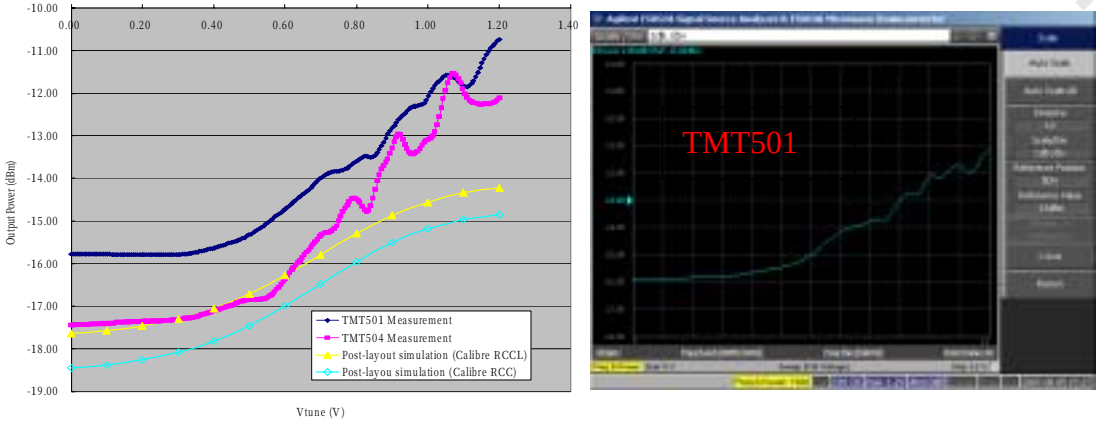


Fig 14 Output Power

2. Assura RCCL mode and RCC mode

TBD

7. GDS Layout

For easy measurement on probe station and COB (Chip on Board), this layout plan is put DC pad on the top area, and SGS pad on the bottom.

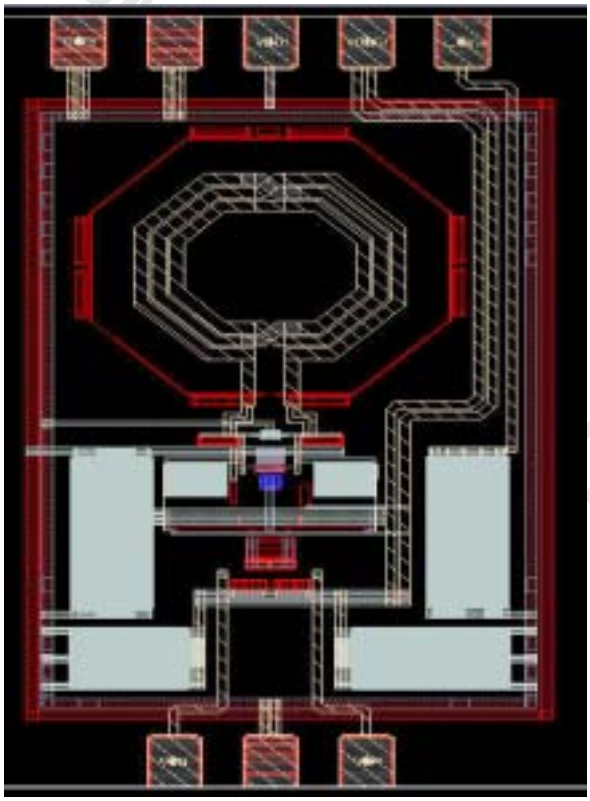


Fig 15 VCO Layout

8. Test Bench

1. PCB Board

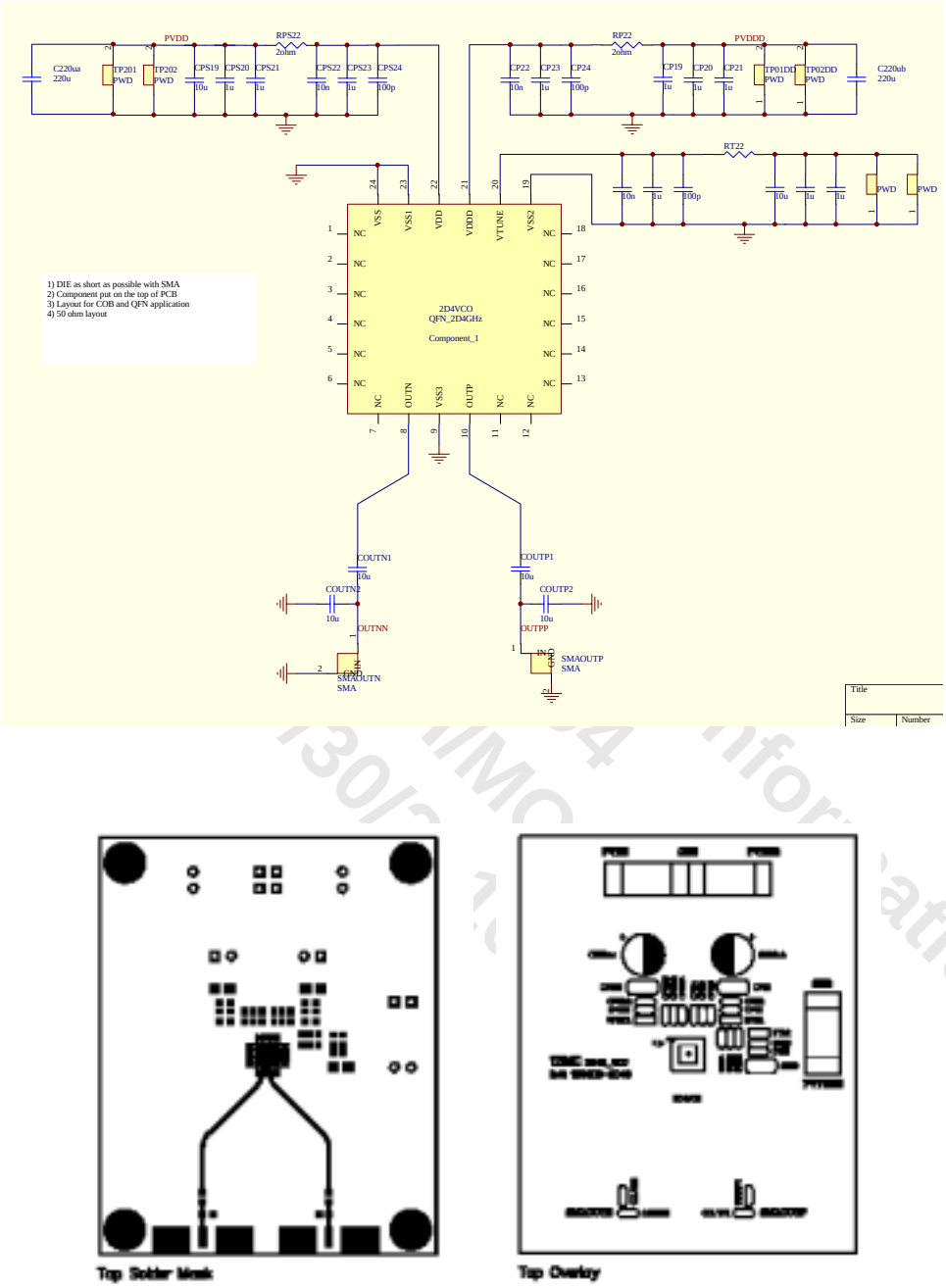


Fig 16 PCB schematic and layout

2. Test Equipment

Agilent E5052A

9. Summary

For this preliminary version of design flow and report, RFDP have implement circuit design from pre-simulation, post-simulation procedure and compare to silicon chip measurement results. It look well of this results.