ERC Usage

PDKD/TSMC

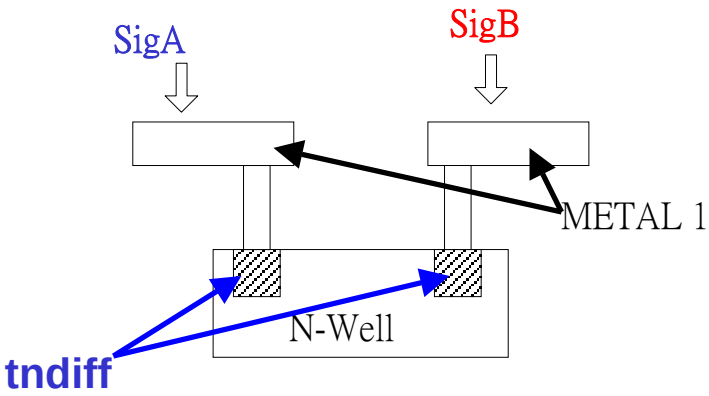
Version1.3 Oct. 2008

What is ERC (Electrical Rule Checking)

- ERC is a special option for designers. Some errors can be waived, but others may be fatal errors. So, designers **MUST** review every error or warning for LVS/ERC report.
- Some ERC rules are included in TSMC official LVS command files.
  - **Soft connect checking (mainly for nwell or psub)**
  - **Path checking**
  - **Ptap / ntap checking**
  - **MOS s/d power&ground checking**
  - **Gate directly connecting to power or ground.**
  - **Floating gate**
  - **Floating well**

Soft-connection and Soft-check

- **N-well and P-well are high resistor materials**



1. Treat as Short
Sig A connect to Sig B
--> If Sig A is a power line and Sig B connect to a IP power.
--> The IP get a high resistor power, it means IR drop is very serious.
----> **ERROR**

2. Treat as open
Sig A does not connect to Sig B
--> If Sig A is a power signal and sig B is ground signal
--> power and ground short
--->**ERROR**

➢ **There are two methods to solve this problem**

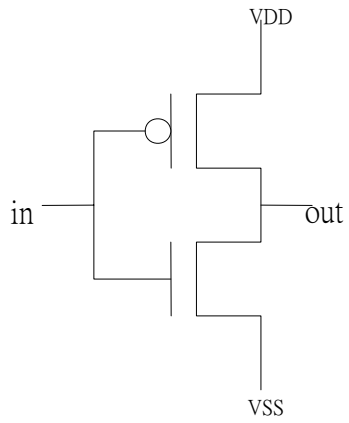
- Run two LVS command file, one is " treat as short", the other is "treat as open".
- Use soft connect commands and do soft check!!!

What is Soft-connection and Soft-checking

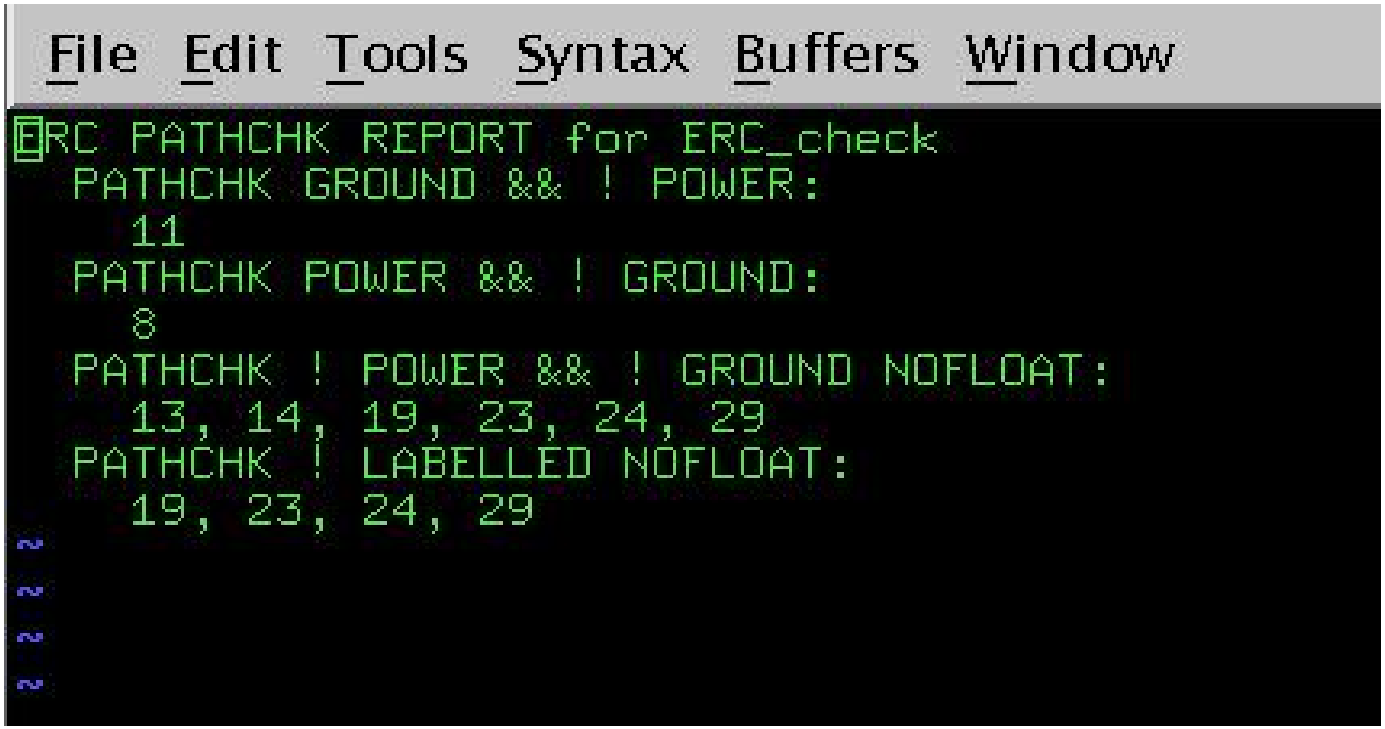
- **Soft-connection definition:**
  - Passes established connectivity from the upper layer polygons onto the specified lower layer polygons (one-directional)
    < adopt by Calibre tool manual >
- **Soft-check:**
  - Help designers to search which contact connects to WELL
- **ERC results:**
  - TSMC LVS/ERC command files contain those options and those errors/warnings are reported in **<lvs.rep>** or **<lvs.rep.ext>**
  - Please confirm every error or warning of those three file <**~.rep>/<~.rep.ext>/ <svdb/~.rep>**
  - Give user a warning on the **<lvs.rep.ext>** file. User can debug this error by **"calibre -rve"** and open the **<svdb/~.softchk>** file .

Device Path Check

- **Purpose**
  - Help designers to check if the circuit misses something.
- **Four kinds of path checking**
  - Nodes with a path to power but not ground
  - Nodes with a path to ground but not power
  - Nodes without a path to both path and ground
  - Nodes without a path to pin



Pathchk Report (svdb/~.Rep)

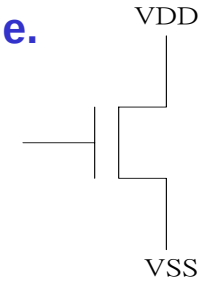


ERC Steps and Reports

- **Get ERC report in LVS stage.**
- **Calibre :**
  - % calibre –lvs **–spi layout.net** calibre_rule_deck
  - For Calibre, please check the "**calibre_erc.db**" and "**calibre_erc.sum**" files.
  - And please find whether it has soft_check warnings in "**<lvs.rep>.ext**" report.
- **Hercules :**
  - % hercules hercules_rule_deck
  - For Hercules, please check the "**<Top>.LAYOUT_ERRORS**" file.
- **Assura :**
  - %> assura LVS.rsf | tee lvs.log
  - For Assura, please check the "**<Top>.err**" file.

PTAP/NTAP/Special MOS Connectivity Check

- **PTAP connects to power or NTAP connects to ground.**
  - Check ERC errors of "**PPVDD49**" for PTAP.
  - Check ERC errors of "**NPVSS49**" for NTAP.
- **For N /P MOS, one of source/drain connects to POWER and the other connects to ground.**
  - Check ERC errors "**mppg**" for PMOS.
  - Check ERC errors "**mnpg**" for NMOS.
  - We can check MOS types included : **CORE/IO/HVD**(above 45/65nm), not included SRAM/VARACTOR/RF devices.
- **For Calibre, please check the "calibre_erc.db" and "calibre_erc.sum" files.**
- **For Hercules, please check the "<Top>.LAYOUT_ERRORS" file.**
- **For Assura, please check the "<Top>.err" file.**



Gate Directly Connect to Power/Ground

- **PMOS gates directly connects to POWER w/o the 2.5v and 3.3v IO devices.**
  - For ESD protection, if core or 1.8v PMOS gates directly connects to POWER node, gates will be damaged.
  - Check ERC errors **“ppvdd150”** for PMOS gates.
- **NMOS gates directly connects to GROUND w/o the 2.5v and 3.3v IO devices.**
  - For ESD protection, if core or 1.8v NMOS gates directly connects to GROUND node, gates will be damaged.
  - Check ERC errors **“npvss150”** for NMOS gates.
- **For Calibre, please check the “calibre_erc.db” and “calibre_erc.sum” files.**
- **For Hercules, please check the “<Top>.LAYOUT_ERRORS” file.**
- **For Assura, please check the “<Top>.err” file.**

Floating Gate

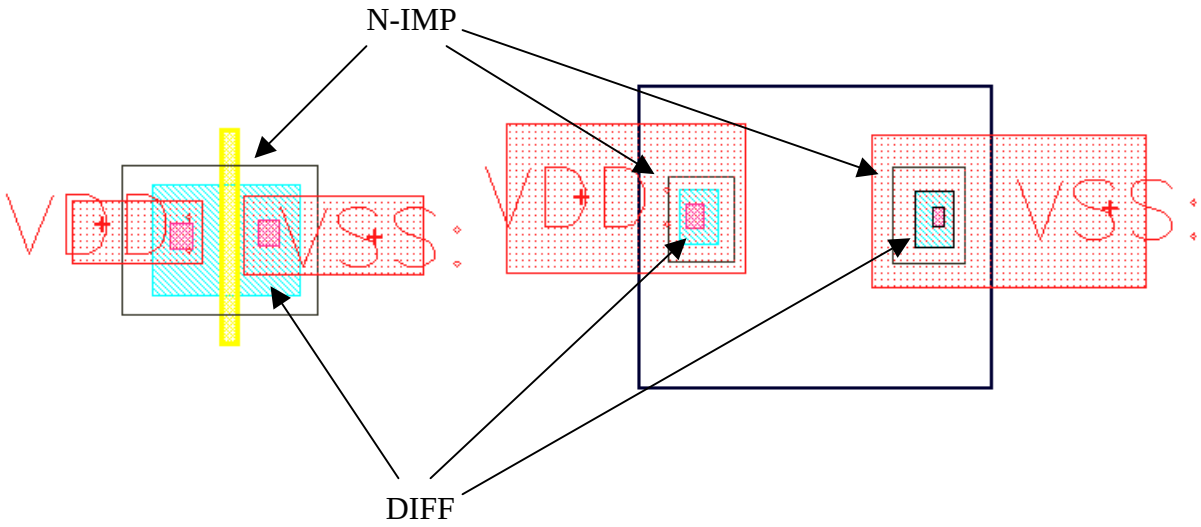
- Before version 1.3b, we will check floating gate in ERC check section, but DRM already covered this check rule, after version 1.4a we will not support this rule checking any more.
- Please refer rule “PO.R.8” in N65 DRM document T-N65-LO-DR-001 for floating gate types.

Floating Well

- **There is no POWER or GROUND node information connecting to NWELL or P-SUBSTRATE.**
  - Check ERC errors "**floating.nxwell**" for NWELL.
  - Check ERC errors "**floating.psub**" for PSUB.

- **For Calibre, please check the "calibre_erc.db" and "calibre_erc.sum" files.**
- **For Hercules, please check the "<Top>.LAYOUT_ERRORS" file.**
- **For Assura, please check the "<Top>.err" file.**

Layout Example



~.sum

```
---------------------------------------------------------------------------
--- RULECHECK RESULTS STATISTICS
---
RULECHECK mppg .... TOTAL Result Count = 1
RULECHECK mnpg .... TOTAL Result Count = 0
RULECHECK ppvdd49 ... TOTAL Result Count = 0
RULECHECK npvss49 ... TOTAL Result Count = 1
---------------------------------------------------------------------------
```

~.ext

WARNING: Stamping conflict in SCONNECT - Multiple source nets stamp one target net.
Use LVS REPORT OPTION S or LVS SOFTCHK statement to obtain detailed information.

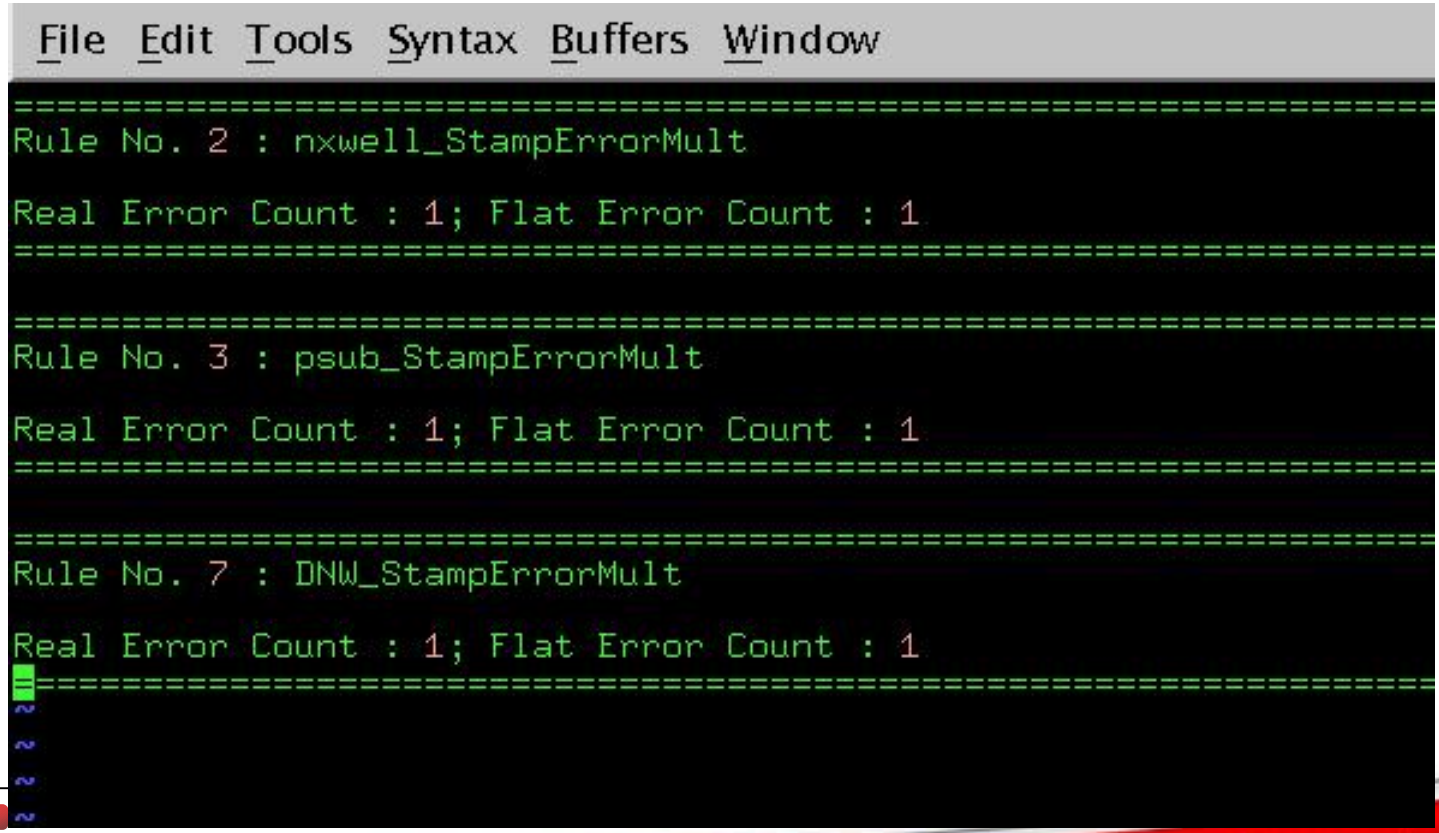
Hercules ERC Check Error File

- Please check the Top.LAYOUT_ERRORS file.

```
File  Edit  Tools  Syntax  Buffers  Window
Structure name:  ERC_check

                        ERROR SUMMARY

No Comment
 ERR_TEXT_SHORT_DISCARD ..................................... 2 violations found.

No Comment
 C_THRU nplug INSIDE nxwell { } (1;0) ....................... 2 violations found.

No Comment
 C_THRU pplug INSIDE psub_term { } (1;1) .................... 2 violations found.

No Comment
 C_THRU pplug INSIDE psub { } (1;2) ......................... 2 violations found.

No Comment
 C_THRU n_pplug INSIDE n_psub { } (1;4) ..................... 2 violations found.

No Comment
 C_THRU dnwc INSIDE DNW { } (1;6) ........................... 2 violations found.

No Comment
 ERR_TEXT_SHORT_DISCARD ..................................... 2 violations found.

No Comment
 ERR_TEXT_SHORT_DISCARD ..................................... 2 violations found.

No Comment
 NET_PATH_CHECK { } PERM=path1_Out(1;13) .................... 13 violations found.

No Comment
 NET_PATH_CHECK { } PERM=path3_Out(1;15) .................... 16 violations found.

No Comment
 NET_PATH_CHECK { } PERM=path4_Out(1;16) .................... 16 violations found.
```

Assura ERC Check Error File

- Please check the Top.err file.
- Currently the Assura can not support the net-path check function.



Summary for ERC checker

- Please confirm every error or warning of these three files --- “~.rep” “~.rep.ext” “svdb/~.rep” for Calibre.
- Please confirm the <Top>.LAYOUT_ERRORS file for Hercules.
- Please confirm the <Top>.err file for Assura.
- Every soft connect error must be fixed.
- Other ERC errors/warnings need to be reviewed by circuit designers.