Reference Manual

For

Generic (cds_ff_mpt)
0.8V/1.8V
Finfet/Multi Patterned
8 Metal

Process Design Kit (PDK)

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Overview

The purpose of this Reference Manual is to describe the technical details of the Advanced Node Generic Process Design Kit (“cds_ff_mpt”) provided by Cadence Design Systems, Inc. (“Cadence”) for use on Cadence Product Releases ICADV123, SPECTRE171, and PVS161.

Software Environment

The CDS_FF_MPT has been designed for use within a Cadence software environment that consists of the following tools –

- Schematic (L, XL)
- Analog Design Environment (L, XL, GXL)
- Spectre Circuit Simulator
- Layout (L, XL, GXL)
- PVS (DRC, LVS)

This PDK requires the following UNIX environmental variables:

"CDS_Netlisting_Mode" to be set to "Analog"

"CDSHOME" to be set to the Cadence DFII installation path

Documents

Documents Used		Rev Date
Design Rule Document	CDS_FF_MPT_DRM.pdf	04/02/2018

What makes up a PDK?

PDK stands for Process Design Kit. A PDK contains the process technology and needed information to do device-level design in the Cadence DFII environment.

Installation of the PDK

The user who will own and maintain the PDK should logon to the computer.

Choose a disk and directory under which the PDK will be installed. This disk should be exported to all client machines and must be mounted consistently across all client machines.

Connect to the directory where the PDK will be installed:

cd <**pdk_install_directory**>

Extract the PDK from the archive using the following commands:

zcat <path_to_pdk_tar_file>/cds_ff_mpt_<version>.tar.gz | tar xf -

The default permissions on the PDK have already been set to allow only the owner to have write, read and execute access. Other users will have only read and execute access.

PDK Install Directory Structure/Contents

Within the <**pdk_install_directory>** directory there are several directories to organize the information associated with the PDK.

cds_ff_mpt - Directory the PDK library

docs - Directory containing the Cadence PDK documentation and the Process

design rule manual

models - Directory containing the device spectre models

pvs – Directory containing the Physical Verification DRC and LVS rule decks

cds.lib - File containing the Cadence library definition file

display.drf – File containing the Cadence Virtuoso display definitions

pvtech.lib – File containing the PVS initialization path

Creation of a Design Project

A unique directory should be created for each circuit design project. The following command can be executed in UNIX:

mkdir ~/circuit_design

cd ~/circuit_design

All work by the user should be performed in this circuit design directory. The following file should be copied from the PDK install directory to begin the circuit design process. The following command can be used:

cp <**pdk_install_directory**>/display.drf .

Next the user should create a "cds.lib" file. Using any text editor the following entry should be put in the cds.lib file:

INCLUDE <**pdk_install_directory**>/cds.lib

Where "**pdk_install_directory**" is the path to where the CDS_FF_MPT PDK was installed.

The following UNIX links are optional but may aid the user in entering certain forms with the Cadence environment. In UNIX the following command can be used:

ln -s <**pdk_install_directory**>/models

Where, again, "**pdk_install_directory**" is the path to where the CDS_FF_MPT PDK was installed.

Technology File Methodology

The CDS_FF_MPT Library techfile will be designated as the **master** techfile. This techfile will contain all required techfile information. An ASCII version of this techfile is shipped with the PDK. This ASCII version represents the techfile currently compiled into the cds_ff_mpt library

The **attach** method should be used for any design library that is created. This allows the design database techfile to be kept in sync with the techfile in the process PDK. To create a new library that uses an attached techfile, use the command *File->New->Library* from either the CIW or library manager and select the *Attach to an existing techfile* option. Select the cds_ff_mpt library when asked for the name of the *Attach To Technology Library*.

Note: This PDK is using 2000uu/dbu for all layout views.

Customizing Layer Display Properties

The display.drf file is automatically loaded by the libInit.il file whenever the cds_ff_mpt library is opened.

To auto-loaded your own display.drf file at Cadence start-up time put the display.drf file in the Cadence start-up directory. To manually load the display.drf file (or load a new version), choose *Tools->Display Resources->Merge Files...* from the CIW and enter the location of the display.drf file that you want to use. If the display.drf file is not auto-loaded and you do not manually load it, you will get error messages about missing packets when you try to open a schematic or layout view and you will not be able to see any process specific layers.

A display.drf file for the CDS_FF_MPT can be found in the PDK install directory under techFiles directory.

Listed below are the packet, color, lineStyle, and stipplePattern definitions for a metal3 drawing layer. The packet info references predefined color, lineStyle, and stipplePattern definitions. Any of these can be changed to suit an individual user's preferences in the project copy of the display.drf file.

```
drDefinePacket(
;( DisplayName  PacketName          Stipple        LineStyle              Fill      Outline
)
  ( display      m3                  dots           solid          green   green )
)
```

```
drDefineColor(
;( DisplayName  ColorName           Red          Green        Blue     Blink )
  ( display     green       0           204          102      nil )
)

drDefineLineStyle(
;( DisplayName  LineStyle           Size         Pattern )
  ( display     solid       1           (1 1 1) )
)

drDefineStipple(
;( DisplayName  StippleName         Bitmap )
  ( display     dots                (
                            (0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0)
                            (0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0)
                            (0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1)
                            (0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0)
                            (0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0)
                            (0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0)
                            (0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1)
                            (0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0)
                            (0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0)
                            (0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0)
                            (0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1)
                            (0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0)
                            (0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0)
                            (0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0)
                            (0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1)
                            (0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0)
)
```

Schematic Design

The user should follow the guidelines listed below while building schematics using Composer:

Project libraries should list the primitive PDK library as a reference library in the library properties form.

Users can add instances from the PDK library to designs stored in the project libraries.

When performing hierarchical copy of schematic designs, care should be taken to preserve the references to the PDK libraries. These references should not be copied locally to the project directories and the references set to the local copy of PDK cells. This would prevent your designs from inheriting any fixes done to the PDK library from an upgrade.

Users should exercise caution when querying an instance and changing the name of the cell and replacing it with a reference to another cell. While similar parameters will inherit values, callbacks are not necessarily executed. This would cause dependent parameters to have incorrect values.

Schematics should be designed with schematic driven layout methodology in mind. Partitioning of schematics, hierarchical design, input and output ports, should be done in a clean and consistent fashion.

Library Device Setup

Resistors

The resistors in the library consist of three types; *diffused*, *insulated,* and *metal*. The diffused types include p+ and n+. The insulated resistors are those that are isolated from silicon by an insulator (oxide) such as poly resistors. The metal resistors are those resistors that are used as interconnect and feed-through. All resistor models are two-terminal device models. Serpentine resistor layouts are not allowed.

Units:

The length and width are specified in meters for the metal resistors. The number of fins and poly pitch are used to specify the poly and diffusion resistors.

Calculation:

The user has two choices in determining how the final resistor configuration is calculated. The user may request the calculation of either the resistor length or the resistor value. In both cases, the calculated values are determined based upon a combination of the length/fins, width,

resistance value, number of resistor segments (series or parallel), and contact resistance. The width,length, fins are snapped to grid, and the resistances are recalculated and updated on the component form based on actual dimensions.

Simulation:

Subcircuit definitions are used to model the resistors

Mosfets

All mosfets in the PDK library are 4 terminals, with the body terminal explicitly connected.

Units:
Number of fins is an integer number(In 48nm steps). The length is bounded by the Poly Pitch. The number of fingers is and integer.

Poly86 18nm

Poly90 18nm, 20nm

Poly84 18nm, 20nm, 24nm

Poly102 18nm, 20nm, 24nm, 28nm

Poly104 18nm, 20nm, 24nm, 28nm, 30nm

Simulation:

These mosfets are netlisted as their predefined device names for simulation purposes.

Bipolar Transistors

The bipolar npn in the PDK library are 3 terminal.

Units:
Only fixed size devices are allowed. A cyclic is used to enter the desired size.

Calculation:

The Emitter Width and Emitter Length are calculated from the emitter size cyclic.

Simulation:

These BJT is netlisted as it's predefined device names for simulation purposes.

Diodes

All diodes in the PDK library are two-terminal.

Units:
Number of fins is an integer number(In 48nm steps). The length is bounded by the Poly Pitch. The number of fingers is and integer.

Calculation:

The width, length, and area are calculated from the fins and poly pitch entered.

Simulation:

These diodes are netlisted as their predefined device names for simulation purposes.

Capacitor

The metal capacitor in the PDK library are two-terminal.

Units:
The Length and width are enter in microns.

Calculation:

The user has three choices in determining how the final capacitor configuration is calculated. The user may request the calculation of either the capacitor length, the capacitor width, or the capacitor value. In all cases, the calculated values are determined based upon a combination of the length, width, capacitance value, The width and length are snapped to grid, and the capacitance is recalculated and updated on the component form based on actual dimensions.

Simulation:

The capacitor is netlisted as it's predefined device name for simulation purposes.

Supported Devices

Mosfets

- n1svt – 0.8 volt standard Vt NMOS transistor
- n1hvt – 0.8 volt high Vt NMOS transistor
- n1lvt – 0.8 volt low Vt NMOS transistor
- n2svt – 1.8 volt standard Vt NMOS transistor
- p1svt – 0.8 volt standard Vt PMOS transistor
- p1hvt – 0.8 volt high Vt PMOS transistor
- p1lvt – 0.8 volt low Vt PMOS transistor

- p2svt – 1.8 volt standard Vt PMOS transistor

Resistors

- rnsnd - N+ diffused resistor w/o salicide
- rnspd - P+ diffused resistor w/o salicide
- rsnd - N+ diffused resistor w/i salicide
- rspd - P+ diffused resistor w/i salicide
- rnws - N-Well resistor under STI
- rnwo - N-Well resistor under OD
- rsnp - N+ Poly resistor w/salicide
- rspp - P+ Poly resistor w/salicide
- rnsnp - N+ Poly resistor w/o salicide
- rnspp - P+ Poly resistor w/o salicide
- resm<k> - Metal <k> resistor (k=1-7,t)

Capacitor

- cmim – CMT-M7 metal cap

Bipolars

- npn - Bipolar NPN with variable 1x1 or 2x2 emitter size

Diodes

- nd1svt – 0.8 volt standard Vt N+/psubstrate diode
- nd1hvt – 0.8 volt high Vt N+/ psubstrate diode
- nd1lvt – 0.8 volt low Vt N+/ psubstrate diode
- nd2svt – 1.8 volt standard Vt N+/ psubstrate diode
- pd1svt – 0.8 volt standard Vt P+/nwell diode
- pd1hvt – 0.8 volt high Vt P+/nwell diode
- pd1lvt – 0.8 volt low Vt P+/nwell diode
- pd2svt – 1.8 volt standard Vt P+/nwell diode

Views provided

The following table explains the use of the cellviews provided as part of this PDK:

symbol	Used in Composer schematics
spectre	Simulation / netlisting view for the Spectre & UltraSim simulator
schematic	Simulation / netlisting view for all simulators; Resistors use schematic to call other simulator resistor views. It is used to implement series and parallel features in those resistors.
auLvs	Netlisting view for DIVA and Assura
auCdl	Circuit Descriptive Language netlisting view typically used to generate a netlist for Dracula or third party simulators.
ivpcell	Device recognition symbol used in the extracted layout for netlisting purposes with DIVA and Assura
layout	Fixed cell or pcell used in Virtuoso Layout Editor.

Mosfets

- Four terminals (D, G, S, B)
- symbol, spectre, auLvs, auCdl, ivpcell, layout (Pcells)

Resistors

- Two terminals (PLUS, MINUS) for diffused, poly, and metal resistors
- symbol, schematic, auLvs, auCdl, ivpcell, layout (Pcells)
- Resistors called in schematic views include views for all simulators, symbol, spectre

Capacitor

- Two terminals (PLUS, MINUS)
- symbol, spectre, auLvs, auCdl, ivpcell, layout (Pcells)Diodes
- Two terminals (PLUS, MINUS)
- symbol, spectre, auLvs, auCdl, ivpcell, layout (Pcells)

Bipolars

- Three terminals (C, B, E)

- symbol, spectre, auLvs, auCdl, ivpcell, layout(Pcells)

CDF parameters

Mosfets

Model Name - spectre model name (non-editable)

Fin Pitch (M) – Fin spacing pitch (non-editable)

Number of Fins per Finger - width of each poly finger in integer fin pitches

Poly Pitch – Allowed poly gate pitches

Length (M) - gate length in meters

Number of Fingers - number of poly gate fingers used in layout

Multiplier - number of parallel MOS devices

Show Layout Parameters – Show layout cdf parameters in form

Mos Poly Finger Width (M) - gate width (non-editable)

Left Edge Poly – Turn left edge poly on/off

Right Edge Poly – Turn right edge poly on/off

Number of Left Dummy Poly – Number of left dummy polys

Number of Right Dummy Poly – Number of right dummy polys

Remove M1/V0 – Turn M1/V0 layers on/off

Show Sim Parameters - Show Simulation cdf parameters in form

Edit Area & Perim – Turn following simulation params to editable

Source to Substrate Overlap Area - Source to substrate overlap area through oxide(all fingers) (m2)

Drain to Substrate Overlap Area - Drain to substrate overlap area through oxide(all fingers) (m2)

Source to Substrate Overlap Perimeter - Perimeter of source to substrate overlap region through oxide (m)

Drain to Substrate Overlap Perimeter - Perimeter of drain to substrate overlap region through oxide (m)

Source Junction Area - Source junction area (all Fingers) (m2)

Drain Junction Area - Drain junction area (all Fingers) (m2)

Source junction perimeter - Source junction perimeter (all Fingers) (m)

Drain junction perimeter - Drain junction perimeter (all Fingers) (m)

Length of the Source/Drain - Length of the source/drain (m)

Edge Gate Poly Ext Length - end-cap poly (gate) extension length (m)

Poly_Width - the reference width of poly that is used to assess the length of gate extension (m)

Resistors

Model Name – Spectre model name (non-editable)

Sheet Resistivity – Resistor Sheet Rho (non-editable)

Calculated Parameter – Cyclic that determines whether resistance or length is the calculated value when instantiating a new resistor device

Resistance – total resistance value equal to the sum of body resistance, contact resistance, end resistance, and grain resistance

Segment Width – resistor segment width in meters

Segment Length – resistor segment length in meters

Segments – number of series or parallel segments for a resistor

Segment Connection – cyclic field used for series or parallel segments

Effective Width – effective resistor segment width in meters (non-editable)

Effective Length – effective resistor segment length in meters (non-editable)

Show Layout Parameters – Show layout cdf parameters in form

Left Dummy – boolean value used to place a dummy resistor strip on the left side of the main resistor

Right Dummy – boolean value used to place a dummy resistor strip on the right side of the main resistor

Show Sim Parameters - Show Simulation cdf parameters in form

dw – resistor width process variation value in meters (non-editable)

pt – ambient temperature reference (non-editable)

ptc1 – temperature coefficient #1 for resistor (non-editable)

ptc2 – temperature coefficient #2 for resistor (non-editable)

Capacitor

Model Name - spectre model name (non-editable)

Plate Capacitance – Capacitance per unit area used in parameter calculations (non-editable)

Fringe capacitance – Fringe Capacitance of perimeter used in parameter calculations (non-editable)

Calculated Parameter - Calculated parameter cyclic (capacitance, length, width)

Capacitance – total capacitance

Capcitor Width – Capacitor width in meters

Capcitor Length - Capacitor length in meters

Multiplier - number of Parallel MOS devices

Bipolars

Model name - Model name used in simulation

Emitter Size - Emitter area cyclic (1x1, 2x2)

Poly Pitch – Allowed poly gate pitches

Multiplier - Number of Parallel Bipolar devices

Emitter Width - Emitter width microns

Emitter Length - Emitter length microns

Diodes

Model Name - spectre model name (non-editable)

Fin Pitch (M) – Fin spacing pitch (non-editable)

Number of Fins per Finger - width of each poly finger in integer fin pitches

Diode Width (M) - Diode width in meters (non-editable)

Poly Pitch – Allowed poly gate pitches

Number of Poly Fingers - number of poly gate fingers used in layout

Diode Length (M) - Diode length in meters (non-editable)

Multiplier - Number of Parallel Diode devices

Diode Area - Diode area in meters squared (non-editable)

Diode Periphery - Calculated diode periphery in meters (non-editable)

Show Layout Parameters – Show layout cdf parameters in form

Number of Left Dummy Poly – Number of left dummy polys

Number of Right Dummy Poly – Number of right dummy polys

Model Setup

This PDK supports the Cadence Spectre, Ultrasim, and AMS, circuit simulators, including corner modeling of the MOSFETs.

The following model sections are defined in the <**pdk_install_directory**>/models/spectre/cds_ff_mpt.scs file.

Section

tt – Typical/Typical

ff – Fast/Fast

ss – Slow/Slow

fs – Fast/Slow

sf – Slow/Fast

mc – Monte Carlo

Techfile Layers

Cadence will provide a standard display setup, and will not support desired changes to the display. The customer is free to modify the display.drf file used on-site to achieve any desired display.

CDS #	GDS #	CDS name	Description
3	3	BurriedNWell	Buried N+ Layer
5	5	NWell	N+ Well Layer
10	10	Active	Oxide Layer

11	10:20	CutActive	Oxide Cut Layer
12	300	FinArea	Fin Creation Layer
15	15:0	Psvt	P+ standard Vt Implant Layer
16	16:0	Nsvt	N+ standard Vt Implant Layer
20	20	Poly	Poly Layer
21	21	CutPoly	Poly Cut Layer
25	24	LiPo	Poly Local Interconnect Layer
40	22	LiAct	Oxide Local Interconnect Layer
50	25	V0	Contact Layer
60	30	M1	Metal1 Layer
70	32	V1	Via1 Layer
80	34	M2	Metal2 Layer
90	36	V2	Via2 Layer
100	38	M3	Metal3 Layer
105	40	V3	Via3 Layer
110	42	M4	Metal4 Layer
115	44	V4	Via4 Layer
120	46	M5	Metal5 Layer
125	48	V5	Via5 Layer
130	50	M6	Metal6 Layer
135	52	V6	Via6 Layer
140	54	M7	Metal7 Layer
145	62	VT	Via7 Layer
150	64	MT	Metal8 Layer
99900	60	CMT	Capacitor Metal Layer
99901	30:12	m1res	Metal1 Resistor Marker Layer
99902	34:12	m2res	Metal2 Resistor Marker Layer
99903	38:12	m3res	Metal3 Resistor Marker Layer
99904	42:12	m4res	Metal4 Resistor Marker Layer

99905	46:12	m5res	Metal5 Resistor Marker Layer
99906	50:12	m6res	Metal6 Resistor Marker Layer
99907	54:12	m7res	Metal7 Resistor Marker Layer
99908	64:12	mtres	MetalT Resistor Marker Layer
99912	5:12	nwstires	NW in STI Resistor Marker Layer
99913	5:13	nwodres	NW Oxide Resistor Marker Layer
99914	10:12	diffres	Diffusion Resistor Marker Layer
99915	20:12	pcres	Poly Resistor Marker Layer
99916	153	diodmy	Diode Marker Layer
99918	11	ThickOx	Thick Oxide Layer
99920	16:1	Nlvt	N+ low Vt Implant Layer
99921	16:2	Nhvt	N+ high Vt Implant Layer
99930	15:1	Plvt	P+ low Vt Implant Layer
99931	15:2	Phvt	P+ high Vt Implant Layer
99932	6	SaB	Salicide Blocking Layer
99933	154	NPNdummy	NPN Marker Layer
99934	155	mimW	Mimcap Width Marker Layer
99935	156	mimL	Mimcap Length Marker Layer

PVS Decks

Cadence has developed the PVS DRC and LVS rule files from the documentation provided.

These decks can be found in the extracted PDK directory tree in the directory:

- pvs

PVS DRC

The PVS DRC file provided is named

- pvlDRC.rul

PVS LVS

The PVS LVS files provided is named

- pvlLVS.rul