N65/N55 Calibre LVS/LPE Deck Usage

PDKD/TSMC

Contents

- Variable and Switch Setting
- DFM LPE Setting
- Calibre LVS/XRC Flow
- Calibre/StarRCXT LVS/CCI Flow
- Calibre LVS/XRC GUI Flow

Switch and Variable Setting

Calibre Switches(I)

- **#define DFM_RULE**
  - This switch is used for DFM action required rules.
  - Turn on this switch to enable LPE to consider four DFM effects.
- **#define RC_DECK – Calibre Flow**
  - Turn on this switch for Calibre XRC extraction.
  - For MOS devices, the properties w, l, as, ad, ps, pd, nrs, nrd, and LOD, WPE effects will be extracted.
- **#define CCI_DECK – CCI Flow**
  - Turn on this switch for Calibre+StarRCXT extraction in CCI deck.
  - For MOS devices, the properties w, l, as, ad, ps, pd, nrs, nrd, and LOD, WPE effects will be extracted.
- **#define LVS_DECK – CCI Flow**
  - Turn on this switch for Calibre LVS check in CCI deck.
- **#define ZERO_NRS_NRD**
  - Turn on this switch to set NRS=NRD=0.
  - XRC extracts NRS/NRD by default. In order to avoid double count in source and drain regions, please turn on this switch.

Calibre Switches(II)

- **#define extract_dnwdio**
  - Turn on this switch to extract RW/DNW and DNW/PSUB diodes.
  - NPN devices will not extract “pwdnw” (model has covered) even turn-on this switch.
- **#define top2_thick**
  - Turn on this switch to set Mtop-1 as thick metal.
  - Mtop of 1P9M process is always thick metal, no this switch.
- **#define extract_as_ad**
  - This switch is for TSMC internal library team using only.
- **#define NW_RING**
  - Turn on this switch to enable NW ring to separate the node from BULK.
- **#define STD_LIB_9_TRACK**
  - Turn on this switch to estimate 9 track WPE on standard cells.
  - Do not turn on STD_LIB_11_TRACK at the same time.
- **#define STD_LIB_11_TRACK**
  - Turn on this switch to estimate 11 track WPE on standard cells.
  - Do not turn on STD_LIB_9_TRACK at the same time.

Calibre Switches(III)

- **#define CELLIMP // default off**
  - This switch added after version 1.4a, only for using N65 LP SRAM devices usage. (corresponding model: CLN65LP SRAM, released in Oct. 13st. 2006, version 1.2)
  - In N65G SRAM, we named nchpd_sr, but it seperated into two devices nchpd_wisr and nchpd_wosr in N65LP SRAM. We will set this switch as default off.
- **#define AP_UT // default off**
  - N65LP model cards include rmap_ut device for thick ALRDL (28k) resistor
  - Turn-on it can extract ALRDL resistors as “rmap_ut” model name, instead of rm10
- **#define FILTER_DGS_TIED_MOS**
  // uncomment this line to filter MOS with D, G and S tied together (default filter MOS with all pins tied)
  - #IFNDEF FILTER_DGS_TIED_MOS
  - LVS FILTER UNUSED OPTION AG RC RE RG
  - #ELSE
  - LVS FILTER UNUSED OPTION AB RC RE RG
  - #ENDIF
- **Strongly recommend to comment FILTER_DGS_TIED_MOS switch**
  - AG -- Filters MOS with all pins(S,D,G,B) tied together
  - AB -- Filters MOS devices with source, drain, and gate pins tied together.
  - RC -- Filters resistors with POS and NEG pins tied together.
  - RE -- Filters capacitors with POS and NEG pins tied together.
  - RG -- Filters diodes with POS and NEG pins tied together.

Calibre Switches(IV)

- **About ERC rule switches:**
  We provide 5 switches for important ERC checking rules, and we have suggestion for default on or off.
  - **#define WELL_TO_PG_CHECK :**
    Default is on. Turn on to highlight if nwell connects to ground or psub connects to power.
  - **#define GATE_TO_PG_CHECK**:
    Default is off. Turn on to highlight if a mos gate directly connects to power or ground.
  - **#define PATH_CHECK:**
    Default is off. Please refer in the deck for detailed conditional situation.
  - **#define DS_TO_PG_CHECK:**
    Default is on. Turn on to highlight if drain connects to power and source connects to ground.
  - **#define FLOATING_WELL_CHECK:**
    Default is on. Turn on to highlight if well does not connect to power or ground, and the NW of moscaps and nwell-resistor are excluded.

Calibre Variables

- **VARIABLE POWER_NAME**
  - Power name string setting.
- **VARIABLE GROUND_NAME**
  - Ground name string setting.
- **VARIABLE PMOS_TOP_EXT**
  - Variable of PMOS top boundary extend value for standard cells.
- **VARIABLE NMOS_BOT_EXT**
  - Variable of NMOS bottom boundary extend value for standard cells.
- **VARIABLE MOS_LR_EXT**
  - Variable of MOS horizontal boundary extend value for standard cells.
- **VARIABLE PRESCALE**
  - Scale factor for WPE and DFM effect.
  - For N65 process, PRESCALE=1.0 ; for N55 process, PRESCALE=0.9.
  - Please do not change the default value.
- **VARIABLE WPED**
  - Variable of maximum WPE boundary.
  - For N65 process, WPED=5.0 ; for N55 process, WPED=5.556.
  - Please do not change the default value.

Runset Options

- **Virtual connection setting:**
  - By default, **“VIRTUAL CONNECT COLON”** is set yes.
  - Please set to "NO" in LVS command file as doing full-chip checking.
  - VIRTUAL CONNECT COLON YES
    → VIRTUAL CONNECT COLON NO

DFM LPE Setting

DFM LPE Setting

- **DFM switches**
  - Turn on the switch DFM_RULE and RC_DECK(CCI_DECK) for DFM LPE extraction.
    DFM folder
  - Please move the folder “DFM” to the same directory with your Calibre deck or change the path to correct “DFM” folder location in your Calibre deck.
  - **INCLUDE ./DFM/dfm_device**
- **DFM variable file**
  - Under the folder “DFM”, there is a variable file named “**variable_file**”. There are three additional variable files. Their file names are “variable_file_G”, “variable_file_G+”, and “variable_file_LP” respectively. By default, the content of “variable_file” is for G+ process. If customers want to use other processes, please overwrite “variable_file” with the correct variable file. For example, if customers use LP process, please use “variable_file_LP” to overwrite “variable_file”.
- **ZERO_NRS_NRD switch in DFM**
  - The definition of NRS/NRD in DFM LPE deck is
    NRS = NRS1(original)+NRS2+NRS3 NRD = NRD1(original)+NRD2+NRD3
  - If #define ZERO_NRS_NRD, the deck will only set NRS1=NRD1= 0

Calibre LVS/XRC Flow

Calibre LVS Flow

- **Run LVS deck(default):**
  - Include “source.added” file in your source netlist for subcircuits.
    - .include source.added
  - Comment the following line for LVS check.
    - //#define RC_DECK
  - Fill in the gds file name and top_cell name in the rule deck.
    - LAYOUT PRIMARY “top_cell”
    - LAYOUT PATH “top_cell.gds”
  - Fill in the source netlist name and top_cell name in the rule deck.
    - SOURCE PRIMARY “top_cell”
    - SOURCE PATH “top_cell.cdl”
  - Run Calibre
    - **% calibre –lvs –hier –spi layout.net calibre_rule_deck**
    - Files lvs.rep and lvs.rep.ext are LVS result and path check report.
  - It’s recommend to flatten dummy patterns for performance.
    - FLATTEN CELL top_cell_DM top_cell_DODDPO

Calibre XRC Extraction Flow(1)

- **Prepare XRC technology file :**
  - Download the xCalibre RC technology file corresponding to the process you used from TSMC online.
    - For example, if your design is based on TSMC 65nm LOGIC 1P9M+ALRDL SALICIDE LP 1.2V/2.5V process(T-N65-CL-SP-009-X1), you need to download the XRC technology file corresponding to this process.
  - Unzip the zip file and extract the capacitance rule statement file (rules) and resistor statement file(File name looks like "cln65lp.res").
  - Use the Unix command 'cat' to combine these two files into a new rule file, and rename the new rule file "rules".
    - **% cat cln65lp.res >> rules**
  - Finally, run RCX on your design. Make sure the "rules" file is located in the working directory.

Calibre XRC Extraction Flow(2)

- **Run RC deck:**
  - Include “source.added” file in your source netlist for subcircuits.
    - .include source.added
  - Uncomment the following line for RC extraction flow.
    - #define RC_DECK
  - Fill in the gds file name and top_cell name in the rule deck.
    - LAYOUT PRIMARY “top_cell”
    - LAYOUT PATH “top_cell.gds”
  - Fill in the source netlist name and top_cell name in the rule deck.
    - SOURCE PRIMARY “top_cell”
    - SOURCE PATH “top_cell.cdl”
  - Run Calibre XRC steps:
    - Because Mentor will not support wild card symbol(*) in hcell file after calibre tool version 2008.1~ Original cell-blocking format must be changed to let blocking function work.

Calibre XRC Extraction Flow(3)

- **Run RC deck:**
  - For above reasons, we have to rename hcell to xcell for XRC LPE flow, and put all parameterized cells into calibre_rule_deck. That means the steps will be minor changed to be :
  - Changed in Cailbre command files: (add three lines)
    - **LVS PRESERVE PARAMETERIZED CELLS YES**
    - **LAYOUT CELL LIST pcells "crtmom_rf*" "lincap_rf*" "nmos_rf" …..**
    - **LAYOUT PRESERVE CELL LIST pcells**
  - Changed in xCalibre steps :
  - File "xcell" is used for RC cell blocking in RF devices. (original hcell → xcell)
  - **% calibre –xrc –phdb calibre_rule_deck**
  - **% calibre –xrc –pdb –xcell xcell –rc calibre_rule_deck**
  - **% calibre –xrc –fmt –all calibre_rule_deck**
  - Files net.dist , net.dist.pex, and net.top_cell.pxi are created.

Calibre/StarRCXT LVS/CCI Flow

Calibre LVS/CCI Flow

- **Run LVS deck:**
  - Include “source.added” file in your source netlist for subcircuits.
    - .include source.added
  - Comment the following line for LVS check.
    - //#define CCI_DECK
  - Uncomment the following line for LVS check.
    - #define LVS_DECK
  - Fill in the gds file name and top_cell name in the rule deck.
    - LAYOUT PRIMARY “top_cell”
    - LAYOUT PATH “top_cell.gds”
  - Fill in the source netlist name and top_cell name in the rule deck.
    - SOURCE PRIMARY “top_cell”
    - SOURCE PATH “top_cell.cdl”
  - Run Calibre
    - **% calibre –lvs –hier –spi layout.net calibre_rule_deck**
    - Files lvs.rep and lvs.rep.ext are LVS result and path check report.
  - It’s recommend to flatten dummy patterns for performance.
    - FLATTEN CELL top_cell_DM top_cell_DODDPO

Calibre/StarRCXT CCI FLOW

- **Run CCI deck(default) :**
  - Include “source.added” file in your source netlist for subcircuits.
    - .include source.added
  - Comment the following line for CCI StarRCXT flow.
    - //#define LVS_DECK
  - Uncomment the following line for CCI StarRCXT flow.
    - #define CCI_DECK
  - Run Calibre
    - **% calibre -lvs –hier –spi layout.net calibre_rule_deck**
    - **% calibre -query svdb < query_cmd**
  - Run StarRCXT :
    - The StarRCXT mapping files with different metal scheme are put in CCI_FLOW/STAR_MAP catalog.
    - Download StarRCXT tech file(*.nxtgrd file) from TSMC online.
    - In order to get a correct spice model name for simulation in CCI flow, please add cross reference command “XREF: YES” in your star_cmd file.
    - Please use star extraction command.

      % StarXtract -clean star_cmd

StarRCXT Mapping File Notice

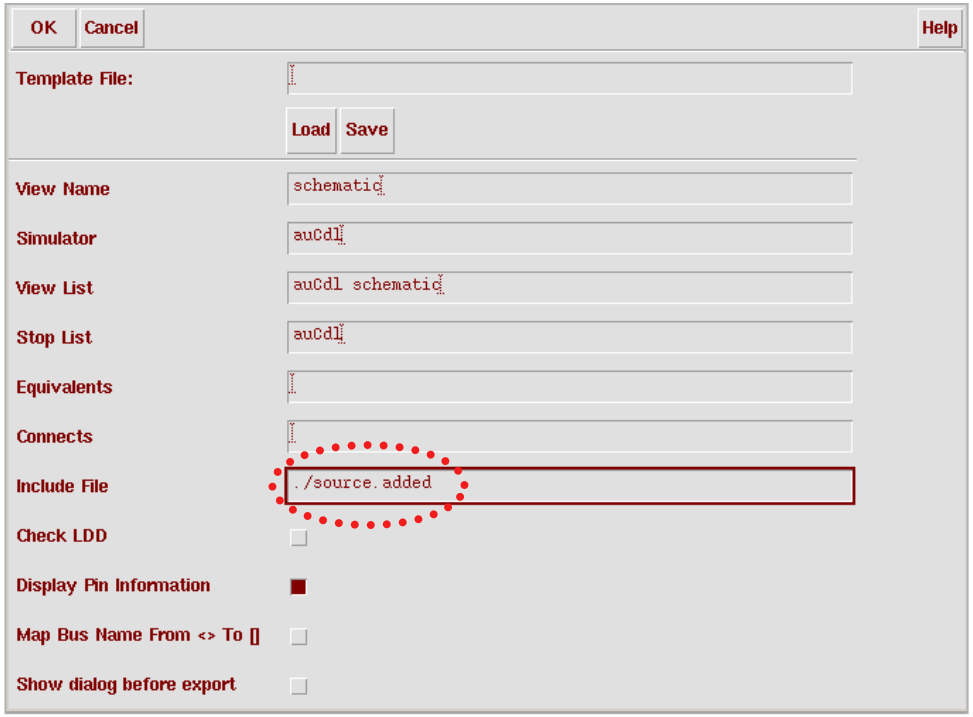
- If no eDRAM devices, please move "p3", "blc", "p3Cont" and "crown" to remove layer section.
- If no MIMCAP devices, please move "ctm", "cbm", "ctm_via" and "cbm_via" to remove layer section.
- When the switch "extract_dnwdio" is turn off, please move layer "psub_term" to remove layer.
- By default ZERO_NRS_NRS = 0, user has to set RPSQ of tndiff/tpdiff to zero (RPSQ=0.0000001) to avoid double count. Then NRS/NRD will be extracted by Calibre and output as device parameters.
  - tndiff OD RPSQ=0.0000001
  - tpdiff OD RPSQ=0.0000001
- If set ZERO_NRS_NRD = 1, users have to remove RPSQ=0.0000001 of tndiff/tpdiff. Then NRS/NRD will be extracted by StarRCXT and output as parasitic RC network.
  - tndiff OD
  - tpdiff OD
- Please ignore the warning message in StarRCXT CCI flow, it won't impact any accuracy.

Calibre LVS/XRC GUI Flow

Calibre LVS Flow(I)

1. Specify the “source.added” file as an include file for netlist export by click “Calibre->Setup->Netlist Export…”.

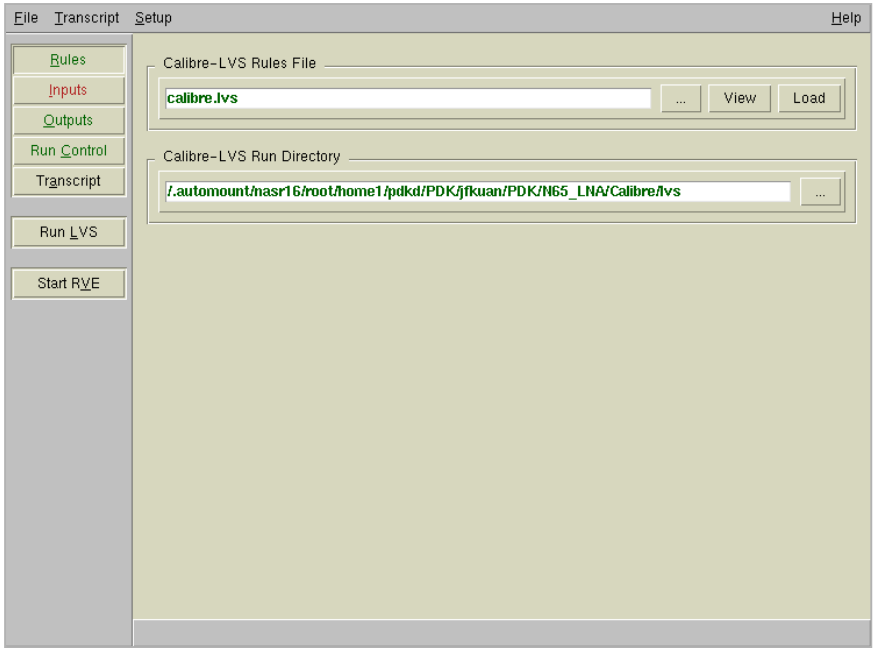
2. Click “Calibre->Run LVS” in layout window to invoke Calibre LVS graphic user interface.

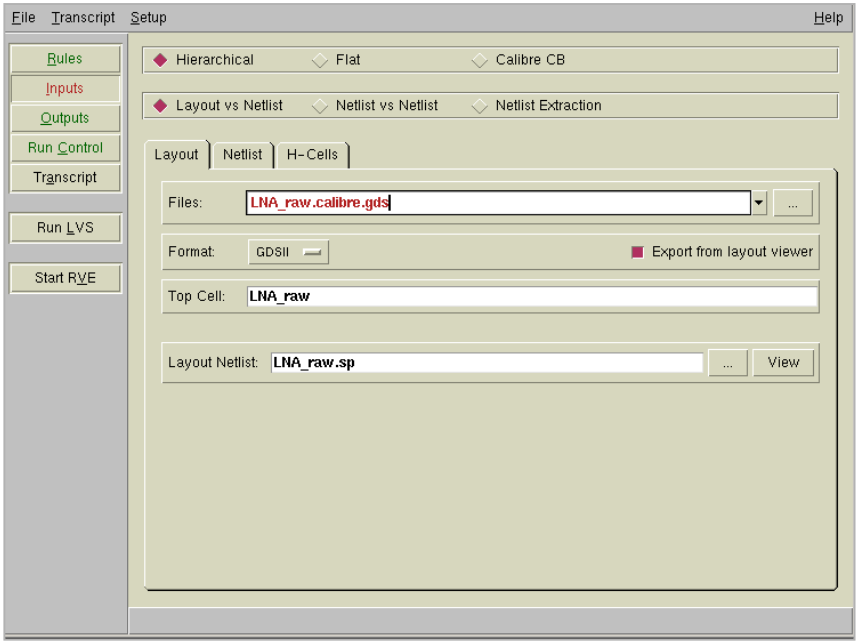


Calibre LVS Flow(II)

3. Specify the “Calibre-LVS rules file“, working directory and “Primary cell” in Calibre LVS window. If you need to change some LVS switches, you have to edit the Calibre LVS deck first.

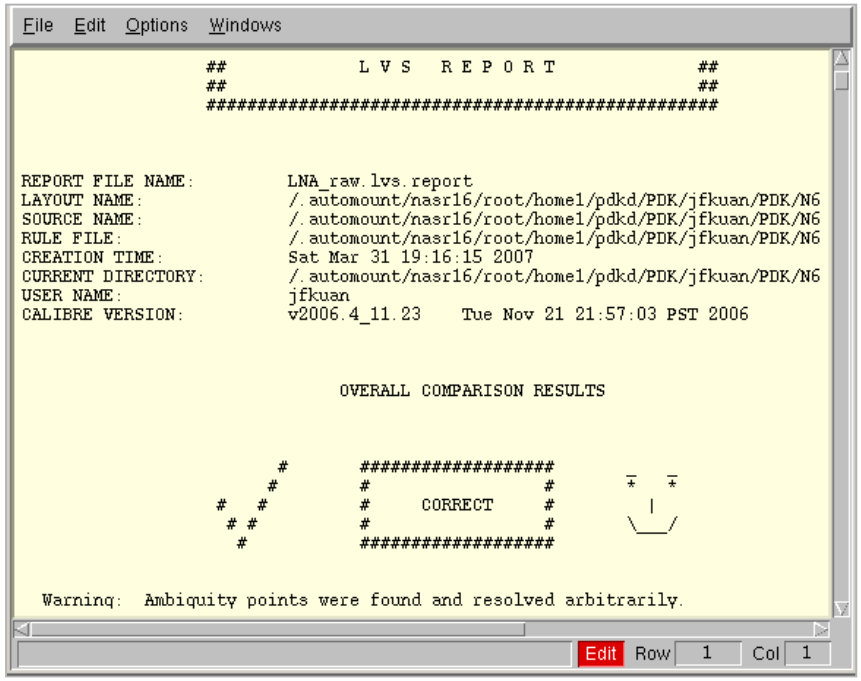
4. Click “OK” to run the Calibre GUI LVS and see the result. If the layout isn’t matched to schematic, you have to fix the layout and re-run the LVS check to make the LVS result matched.

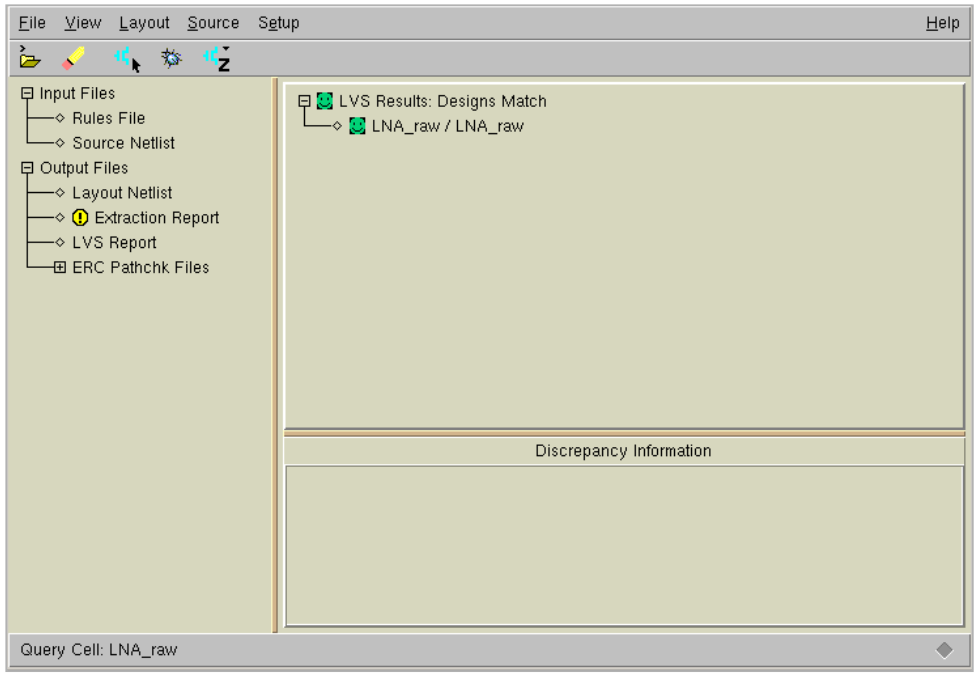




Calibre LVS Flow(III)

Below is the LVS result that shows good match between layout and schematic.





Calibre XRC Flow(I)

Before running XRC flow

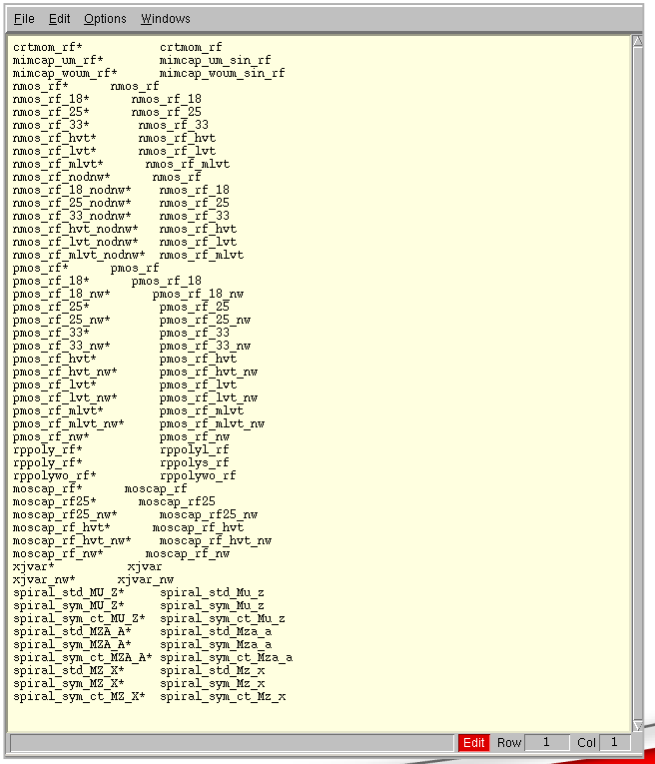
Since all of the parasitics in the P-cell have been accounted by RF PDK device model. The extraction tool must not extract parasitics inside the specified devices to avoid double counting. The following steps should be taken to run pre-characterized device (PCD) flow:

1. Add following statements in your XRC rule file:

   SOURCE CASE YES

   LVS COMPARE CASE NAMES

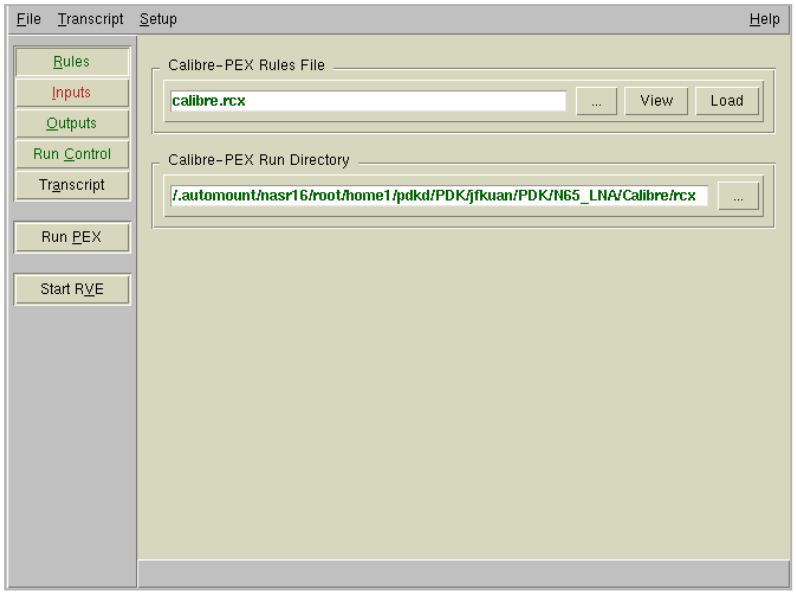
2. Add ***PEX IDEAL XCELL YES*** in your XRC rule file.
3. Prepare h-cell file for RC blocking in RF devices:

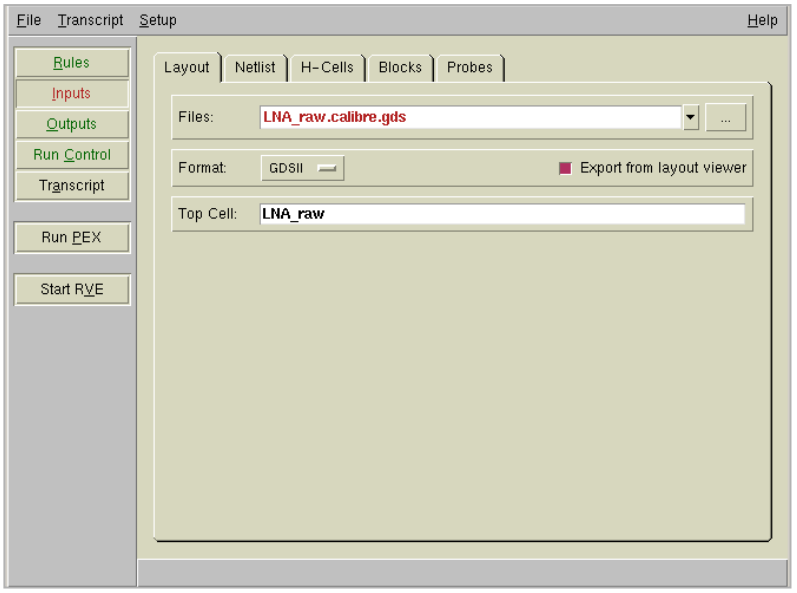


Calibre XRC Flow(II)

1. Click “Calibre->Run PEX” in layout window to invoke Calibre XRC graphic user interface.

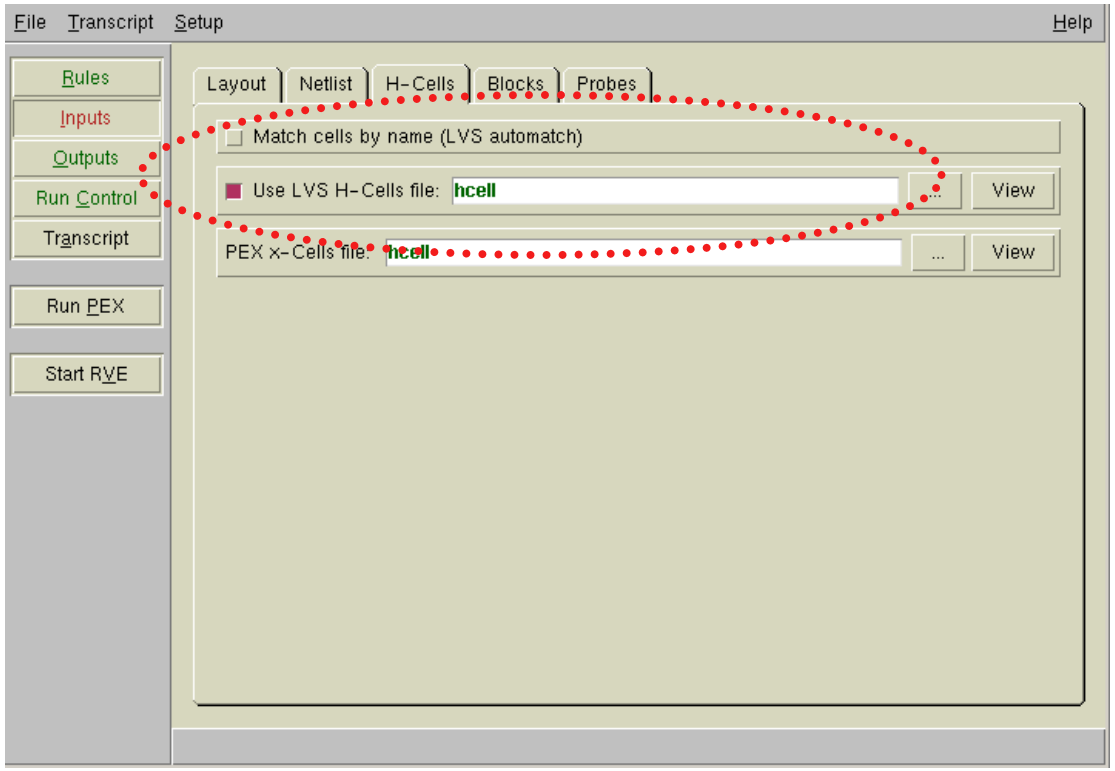
2. Specify the “Calibre-PEX rules file“, working directory and “Top cell” in Calibre XRC window. If you need to change some XRC switches, you have to edit the Calibre XRC deck first.





Calibre XRC Flow(III)

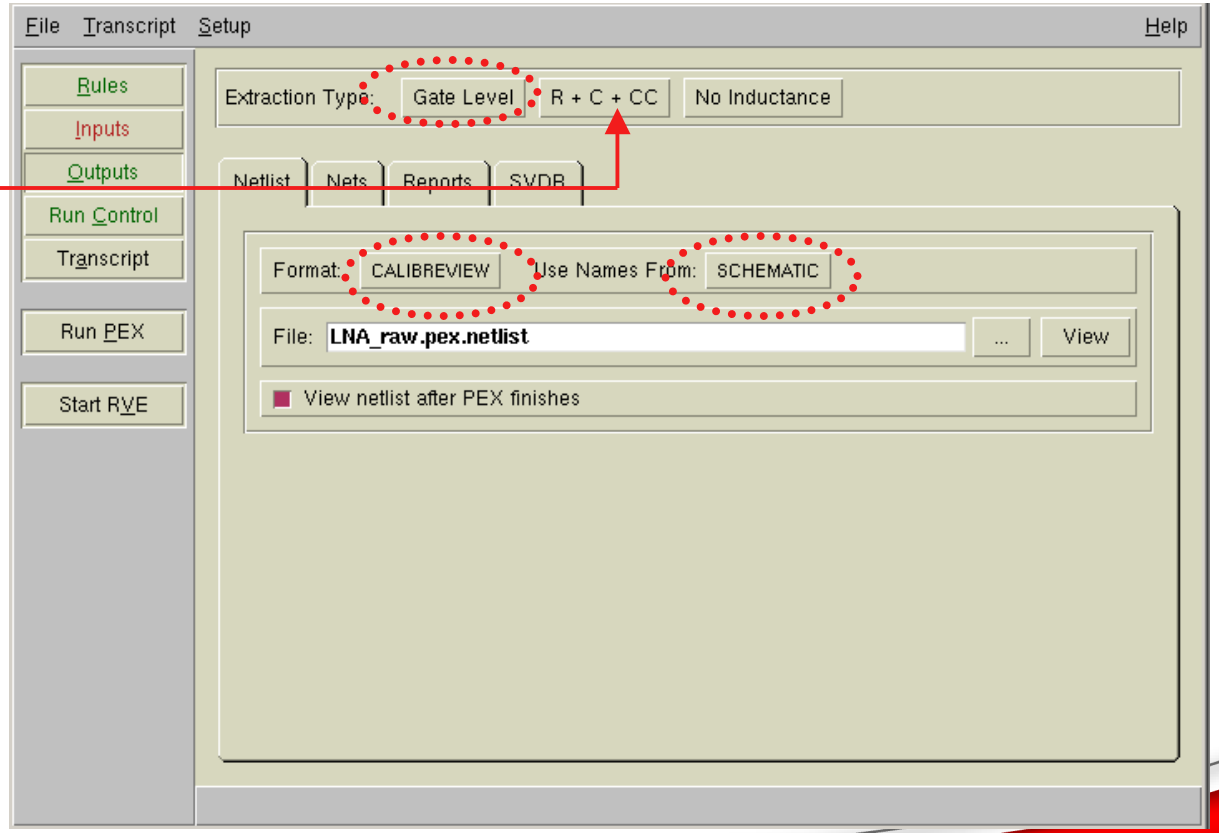
3. Enable "**Use LVS H-Cells file**" in" **Inputs->H-Cells**". Specify the H-cell file name and PEX x-Cell file name which is the hcell file that is included in LVS package.



Calibre XRC Flow(IV)

4. Select the "**Outputs**", set the "**Extraction Type**" to "**Gate Level**". Specify the output format to be "**CALIBREVIEW**" and "Use Names From" to be "**SCHEMATIC**".

Select the extraction type which you want to run.
(no parasitic, C+CC, R, R+C, R+C+CC)



Calibre XRC Flow(V)

4. Click “OK” to run the Calibre GUI RC extraction. When the extraction run is completed, a calibre view setup window will pop up. Specify the “Cellmap File”, “Magnify symbols by” .

5. Click “OK” in the Calibre view setup window to create the Calibre view.