LEGEND:
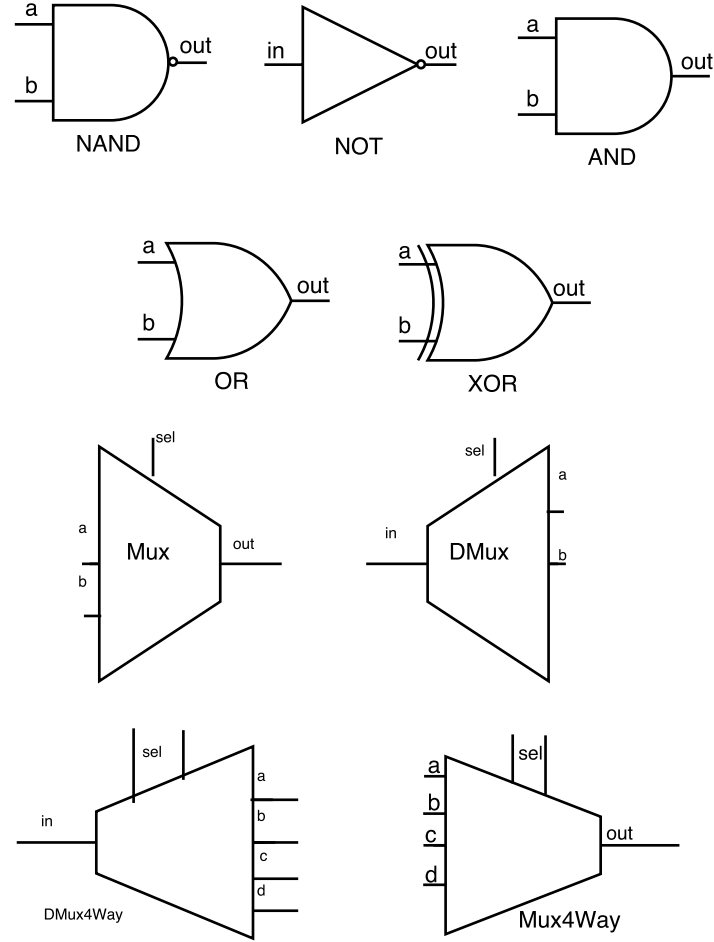
NAND

NOT

AND

OR

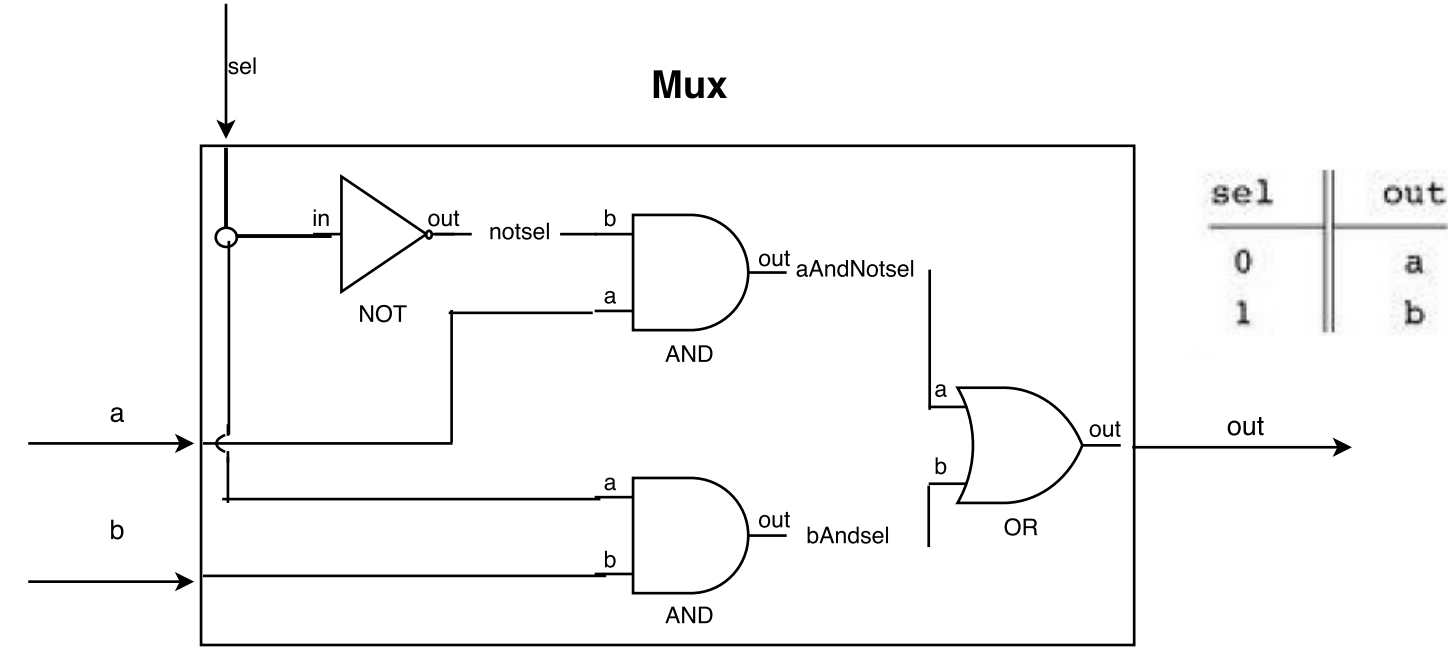XOR

Mux

DMux

DMux4Way

Mux4Way

Homework #2
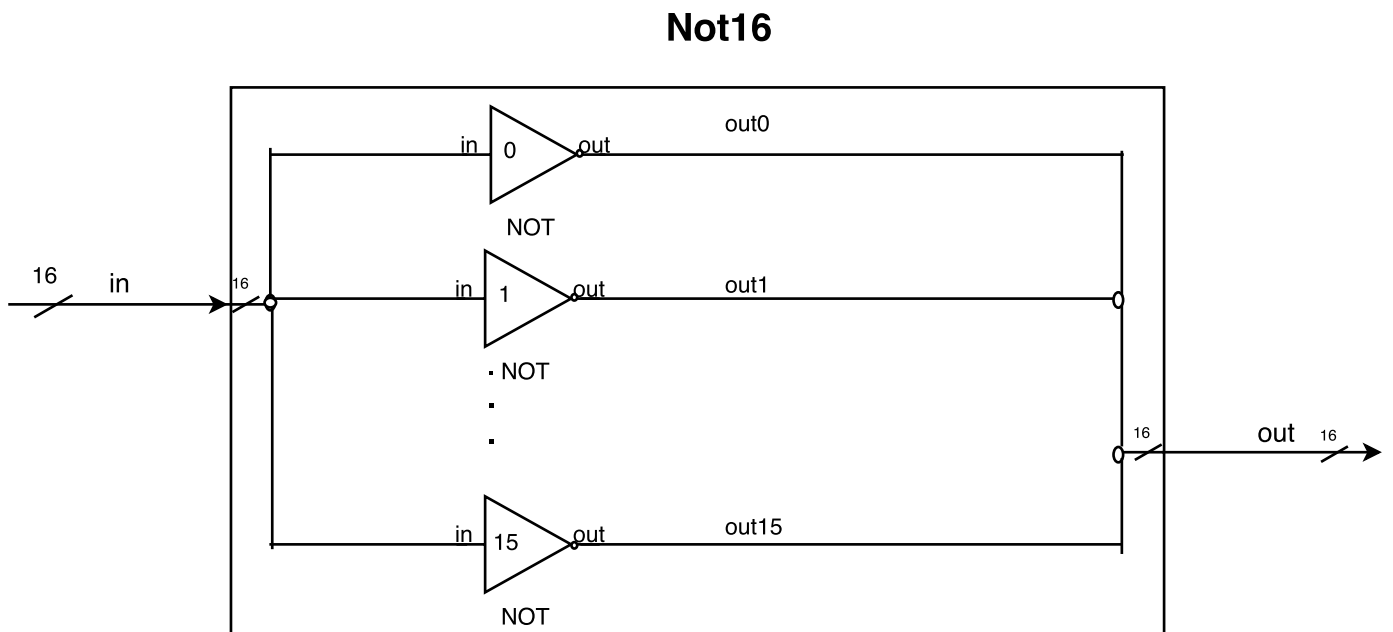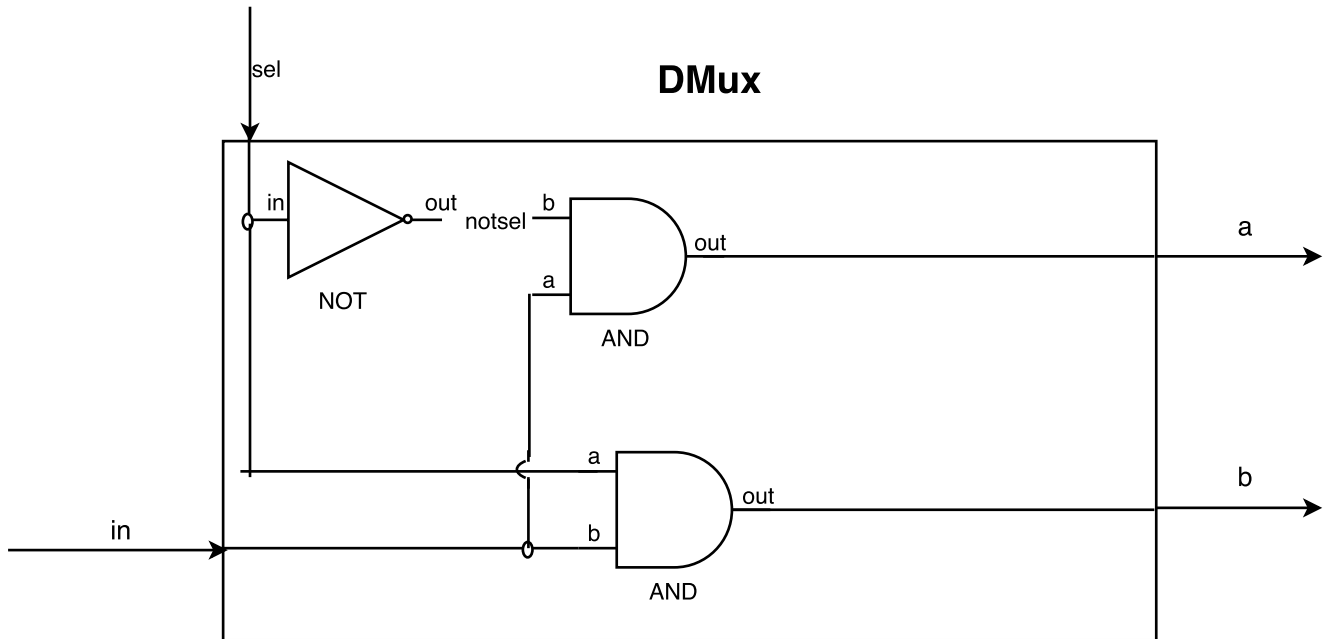
CS220 - Computer Architecture + Machine Language

Author: Tina Taleb

Section: 2653 M/W 3:30pm - 5:20pm

Last Modified: 2/5/17

Mux

notsel

NOT

out aAndNotsel

bAndsel

AND

AND

OR

out

out

sel

a

b

sel	out
0	a
1	b

sel	a	b
0	in	0
1	0	in

DMux

sel

in   out   notsel   b

NOT

a

AND   out   a

a

in   b

AND   out   b

Not16

16   in

16

in   0   out   out0

NOT

in   1   out   out1

NOT

in   15   out   out15

NOT

16

out   16

And16

Or16

Mux16

a —16—→ 16 ⊸

b —16—→ 16

sel ↓

0 Mux	out0
1 Mux	out1
15 Mux	out15

out —16—→

Or8Way

in —8—→ 8 ⊸

OR → out or01	
OR → out or23	OR → out or0123
OR → out or45	
OR → out or67	OR → out or4567

OR → out

out →
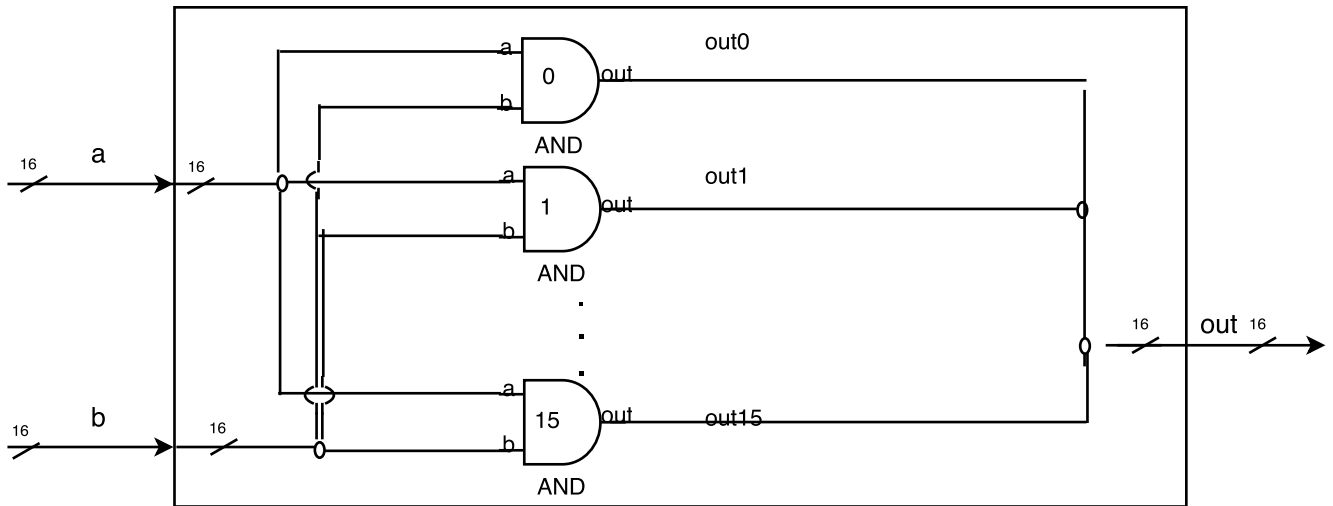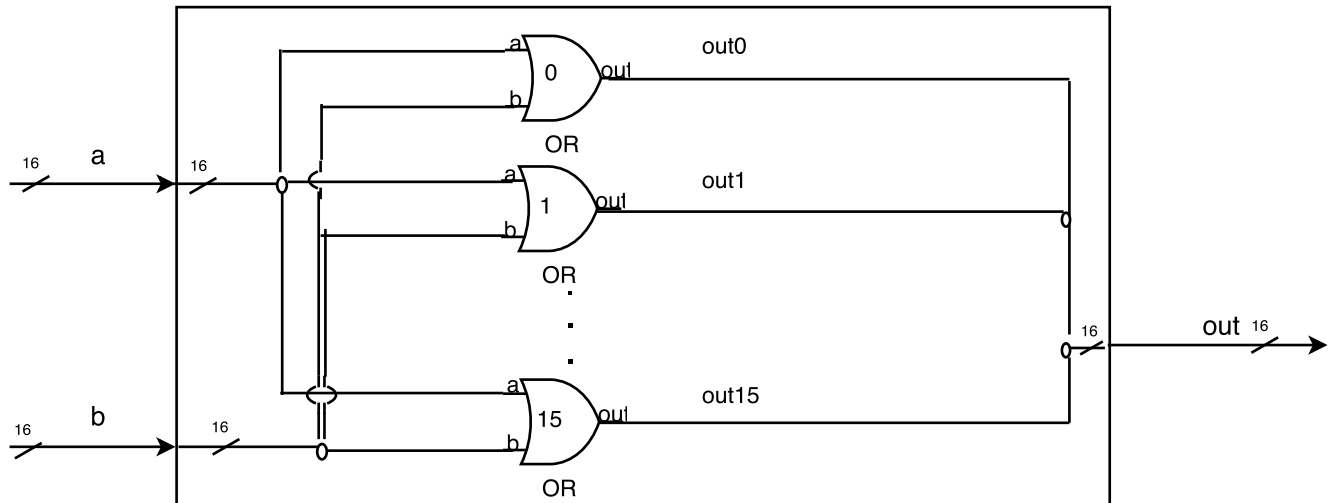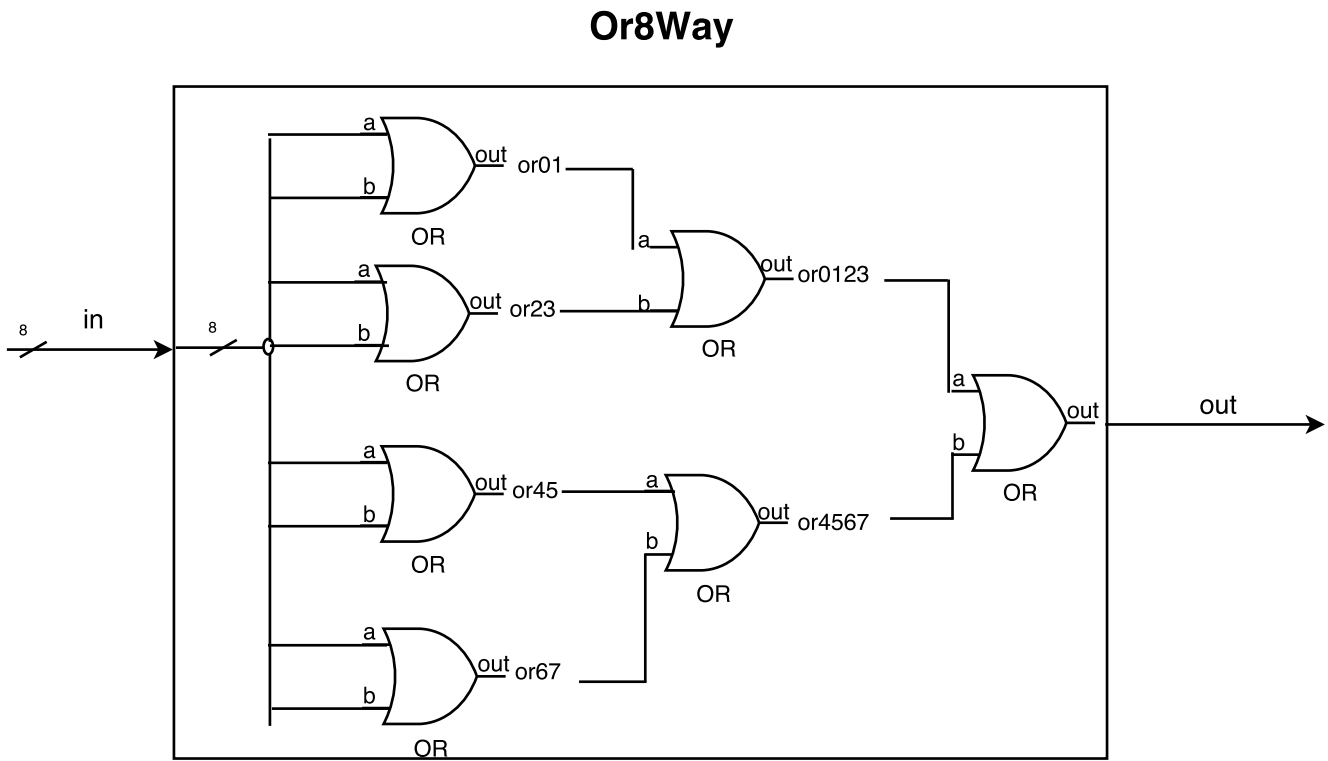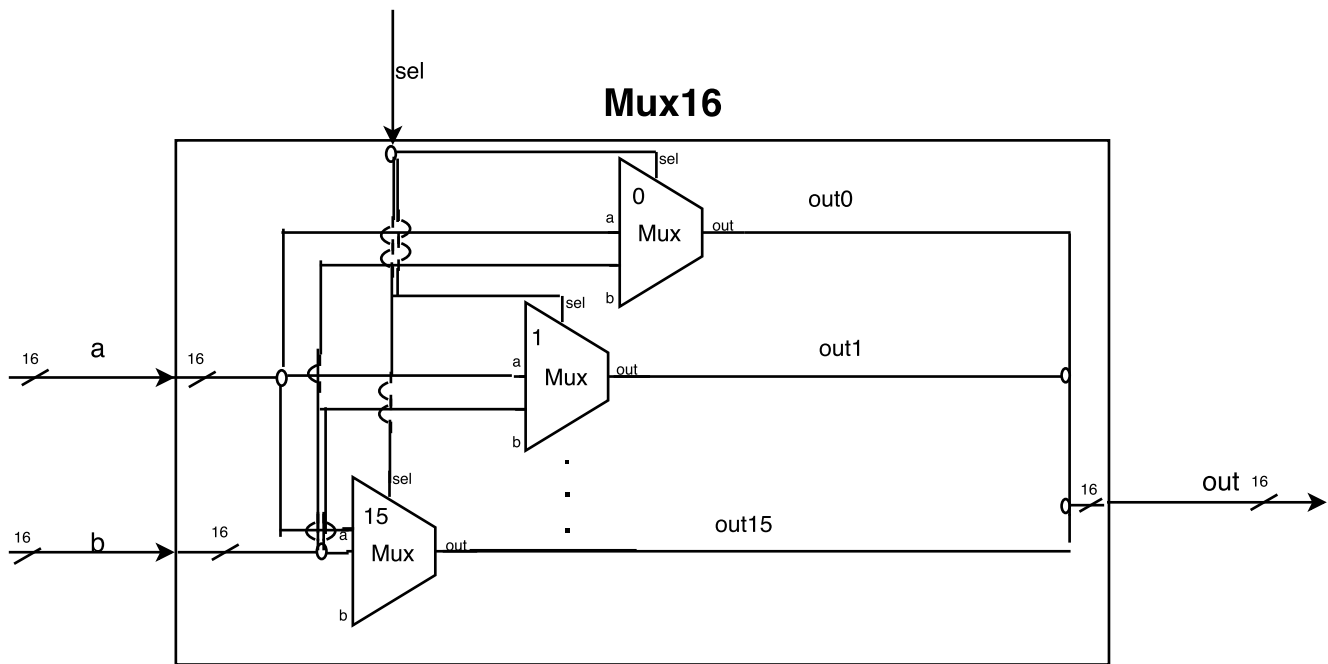
sel[1]	sel[0]	out
0	0	a
0	1	b
1	0	c
1	1	d

Mux4Way16
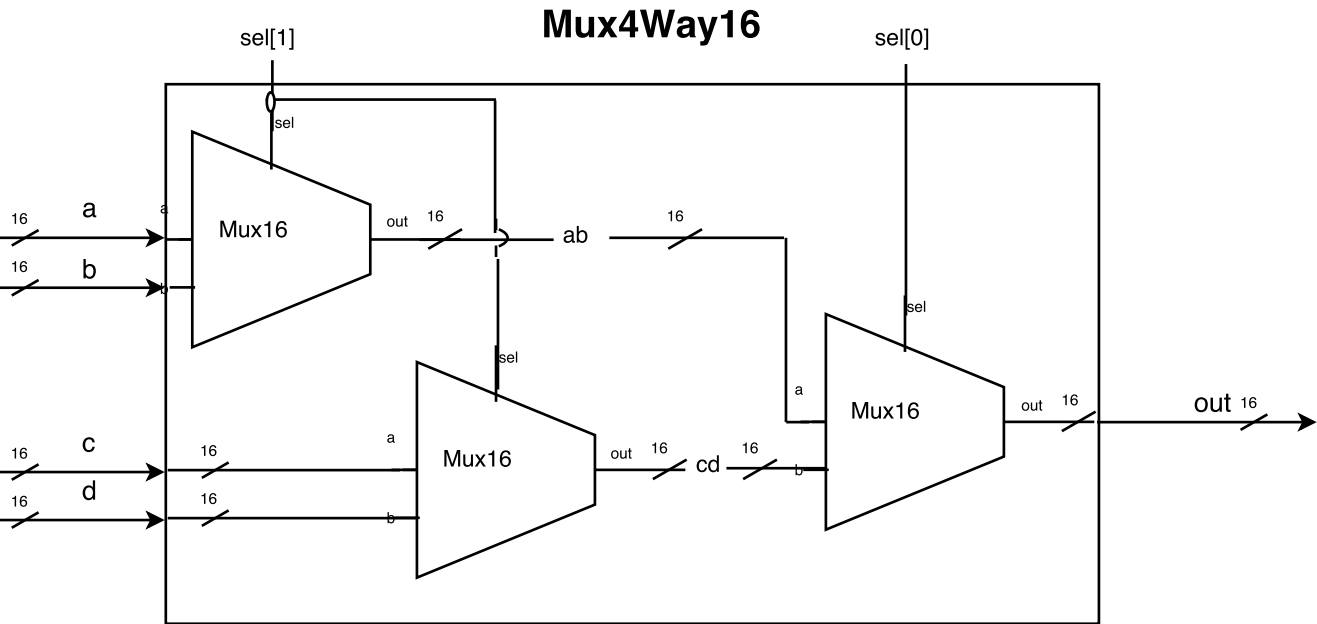
sel[1]	sel[0]	a	b	c	d
0	0	in	0	0	0
0	1	0	in	0	0
1	0	0	0	in	0
1	1	0	0	0	in

DMux4Way
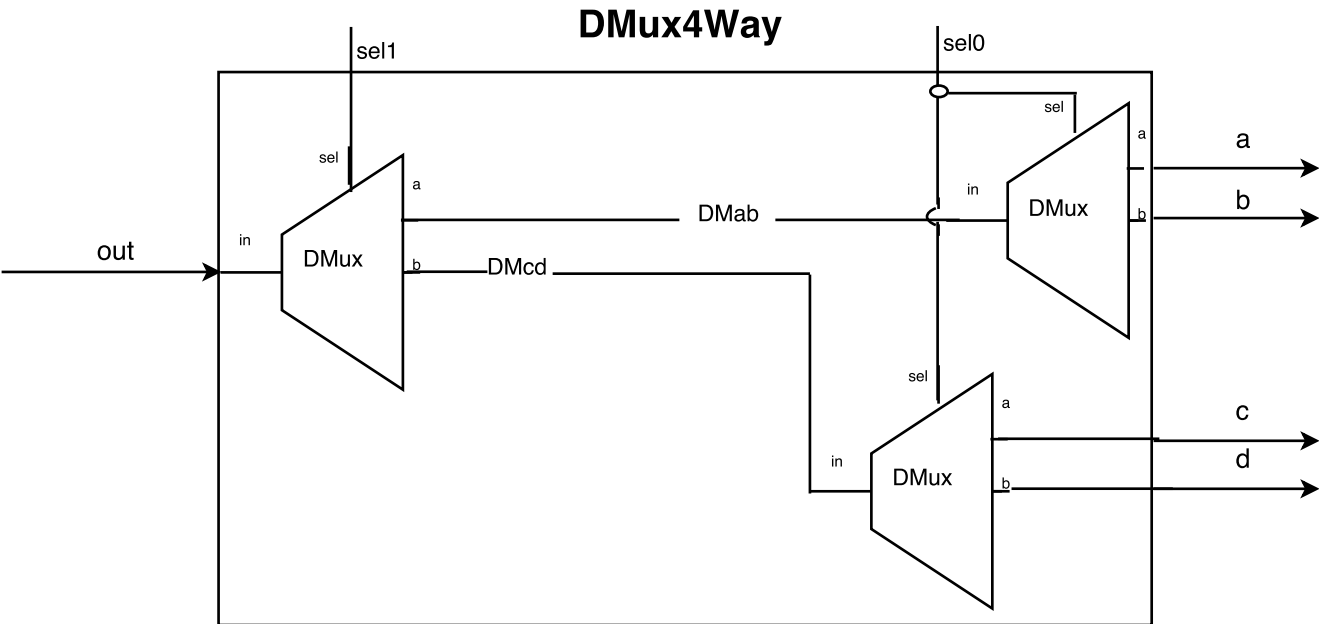
sel[2]	sel[1]	sel[0]	out
0	0	0	a
0	0	1	b
0	1	0	c
0	1	1	d
1	0	0	e
1	0	1	f
1	1	0	g
1	1	1	h

Mux8Way16

sel[0] sel[1] sel[2]

16 a

16 b

16 c

16 d

a
b
c
d

sel

out

Mux4Way

16 abcd

sel

16 a Mux16 out 16

16 b

out 16

16

16 e

16 b

16 g

16 h

a
b
c
d

sel

out

efgh

Mux4Way

out 16
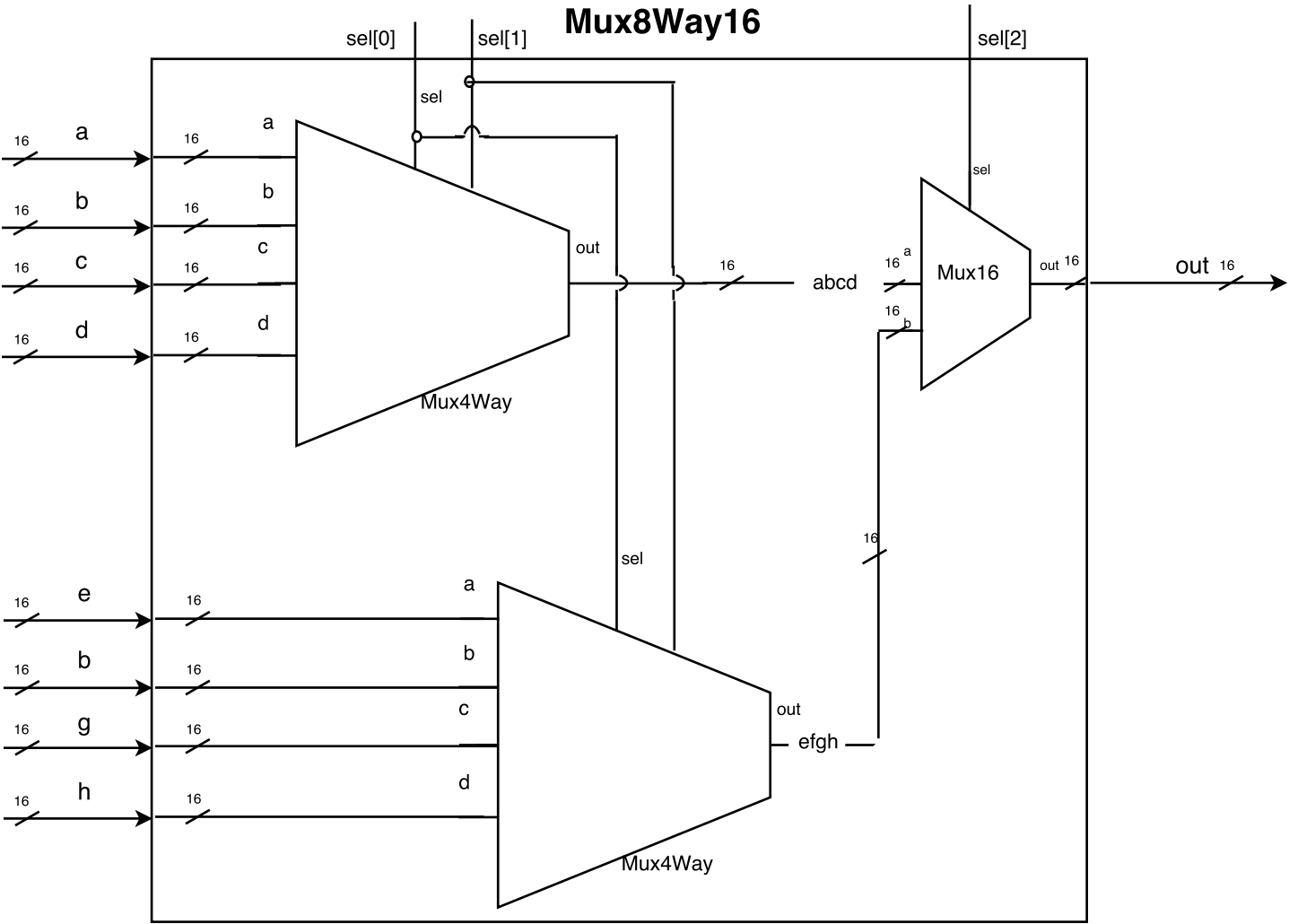
sel[2]	sel[1]	sel[0]	a	b	c	d	e	f	g	h
0	0	0	in	0	0	0	0	0	0	0
0	0	1	0	in	0	0	0	0	0	0
0	1	0	0	0	in	0	0	0	0	0
0	1	1	0	0	0	in	0	0	0	0
1	0	0	0	0	0	0	in	0	0	0
1	0	1	0	0	0	0	0	in	0	0
1	1	0	0	0	0	0	0	0	In	0
1	1	1	0	0	0	0	0	0	0	in

DMux8Way