Resistive switching in transition metal oxides

Rapid advances in information technology rely on high-speed and large-capacity nonvolatile memories. A number of alternatives to contemporary Flash memory have been extensively studied to obtain a more powerful and functional nonvolatile memory. We review the current status of one of the alternatives, resistance random access memory (ReRAM), which uses a resistive switching phenomenon found in transition metal oxides. A ReRAM memory cell is a capacitor-like structure composed of insulating or semiconducting transition metal oxides that exhibits reversible resistive switching on applying voltage pulses. Recent advances in the understanding of the driving mechanism are described in light of experimental results involving memory cells composed of perovskite manganites and titanates.

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Modern semiconductor nonvolatile memories, such as Flash memory, have been successfully scaled down to achieve large-capacity memories through improvements in photolithography technology. However, conventional memory scaling is expected to come up against technical and physical limits in the near future. In order to overcome this problem, 'equivalent scaling', i.e. functionalization by introducing new materials and/or three-dimensional structures, has been proposed as a new alternative to the conventional scaling technology.

Candidates for equivalent scaling based on new materials, including ferroelectric random access memory (FeRAM), in which the polarization

of a ferroelectric material is reversed, magnetoresistive RAM (MRAM), which uses magnetic tunnel junctions, and phase-change RAM (PRAM), which uses the change in resistance between crystalline and amorphous states of a chalcogenide compound, have attracted a great deal of attention for use as next-generation nonvolatile memories.

Recently, a new candidate has emerged: resistance random access memory (ReRAM). It is based on new materials, such as metal oxides^{1,2} and organic compounds^{3–5}, which show a resistive switching phenomenon. The ReRAM memory cell has a capacitor-like structure composed of insulating or semiconducting materials sandwiched between two metal electrodes (Fig. 1). Because of its simple structure,

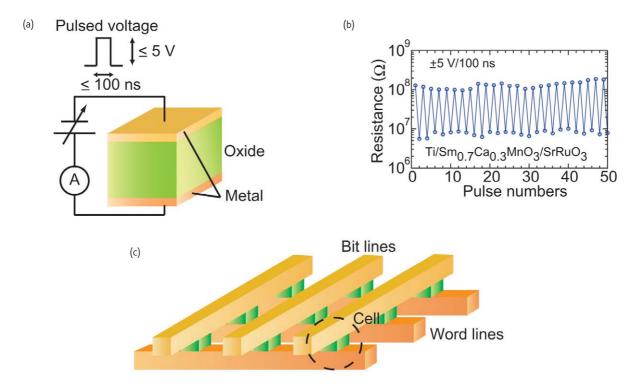


Fig. 1 (a) Diagram of a ReRAM memory cell with a capacitor-like structure in which an insulating or semiconducting oxide is sandwiched between two metal electrodes. (b) Resistive switching in a $Ti/Sm_{0.7}Ca_{0.3}Mn_3/SrRuO_3$ (MIM) cell at room temperature. By applying pulsed voltages of ± 5 V, the resistance of the cell changes reversibly between high and low resistance states. (c) Diagram of a cross-point memory structure. Word and bit lines are used for selecting a memory cell and writing/reading data, respectively.

highly scalable cross-point and multilevel stacking memory structures have been proposed⁶. In the resistive switching phenomenon, a large change in resistance (>1000%) occurs on applying pulsed voltages (Fig. 1), and the resistance of the cell can be set to a desired values by applying the appropriate voltage pulse¹. A recent study has shown that the switching speed can be faster than several nanoseconds⁷.

Among the materials that exhibit a resistive switching phenomenon, oxide materials have been studied intensively. In 1962, Hickmott⁸ first reported hysteretic current–voltage (*I–V*) characteristics in metal-insulator-metal (MIM) structures of Al/Al₂O₃/Al, indicating that resistive switching occurs as a result of applied electric fields. Resistive switching has subsequently been reported in a wide variety of MIM structures composed of binary metal oxides, such as SiO⁹ and NiO¹⁰.

Some models for the driving mechanism of resistive switching have been proposed, e.g. the charge trap model⁹ and conductive filament model¹⁰. These studies on binary metal oxides were mainly conducted in the 1960s and 1980s and have been reviewed previously^{11–13}. In the 1990s, complex transition metal oxides, such as perovskite-type manganites and titanates, became the focus because of a report of resistive switching in Pr_{0.7}Ca_{0.3}MnO₃ (PCMO) by Asamitsu *et al.* ¹⁴. Recently, prototype ReRAM devices composed of PCMO and NiO have been demonstrated by Sharp Corporation and the University of Houston¹ and Samsung², respectively.

Because a design guide for ReRAM based on a driving mechanism has not been produced, its development is less advanced than other candidates for next-generation nonvolatile memories, such as FeRAM, MRAM, and PRAM. Therefore, elucidation of a driving mechanism is currently a very important issue in the development of ReRAM. Detailed experimental 15–43 and theoretical 44–47 studies on the resistive switching phenomenon have been carried out to determine the driving mechanism, and some possible models have been proposed. The models can be grouped into categories depending on the switching behavior and conducting path.

Classification of resistive switching behavior

The resistive switching phenomenon has been observed in a wide variety of transition metal oxides, such as PCMO¹⁵, Cr-doped SrZrO₃¹⁶, SrTiO₃¹⁷, NiO^{2,10}, TiO₂²⁹, and Cu₂O³¹. However, the observed switching behavior seems to differ depending on the material. On the basis of I–V characteristics, the switching behaviors can be classified into two types: unipolar (nonpolar) and bipolar, for which typical I–V curves are shown in Figs. 2a and 2b, respectively.

In unipolar resistive switching, the switching direction depends on the amplitude of the applied voltage but not on the polarity. An as-prepared memory cell is in a highly resistive state and is put into a low-resistance state (LRS) by applying a high voltage stress. This

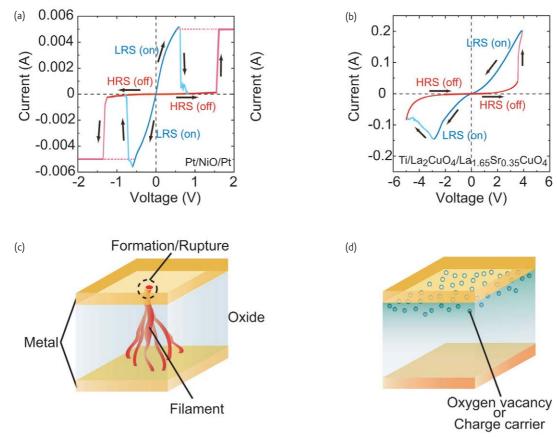


Fig. 21-V curves for (a) unipolar (nonpolar) switching in a Pt/NiO/Pt cell and (b) bipolar switching in a $Ti/La_2CuO_4/La_{1.65}Sr_{0.35}CuO_4$ cell. In unipolar switching, the switching direction depends on the amplitude of the applied voltage. Bipolar switching shows directional resistance switching according to the polarity of the applied voltage. Proposed models for resistive switching can be classified according to either (c) a filamentary conducting path, or (d) an interface-type conducting path. (Part (a) courtesy of I. H. Inoue, AIST.)

is called the 'forming process'. After the forming process, the cell in a LRS is switched to a high-resistance state (HRS) by applying a threshold voltage ('reset process'). Switching from a HRS to a LRS ('set process') is achieved by applying a threshold voltage that is larger than the reset voltage. In the set process, the current is limited by the current compliance of the control system or, more practically, by adding a series resistor. This type of switching behavior has been observed in many highly insulating oxides, such as binary metal oxides².

Bipolar resistive switching shows directional resistive switching depending on the polarity of the applied voltage (Fig. 2b). This type of resistive switching behavior occurs with many semiconducting oxides, such as complex perovskite oxides 16,21-23, and will be discussed in detail in this review.

Classification of resistive switching mechanisms

In addition to classification in terms of switching behavior, the type of conducting path is also used to categorize the resistive switching. One class shows a filamentary conducting path, in which the resistive

switching originates from the formation and rupture of conductive filaments in an insulating matrix (Fig. 2c). This can be associated with both unipolar and bipolar switching behavior.

Fig. 3 shows a possible driving mechanism for filament-type resistive switching that shows unipolar switching behavior. In the forming process (1), filamentary conducting paths form as a soft breakdown in the dielectric material. Rupture of the filaments takes place during the reset (2) process, and filament formation during the set process (3). Thermal redox and/or anodization near the interface between the metal electrode and the oxide is widely considered to be the mechanism behind the formation and rupture of the filaments^{32,33}. In contrast, in bipolar-type switching, electrochemical migration of oxygen ions is regarded as the driving mechanism²⁶.

Clear visualization of the conducting filaments in insulating oxides has not been achieved. Recent studies involving highresolution transmission electron microscopy and electron energy loss spectroscopy of NiO memory cells suggest that the filamentary conducting paths form in the grain boundaries³⁵. Fujiwara et al.³⁶ have investigated filaments in planar cells and reported the formation

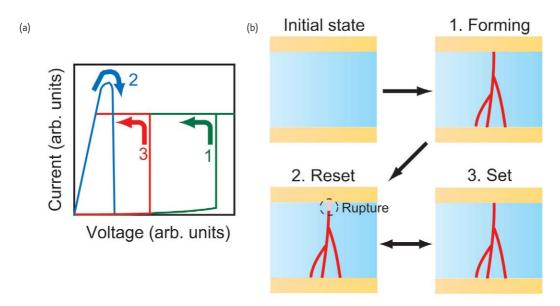


Fig. 3 (a) Unipolar resistive switching behavior. (b) Schematics of the initial state (as-prepared sample) and (1) forming, (2) reset, and (3) set processes.

of a filament-like structure in a polycrystalline CuO film between Pt electrodes during the forming process (Fig. 4), after which the cell switches into a LRS. They have also shown that the cell resistance returns almost to the original value when a part of the filament-like structure is cut with a focused ion beam, indicating that the filament-like structure is the conducting path in the cell³⁶.

The other type of conducting path is an interface-type path, in which the resistive switching takes place at the interface between the metal electrode and the oxide (Fig. 2d). Using multilead resistance measurements on perovskite oxide cells, Baikalov *et al.* ¹⁸ have recently shown that the contact resistance between the metal electrode and the perovskite oxide changes upon the application of an electric field. This switching mechanism is usually related to the bipolar-type resistive switching behavior observed in semiconducting perovskite oxides. A number of models have been proposed for the driving mechanism in resistive switching involving an interface-type conducting path, such as electrochemical migration of oxygen vacancies ^{18,19,25,37,38,47}, trapping of charge carriers (hole or electron)^{21–23}, and a Mott transition induced by carriers doped at the interface ^{43–46}.

The difference between the filament and interface types of resistive switching can be understood by considering the area dependence of the cell resistance. As seen in Fig. 5, a cell composed of semiconducting Nb-doped SrTiO $_3$ has a resistance that is inversely proportional to the cell area, whereas that of an insulating NiO cell is much less dependent on cell area 27 . These results indicate that resistive switching in the Nb-doped SrTiO $_3$ cell takes place over the whole area of the cell, i.e. the entire interface, whereas switching occurs locally in the NiO cell through the formation of filamentary conducting paths.

The details of filament-type resistive switching have recently been reviewed by Waser and Aono⁴⁸. Therefore, we now focus on

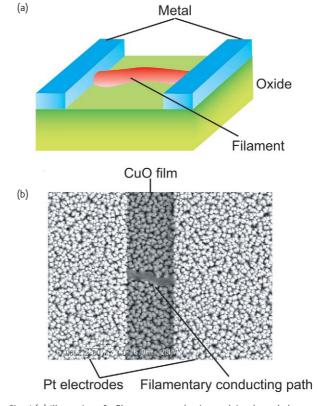


Fig. 4 (a) Illustration of a filamentary conducting path in a lateral planar configuration. (b) Scanning electron microscope image of a filamentary conducting path in a CuO film between Pt electrodes. (Courtesy of K. Fujiwara and H. Takagi, University of Tokyo.)

interface-type resistive switching and describe recent advances in our understanding of the mechanism obtained from research on metal/transition metal oxide junctions.

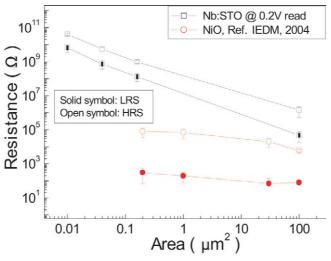


Fig. 5 Area dependence of resistance values in high and low resistance states for Nb-doped SrTiO₃ (Nb:STO) and NiO memory cells. The resistance of Nb:STO memory cells depends linearly on the area, suggesting that the resistive switching takes place over the entire area of the interface. The resistance of NiO memory cells is almost independent of the area, suggesting that resistive switching is a local phenomenon. (Reprinted with permission from²⁷. © 2005 IEEE.)

Origin of contact resistance

In order to elucidate the mechanism for interface resistive switching, it is first necessary to clarify the origin of the contact resistance, which can be changed by applying an electric field. Since the memory cell has a capacitor-like structure composed of insulating or semiconducting oxides sandwiched between metal electrodes, a Schottky barrier seems to be the most probable origin of the contact

resistance. The dependence of the interface transport properties of the memory cells on the electrode material can provide insight into this problem.

Fig. 6 shows I-V curves for $M/Pr_{0.7}Ca_{0.3}MnO_3/SrRuO_3$ (M/PCMO/SRO) and $M/SrTi_{0.99}Nb_{0.01}O_3/Ag$ (M/Nb:STO/Ag) cells. PCMO and STO are p- and n-type semiconductors that form the basic elements for resistive switching^{21,22}. M is the top electrode of Ti, Au, or SRO, with

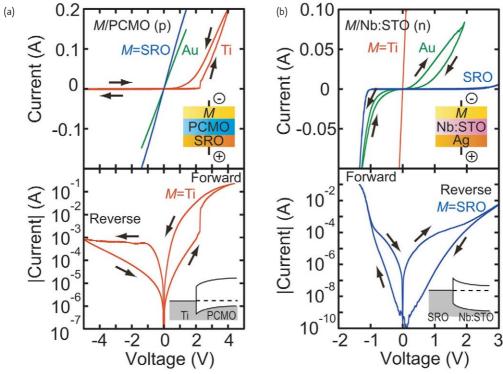


Fig. 6 I—V curves for (a) p-type M/PCMO/SRO cells and (b) n-type M/Nb:STO/Ag cells, where M = Ti, Au, and SRO. Rectification behavior is observed for Ti/PCMO/SRO, Au/Nb:STO/Ag, and SRO/Nb:STO/Ag cells. In addition to rectification, hysteretic behavior is also observed in these I—V curves, indicating resistive switching.

work functions of \sim 4.3 eV, \sim 5.1 eV, and \sim 5.3 eV, respectively. The SRO and Ag bottom electrodes serve as ohmic contacts to the PCMO and Nb:STO, respectively.

In p-type PCMO cells, as the work function of M decreases, the contact resistance between M and PCMO increases, and the Ti/PCMO interface shows rectification behavior in the I-V curves. In the case of n-type Nb:STO cells, the contact resistance between M and Nb:STO increases with an increase in the work function of M, and the Au/Nb:STO and SRO/Nb:STO interfaces show rectification behavior.

These work function dependences and rectifications can be understood as the formation of a Schottky-like barrier at the interface, as shown in the insets of the lower panels of Fig. 6. In addition to the rectification, *I–V* curves for Ti/PCMO, Au/Nb:STO, and SRO/Nb:STO interfaces exhibit hysteretic behavior indicative of resistive switching. However, the ohmic *I–V* curves for Au/PCMO, SRO/PCMO, and Ti/Nb:STO interfaces show no resistive switching. These results suggest that the Schottky-like barrier plays an important role in the onset of resistive switching. Furthermore, these experiments provide insight into the directionality of the switching. In the case of the resistive switching that appears at Schottky-like interfaces, the resistance state changes from HRS to LRS (LRS to HRS) when a forward (reverse) bias voltage is applied to the interface, as shown in the lower panels of Fig. 6.

Alteration of the potential profile in the depletion layer

The data in Fig. 6 suggest that the contact resistance originates in the Schottky-like barrier and is changed by applying voltage stresses. Since, in the conventional Schottky model, the amplitude of the contact resistance is attributed to the potential profile of the barrier, i.e. the depletion layer, we can expect different HRS and LRS potential profiles.

The potential profile of the depletion layer can be determined from a capacitance–voltage (C–V) curve. In the conventional Schottky model, the capacitance is given by $C = \epsilon_0 \epsilon_S S/W_d$, where W_d is the depletion layer width and is proportional to the square root of the applied voltage in the reverse bias region, ϵ_0 is the relative dielectric constant of a vacuum, ϵ_S is the relative dielectric constant of the semiconductor, and S is the cell area.

As seen in Fig. 7, the C-V curve for the Ti/PCMO interface shows hysteretic behavior, and C is larger in the LRS than in the HRS³⁹. This suggests that W_d is narrower in the LRS than in the HRS (Fig. 7). Thus, electrons possibly pass through the thin Schottky-like barrier via a tunneling process in the LRS, whereas the thick barrier in the HRS prevents tunneling. Electrochemical migration of oxygen vacancies in the vicinity of the interface is considered to be the driving mechanism for the change in W_d (Fig. 7), and the details are discussed later.

The active region for resistive switching

In the case of interface resistive switching, we can expect the switching characteristics to depend on the electronic properties in the vicinity of the interface. In fact, recent studies have demonstrated that modifying the electronic properties at the interface causes a change in the switching characteristics^{40,41}.

Fig. 8a shows I-V curves for Ti/Sm_{0.7}Ca_{0.3}MnO₃ (n unit cells)/ La_{0.7}Sr_{0.3}MnO₃/SRO (Ti/SCMO(n)/LSMO/SRO) cells. One unit cell of SCMO corresponds to a thickness of about 0.4 nm⁴⁰. In the cells, the SCMO and LSMO have an identical doping level, but SCMO (LSMO) is semiconducting (metallic) because of a narrow (wide) effective one-electron bandwidth^{49,50}.

The Ti/LSMO/SRO cell (n = 0) shows an almost ohmic I-V curve without hysteresis, indicating no resistive switching in the cell.

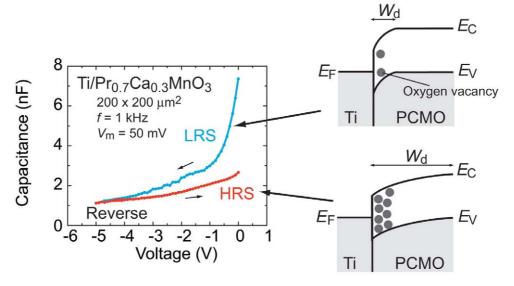


Fig. 7 C–V curves under reverse bias for a Ti/PCMO/SRO cell show hysteretic behavior. This indicates that the depletion layer width (W_d) at the Ti/PCMO interface is altered by applying an electric field. (Adapted with permission from 39 . © 2005 SPIE.)

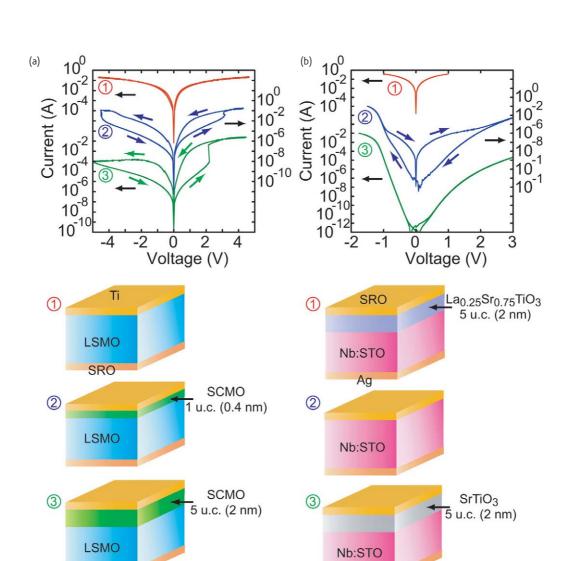


Fig. 8 Examples of interface-engineered resistive switching. (a) I-V curves for Ti/SCMO(n)/LSMO/SRO cells. The insertion of a thin semiconducting SCMO layer $(n \ge 1)$ between the Ti and LSMO layers induces resistive switching. (b) I-V curves for SRO/X/Nb:STO/Ag) cells, where X is heavily carrier-doped La:STO or pristine STO with a thickness of STO unit cells $(\sim 2 \text{ nm})$. Resistive switching is reversed with the insertion of thin La:STO and STO layers.

Since the cell can be regarded as a metal/metal/metal junction, a Schottky-like barrier, which plays an important role in resistive switching, cannot form at the interfaces. When thin semiconducting SCMO layers ($n \ge 1$) are inserted between the Ti and LSMO layers, the cells show rectification behavior in the I-V curves with hysteresis, suggesting that the semiconducting property within a few nanometers of the interface induces resistive switching. This result also indicates that a semiconducting manganite layer as thin as a few unit cells adjacent to the interface can give rise to resistive switching.

In addition to the conductivity of the oxides, the doping level, i.e. carrier concentration, in the vicinity of the interface plays an important role in resistive switching. Fig. 8b shows the change in the I-V curves for n-type SRO/Nb:STO/Ag cells as the doping level at the SRO/Nb:STO interface is modified⁴¹. To modify the doping level, SRO/X(2 nm)/

Nb:STO/Ag cells are prepared, where X is either undoped STO or very heavily doped La_{0.25}Sr_{0.75}TiO₃ (La:STO). The substitution of La³⁺ for Sr²⁺ provides electrons to the conduction band more effectively⁵¹ than substitution of Nb⁵⁺ for Ti⁴⁺.

The SRO/La:STO/Nb:STO junction shows quasi-ohmic behavior and no resistive switching. Because SRO/La:STO/Nb:STO can be regarded as a metal/ n^+/n junction, the Schottky barrier width in the vicinity of the interface is reduced. Thus, electrons can pass through the thin barrier via a tunneling process. The SRO/STO/Nb:STO cell shows rectification behavior in the I-V curve; however, it shows no hysteretic behavior. In this cell, the Schottky barrier width is expected to be wider, because there is no dopant (donor) in the STO layer. The results obtained in these experiments indicate the possibility that the switching characteristics can be optimized by modifying the interface.

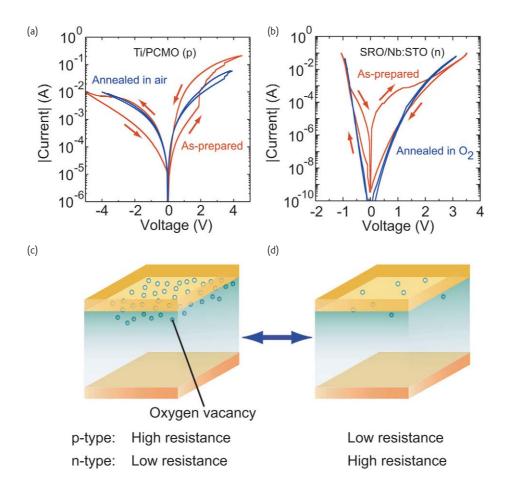


Fig. 9 I–V curves for (a) Ti/PCMO/SRO cells, and (b) SRO/Nb:STO/Ag cells. The as-prepared cells show hysteretic I–V characteristics, indicating resistive switching. Annealing in air and under an O_2 atmosphere (oxidative treatment) switches the p-type Ti/PCMO/SRO and n-type SRO/Nb:STO/SRO cells into a LRS and HRS, respectively. (c) Schematics of the changes in the oxygen vacancy density in the vicinity of the interface. The resistance states of the memory cells are possibly determined by the oxygen vacancy density.

The role of oxygen vacancies

To understand the origin of resistive switching definitively, the driving mechanism involved in the switching between two or more resistance states should be elucidated. Recent studies have indicated that the electrochemical migration of oxygen vacancies in the vicinity of the interface drives resistive switching 19,37,38,52. For example, oxidative treatment of memory cells has been shown to change the resistive switching properties 52.

Fig. 9 shows I-V curves for Ti/PCMO/SRO and SRO/Nb:STO/Ag cells. The as-prepared cells show hysteresis. After acquiring the I-V curves, the Ti/PCMO/SRO and SRO/Nb:STO/Ag cells were annealed at 400°C in air and an O_2 atmosphere, respectively. In the annealing process, the PCMO and Nb:STO layers are oxidized, i.e. the number of oxygen vacancies in the oxide layers is reduced. The annealed Ti/PCMO/SRO cells converted to a LRS and the SRO/Nb:STO/Ag cells converted into a HRS, and the hysteretic behavior (resistive switching) was suppressed.

In *p*-type oxide semiconductors, oxygen vacancies are considered to be an acceptor scavenger. Therefore, the reduction

in oxygen vacancies at the interfaces upon annealing may cause the depletion layer to become narrower in PCMO, resulting in a decrease in the contact resistance. On the other hand, since an oxygen vacancy acts as an effective donor in *n*-type oxide semiconductors, the reduction in the number of oxygen vacancies may cause the depletion layer to become wider in Nb:STO, resulting in an increase in the contact resistance. Almost full oxidation of the PCMO and Nb:STO layers may suppress the migration of oxygen vacancies (or oxygen ions), resulting in the suppression of resistive switching. Although these results are not definitive evidence for an electrochemical redox reaction, they do indicate that the number of oxygen vacancies plays an important role in the change in resistance.

ReRAM devices

One of the significant advantages of ReRAM is the potential for high-density memorys. The multilevel programming and cross-point memory structure, in which the memory cells have an area of about $4F^2$ (F is the minimum feature size on a given process) enable us to fabricate a high-density memory¹. Furthermore, multilevel stacking technology can increase the density⁶. To fabricate the cross-point memory structure, a diode has to be connected to a memory cell in series to prevent signal bypasses through 'ON'-state memory cells. A two-layer 4 x 5 cross-point memory array employing NiO memory cells combined with oxide-based p-n diodes has been

The critical issues for the future development of ReRAM devices are reliability, such as data retention and memory endurance (the number of erase and program cycles), and the characteristic variation from cell to cell and from chip to chip. A data retention time over 10 years can be extrapolated from retention characteristics measured at high temperatures^{27,53,54}, and a memory endurance of over 10⁶ cycles has been demonstrated for a NiO memory cell². These reported characteristics seem to be enough for an alternative to Flash memory. However, little data about the characteristic variation has been reported, and an integrated circuit ReRAM memory consisting of a sufficient number of cells to be practical has not yet been demonstrated. Therefore, a statistical study on reliability is essential for the future development of ReRAM.

Summary

A deep understanding of the driving mechanism for resistive switching is required in order to optimize ReRAM device characteristics and develop guidelines for scaling, reliability, and reproducibility. Recent studies indicate that a thermal or electrochemical redox reaction in the vicinity of the interface between the oxide and the metal electrode is a plausible mechanism for resistive switching. However, further research from chemical, electronic, and crystallographic viewpoints is needed to elucidate definitively a 'microscopic' mechanism, because the chemical, electronic, and crystallographic properties of the oxides, as well as the metal electrodes, affect the mechanism. We believe that, by taking into account the differences in each type of resistive switching, tailoring materials to specific applications will become a major area in the future development of ReRAM.

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