Supporting Information

Nanoscale Memristor Device as Synapse in Neuromorphic Systems

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Memristor fabrication

The memristor device consists of a bottom tungsten nanowire electrode, a sputtered silicon layer (2~4 nm), a PECVD (plasma enhanced chemical vapor deposition) deposited amorphous silicon (a-Si) layer (2.5-4.5 nm), a co-sputtered silver and silicon layer (20-30 nm thick) and a top chrome/platinum nanowire electrode as schematically illustrated in Figure 1a in the main text. The bottom

tungsten nanowire electrode was fabricated by e-beam lithography, mask layer lift-off, and RIE (reactive ion etching). Following that, the a-Si deposition, co-sputtering and top metal lift-off processes were performed, followed by another RIE step to remove the co-sputtered layer outside the cross-point regions defined by the of top and bottom electrodes. Memristors of device size of 500 nm × 500 nm were used in Figure 1, 2, 4 in the main text; memristors of device size of 100 nm × 100 nm were used to obtain the STDP data in Figure 3 in the main text.

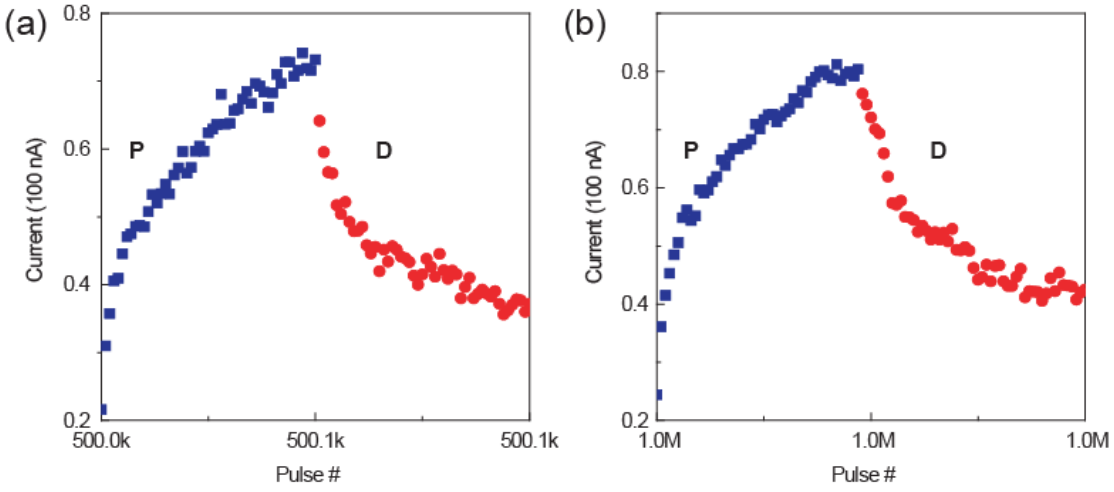

Figure S1. Response of the memristor device after 5.0×10^5 P/D pulses (a) and 1.0×10^6 P/D pulses. In each test, 3. V, 500 μs potentiating pulses, -2.6 V, 500 μs depressing pulses and 1 V, 2 ms read pulses were used. After each programming pulse, the device conductance was measured by a read pulse and recorded.

Neuron Circuits

The neuron circuit involves a mixed analog-digital design. Time Division Multiplexing (TDM) – events occur at their prescribed time periods – is used in this design[1]. Timeslots are used to organize communication between the neurons. This system is compatible with digital systems in which a global clock is used to synchronize communication and thereby instill a greater external control over the neurons. Three timeslots are used in this design and are explained further with the aid of Figure S2 which shows the spiking characteristics of a neuron as well as the use of TDM.

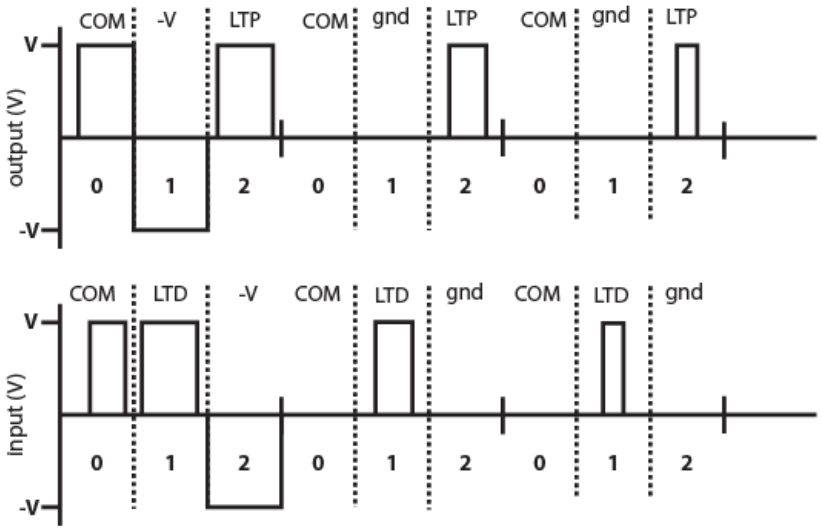

Figure S2. A generic neuron's spiking characteristics.

On the output side of the neuron, the three timeslots are 0 (Communication), 1 (Response), and 2 (LTP). In the Communication (COM) timeslot, the neuron can give out a spike signal with a voltage amplitude *V*. The amplitude *V* is chosen to be between $V_T/2$ and V_T so that a single LTP or LTD pulse will not change the memristor

synaptic weight but a simultaneous application of either an LTP and a $-V$ pulse or an LTD and a V pulse across the memristor will. The COM timeslot signifies the only time when the neuron can spike or declare it has spiked. In the Response (gnd, -V) timeslot, if the neuron spikes, then the output of the neuron goes to a voltage of $-V$. If the neuron does not spike, then the output goes to or remains at a ground potential. In the LTP timeslot, the neuron gives pulses of decaying width for the next frames. Each frame is three timeslots long labeled 0, 1, and 2 as depicted in Figure S2. The number of frames of decaying pulses depends on the characteristic of the neuron. On the input side of the neuron, the three timeslots are similar, but 0, 1, and 2 correspond to COM, LTD, and Response. The COM timeslot represents when the input of the neuron can vary based on the current being received through the memristor. LTD and Response behave similarly to LTP and Response on the output side. Combining the output of a pre-neuron to the input of a post-neuron would yield results depicted in Figure S3.

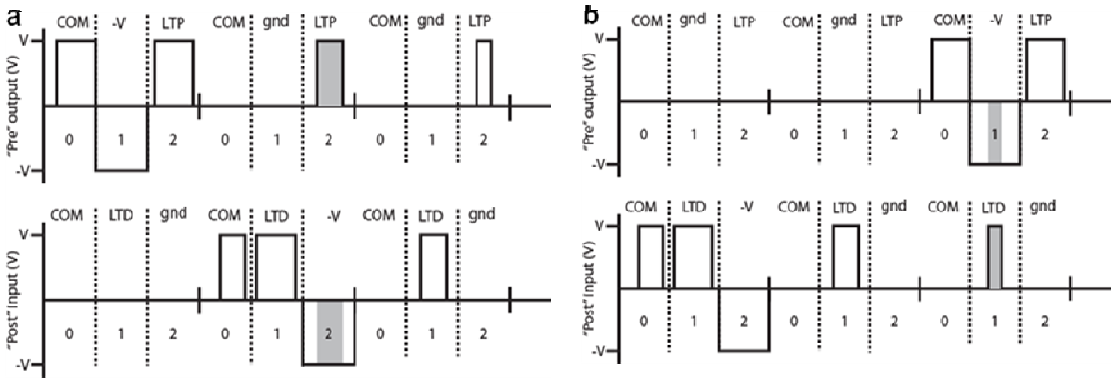

Figure S3. Two spiking situations showing the timeslots where synaptic change occurs. **(a)** Potentiation: the post-synaptic neuron spikes 1 frame after the pre-synaptic neuron. **(b)** Depression: the post-synaptic neuron spikes 2 frames before the pre-

synaptic neuron. The shaded regions represent the time duration where the voltage across the memristor synapse is larger than V_T.

In Figure S3a, the post-synaptic neuron ("Post") spikes a frame after the pre-synaptic neuron ("Pre") spikes, so this entails potentiation. During timeslot 2 of this frame, the "Pre" goes to $+V$ while the "Post" goes to $-V$ so the effective voltage across the memristor will be $+2V$ which is enough to change the conductance of the memristor. The time the memristor is exposed to this above threshold voltage is shown in gray in Figure S3a. In Figure S3b, a similar spiking scenario is shown, except this scenario shows depression when the "Pre" spikes two frames after the "Post". The effective voltage in gray is $-2V$ and for a shorter amount of time than shown in Figure S3b. Using the TDM concept, a neuron circuit was built with discrete components and an FPGA to test the writing and erasing of a memristor and obtain the STDP curve.

Figure S4 depicts the neuron architecture used to obtain the I/O behavior shown Figure S2.

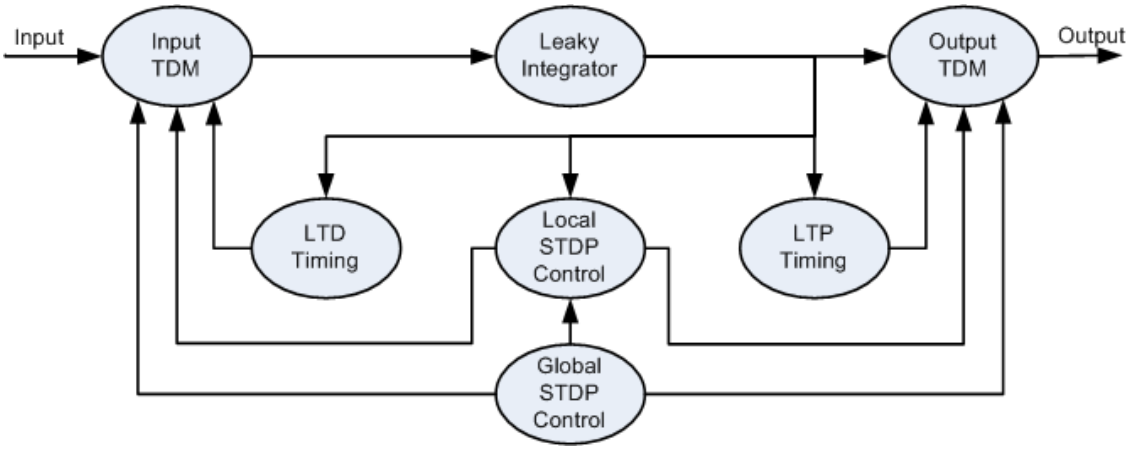

Figure S4. Overall neuron architecture grouped by components.

The input to the neuron system is a current – assuming a memristor is connected directly to the input of the neuron. The Input TDM is essentially a demux that allows the input current, LTD voltage, or the $-V$ voltage to pass at each appropriate timeslot. The leaky integrator integrates the input current, and once threshold is reached, sends out a spike signal to activate the LTP/LTD pulses and set the appropriate local controls. The Local STDP control sets the control signal for passing $-V$ at the appropriate timeslot whenever the leaky integrator gives out a spike signal. The Global STDP control sets the individual timeslots for each frame and gives the designer auxiliary inputs to the neuron. Both the Local and Global STDP controls were implemented on an Altera DE1 Development board while the other components were realized on a breadboard using off-the-shelf components. Eight time frames were used during each neuron spike. Figure S5 shows the pulse widths of the potentiating and depressing pulses generated by the CMOS neuron circuit as a function of the relative timing Δt of the neuron spikes. The exponentially decreasing potentiating or depressing pulses are applied across the memristor synapse to achieve the desired synaptic changes.

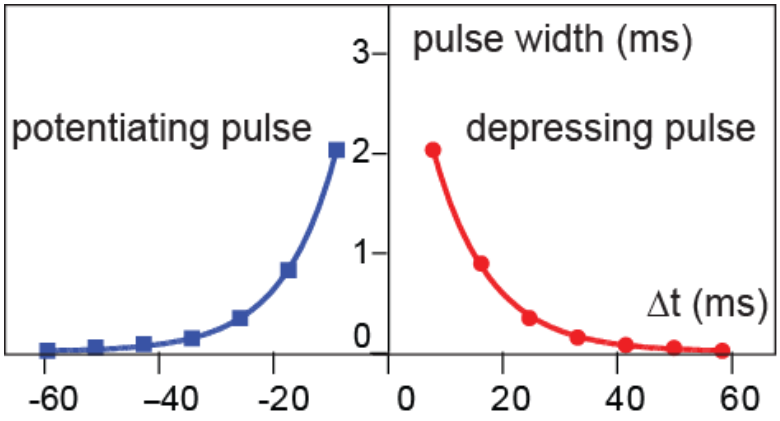

Figure S5. Pulse widths of the potentiating and depressing pulses generated by the CMOS neuron circuit.

References

(1) Snider, G. S. *2008 IEEE/ACM International Symposium on Nanoscale Architectures*, pp 85-92.