CSC258 PRELAB #4

Tingfeng Xia

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PART I

1. Here is my logic gate level schematic

4. To avoid uncertainty, we shall avoid any case where $Clk \leftarrow 0$ at initial state. Since D is unspecified, the behavior of the circuit can be unpredictable.

PART II

1. Here is my code for RegisterALU:

2. Here are the screen shots for the simulations:

PART III

1. If `load_n = 1` and `ShiftRight = 0`, then the register remains unchanged during the entire process. Since `ShiftRight` is connected to the `shift` input of each ShifterBit and this essentially feed back the register with its own value.