Fall, 2025
Week 2
2025.09.08

組別：_____ 簽名：_____

[group13]

1. Two processors P1 and P2 implement the same ISA and run at the same clock rate. Instructions are divided into four classes (I, J, K, L). Their CPIs are as follows:
   - **P1:** I = 1, J = 3, K = 3, L = 5
   - **P2:** I = 2, J = 2, K = 2, L = 2

   A certain program's instruction mix is:
   - 25% I, 25% J, 40% K, 10% L.

   Which processor delivers better performance?

P1 = 0.25 + 0.75 + 1.2 + 0.5
= 2.7

P2 = 0.5 + 0.5 + 0.8 + 0.2
= 2

win

Ans:
Since both processors have the same clock rate, we only need to compare their average CPI.
Average CPI of P1:
CPI=1×0.25+3×0.25+3×0.40+5×0.10=0.25+0.75+1.2+0.5=2.7
Average CPI of P2:
CPI=2×(0.25+0.25+0.40+0.10)=2×1.0=2.0
Conclusion: P2 has better performance (lower CPI = 2.0 vs. 2.7).

[group13]

2. Why does MIPS need to include immediate instructions?

Ans:
The design of immediate instructions in MIPS is motivated by the fact that small constants appear very frequently in programs (about 50% of the operands). If these constants were always loaded from memory, performance would suffer. By embedding constants directly in the instruction, operations can be executed faster, which follows the design principle of "Make the common case fast."

[group3]

3. 用 MIPS(millions of instructions per second)來判斷處理器的 performance 不一定是個準確的方式，請判斷以下兩個處理器，誰有較大的 MIPS？誰有較好的 performance？

- P1: clock rate: 4 GHz, average CPI: 0.9, requires $5 * 10^9$ instructions
- P2: clock rate: 3 GHz, average CPI: 0.75, requires $1 * 10^9$ instructions

Ans:

MIPS = $\frac{clock\ rate}{CPI * 10^6}$ = Cycles Per Second

P1: $\frac{4 * 10^9}{0.9 * 10^6} = 4444.4\ MIPS$

P2: $\frac{3 * 10^9}{0.75 * 10^6} = 4000\ MIPS$

Performance (Execution Time)

$\frac{Instructions * CPI}{clock\ rate}$

P1: $\frac{5 * 10^9 * 0.9}{4 * 10^9} = 1.125s$

P2: $\frac{1 * 10^9 * 0.75}{3 * 10^9} = 0.25s$

MIPS: P1 > P2

Performance P2 better than P1

P1 = $\frac{4 \times 10^9}{0.9 \times 10^6}$ = 4444.4 MIPS win MIPS

P2 = $\frac{3 \times 10^9}{0.75 \times 10^6}$ = 4000 MIPS

P1 = $\frac{0.9 \times 5 \times 10^9}{4 \times 10^9}$ = 1.125 s

P2 = $\frac{0.75 \times 1 \times 10^9}{3 \times 10^9}$ = 0.25 s win performance

[group 4]

4. Assume the base address of integer array A is stored in register $s0 and integer variables b, c are assigned to register $s1, $s2. **Translate the following C code into MIPS:**

   b = 3;

   A[--b] = c++;

Ans:

```
addi $s1, $zero, 3 # b = 3
addi $s1, $s1, -1 # --b
add $t0, $s1, $s1 # t0 = b*2
add $t0, $t0, $t0 # t0 = b*4
add $t0, $t0, $s0 # t0 = &A[b]
sw $s2, 0($t0) # A[b] = c
addi $s2, $s2, 1 # c++
```

```
addi $s1, $zero, 3 # s1 = b = 3
addi $s1, $s1, -1
add $t0, $s1, $s1 # t0 = bx2
add $t0, $t0, $t0 # t0 = bx4
add $t0, $s0, $t0 # t0 = &A[b]
sw $s2, 0($t0)
addi $s2, $s2, 1
```

[group 4]

5. Assume that variables f, g, and h are assigned to registers $s0, $s1, and $s2, respectively. The base addresses of arrays A and B are stored in $s3 and $s4, respectively. **Translate the following MIPS code into C:**

1. add $t0, $s2, $s2
2. add $t0, $t0, $t0
3. add $t0, $s3, $t0
4. lw $t1, 0($t0)
5. add $t1, $t1, $s1
6. add $t2, $t1, $t1
7. add $t2, $t2, $t2
8. add $t1, $s4, $t2
9. sw $s0, 4($t1)

1. h x 2
2. t0 = h x 4
3. t0 = &A[h]
4. t1 = A[h]
5. t1 = A[h] + g
6. t2 = 2 x (A[h] + g)
7. t2 = 4 x (A[h] + g)
8. t1 = &B[A[h] + g)
9. B[A[h] + g] = f

f = $s0
g = $s1
h = $s2
A[] = $s3
B[] = $s4

Ans:

B [A[h] + g + 1] = f;

one more 4byte offset in 9.

[group 5]

6. Why are there 32 registers in MIPS architecture instead of more?

Ans:

Because of design principle 2: "Smaller is faster."

[group 11]

7. What are three fundamental design principles of instruction set architecture (ISA)? Additionally, which principle explains why MIPS uses only 32 registers?

Ans:

- simplicity favors regularity
- smaller is faster
- make the common case fast

[group 11]

8. According to Amdahl's Law, suppose there is a model where 75% of the execution time can be optimized. By how much must we speed up the optimizable portion in order to double the overall system performance?

Ans: 3

25 + 75 (optimizeable) ⇒ 25 + 25 ⇒ 75/25 = 3

[group 10]

9. Transfer the following C code to MIPs Code:

   a = (b - c) + (d - e)

Ans:

Sub t0, b, c

Sub t1, d, e

Add a, t0, t1

sub $t0, b, c
sub $t1, d, e
add a, $t0, $t1

[group 10]

10. What is Instruction Set Architecture (ISA)? What is its value?

Ans:

ISA is the interface between the processor and software, defining the instruction set and execution rules. In the early days of computing, machines could only handle fixed tasks. ISA made computers more flexible by translating computations into program instructions, similar to today's assembly language.

[group 7]

11. Explain Amdahl's Law and calculate the maximum speedup of a program that is 40% serial and 60% parallelizable. Why does the speedup have a limit even with infinite processors?

Ans:

Amdahl's Law: $S(N) = \frac{1}{(1-P)+\frac{P}{N}}$, note: $N\ is\ \#\ Processor, P = 0.6,\ S(N) = Speedup\ for\ N - Processor$

加速倍數 可加速部份

$$\lim_{N\to\infty} S(N) = \frac{1}{(1-0.6)+\frac{0.6}{N}} = \frac{1}{0.4} = 2.5$$

不可加速部份

趨近0

Max speedup for 40% serial and 60% parallel program is 2.5X.