Midterm Project Report

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 Questions (Brief and concise explanation of one to two pages would be enough. You may use Chinese.)

 How do you design your accelerator? Please draw the FSM and block diagram to explain the overall architecture. (2%)

Ans:

依序經過 WAIT、READ、LENET、WRITE、DONE 五個 state

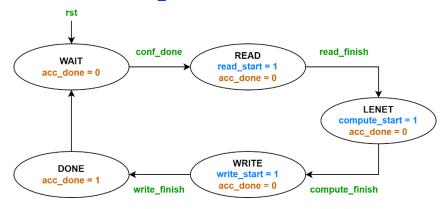
WAIT: 等待 conf done 變為 1

READ: dma read 將資料由 DRAM 讀入 SRAM

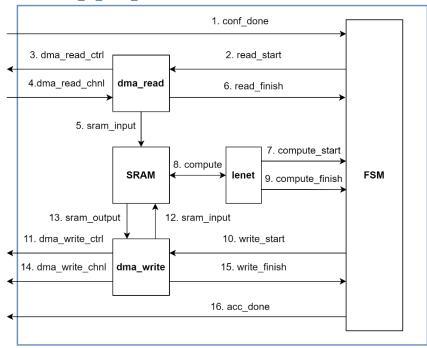
LENET: lenet 進行運算,從 SRAM 讀出所需資料,算完後再寫回 SRAM

WRITE: dma write 將資料由 SRAM 寫入 DRAM

DONE: 結束,將 acc done 變為 1



lenet_rtl_basic_dma64



 How do you design your DMA controller interface to transfer data? Please draw the block diagram and FSM. (2%)

Ans:

分為 dma_read 與 dma_write 兩個 module

dma read :



How do you build two SRAMs in this project? Please draw the block diagram.(2%)
 Ans:

SRAM_activation_1024x32b 由 4 個 BRAM_2048x8 組成。

SRAM_weight_16384x32b 由 4 個 BRAM_8x2048x8 組成, BRAM_8x2048x8 則由 8 個



 Please briefly explain why we write images from mem[20000] to mem[20255], but read images from address 10000 to address 10127 in the accelerator? (2%)
 Ans:

software 的 data width 為 32-bit,DMA 的 data width 則為 64-bit,因此讀取位址的算法為 [20000/2]~[20255/2]。

• What is the function of the following code? (1%)

```
iowrite32(dev, LENET_SCALE_CONV2_REG, scale_CONV2);
iowrite32(dev, LENET_SCALE_CONV3_REG, scale_CONV3);
iowrite32(dev, LENET_SCALE_CONV1_REG, scale_CONV1);
iowrite32(dev, LENET_SCALE_FC2_REG, scale_FC2);
iowrite32(dev, LENET_SCALE_FC1_REG, scale_FC1);
```

Ans:

將各層的 scale 寫入 register 中。

What is the function of the following code? Please explain line by line (1%)

```
done = 0;
while (!done) {
    done = ioread32(dev, STATUS_REG);
    done &= STATUS_MASK_DONE;
}
iowrite32(dev, CMD_REG, 0x0);
```

Ans:

先把 done 設為 0,當 done 為 0 時,進入 while loop,讀出 STATUS_REG 的值並& STATUS_MASK_DONE,取出 done 的值;當 done 不為 0 時,跳出 while loop,將 CMD REG 寫入 0。

Result

Item	Description	Unit
RTL simulation	PASS	

- 3. Others (optional)
 - Suggestions or comments about this class to teacher or TA.