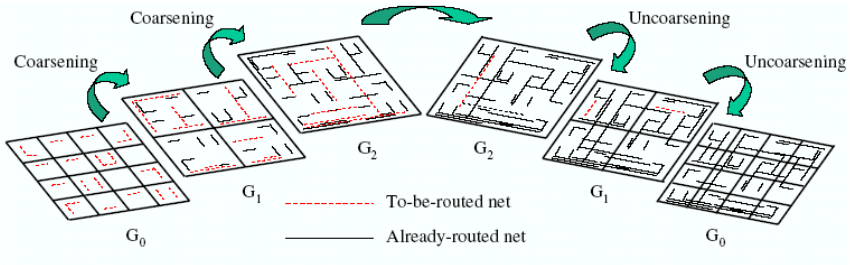
Multilevel Full-Chip Routing Framework

- Lin and Chang, "A novel framework for multilevel routing considering routability and performance," ICCAD'02 (TCAD, 2003).
- Multilevel framework: coarsening followed by uncoarsening.
- Coarsening (bottom-up) stage:
  - Constructs the net topology based on the minimum spanning tree.
  - Processes routing tiles one by one at each level, and only local nets (connections) are routed.
  - Applies two-stage routing of global routing followed by detailed routing.
  - Uses the L-shaped & Z-shaped pattern routing.
  - Performs resource estimation after detailed routing to guide the routing at the next level.
- Uncoarsening (top-down) stage
  - Completes the failed nets (connections) from the coarsening stage.
  - Uses a global and a detailed maze routers to refine the solution.

A Multilevel Full-Chip Routing Framework

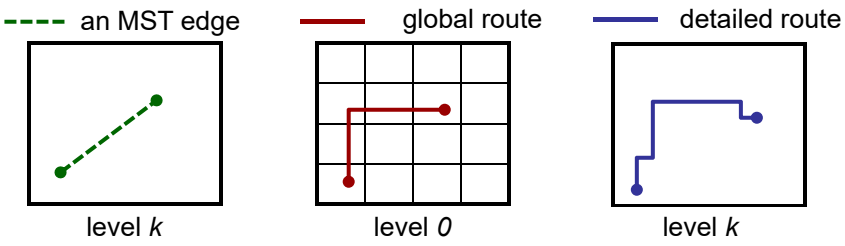


Perform global routing and A*-search (or Dijkstra's) shortest path detailed routing for local connections and then estimate routing resources for the next level

Use global maze routing and A*-search (or Dijkstra's) shortest path detailed routing to reroute failed connections and refine the solution.

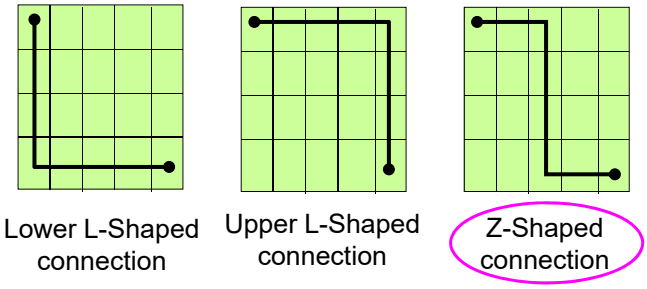
Coarsening Stage

- Build MSTs for all nets and decompose them into two-pin connections.
- Route **local nets (connections)** from level 0.
  - Two-stage routing (global + detailed routing) for a local net.



Global Routing

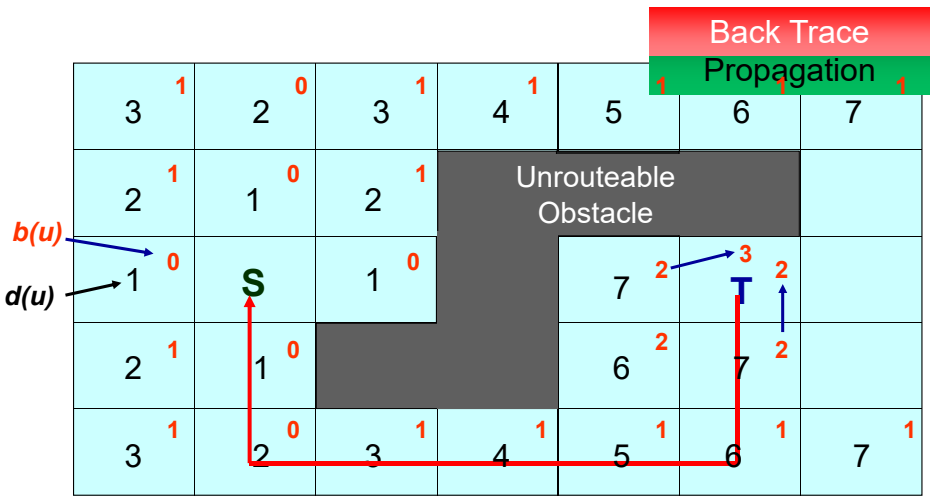
- Apply pattern routing for global routing
  - Use L-shaped and Z-shaped connections to route nets.
  - Has lower time complexity than maze routing.



Detailed Routing

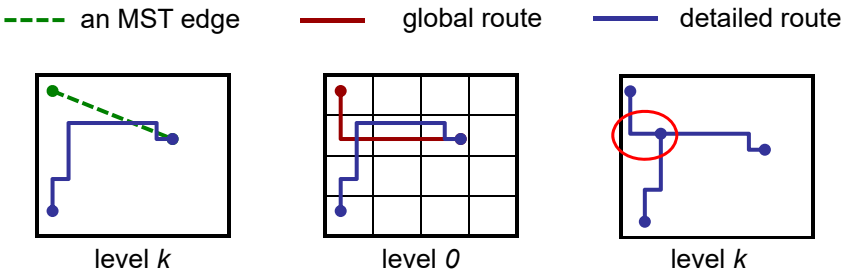
- Via minimization
  - Modify the maze router to minimize the number of bends.
- Local refinement
  - Apply general maze routing to improve the detailed routing results.
- Resource estimation
  - Update the edge weights of the routing graph after detailed routing.

Via Minimization



Local Refinement

- Local refinement improves detailed routing results by merging two connections which are decomposed from the same net.



Resource Estimation

- Global routing cost is the summation of congestions of all routed edges.
- Define the congestion, C_e, of an edge e by

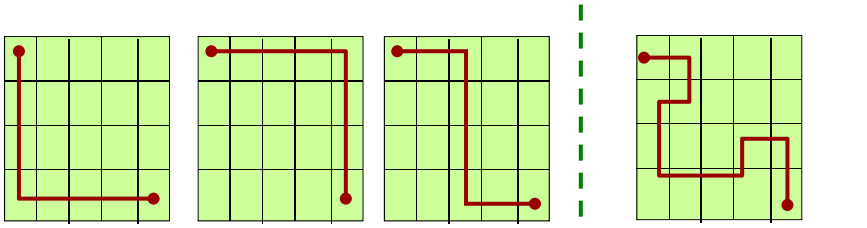
$$C_e = \frac{1}{2^{(p_e - d_e)}},$$

where p_e and d_e are the capacity and density, respectively.

- Update the congestion of routed edges to guide the subsequent global routing.

Uncoarsening Global Routing

- Use maze routing.
- Iterative refinement of a failed net stops when a route is found or several tries have been made.



Routing Comparisons

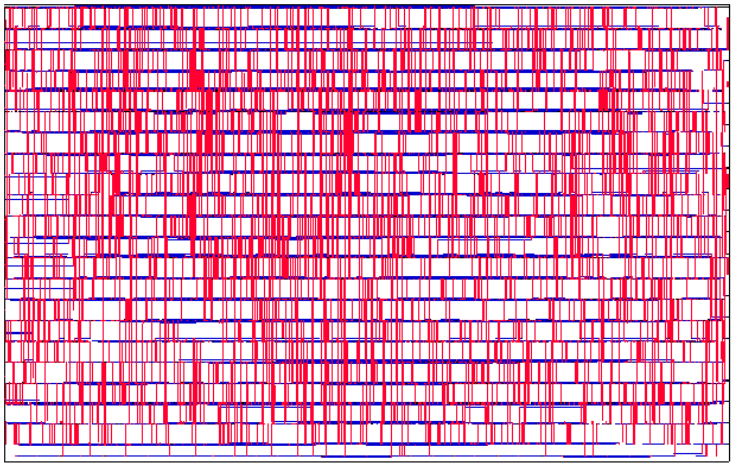
- 100% routing completion for all (11) benchmark circuits
  - Three-level routing: 0 completion (ISPD'2K)
  - Hierarchical routing: 2 completions (ICCAD' 01)
  - Previous multilevel routing: 2 completions (ICCAD' 01)
- Can complete routings using even fewer routing layers.

Ex.	#Layers	(A) Three-Level Routing			(B) Hierarchical Routing with Ripup and Replan			(C) Results of [9]			(D) Our Results		
		Time(s)	#Rtd. Nets	Cmp. Rates	Time(s)	#Rtd. Nets	Cmp. Rates	Time(s)	#Rtd. Nets	Cmp. Rates	Time(s)	#Rtd. Nets	Cmp. Rates
Mcc1	4	933.2	1499	88%	947.9	1600	94.5%	436.7	1683	99.4%	204.7	1694	100%
Mcc2	4	12333.6	5451	72.3%	10101.4	7161	95.6%	7644.8	7474	99.1%	7203.3	7541	100%
Struct	3	406.2	3530	99.4%	324.5	3551	100%	316.8	3551	100%	151.5	3551	100%
Prim1	3	239.1	2018	99.0%	353.0	2037	100%	350.2	2037	100%	165.4	2037	100%
Prim2	3	1331	8109	98.9%	2423.8	8194	100%	2488.4	8196	100%	788.2	8197	100%
S5378	3	430.2	2607	83.4%	57.9	2964	94.9%	54.0	2963	94.8%	10.9	3124	100%
S9234	3	355.2	2467	88.9%	40.7	2564	92.4%	41.0	2561	92.3%	7.7	2774	100%
S13207	3	1099.5	6118	87.5%	161.9	6540	93.5%	188.8	6574	94.0%	38.2	6995	100%
S15850	3	1469.1	7343	88.2%	426.1	7874	94.6%	403.4	7863	94.5%	57.5	8321	100%
s38417	3	3560.9	19090	90.8%	754.6	19596	93.2%	733.6	19636	93.3%	137.6	21035	100%
S38584	3	7086.5	25642	91.0%	1720	26461	93.9%	1721.6	26504	94.1%	316.7	28177	100%
avg.				89.8%			95.7%			96.5%			100%

Table 3: Comparison among (A) the three-level routing [10], (B) the hierarchical routing [9], (C) the multilevel routing [9], and (D) our multilevel routing. Note: (A),(B),(C) ran on a 440 Mhz Sun Ultra-5 with 384 MB memory, (D) ran on a 450Mhz Sun Sparc Ultra-60 with 2GB MB.

Routing Solution for Prim2

- 0.18um technology, pitch = 1 um, 8109 nets.
- Two layers, 100% routing completion.



Summary: Routing

- Hierarchical and multilevel are keys to handle large-scale routing problems.
- Routing frameworks: go parallel??
  - Λ-shaped routing: ICCAD'02 (TCAD-03); ASP-DAC'05 (TCAD-07)
  - V-shaped routing: ASP-DAC'06
  - Two-pass bottom-up routing: DAC-06 (TCAD-08)
- Routing considerations for nanometer technology
  - Noise (crosstalk) & electro-migration constraints
  - Buffer insertion for timing optimization
  - DFM routing: antenna effect, redundant via, OPC (optical proximity correction)[DAC'08], CMP (chemical mechanical polishing) [ISPD'13], double/multiple patterning [DAC'14], e-beam [DAC'13], EUV (extreme ultraviolet lithography), directed self-assembly (DSA) [ICCAD'16, DAC'23], etc.
- Machine-learning-based routing
- Package/PCB routing