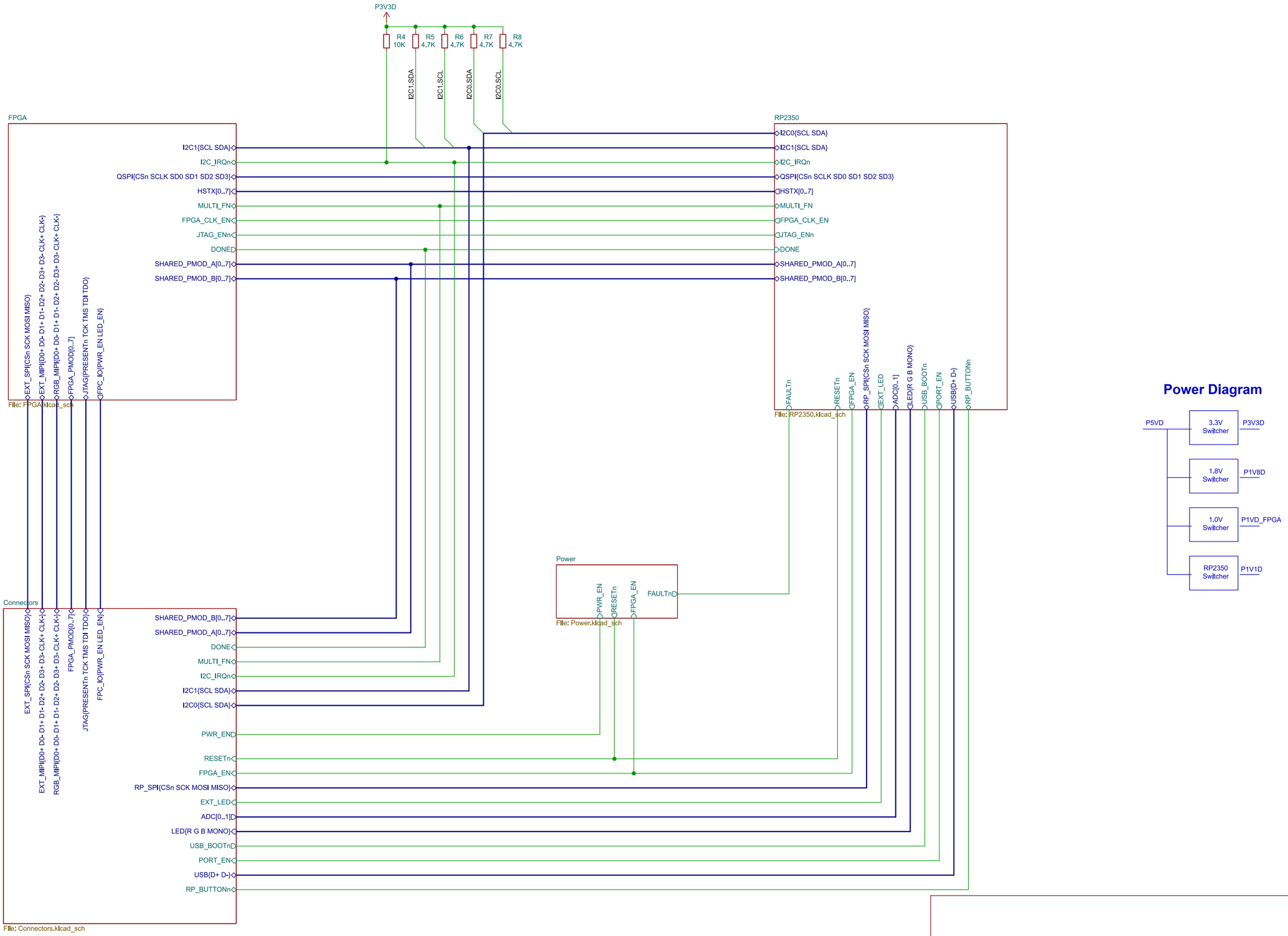

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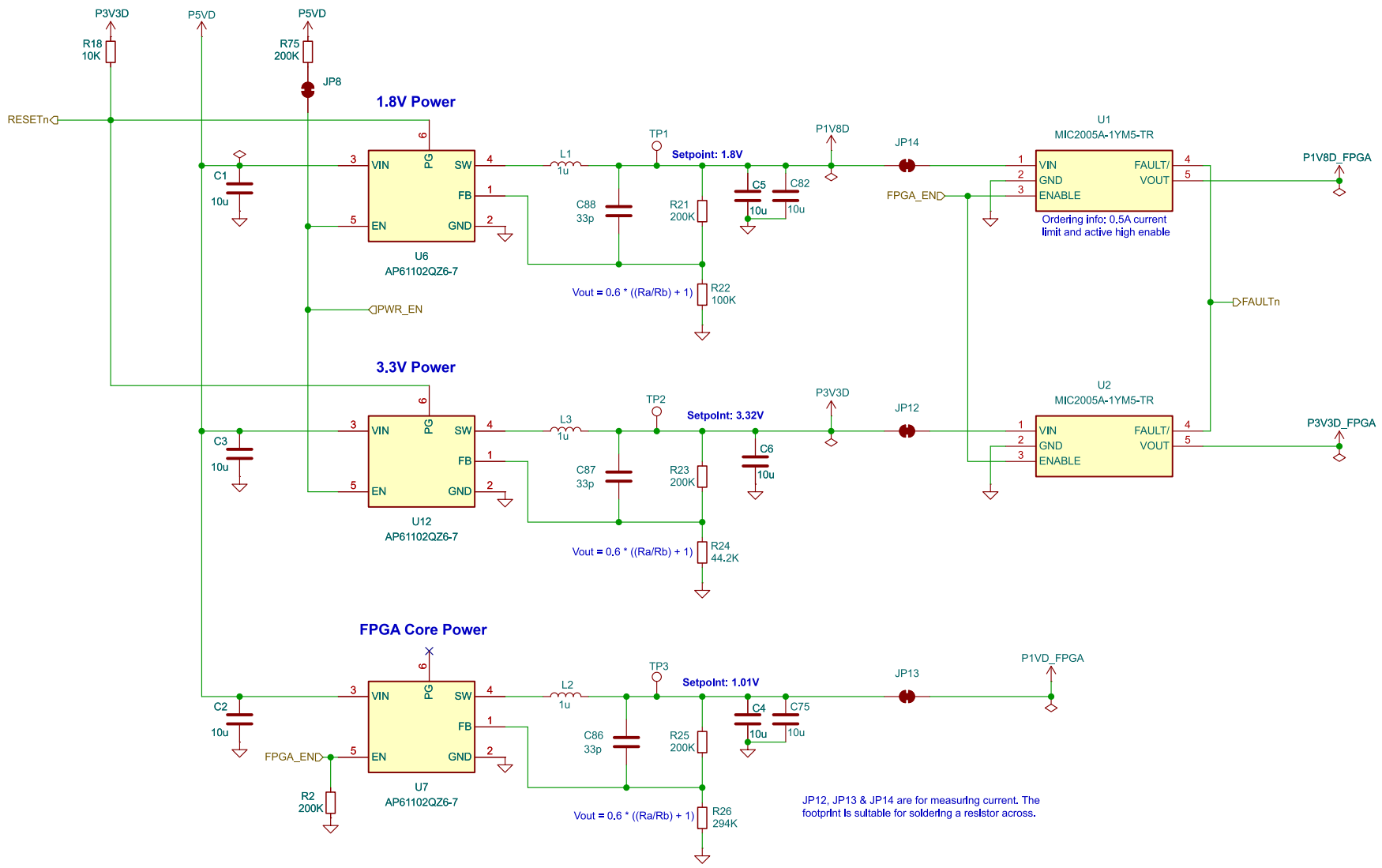
Sheet: /

File: pico2-nx.kicad_sch

Title: PICO2-NX

Size: A3	Date: 2025-06-03	**Rev: 0.1**
KiCad E.D.A. 8.0.4		Id: 1/5



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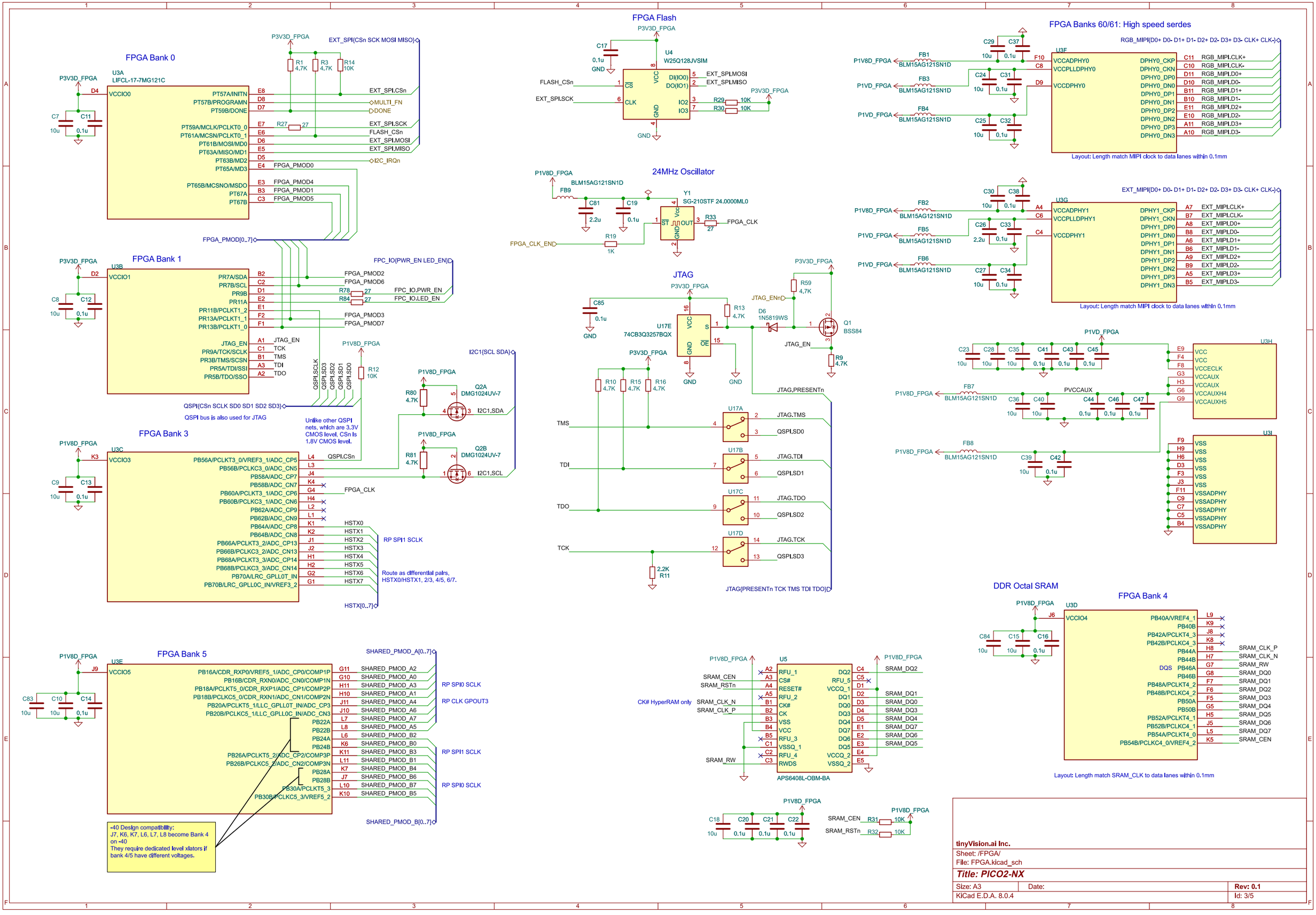
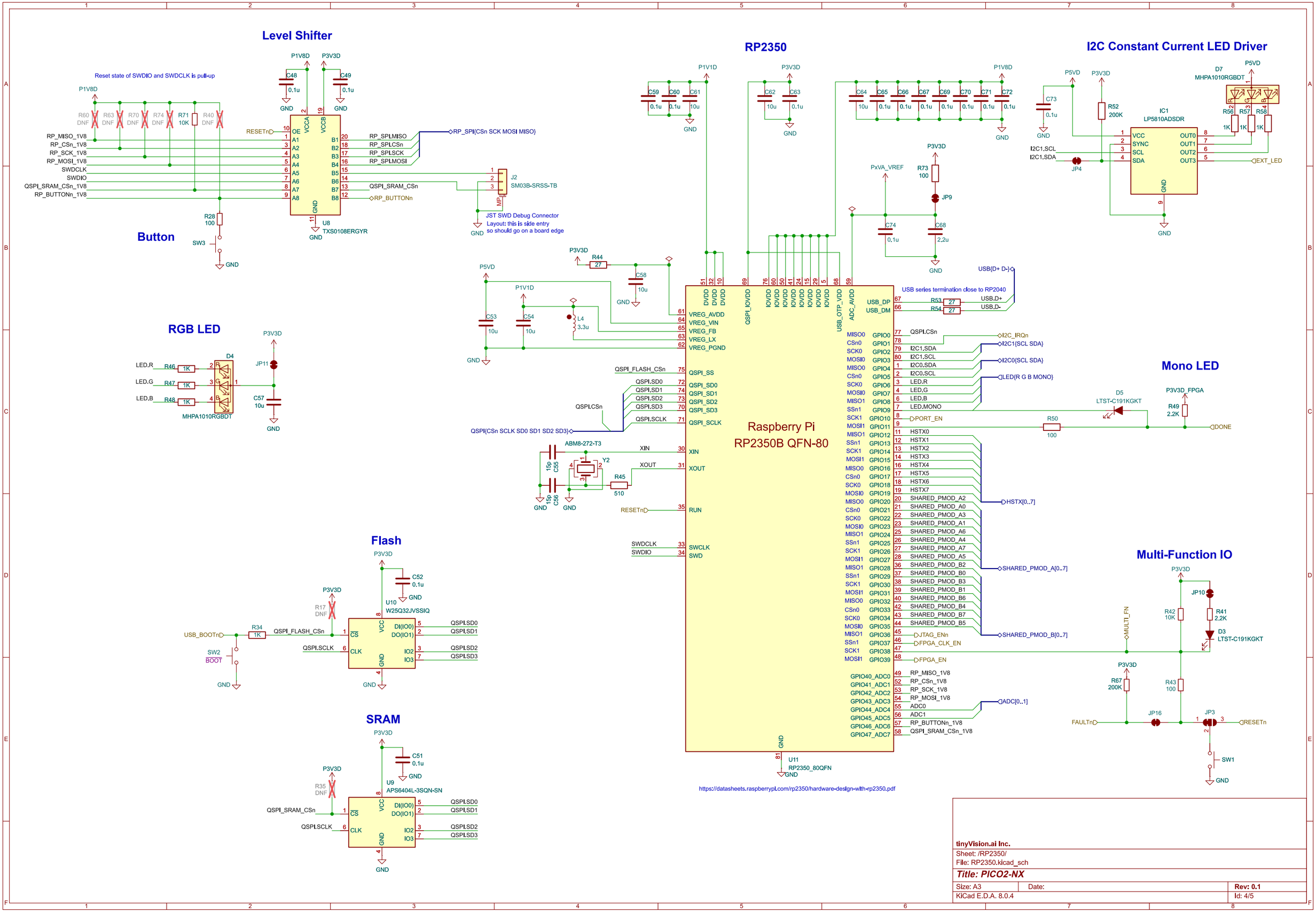
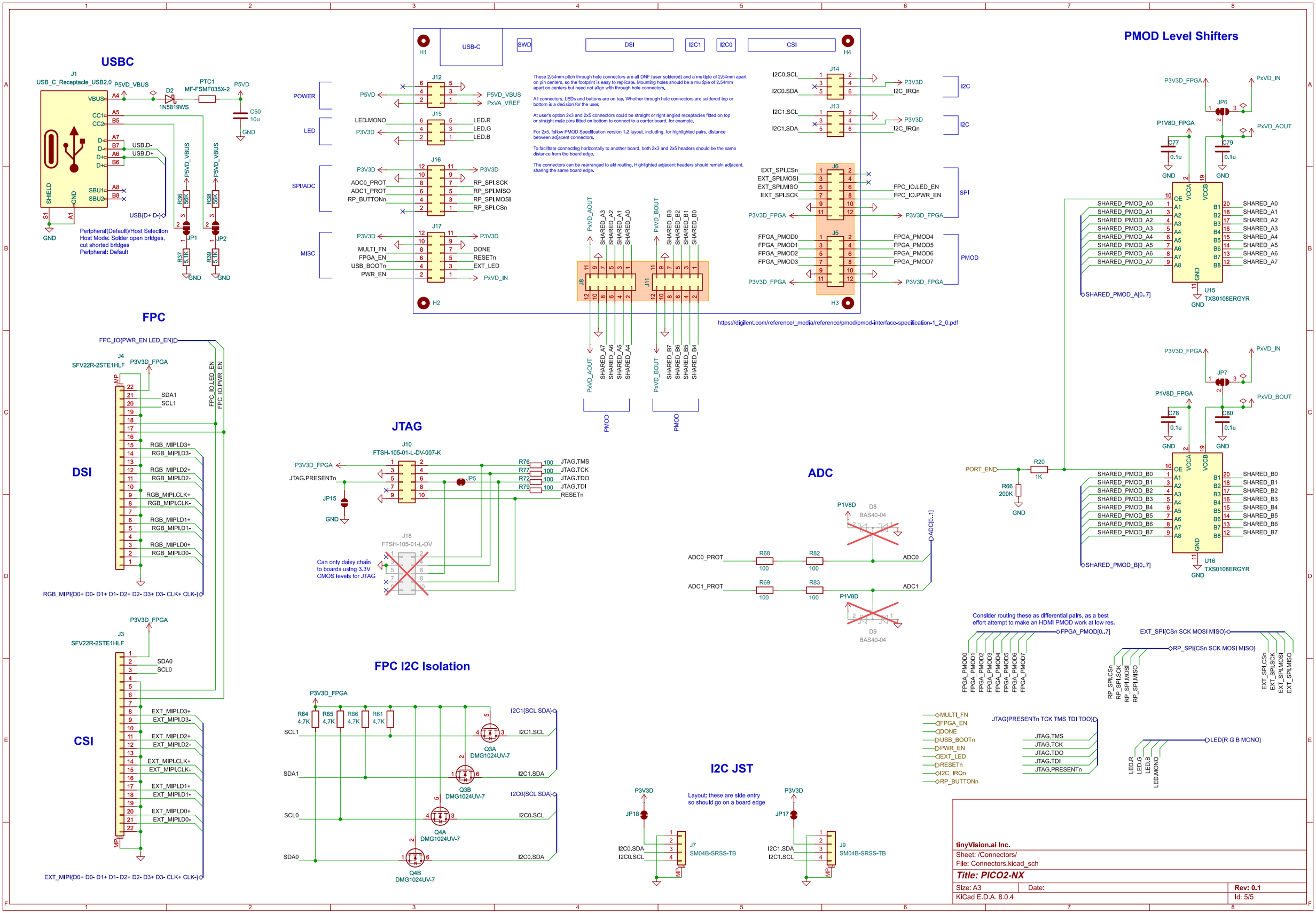
Sheet: /Power/
File: Power.kicad_sch

Title: PICO2-NX

Size: A4	Date:	**Rev: 0.1**
KiCad E.D.A. 8.0.4		Id: 2/5


FPGA Bank 0
U3A
LIFCL-17-7MG121C
FPGA Bank 1
U3B
FPGA Bank 3
U3C
FPGA Bank 5
U3E
FPGA Flash
U4
W25Q128JVSIM
24MHz Oscillator
Y1
SG-210STF 24.0000ML0
JTAG
U17E
74CB3Q3257BQX
Q1
BSS84
Q2A
DMG1024UV-7
Q2B
DMG1024UV-7
FPGA Banks 60/61: High speed serdes
U3F
Layout: Length match MIPI clock to data lanes within 0.1mm
U3G
Layout: Length match MIPI clock to data lanes within 0.1mm
U3H
U3I
DDR Octal SRAM
U5
APS6408L-OBM-BA
FPGA Bank 4
U3D
Layout: Length match SRAM_CLK to data lanes within 0.1mm
QSPI bus is also used for JTAG
Unlike other QSPI nets, which are 3.3V CMOS level, CSn is 1.8V CMOS level.
Route as differential pairs, HSTX0/HSTX1, 2/3, 4/5, 6/7.
-40 Design compatibility:
J7, K6, K7, L6, L7, L8 become Bank 4 on -40
They require dedicated level xlators if bank 4/5 have different voltages.
CK# HyperRAM only
tinyVision.ai Inc.
Sheet: /FPGA/
File: FPGA.kicad_sch
Title: PICO2-NX
Size: A3
Date:
Rev: 0.1
KiCad E.D.A. 8.0.4
Id: 3/5


Level Shifter
Reset state of SWDIO and SWDCLK is pull-up
U8
TXS0108ERGYR
Button
SW3
RP2350
Raspberry Pi
RP2350B QFN-80
U11
RP2350_80QFN
https://datasheets.raspberrypi.com/rp2350/hardware-design-with-rp2350.pdf
I2C Constant Current LED Driver
IC1
LP5810ADSDR
D7
MHPA1010RGBDT
RGB LED
D4
MHPA1010RGBDT
Mono LED
D5
LTST-C191KGKT
Flash
U10
W25Q32JVSSIQ
SRAM
U9
APS6404L-3SQN-SN
Multi-Function IO
D3
LTST-C191KGKT
JST SWD Debug Connector
Layout: this is side entry
so should go on a board edge
J2
SM03B-SRSS-TB
USB series termination close to RP2040
ABM8-272-T3
Y2
tinyVision.ai Inc.
Sheet: /RP2350/
File: RP2350.kicad_sch
Title: PICO2-NX
Size: A3
Date:
Rev: 0.1
KiCad E.D.A. 8.0.4
Id: 4/5


USBC
J1
USB_C_Receptacle_USB2.0
P5VD_VBUS
D2
1N5819WS
PTC1
MF-FSMF035X-2
P5VD
C50
10u
GND
VBUS
CC1
CC2
D-
D+
SHIELD
GND
SBU1
SBU2
USB.D-
USB.D+
USB(D+ D-)
R38
58K
JP1
JP2
R37
5.1K
R39
5.1K
Peripheral(Default)/Host Selection
Host Mode: Solder open bridges,
cut shorted bridges
Peripheral: Default
FPC
FPC_IO{PWR_EN LED_EN}
J4
SFV22R-2STE1HLF
P3V3D_FPGA
SDA1
SCL1
FPC_IO.LED_EN
FPC_IO.PWR_EN
RGB_MIPI.D3+
RGB_MIPI.D3-
RGB_MIPI.D2+
RGB_MIPI.D2-
RGB_MIPI.CLK+
RGB_MIPI.CLK-
RGB_MIPI.D1+
RGB_MIPI.D1-
RGB_MIPI.D0+
RGB_MIPI.D0-
RGB_MIPI{D0- D0+ D1- D1+ D2- D2+ D3- D3+ CLK- CLK+}
DSI
J3
SFV22R-2STE1HLF
SDA0
SCL0
EXT_MIPI.D3+
EXT_MIPI.D3-
EXT_MIPI.D2+
EXT_MIPI.D2-
EXT_MIPI.CLK+
EXT_MIPI.CLK-
EXT_MIPI.D1+
EXT_MIPI.D1-
EXT_MIPI.D0+
EXT_MIPI.D0-
EXT_MIPI{D0- D0+ D1- D1+ D2- D2+ D3- D3+ CLK- CLK+}
CSI
POWER
LED
SPI/ADC
MISC
J12
P5VD
P5VD_VBUS
PxVA_VREF
J15
LED.MONO
P3V3D
LED.R
LED.G
LED.B
J16
ADC0_PROT
ADC1_PROT
RP_BUTTONn
RP_SPI.SCK
RP_SPI.MISO
RP_SPI.MOSI
RP_SPI.CSn
J17
MULTI_FN
FPGA_EN
USB_BOOTn
PWR_EN
DONE
RESETn
EXT_LED
PxVD_IN
USB-C
SWD
DSI
I2C1
I2C0
CSI
H1
H2
H3
H4
These 2.54mm pitch through hole connectors are all DNF (user soldered) and a multiple of 2.54mm apart on pin centers, so the footprint is easy to replicate. Mounting holes should be a multiple of 2.54mm apart on centers but need not align with through hole connectors.
All connectors, LEDs and buttons are on top. Whether through hole connectors are soldered top or bottom is a decision for the user.
At user's option 2x3 and 2x5 connectors could be straight or right angled receptacles fitted on top or straight male pins fitted on bottom to connect to a carrier board, for example.
For 2x5, follow PMOD Specification version 1.2 layout, including, for highlighted pairs, distance between adjacent connectors.
To facilitate connecting horizontally to another board, both 2x3 and 2x5 headers should be the same distance from the board edge.
The connectors can be rearranged to aid routing. Highlighted adjacent headers should remain adjacent, sharing the same board edge.
J14
I2C0.SCL
I2C0.SDA
P3V3D
I2C_IRQn
I2C
J13
I2C1.SCL
I2C1.SDA
J6
EXT_SPI.CSn
EXT_SPI.MOSI
EXT_SPI.MISO
EXT_SPI.SCK
FPC_IO.LED_EN
FPC_IO.PWR_EN
P3V3D_FPGA
SPI
J5
FPGA_PMOD0
FPGA_PMOD1
FPGA_PMOD2
FPGA_PMOD3
FPGA_PMOD4
FPGA_PMOD5
FPGA_PMOD6
FPGA_PMOD7
PMOD
https://digilent.com/reference/_media/reference/pmod/pmod-interface-specification-1_2_0.pdf
PxVD_AOUT
SHARED_A3
SHARED_A2
SHARED_A1
SHARED_A0
PxVD_BOUT
SHARED_B3
SHARED_B2
SHARED_B1
SHARED_B0
J8
J11
SHARED_A7
SHARED_A6
SHARED_A5
SHARED_A4
SHARED_B7
SHARED_B6
SHARED_B5
SHARED_B4
PMOD
PMOD
JTAG
J10
FTSH-105-01-L-DV-007-K
P3V3D_FPGA
JTAG.PRESENTn
JP15
GND
JP5
R76
R77
R72
R79
100
JTAG.TMS
JTAG.TCK
JTAG.TDO
JTAG.TDI
RESETn
J18
FTSH-105-01-L-DV
Can only daisy chain
to boards using 3.3V
CMOS levels for JTAG
FPC I2C Isolation
P3V3D_FPGA
R64
4.7K
R65
4.7K
R86
4.7K
R61
4.7K
SCL1
SDA1
SCL0
SDA0
Q3A
DMG1024UV-7
Q3B
DMG1024UV-7
Q4A
DMG1024UV-7
Q4B
DMG1024UV-7
I2C1{SCL SDA}
I2C1.SCL
I2C1.SDA
I2C0{SCL SDA}
I2C0.SCL
I2C0.SDA
ADC
P1V8D
D8
BAS40-04
D9
BAS40-04
ADC[0..1]
ADC0_PROT
ADC1_PROT
R68
R82
R69
R83
100
ADC0
ADC1
I2C JST
P3V3D
JP18
JP17
Layout: these are side entry
so should go on a board edge
I2C0.SDA
I2C0.SCL
I2C1.SDA
I2C1.SCL
J7
SM04B-SRSS-TB
J9
SM04B-SRSS-TB
PMOD Level Shifters
P3V3D_FPGA
PxVD_IN
JP6
P1V8D_FPGA
PxVD_AOUT
C77
0.1u
C79
0.1u
GND
VCCA
VCCB
OE
SHARED_PMOD_A0
SHARED_PMOD_A1
SHARED_PMOD_A2
SHARED_PMOD_A3
SHARED_PMOD_A4
SHARED_PMOD_A5
SHARED_PMOD_A6
SHARED_PMOD_A7
SHARED_PMOD_A[0..7]
U15
TXS0108ERGYR
JP7
PxVD_BOUT
C78
0.1u
C80
0.1u
PORT_EN
R20
1K
R66
200K
SHARED_PMOD_B0
SHARED_PMOD_B1
SHARED_PMOD_B2
SHARED_PMOD_B3
SHARED_PMOD_B4
SHARED_PMOD_B5
SHARED_PMOD_B6
SHARED_PMOD_B7
SHARED_PMOD_B[0..7]
U16
TXS0108ERGYR
Consider routing these as differential pairs, as a best
effort attempt to make an HDMI PMOD work at low res.
FPGA_PMOD[0..7]
EXT_SPI{CSn SCK MOSI MISO}
RP_SPI{CSn SCK MOSI MISO}
MULTI_FN
FPGA_EN
DONE
USB_BOOTn
PWR_EN
EXT_LED
RESETn
I2C_IRQn
RP_BUTTONn
JTAG{PRESENTn TCK TMS TDI TDO}
JTAG.TMS
JTAG.TCK
JTAG.TDO
JTAG.TDI
JTAG.PRESENTn
LED{R G B MONO}
LED.R
LED.G
LED.B
LED.MONO
tinyVision.ai Inc.
Sheet: /Connectors/
File: Connectors.kicad_sch
Title: PICO2-NX
Size: A3
Date:
Rev: 0.1
KiCad E.D.A. 8.0.4
Id: 5/5