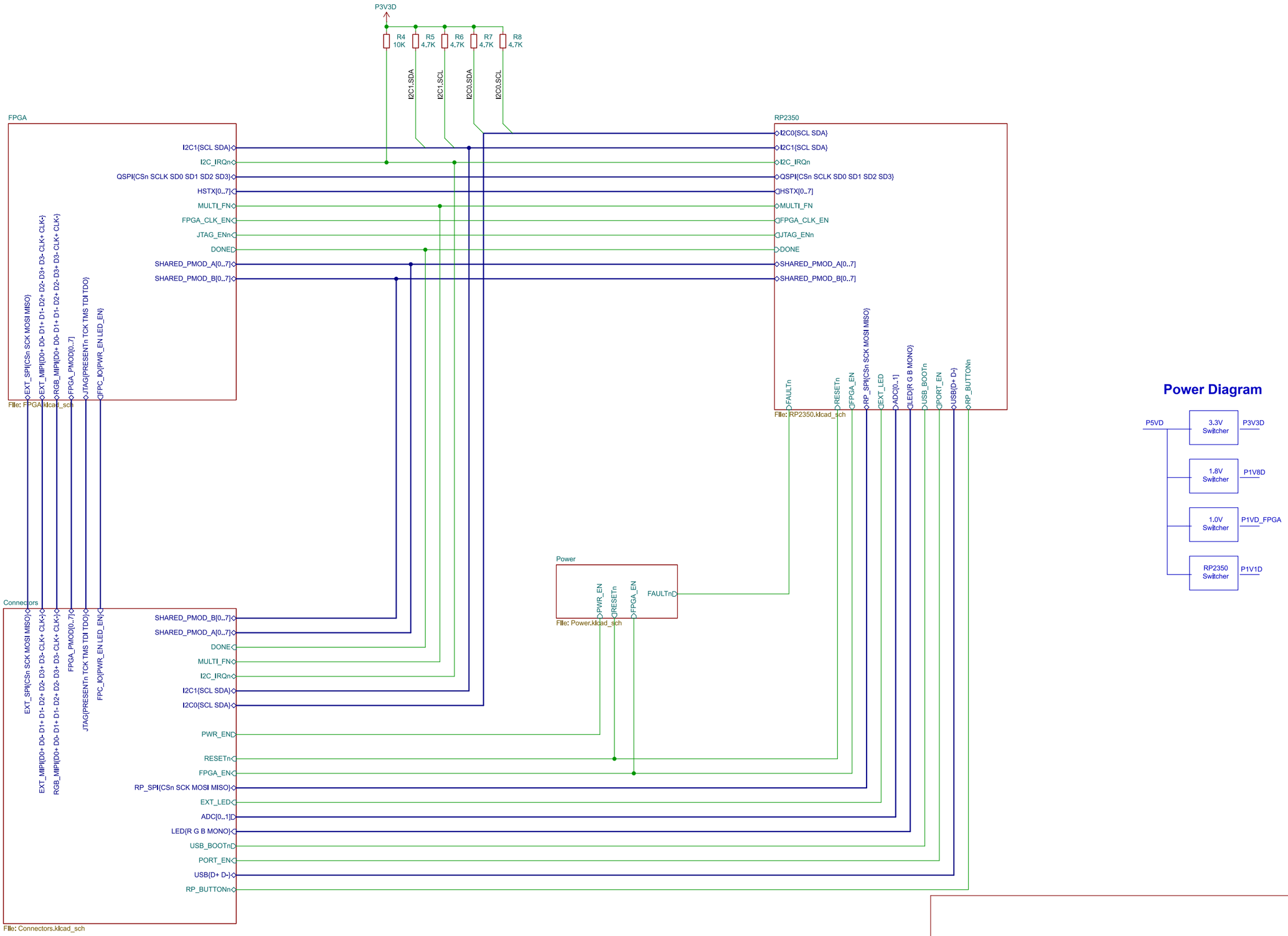

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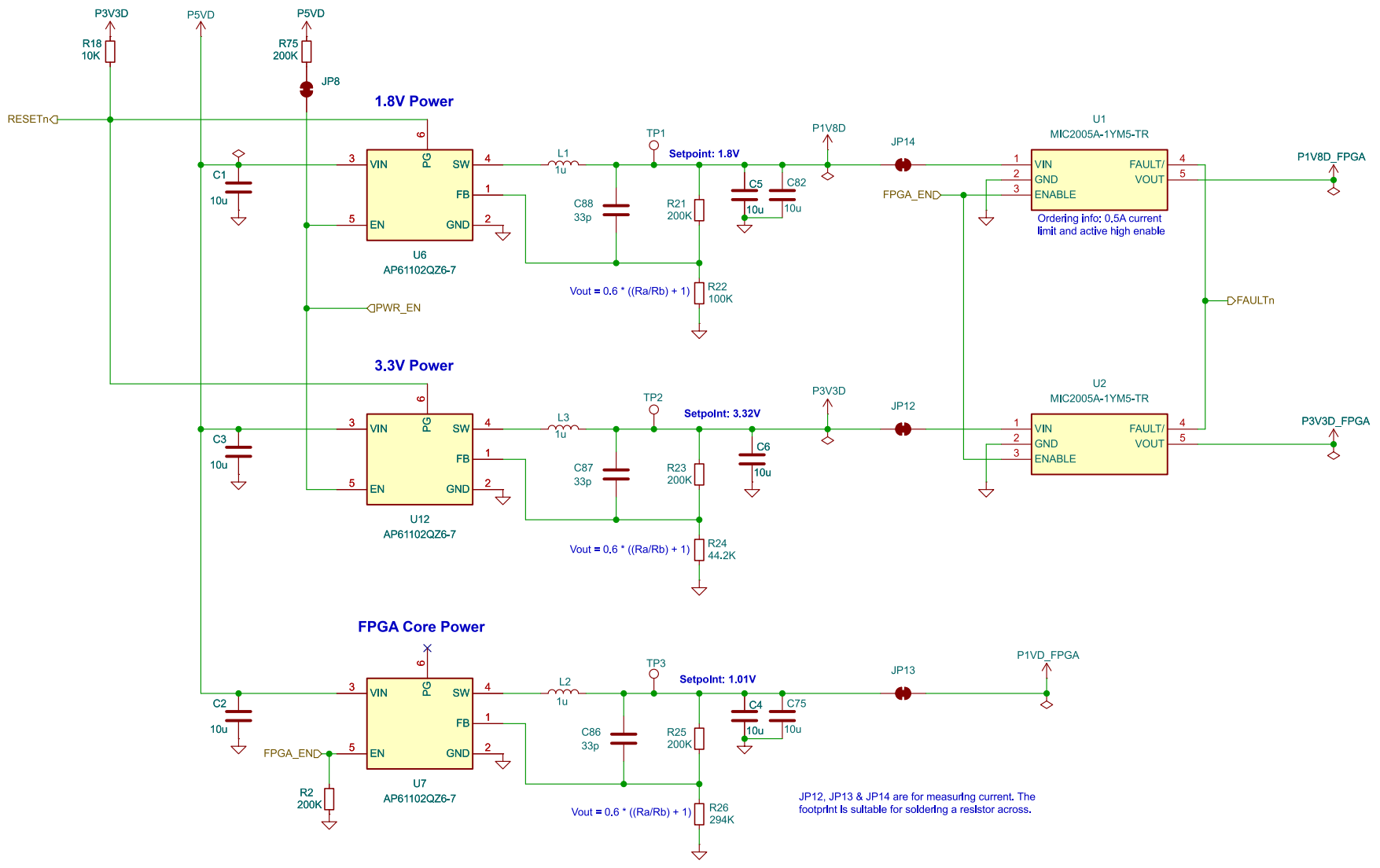
Sheet: /

File: pico2-nx.kicad_sch

Title: PICO2-NX

Size: A3	Date: 2025-06-03	**Rev: 0.1**
KiCad E.D.A. 8.0.4		Id: 1/5



Power Modes:
OFF: EN < 0.9V, uA level current
PWM Mode: 0.91 (type) < EN < P5V-200mV
PFM Mode: P5V-200mV < EN < P5V

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Sheet: /Power/
File: Power.kicad_sch

Title: PICO2-NX

Size: A4	Date:	**Rev: 0.1**
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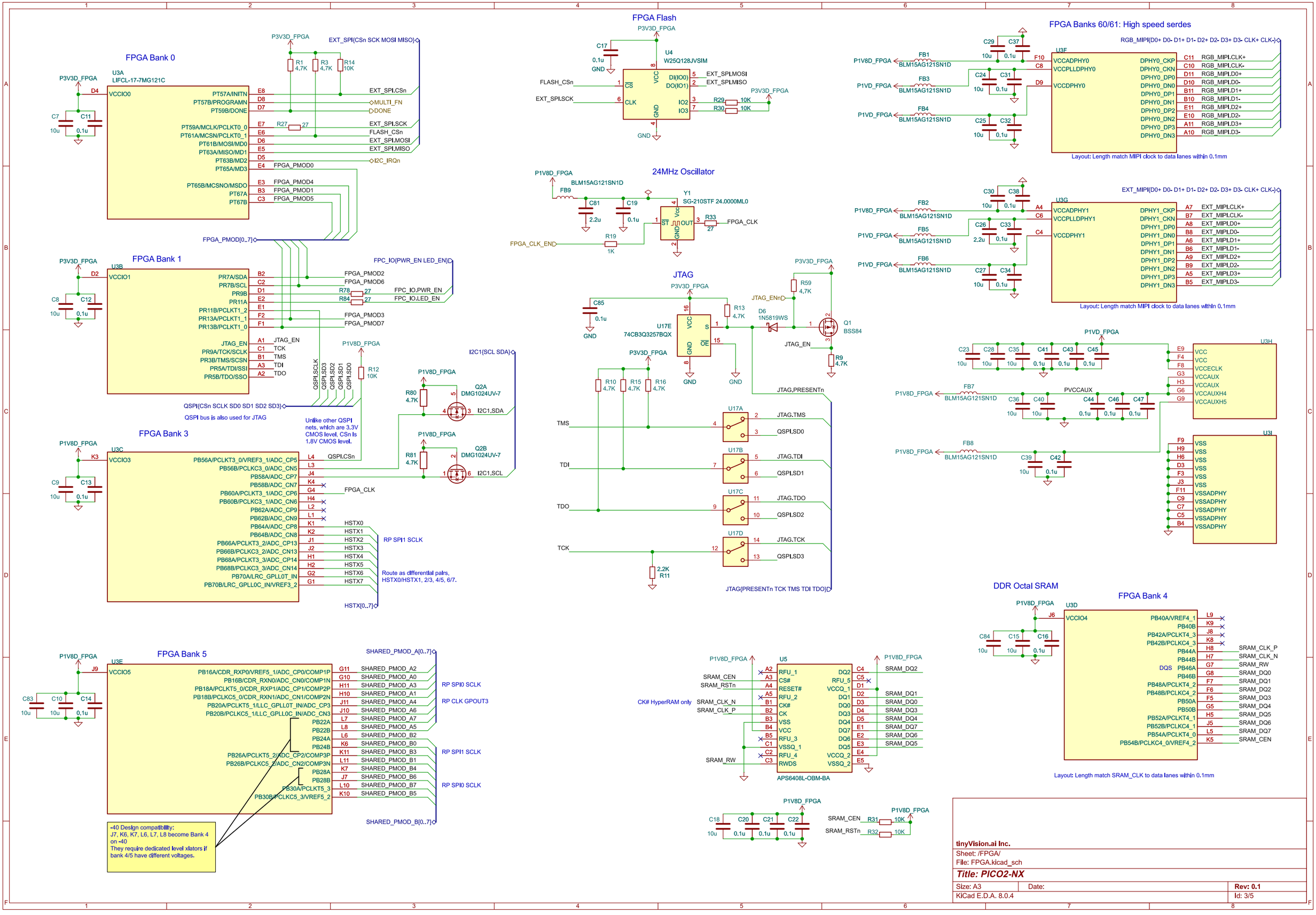
FPGA Bank 0
U3A
LIFCL-17-7MG121C
FPGA Bank 1
U3B
FPGA Bank 3
U3C
FPGA Bank 5
U3E
FPGA Flash
U4
W25Q128JVSIM
24MHz Oscillator
Y1
SG-210STF 24.0000ML0
JTAG
U17E
74CB3Q3257BQX
Q1
BSS84
Q2A
DMG1024UV-7
Q2B
DMG1024UV-7
FPGA Banks 60/61: High speed serdes
U3F
Layout: Length match MIPI clock to data lanes within 0.1mm
U3G
Layout: Length match MIPI clock to data lanes within 0.1mm
U3H
U3I
DDR Octal SRAM
U5
APS6408L-OBM-BA
FPGA Bank 4
U3D
Layout: Length match SRAM_CLK to data lanes within 0.1mm
QSPI bus is also used for JTAG
Unlike other QSPI nets, which are 3.3V CMOS level, CSn is 1.8V CMOS level.
Route as differential pairs, HSTX0/HSTX1, 2/3, 4/5, 6/7.
-40 Design compatibility:
J7, K6, K7, L6, L7, L8 become Bank 4 on -40
They require dedicated level xlators if bank 4/5 have different voltages.
CK# HyperRAM only
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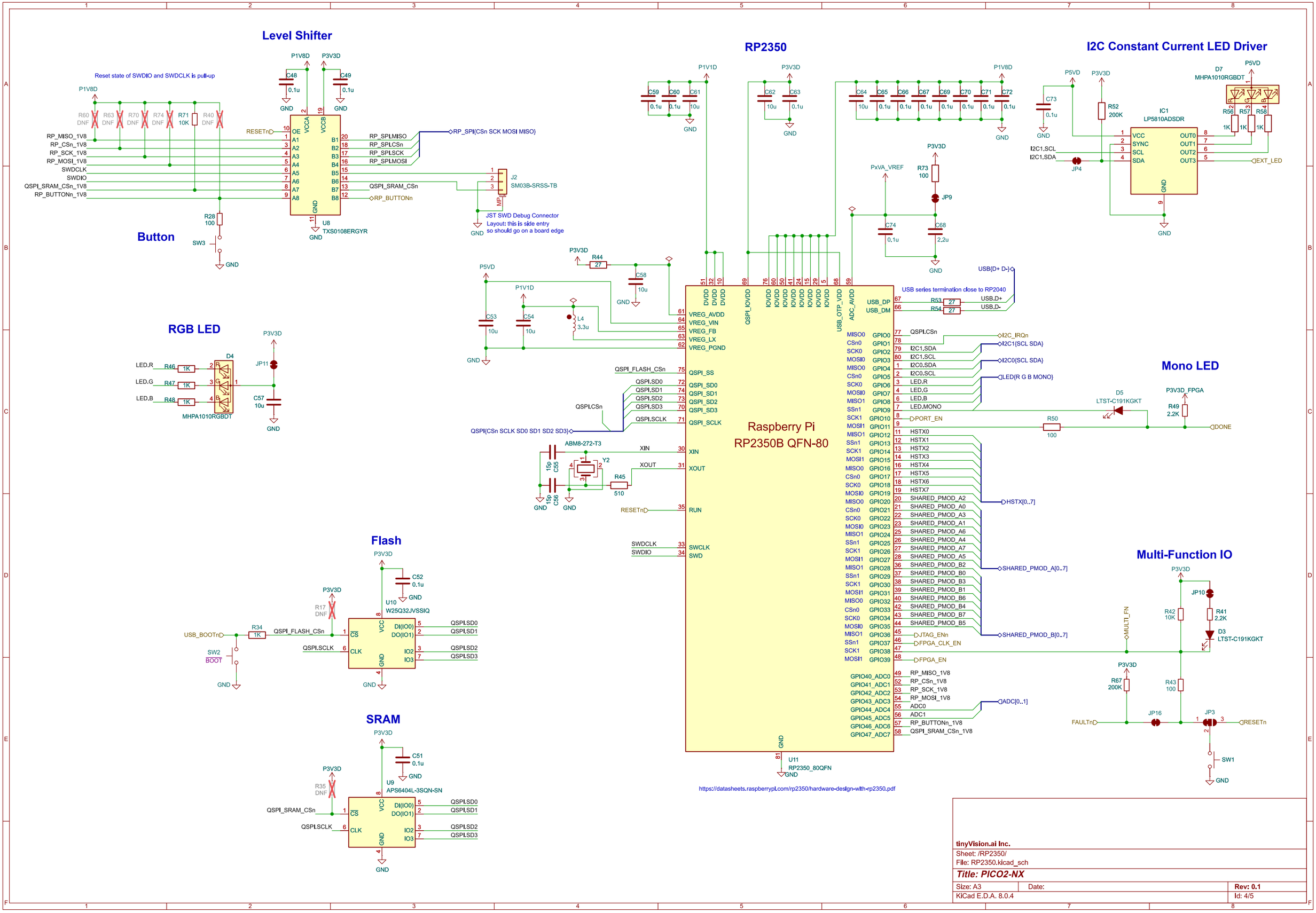
Sheet: /FPGA/
File: FPGA.kicad_sch
Title: PICO2-NX
Size: A3
Date:
Rev: 0.1
KiCad E.D.A. 8.0.4
Id: 3/5


Level Shifter
Reset state of SWDIO and SWDCLK is pull-up
P1V8D
P3V3D
C48 0.1u
C49 0.1u
R60 DNF
R63 DNF
R70 DNF
R74 DNF
R71 10K
R40 DNF
RESETn
OE
VCCA
VCCB
A1
A2
A3
A4
A5
A6
A7
A8
B1
B2
B3
B4
B5
B6
B7
B8
GND
U8
TXS0108ERGYR
RP_MISO_1V8
RP_CSn_1V8
RP_SCK_1V8
RP_MOSI_1V8
SWDCLK
SWDIO
QSPI_SRAM_CSn_1V8
RP_BUTTONn_1V8
RP_SPI.MISO
RP_SPI.CSn
RP_SPI.SCK
RP_SPI.MOSI
QSPI_SRAM_CSn
RP_BUTTONn
RP_SPI{CSn SCK MOSI MISO}
J2
SM03B-SRSS-TB
JST SWD Debug Connector
Layout: this is side entry
so should go on a board edge
Button
R28 100
SW3
GND
RP2350
P1V1D
C59 0.1u
C60 0.1u
C61 10u
C62 10u
C63 0.1u
C64 10u
C65 0.1u
C66 0.1u
C67 0.1u
C69 0.1u
C70 0.1u
C71 0.1u
C72 0.1u
P3V3D
R44 27
C58 10u
P5VD
C53 10u
C54 10u
L4 3.3u
VREG_AVDD
VREG_VIN
VREG_FB
VREG_LX
VREG_PGND
QSPI_FLASH_CSn
QSPI_SS
QSPI_SD0
QSPI_SD1
QSPI_SD2
QSPI_SD3
QSPI_SCLK
QSPI.CSn
QSPI.SD0
QSPI.SD1
QSPI.SD2
QSPI.SD3
QSPI.SCLK
QSPI{CSn SCLK SD0 SD1 SD2 SD3}
ABM8-272-T3
Y2
15p C55
15p C56
R45 510
XIN
XOUT
RESETn
RUN
SWDCLK
SWDIO
SWCLK
SWD
Raspberry Pi
RP2350B QFN-80
U11
RP2350_80QFN
https://datasheets.raspberrypi.com/rp2350/hardware-design-with-rp2350.pdf
USB series termination close to RP2040
USB{D+ D-}
USB_DP
USB_DM
USB.D+
USB.D-
R53 27
R54 27
PxVA_VREF
R73 100
JP9
C74 0.1u
C68 2.2u
I2C Constant Current LED Driver
P5VD
P3V3D
C73 0.1u
R52 200K
IC1
LP5810ADSDR
VCC
SYNC
SCL
SDA
OUT0
OUT1
OUT2
OUT3
I2C1.SCL
I2C1.SDA
JP4
D7
MHPA1010RGBDT
R56 1K
R57 1K
R58 1K
EXT_LED
RGB LED
D4
MHPA1010RGBDT
LED.R
LED.G
LED.B
R46 1K
R47 1K
R48 1K
JP11
C57 10u
Mono LED
D5
LTST-C191KGKT
P3V3D_FPGA
R49 2.2K
R50 100
DONE
PORT_EN
Flash
P3V3D
C52 0.1u
U10
W25Q32JVSSIQ
R17 DNF
USB_BOOTn
R34 1K
QSPI_FLASH_CSn
QSPI.SCLK
QSPI.SD0
QSPI.SD1
QSPI.SD2
QSPI.SD3
SW2
BOOT
SRAM
C51 0.1u
U9
APS6404L-3SQN-SN
R35 DNF
QSPI_SRAM_CSn
Multi-Function IO
JP10
R42 10K
R41 2.2K
D3
LTST-C191KGKT
MULTI_FN
R67 200K
R43 100
FAULTn
JP16
JP3
RESETn
SW1
I2C_IRQn
I2C1{SCL SDA}
I2C0{SCL SDA}
LED{R G B MONO}
HSTX[0..7]
SHARED_PMOD_A[0..7]
SHARED_PMOD_B[0..7]
JTAG_ENn
FPGA_CLK_EN
FPGA_EN
ADC[0..1]
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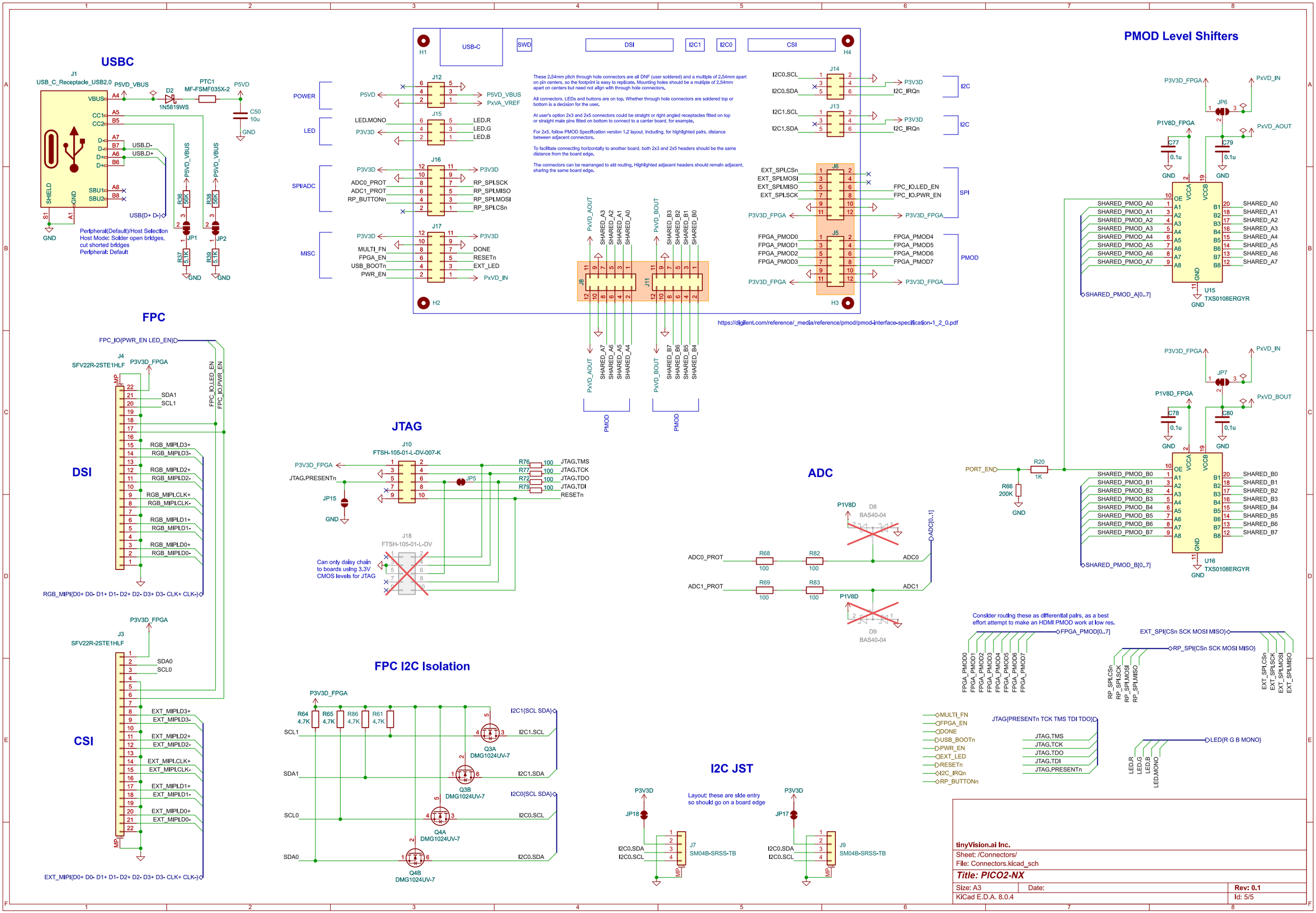
Sheet: /RP2350/
File: RP2350.kicad_sch
Title: PICO2-NX
Size: A3
Date:
Rev: 0.1
KiCad E.D.A. 8.0.4
Id: 4/5



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Sheet: /Connectors/
File: Connectors.kicad_sch

Title: PICO2-NX

Size: A3	Date:	**Rev: 0.1**
KiCad E.D.A. 8.0.4		Id: 5/5