FPGA

Power

FPGA_END ──────── FPGA_EN

File: FPGA.kicad_sch

File: power.kicad_sch

Sheet: /
File: pico2-nx-module.kicad_sch
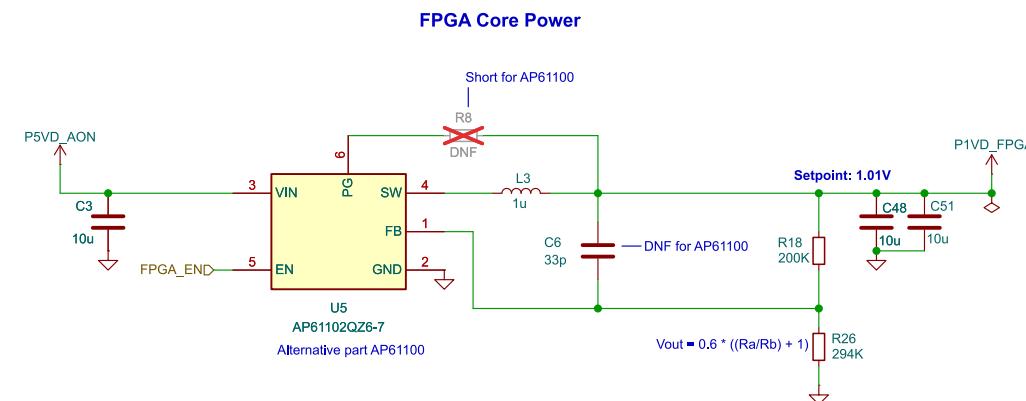
Title: PICO2-NX Module

| Size: A4 | Date: | Rev: 0.1 |
| KiCad E.D.A. 9.0.4 | | Id: 1/3 |

FPGA Core Power

Short for AP61100

R8
DNF

P5VD_AON

R18
200K

Setpoint: 1.01V

P1VD_FPGA

C3
10u

VIN   PG   SW   4

L3
1u

C48   C51
10u   10u

FPGA_END   5   EN   FB   1

C6
33p

DNF for AP61100

GND   2

U5
AP61102QZ6-7
Alternative part AP61100

Vout = 0.6 * ((Ra/Rb) + 1)

R26
294K

FPGA Bank 0

U3A
LIFCL-17-7MG121C

P3V3D_FPGA
D4 VCCIO0
C8 10u C12 0.1u

E8	PT57A/INITN	PT57A
D8	PT57B/PROGRAMN	PROGRAMn
D7	PT59B/DONE	DONE
E7	PT59A/MCLK/PCLKT0_0	SCLK
E6	PT61A/MCSN/PCLKT0_1	FLASH_CSn
D6	PT61B/MOSI/MD0	MOSI
E5	PT63A/MISO/MD1	MISO
D5	PT63B/MD2	SD2
E4	PT65A/MD3	SD3
E3	PT65B/MCSNO/MSDO	
B3	PT67A	PT65B
C3	PT67B	PT67P
		PT67N

R3 27 SCLK
Series termination resistors near FPGA.

FPGA Bank 1

U3B
PVIO1_FPGA
D2 VCCIO1
C9 10u C13 0.1u

B2	PR7A/SDA	PR7P
C2	PR7B/SCL	PR7N
D1	PR9B	PR9B
E2	PR11A	PR11P
E1	PR11B/PCLKT1_2	PR11N
F2	PR13A/PCLKT1_1	PR13P
F1	PR13B/PCLKT1_0	PR13N
A1	JTAG_EN	JTAG_EN
C1	PR9A/TCK/SCLK	TCK
B1	PR3B/TMS/SCSN	TMS
A3	PR5A/TDI/SSI	TDI
A2	PR5B/TDO/SSO	TDO

R12 27 PR9B

FPGA Bank 3

U3C
PVIO3_FPGA
K3 VCCIO3
C10 10u C14 0.1u

L4	PB56A/PCLKT3_0/VREF3_1/ADC_CP5	PB56P
L3	PB56B/PCLKC3_0/ADC_CN5	PB56N
J4	PB58A/ADC_CP7	PB58P
K4	PB58B/ADC_CN7	PB58N
G4	PB60A/PCLKT3_1/ADC_CP6	PB60P RP CLKOUT
H4	PB60B/PCLKC3_1/ADC_CN6	PB60N
L2	PB62A/ADC_CP9	PB62P
L1	PB62B/ADC_CN9	PB62N
K1	PB64A/ADC_CP8	PB64P
K2	PB64B/ADC_CN8	PB64N
J1	PB66A/PCLKT3_2/ADC_CP13	PB66P RP SCLK
J2	PB66B/PCLKC3_2/ADC_CN13	PB66N
H1	PB68A/PCLKT3_3/ADC_CP14	PB68P
H2	PB68B/PCLKC3_3/ADC_CN14	PB68N
G2	PB70A/LRC_GPLL0T_IN	PB70P
G1	PB70B/LRC_GPLL0C_IN/VREF3_2	PB70N

FPGA Bank 5

U3E
PVIO5_FPGA
J9 VCCIO5
C7 10u C11 10u C15 0.1u

G11	PB16A/CDR_RXP0/VREF5_1/ADC_CP0/COMP1P	PB16P
G10	PB16B/CDR_RXN0/ADC_CN0/COMP1N	PB16N
H11	PB18A/PCLKT5_0/CDR_RXP1/ADC_CP1/COMP2P	PB18P
H10	PB18B/PCLKC5_0/CDR_RXN1/ADC_CN1/COMP2N	PB18N
J11	PB20A/PCLKT5_1/LLC_GPLL0T_IN/ADC_CP3	PB20P
J10	PB20B/PCLKC5_1/LLC_GPLL0C_IN/ADC_CN3	PB20N
L7	PB22A	PB22P
L8	PB22B	PB22N
L6	PB24A	PB24P
K6	PB24B	PB24N
K11	PB26A/PCLKT5_2/ADC_CP2/COMP3P	PB26P
L11	PB26B/PCLKC5_2/ADC_CN2/COMP3N	PB26N
K7	PB28A	PB28P
J7	PB28B	PB28N
L10	PB30A/PCLKT5_3	PB30P
K10	PB30B/PCLKC5_3/VREF5_2	PB30N

-40 Design compatibility:
J7, K6, K7, L6, L7, L8 become Bank 4 on -40
They require dedicated level xlators if bank 4/5 have different voltages.

FPGA Flash

P3V3D_FPGA
R9 4,7K
C18 0.1u
GND
U4 W25Q128JVPIQ

1	CS	DI(IO0) 5 MOSI
	VCC	DO(IO1) 2 MISO
6	CLK	IO2 3 SD2
4	GND	IO3 7 SD3

FLASH_CSn
SCLK
R33 4,7K R51 4,7K
P3V3D_FPGA

MIPI

J3 DF40C-60DP-0.4V(51)

SHUTDOWNn
CFPGA_EN
P5VD_AON PVIO5_FPGA P1V8D_FPGA PVIO3_FPGA PVIO1_FPGA P3V3D_FPGA

DPHY0.D0-	2 1	
DPHY0.D0+	4 3	
	6 5	
DPHY0.D1-	8 7	
DPHY0.D1+	10 9	
	12 11	
DPHY0.CLK-	14 13	
DPHY0.CLK+	16 15	
	18 17	PT57A
DPHY0.D2-	20 19	PR9B
DPHY0.D2+	22 21	PT65B
	24 23	PROGRAMn
DPHY0.D3-	26 25	DONE
DPHY0.D3+	28 27	MOSI
	30 29	SCLK
DPHY1.D3+	32 31	TDI
DPHY1.D3-	34 33	TDO
	36 35	SD3
DPHY1.D2+	38 37	TMS
DPHY1.D2-	40 39	JTAG_EN
	42 41	TCK
DPHY1.CLK+	44 43	FLASH_CSn
DPHY1.CLK-	46 45	MISO
	48 47	SD2
DPHY1.D1+	50 49	
DPHY1.D1-	52 51	PT67P
	54 53	PT67N Bank 0
DPHY1.D0+	56 55	
DPHY1.D0-	58 57	PR7P
	60 59	PR7N Bank 1

Connectors on bottom
J2 DF40C-60DP-0.4V(51)

PB16P	2 1	PB58N
PB16N	4 3	PB58P
	6 5	
PB18P	8 7	PB60N
PB18N	10 9	PB60P
	12 11	
PB20P	14 13	PB56P
PB20N	16 15	PB56N
	18 17	
PB26P	20 19	PB62P
PB26N	22 21	PB62N
	24 23	
PB30N	26 25	PB64N
PB30P	28 27	PB64P
	30 29	
PB28P	32 31	PB66N
PB28N	34 33	PB66P
	36 35	
PB22N	38 37	PB68N
PB22P	40 39	PB68P
	42 41	
PB24P	44 43	PB70P
PB24N	46 45	PB70N
	48 47	Bank 3
PB52B	50 49	PR13N
PB52A	52 51	PR13P
PB50B	54 53	PR11N
PB50A	56 55	PR11P
	58 57	
	60 59	Bank 1

Bank 5
Bank 4
Bank 3
P5VD_AON if connected backwards!

FPGA Banks 60/61: High speed serdes

U3F

P1V8D_FPGA FB2 BLM15AG121SN1D
P1VD_FPGA FB3 BLM15AG121SN1D
P1VD_FPGA FB4 BLM15AG121SN1D

C30 10u C37 0.1u
C25 10u C33 0.1u
C26 10u C34 0.1u

F10	VCCADPHY0	C11	DPHY0_CKP	DPHY0.CLK+
	VCCPLLDPHY0	C10	DPHY0_CKN	DPHY0.CLK-
C8	VCCDPHY0	D11	DPHY0_DP0	DPHY0.D0+
D9		D10	DPHY0_DN0	DPHY0.D0-
		B11	DPHY0_DP1	DPHY0.D1+
		B10	DPHY0_DN1	DPHY0.D1-
		E11	DPHY0_DP2	DPHY0.D2+
		E10	DPHY0_DN2	DPHY0.D2-
		A11	DPHY0_DP3	DPHY0.D3+
		A10	DPHY0_DN3	DPHY0.D3-

Layout: Length match MIPI clock to data lanes within 0.1mm

U3G

P1V8D_FPGA FB5 BLM15AG121SN1D
P1VD_FPGA FB6 BLM15AG121SN1D
P1VD_FPGA FB7 BLM15AG121SN1D

C31 10u C38 0.1u
C27 2.2u C35 0.1u
C28 10u C36 0.1u

A4	VCCADPHY1	A7	DPHY1_CKP	DPHY1.CLK+
C6	VCCPLLDPHY1	B7	DPHY1_CKN	DPHY1.CLK-
C4	VCCDPHY1	A8	DPHY1_DP0	DPHY1.D0+
		B8	DPHY1_DN0	DPHY1.D0-
		A6	DPHY1_DP1	DPHY1.D1+
		B6	DPHY1_DN1	DPHY1.D1-
		A9	DPHY1_DP2	DPHY1.D2+
		B9	DPHY1_DN2	DPHY1.D2-
		A5	DPHY1_DP3	DPHY1.D3+
		B5	DPHY1_DN3	DPHY1.D3-

Layout: Length match MIPI clock to data lanes within 0.1mm

U3H

P1VD_FPGA
C24 10u C32 10u C39 0.1u C44 0.1u C47 0.1u C81 0.1u

E9	VCC
F4	VCC
F8	VCCECLK
G3	VCCAUX
H3	VCCAUX
G6	VCCAUXH4
G9	VCCAUXH5

P1V8D_FPGA FB8 BLM15AG121SN1D
PVCCAUX
C40 10u C43 10u C76 0.1u C83 0.1u C84 0.1u

U3I

P1V8D_FPGA FB9 BLM15AG121SN1D
C42 10u C46 0.1u

F9	VSS
H9	VSS
H6	VSS
D3	VSS
F3	VSS
J3	VSS
F11	VSS
C9	VSSADPHY
C7	VSSADPHY
C5	VSSADPHY
B4	VSSADPHY

DDR Octal SRAM

U13
APS6408L-OBM-BA

P1V8D_FPGA

A2	RFU_1	DQ2	C4	SRAM_DQ2
A3	CS#	RFU_5	C5	
A4	RESET#	VCCQ_1	D1	
A5	RFU_2	DQ1	D2	SRAM_DQ1
B1	CK#	DQ0	D3	SRAM_DQ0
B2	CK	DQ3	D4	SRAM_DQ3
B3	VSS	DQ4	D5	SRAM_DQ4
B4	VCC	DQ7	E1	SRAM_DQ7
B5	RFU_3	DQ6	E2	SRAM_DQ6
C2	VSSQ_1	DQ5	E3	SRAM_DQ5
C3	RFU_4	VCCQ_2	E4	
	RWDS	VSSQ_2	E5	

SRAM_CEN
SRAM_RSTn
SRAM_CLK_N
SRAM_CLK_P
SRAM_RW

C20 10u C21 0.1u C22 0.1u C23 0.1u
SRAM_CEN R62 4,7K
SRAM_RSTn R78 4,7K

DDR Octal SRAM

U3D FPGA Bank 4

P1V8D_FPGA
J6 VCCIO4
C29 10u C41 10u C45 0.1u

L9	PB40A/VREF4_1	SRAM_DQ6
K9	PB40B	SRAM_DQ5
J8	PB42A/PCLKT4_3	SRAM_DQ1
K8	PB42B/PCLKC4_3	SRAM_DQ0
H8	PB44A	SRAM_DQ2
H7	PB44B	SRAM_DQ7
G7	PB46A/DQS	SRAM_RW
G8	PB46B	SRAM_CEN
F7	PB48A/PCLKT4_2	SRAM_DQ4
F6	PB48B/PCLKC4_2	SRAM_DQ3
F5	PB50A	PB50A
G5	PB50B	PB50B
H5	PB52A/PCLKT4_1	PB52A
J5	PB52B/PCLKC4_1	PB52B
L5	PB54A/PCLKT4_0	SRAM_CLK_N
K5	PB54B/PCLKC4_0/VREF4_2	SRAM_CLK_P

DQS SRAM_RW

LOGO1
tinyVision logo

P5VD_AON P3V3D_FPGA PVIO1_FPGA PVIO3_FPGA P1V8D_FPGA PVIO5_FPGA

FID1 Fiducial FID2 Fiducial FID5 Fiducial FID6 Fiducial
FID3 Fiducial FID7 Fiducial