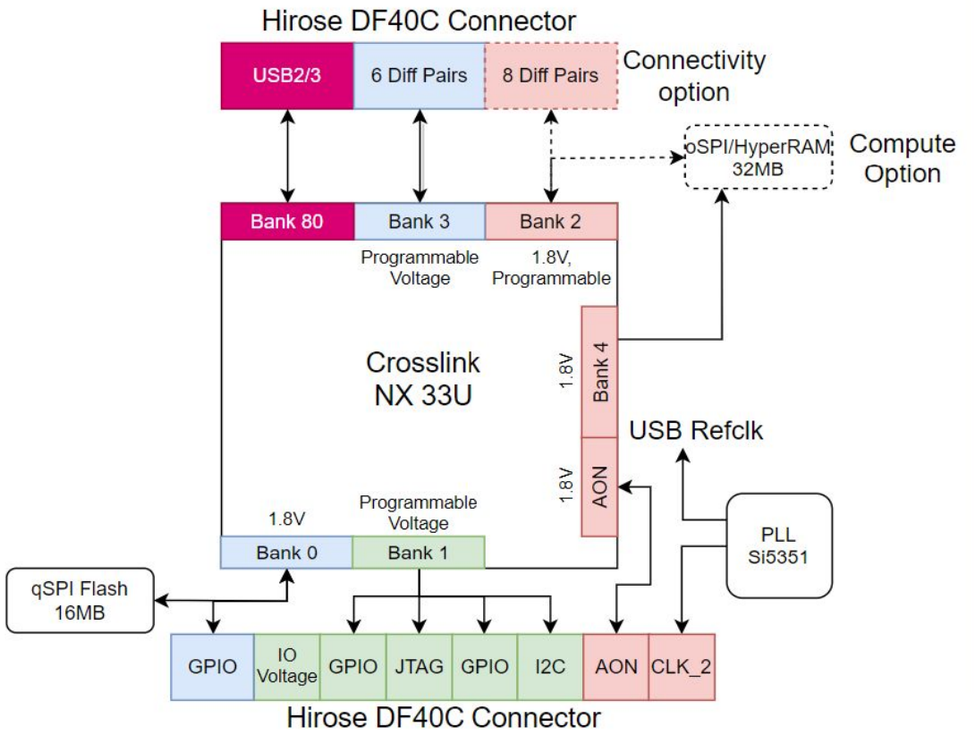
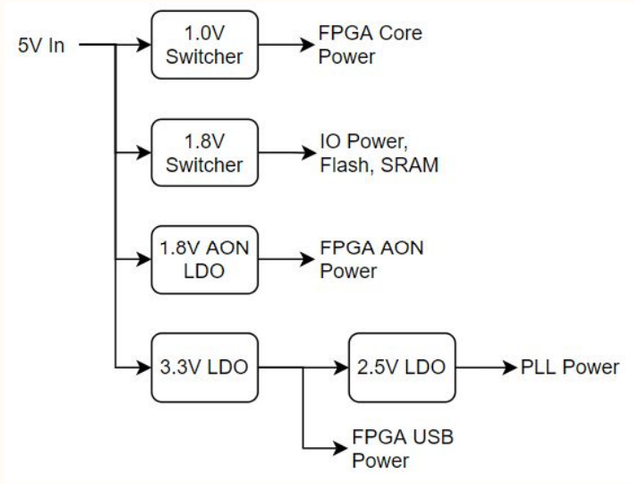
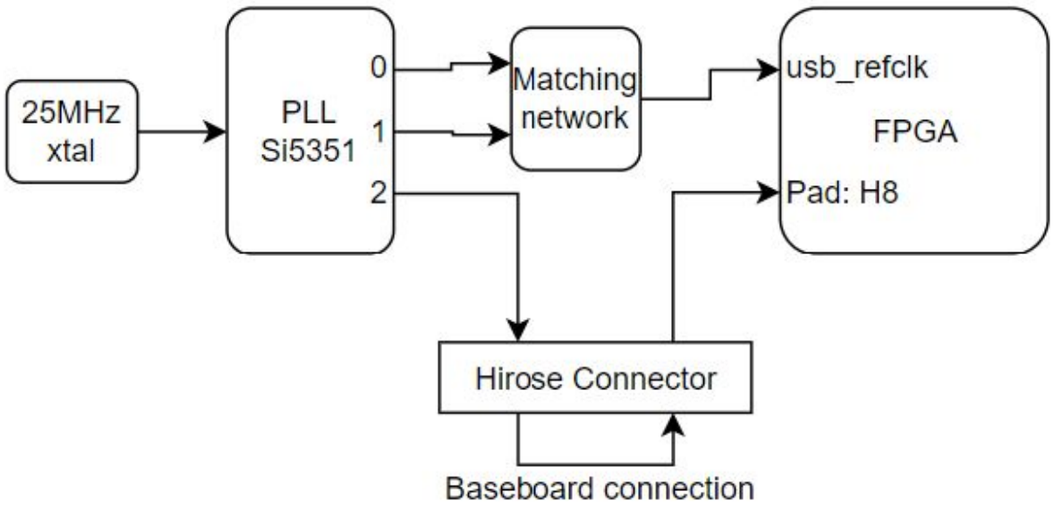
FPGA Bank Allocation



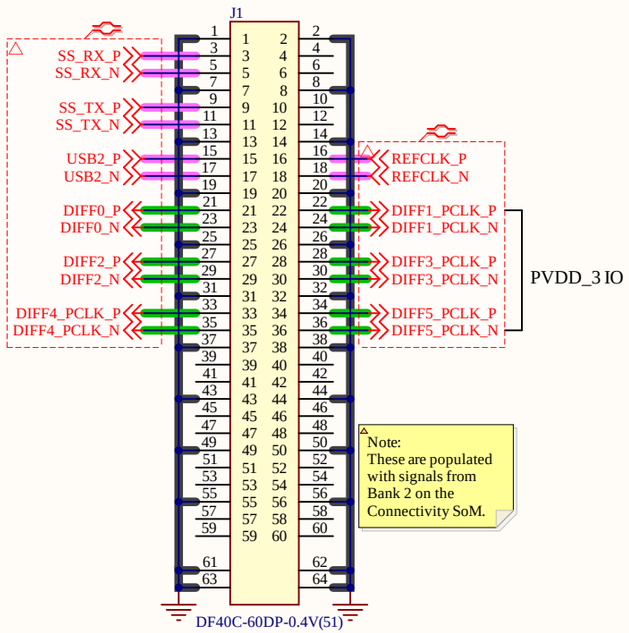
Power Distribution

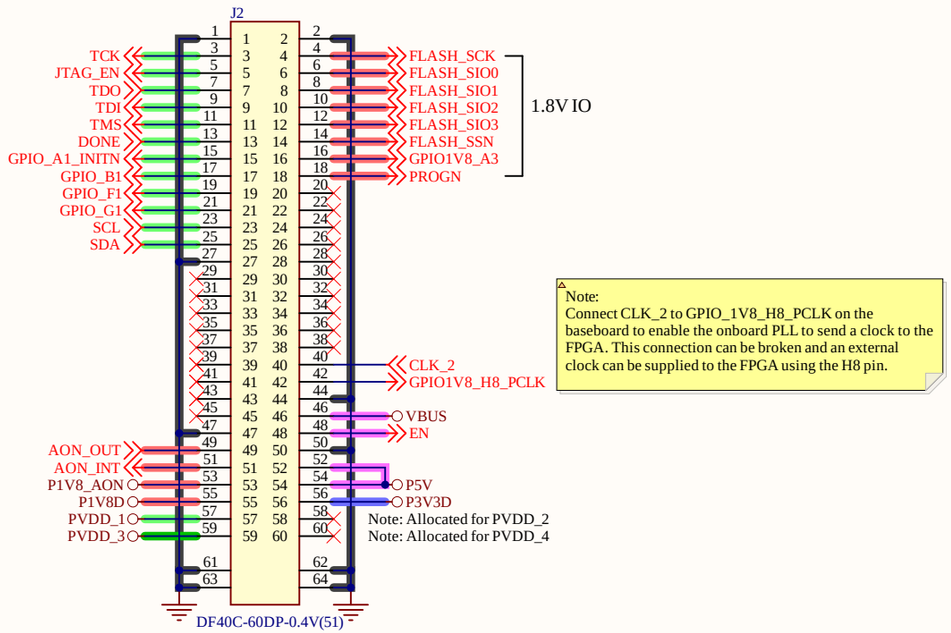


Clocking



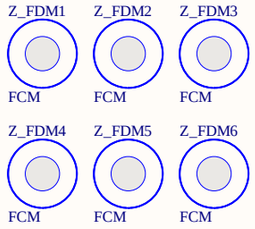
Color Legend:
3.3V IO
USB
1.8V
Bank 1 Voltage (1.2-3.3V)
Bank 2 Voltage (1.2-1.8V)
Bank 3 Voltage (1.2-1.8V)
Ground



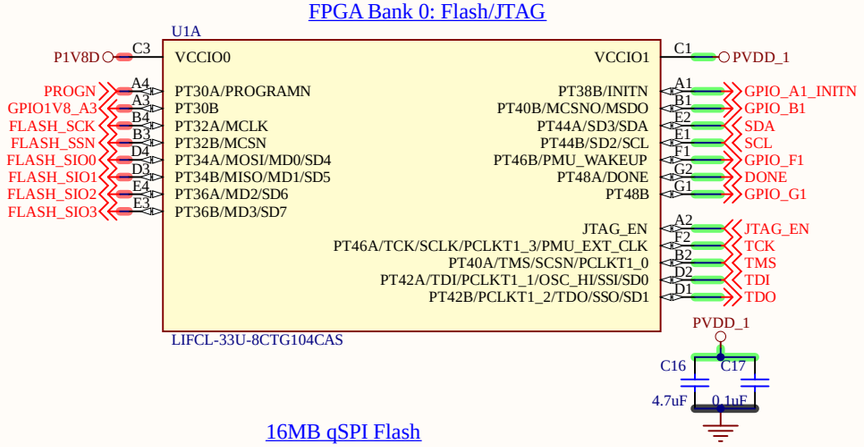


Change Summary from previous version:
- Removed CLK_OUT signal, got used to drive the diff pair to the USB reference clock
- Added PVDD_3 for Bank 3 IO voltage, removed PVDD_2 which is now set to 1.8V
- Changed Flash voltages to 1.8V
- Eliminated a few GPIO that are now used by the SRAM

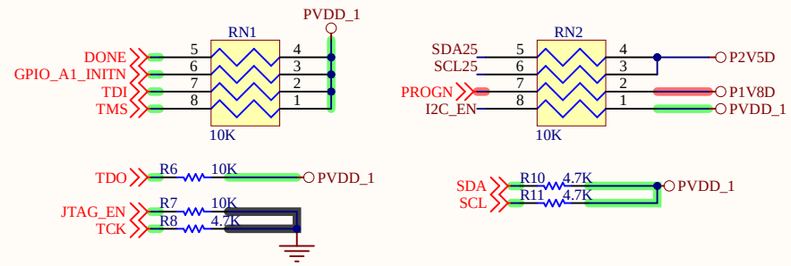
Layout note: Match diff pairs to within 1mm of each other.



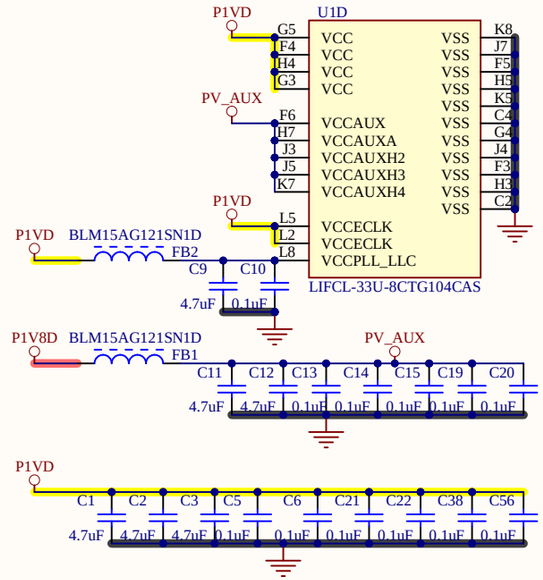
FPGA Bank 0: Flash/JTAG



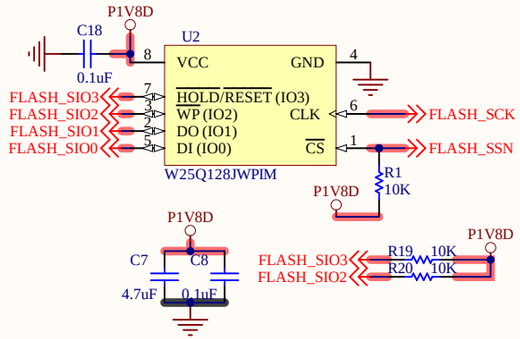
I2C and JTAG Pullups



Power/Ground



16MB qSPI Flash



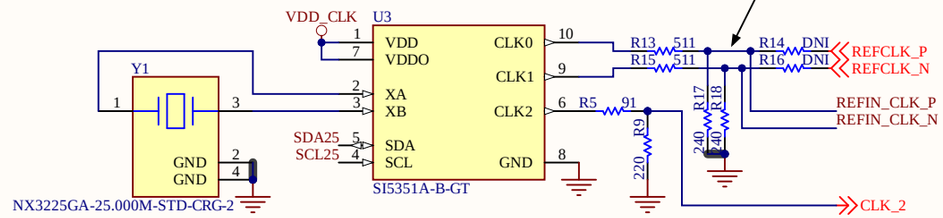
Change Summary from previous version:
- Changed Bank 1 voltage to 1.8V from 3.3V
- Changed I2C xlator part to a different one
- TBD: Change Flash to a part with DTR support
- Changed PLL output so it can drive the USB clock, eliminated an external clock output.
- Changed 25MHz crystal to higher quality part
- Added a resistor divider to convert 2.5V CMOS to 1.8V CMOS on PLL output
- Reduced # of ferrite beads and associated decoupling to match the 33U reference design for lower cost

Clock

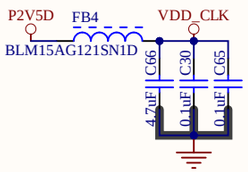
Layout Note:
Place these resistors on a T shape to minimize stubs

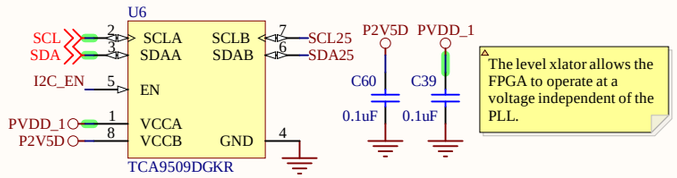
Note:
FPGA must set SRAM_DQS1 to ground for HyperRAM!

Note:
The resistor divider converts single ended to differential. See the Si5351 datasheet for details



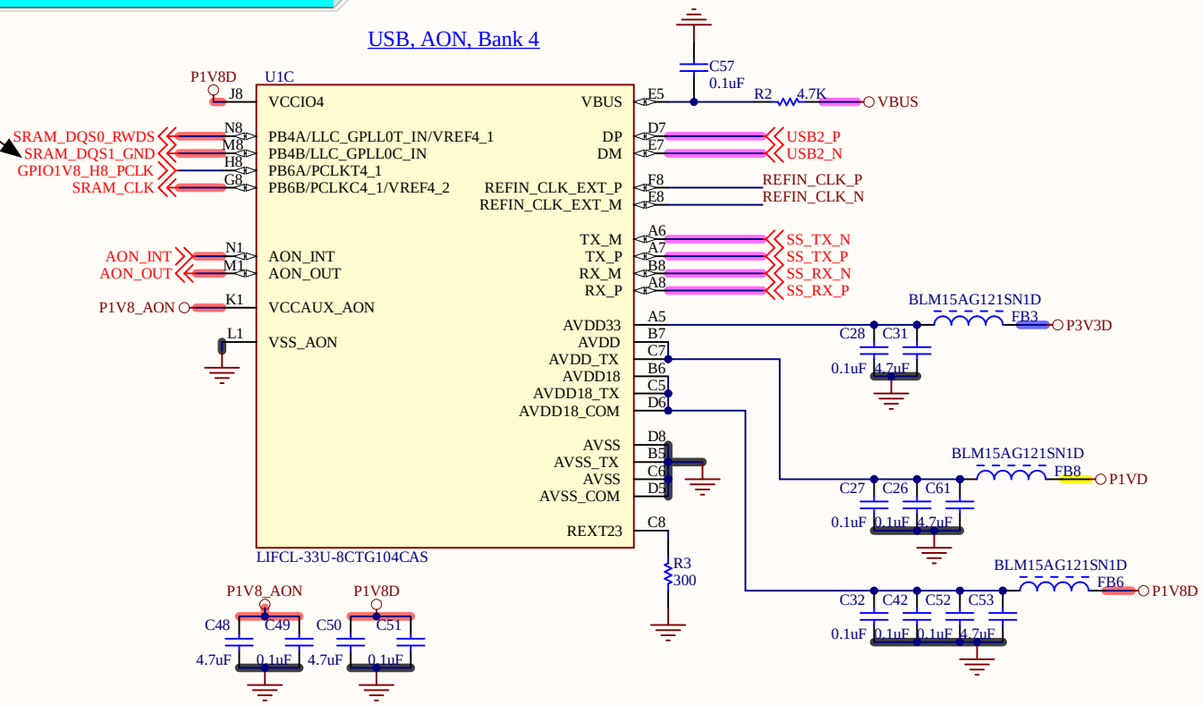
Note:
The resistor divider converts 2.5V CMOS to 1.8V CMOS.



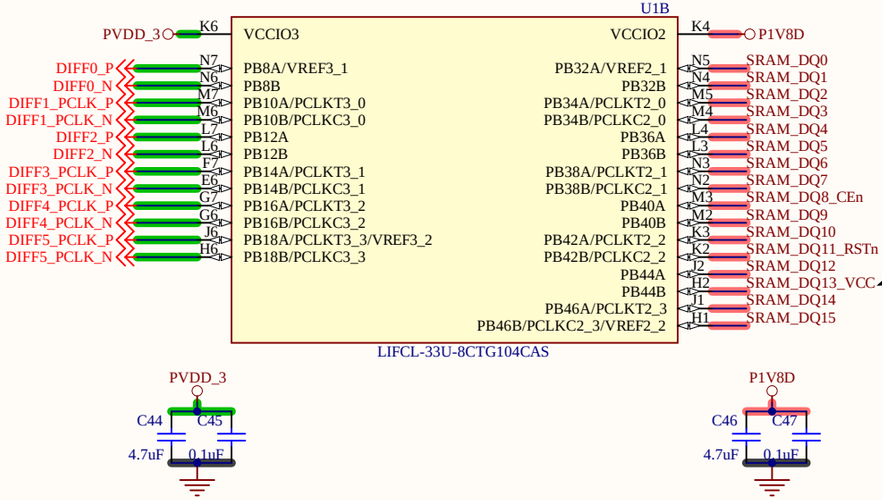


The level xlator allows the FPGA to operate at a voltage independent of the PLL.

USB, AON, Bank 4

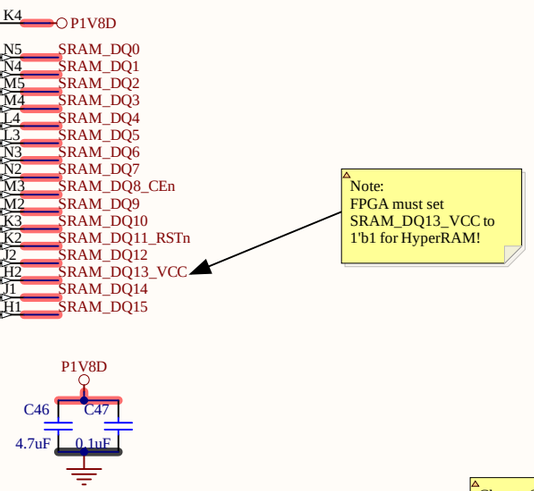


Bank 3: External Interface



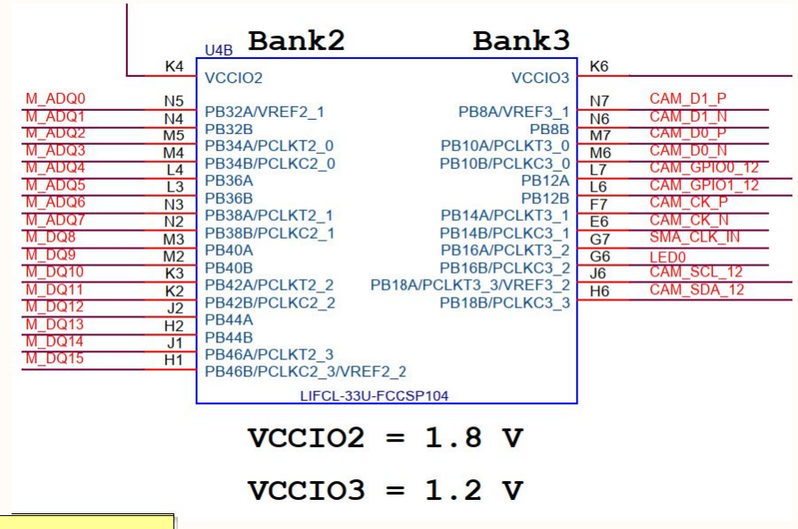
Layout: Length match all Bank 2 diff pairs with 1mm

Bank 2: 32MB oSPI/HyperRAM



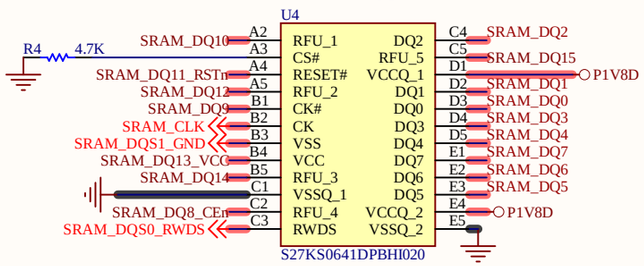
Note:
FPGA must set SRAM_DQ13_VCC to 1'b1 for HyperRAM!

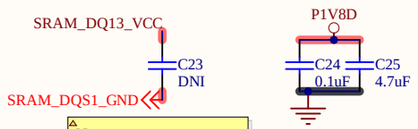
Layout: Length match SRAM_CLK to data lanes within 0.1mm



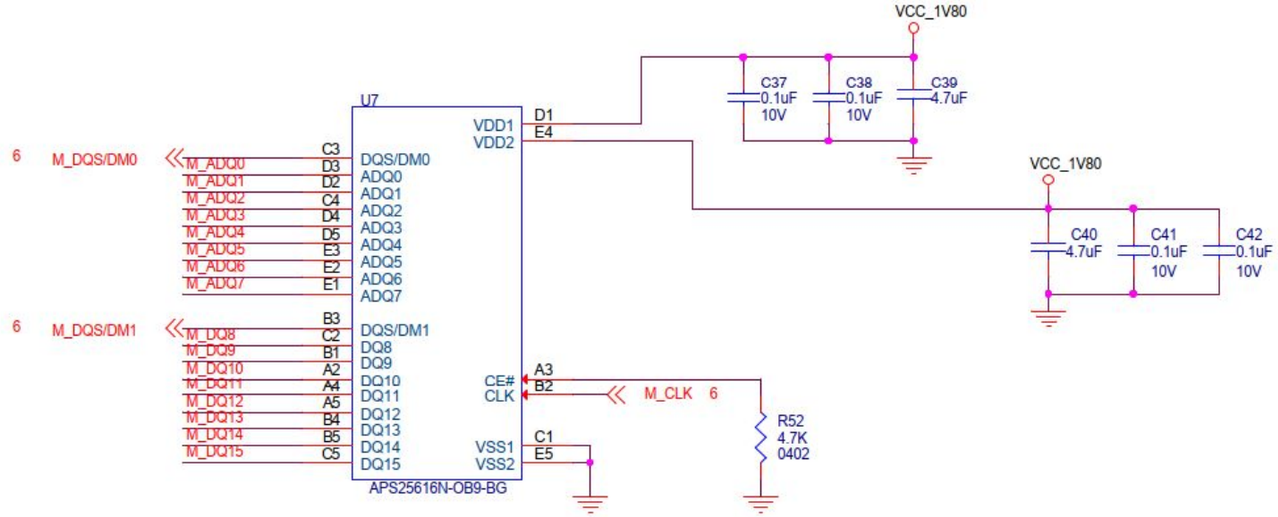
Change Summary from previous version:
- Swapped Bank 2 and 3.
- Added 16 bit memory support with pin compatible footprint for the HyperRAM/APMemory BGA device.

16 wide SRAM/HyperRAM

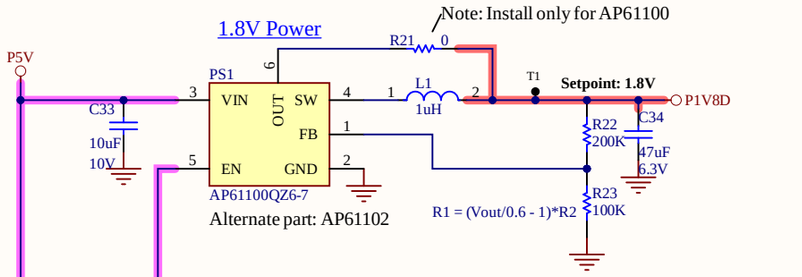




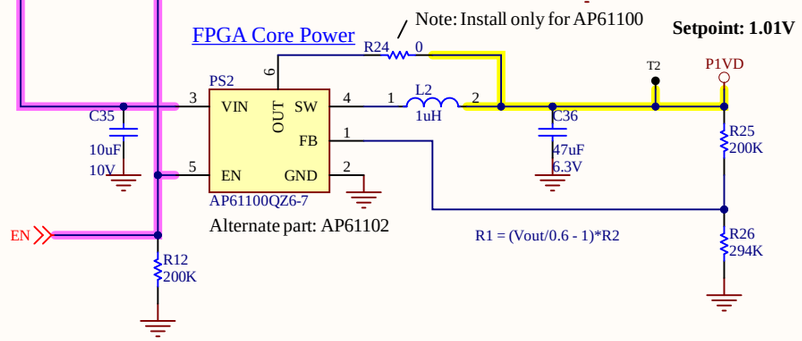
Note:
Install this capacitor for HyperRAM which needs decoupling on these pins.



1.8V Power



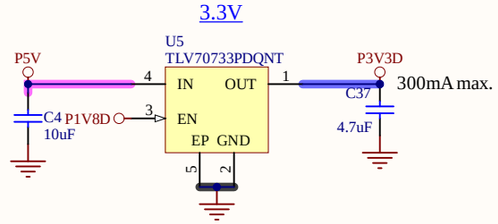
FPGA Core Power



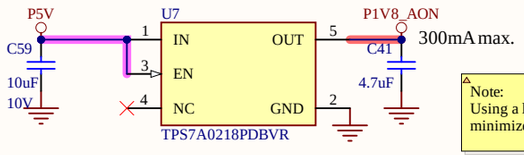
Power Modes:
OFF: EN < 0.9V, uA level current
PWM Mode: 0.91 (type) < EN < P5V-200mV
PFM Mode: P5V-200mV < EN < P5V

Change Summary from previous version:
- Changed 3.3V switcher to 1.8V output
- 3.3V now supplied by an LDO as very little runs on it
- 1.8V AON uses a lower Iq part
- Added 2.5V LDO for the PLL so it can supply a diff clock to the USB reference input

3.3V



1.8V Always On



Note:
Using a low Iq LDO here to minimize AON power

2.5V supply for Clock output