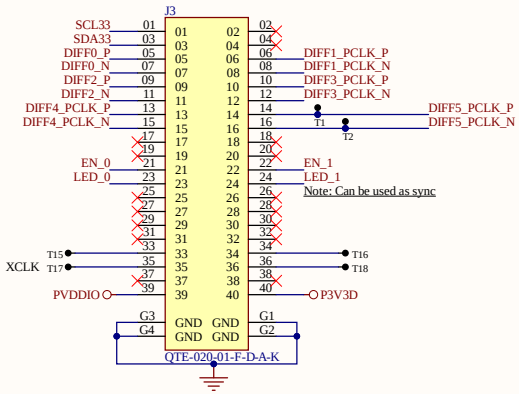
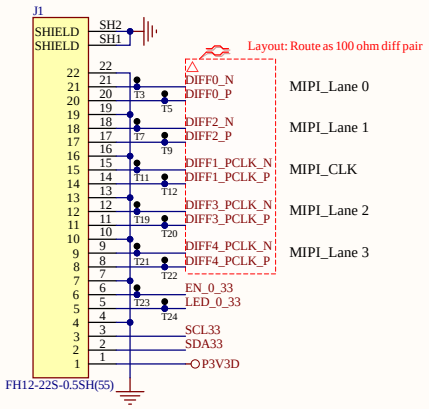
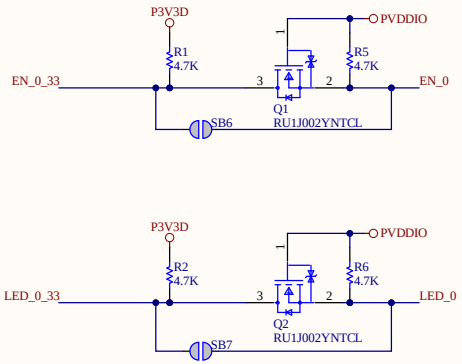
Syzygy Connector



MIPI Sink



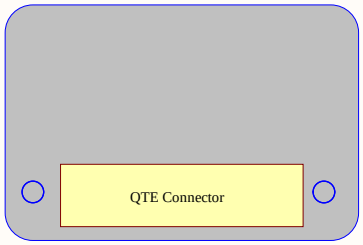
Level Translation



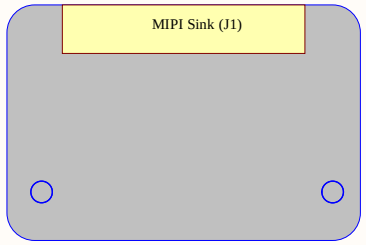
Layout Note: MIPI test points are exposed solder mask on vias

Layout Note: Place all TP's on Top side.

Bottom side:



Top Side:



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