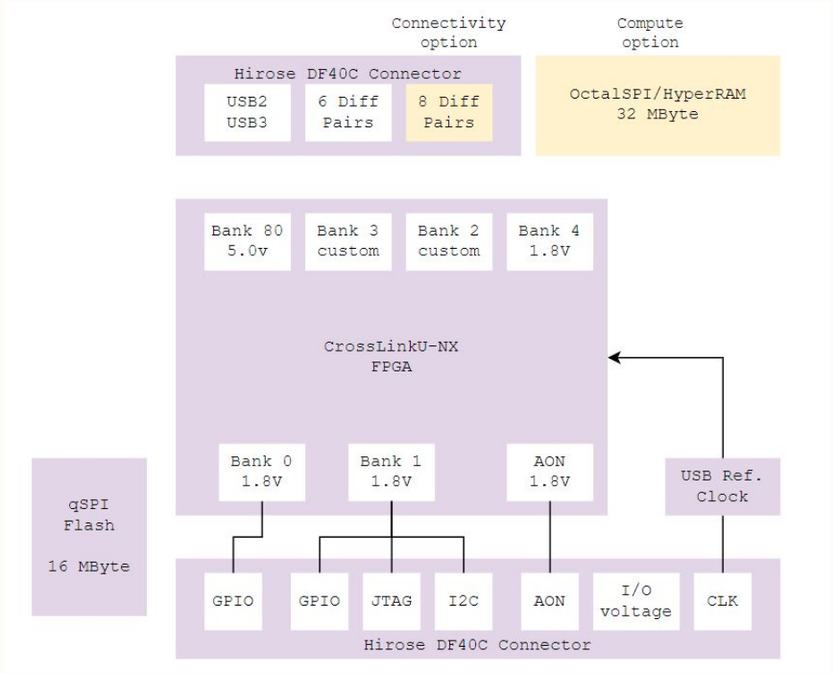
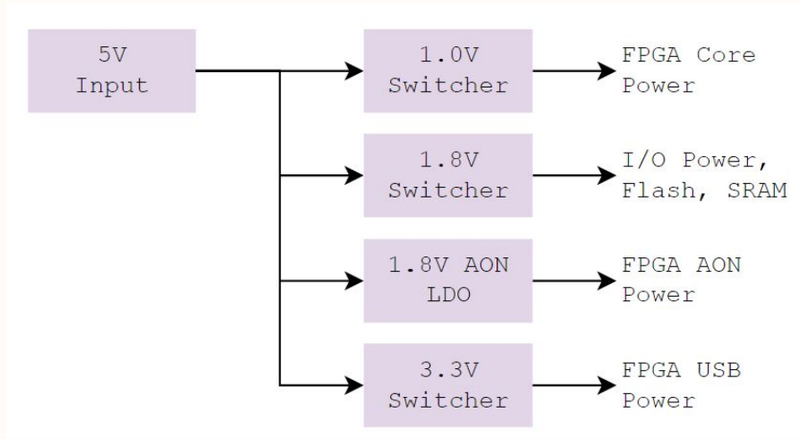
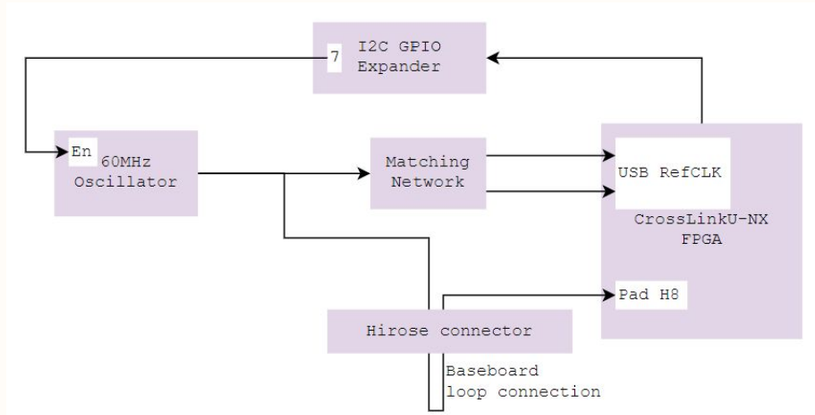
FPGA Bank Allocation



Power Distribution



Clocking



Title:	***tinyCLUNX33_Compute***		
Size: B	Number: BlockDiagram	Revision: 3.0	
Date: 21-06-2025	Time: 12:10:14	Sheet 1 of 5	
File: Block_Diagram.SchDoc			

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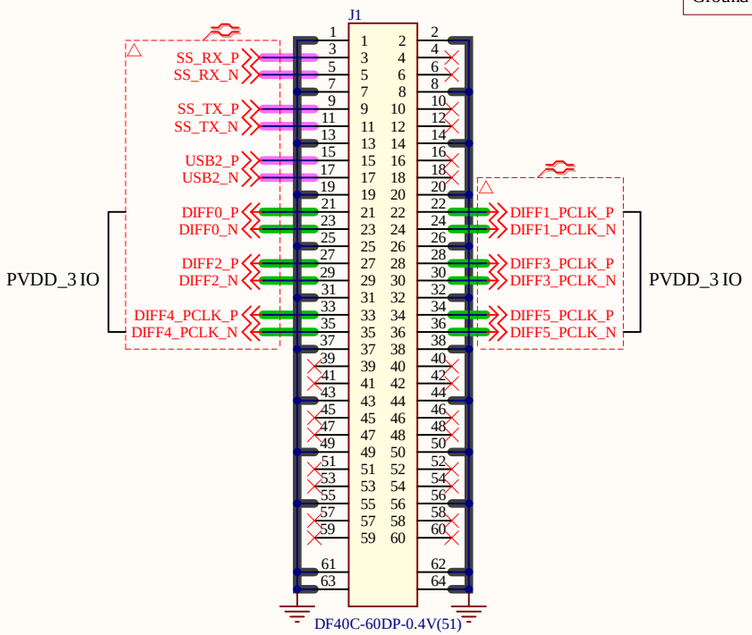
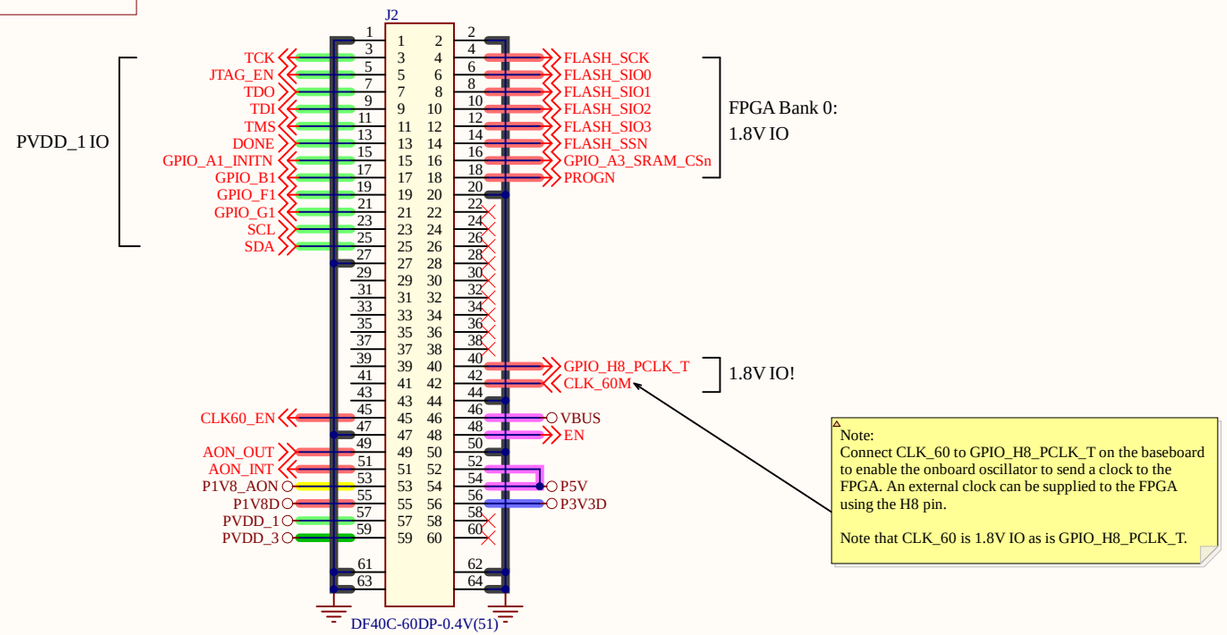
Color Legend:
3.3V IO
USB
1.8V
Bank 1 Voltage (1.2-3.3V)
Bank 2 Voltage (1.2-1.8V)
Bank 3 Voltage (1.2-1.8V)
Always ON (1.8V)
Ground

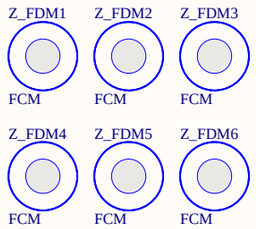




Note:
Connect CLK_60 to GPIO_H8_PCLK_T on the baseboard to enable the onboard oscillator to send a clock to the FPGA. An external clock can be supplied to the FPGA using the H8 pin.

Note that CLK_60 is 1.8V IO as is GPIO_H8_PCLK_T.

Layout note: Match diff pairs to within 1mm of each other.



Title:	***tinyCLUNX33_Compute***		
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Date: 21-06-2025	Time: 12:10:14	Sheet 2	of 5
File: Connectors_DF40.SchDoc			

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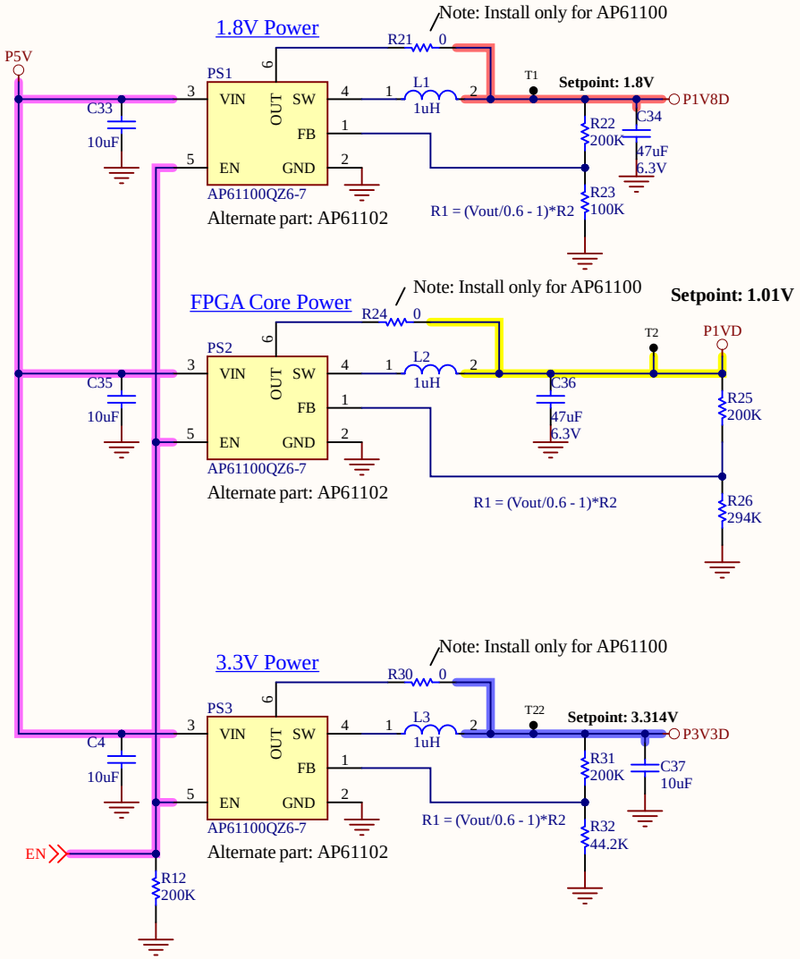
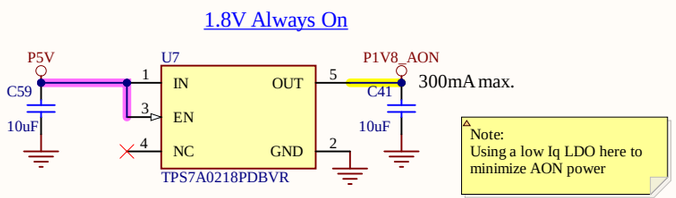


Power Modes:
OFF: EN < 0.9V, uA level current
PWM Mode: 0.91 (type) < EN < P5V-200mV
PFM Mode: P5V-200mV < EN < P5V



Note:
Using a low Iq LDO here to minimize AON power

Title: *tinyCLUNX33_Compute*			
Size: B	Number: Power	Revision: 3.0	
Date: 21-06-2025 Time: 12:10:14		Sheet 3 of 5	
File: Power.SchDoc			

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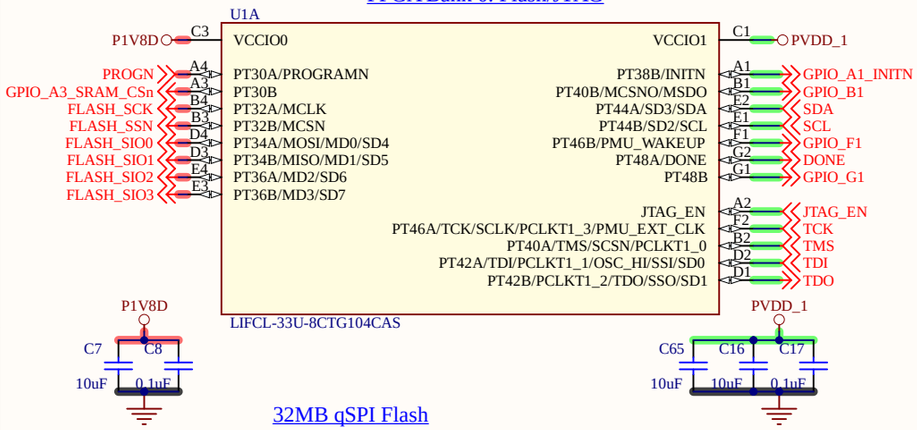
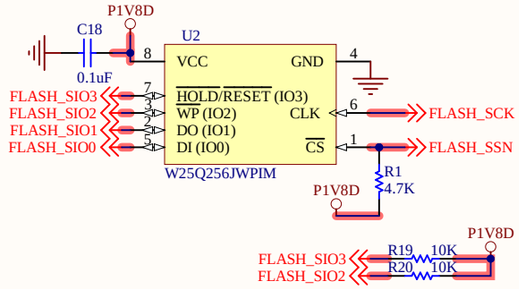
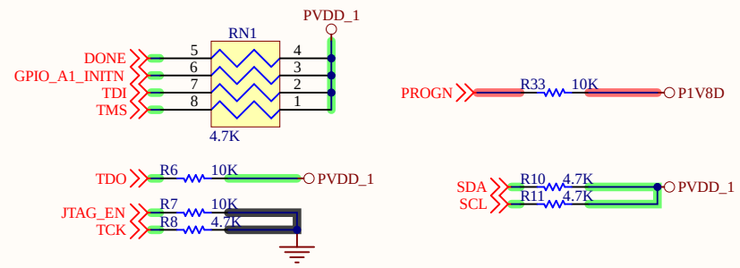
FPGA Bank 0: Flash/JTAG



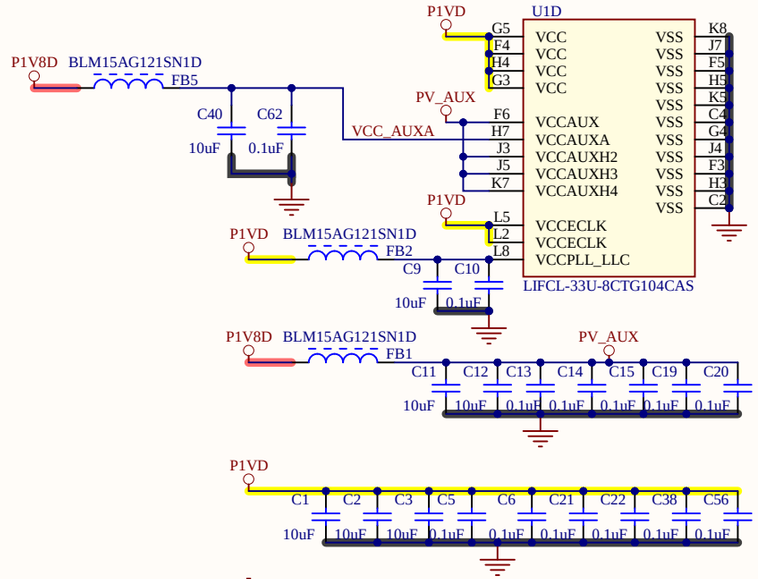
32MB qSPI Flash



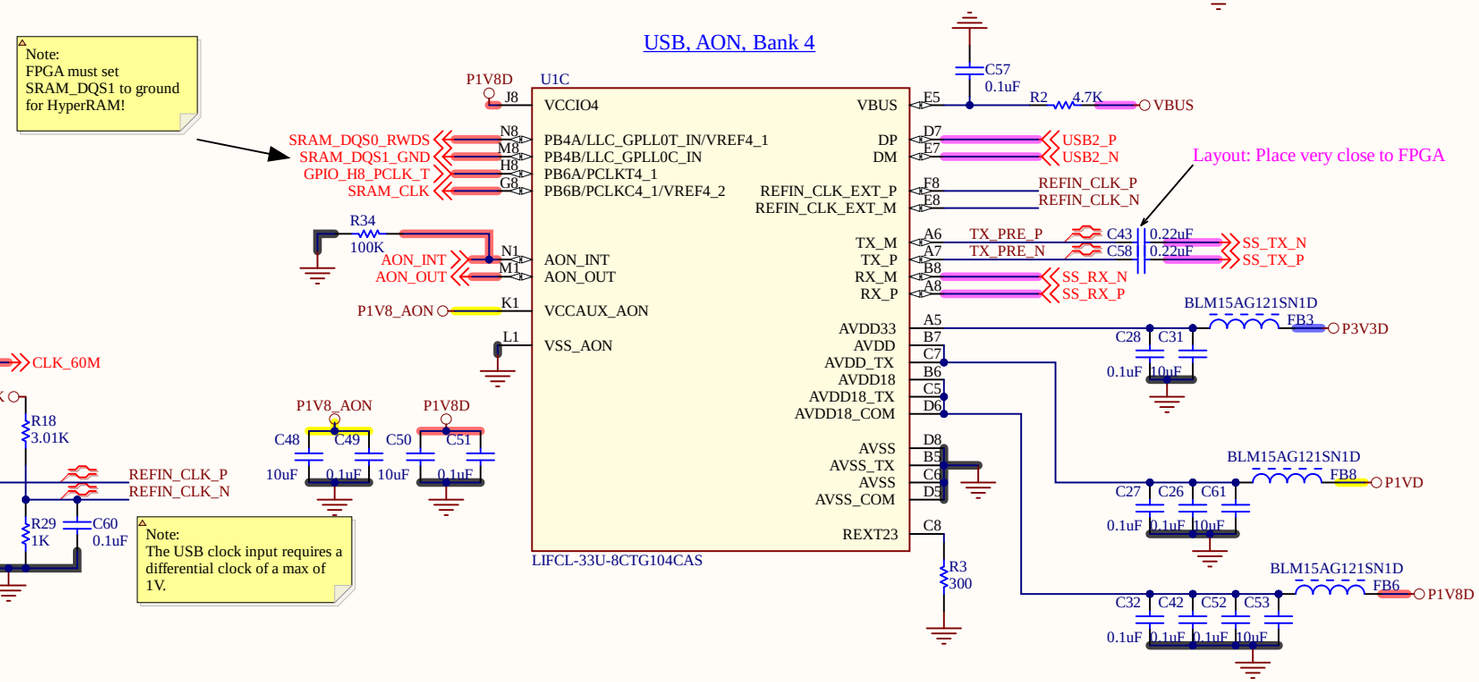
I2C and JTAG Pullups



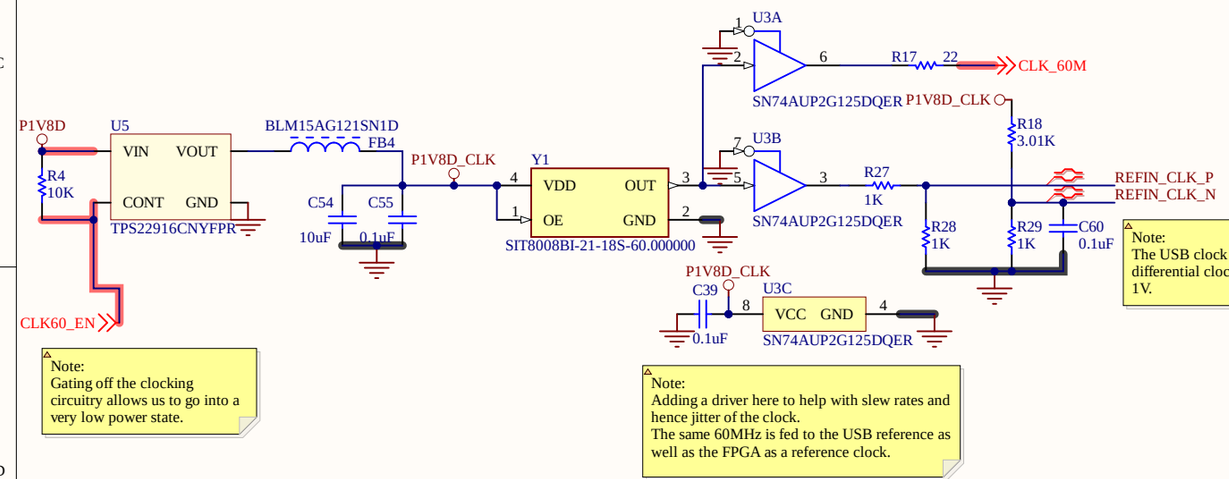
Power/Ground



USB, AON, Bank 4



Clock



Title:	*tinyCLUNX33_Compute*		
Size: B	Number: FPGA	Revision: 3.0	
Date: 21-06-2025	Time: 12:10:14	Sheet 4	of 5
File: FPGA.SchDoc			

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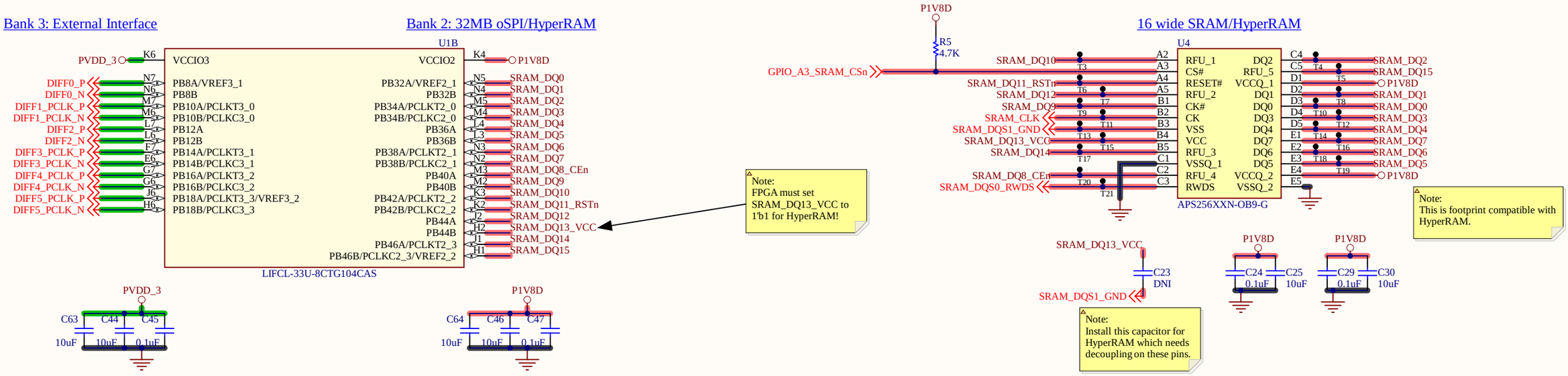
Bank 3: External Interface

Bank 2: 32MB oSPI/HyperRAM

16 wide SRAM/HyperRAM



Layout: Length match all Bank 2 diff pairs with 1mm

Layout: Length match SRAM_CLK to data lanes within 0.1mm

Layout: Test points on the SRAM_* nets are vias with cleared out solder mask

Title:	***tinyCLUNX33_Compute***		
Size: B	Number: FPGA_BANKS	Revision: 3.0	
Date: 21-06-2025	Time: 12:10:15	Sheet 5	of 5
File: FPGA_Bank_2_3_I2C.SchDoc			

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