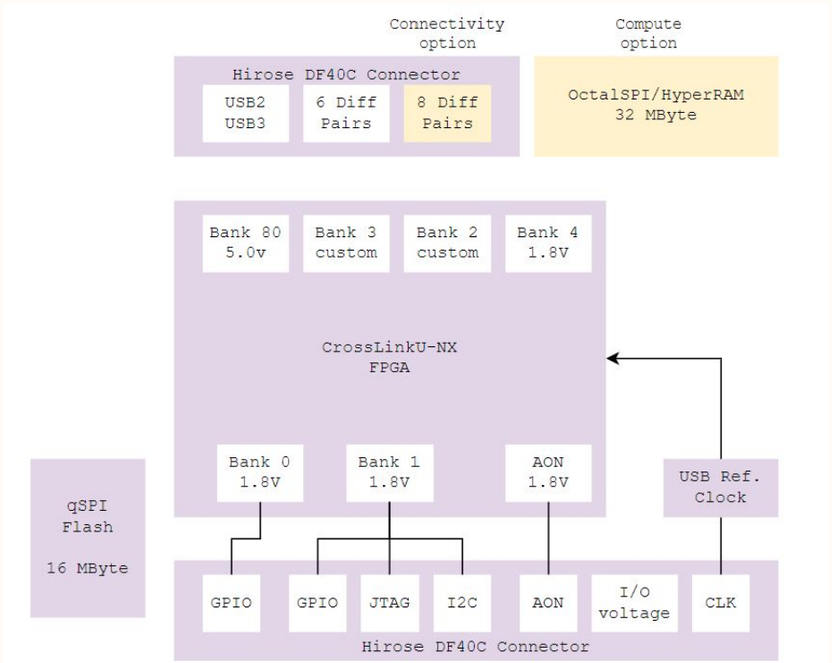
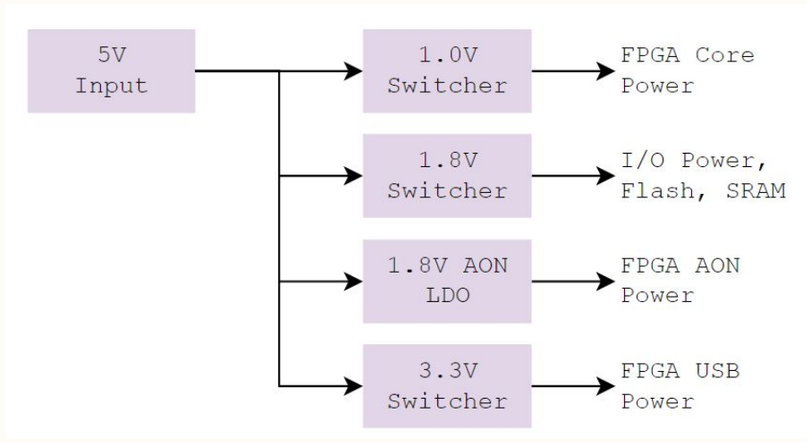
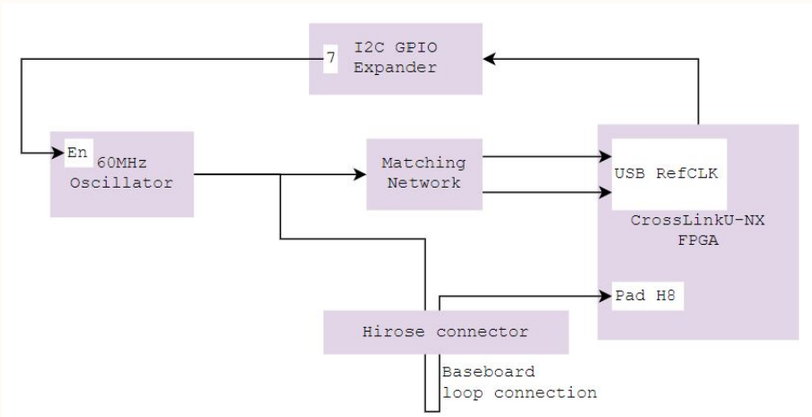
FPGA Bank Allocation



Power Distribution

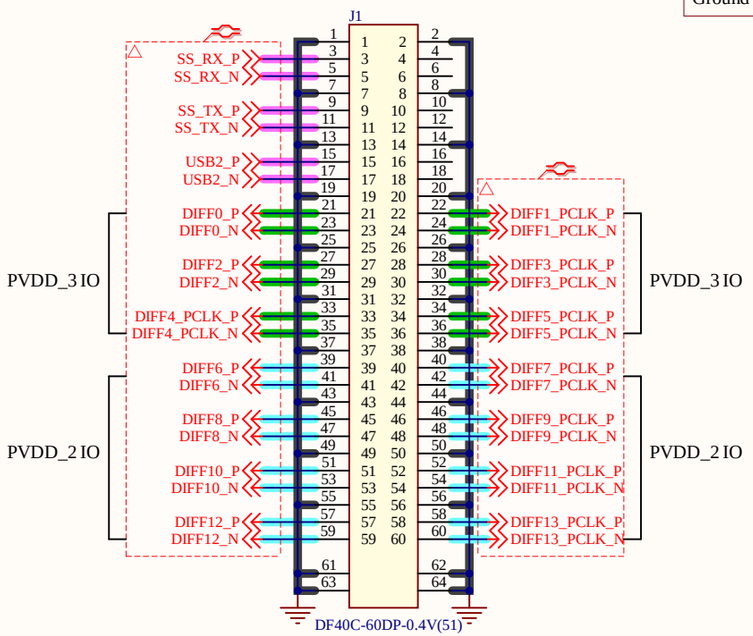


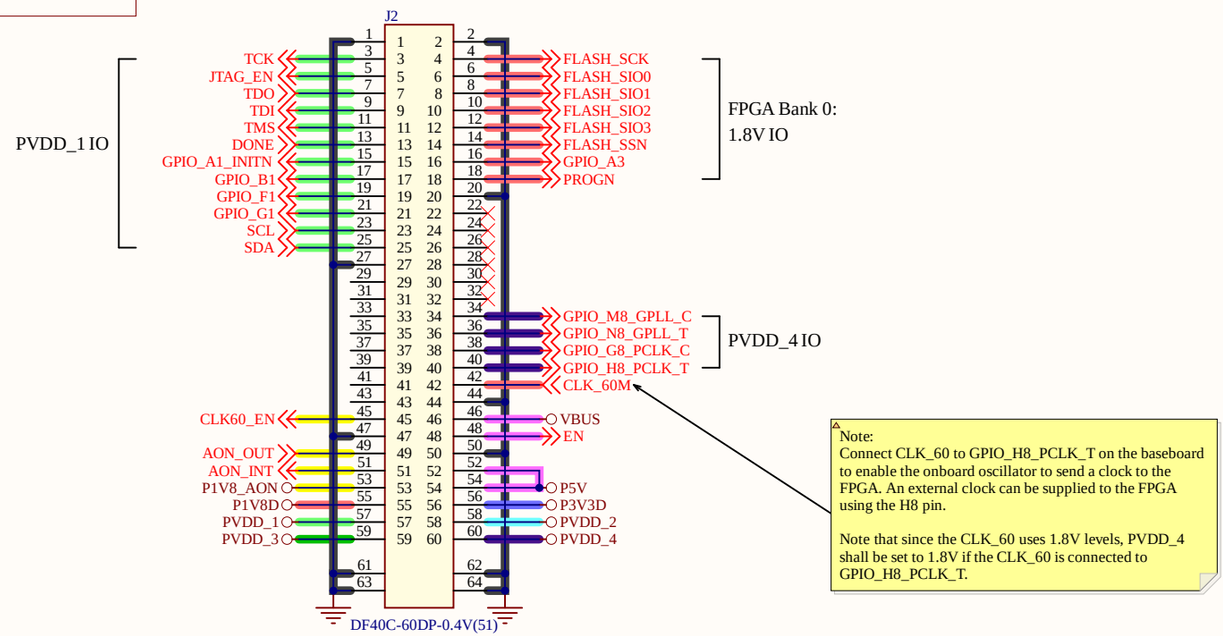
Clocking



Title: *tinyCLUNX33_Connectivity*			tinyvision.ai
Size: B	Number: BlockDiagram	Revision: 3.0	
Date: 21-06-2025 Time: 12:30:43		Sheet 1 of 5	
File: Block_Diagram.SchDoc			

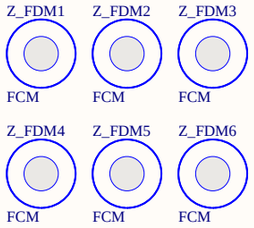
Color Legend:
3.3V IO
USB
1.8V
Bank 1 Voltage (1.2-3.3V)
Bank 2 Voltage (1.2-1.8V)
Bank 3 Voltage (1.2-1.8V)
Always ON (1.8V)
Ground



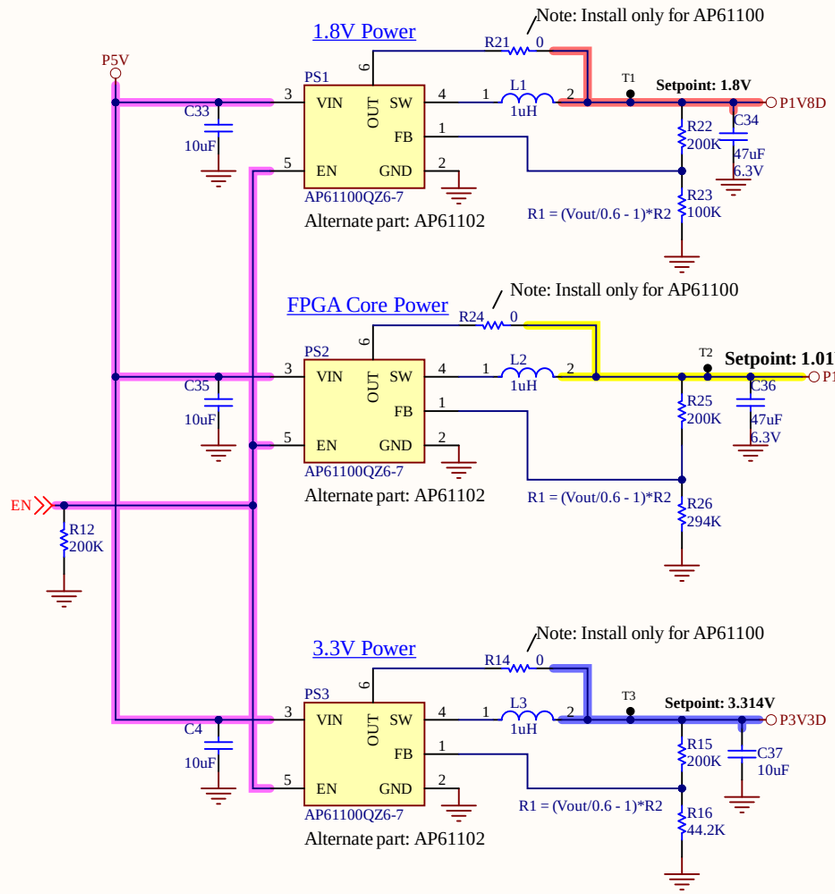


Note:
Connect CLK_60 to GPIO_H8_PCLK_T on the baseboard to enable the onboard oscillator to send a clock to the FPGA. An external clock can be supplied to the FPGA using the H8 pin.

Note that since the CLK_60 uses 1.8V levels, PVDD_4 shall be set to 1.8V if the CLK_60 is connected to GPIO_H8_PCLK_T.



Title: *tinyCLUNX33_Connectivity*			
Size: B	Number: Connector	Revision: 3.0	tinyvision.ai
Date: 21-06-2025 Time: 12:30:43		Sheet 2 of 5	
File: Connectors_DF40.SchDoc			



Power Modes:
OFF: EN < 0.9V, uA level current
PWM Mode: 0.91 (type) < EN < P5V-200mV
PFM Mode: P5V-200mV < EN < P5V

Title:	***tinyCLUNX33_Connectivity***		
Size: B	Number: Power	Revision: 3.0	
Date: 21-06-2025	Time: 12:30:43	Sheet 3	of 5
File: Power.SchDoc			

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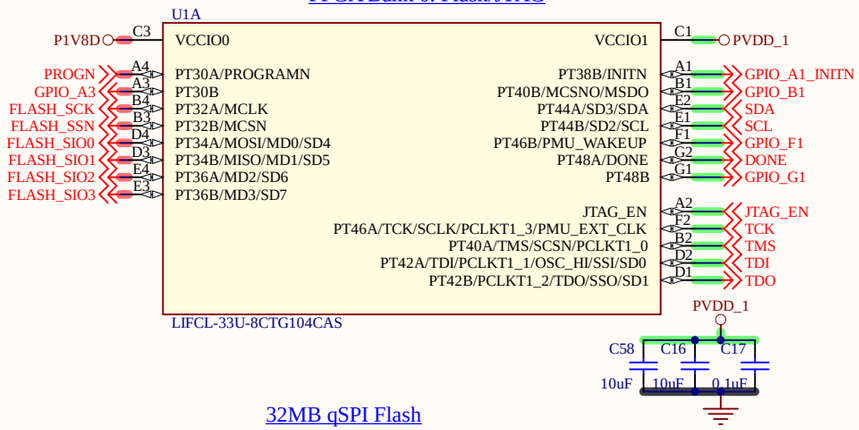
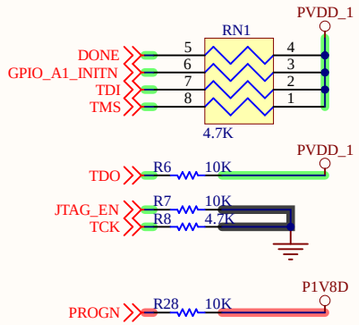
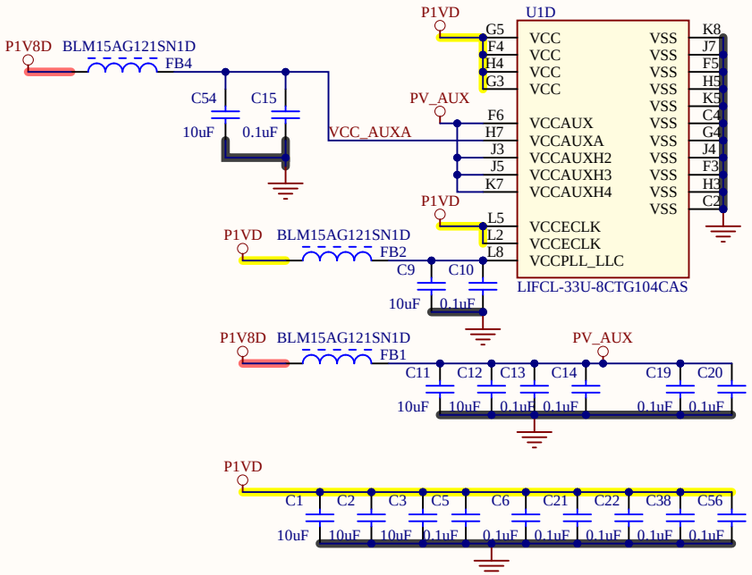
FPGA Bank 0: Flash/JTAG



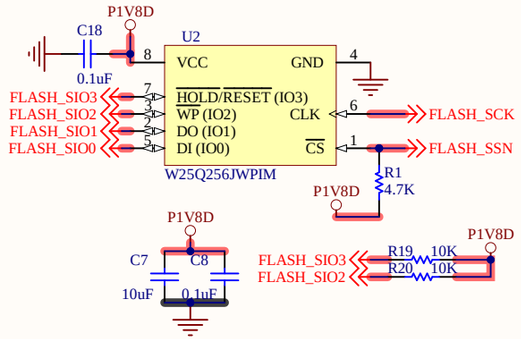
JTAG Pullups



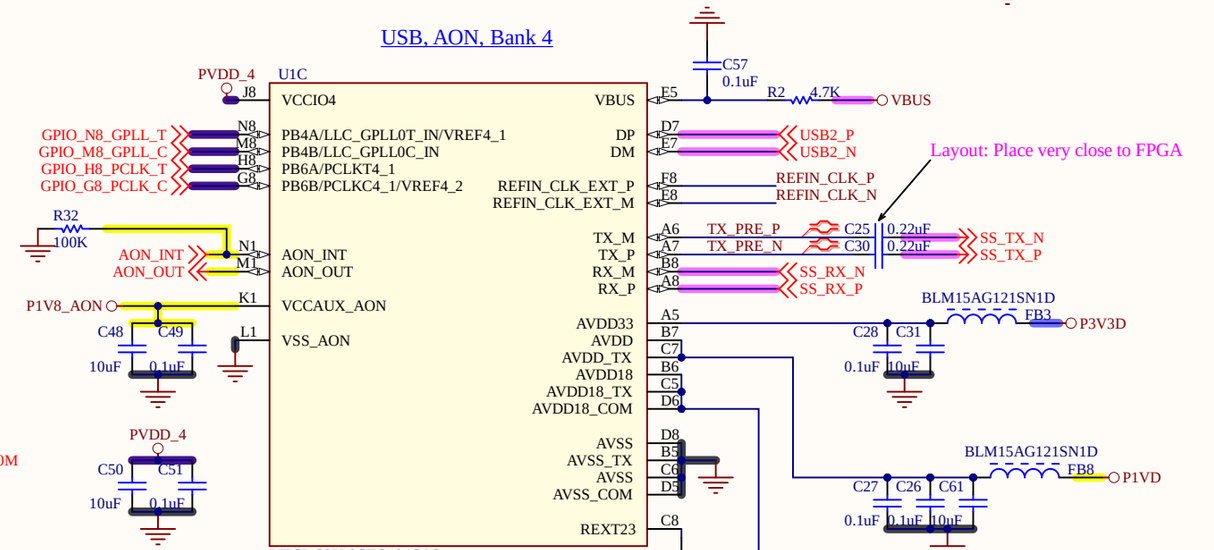
Power/Ground



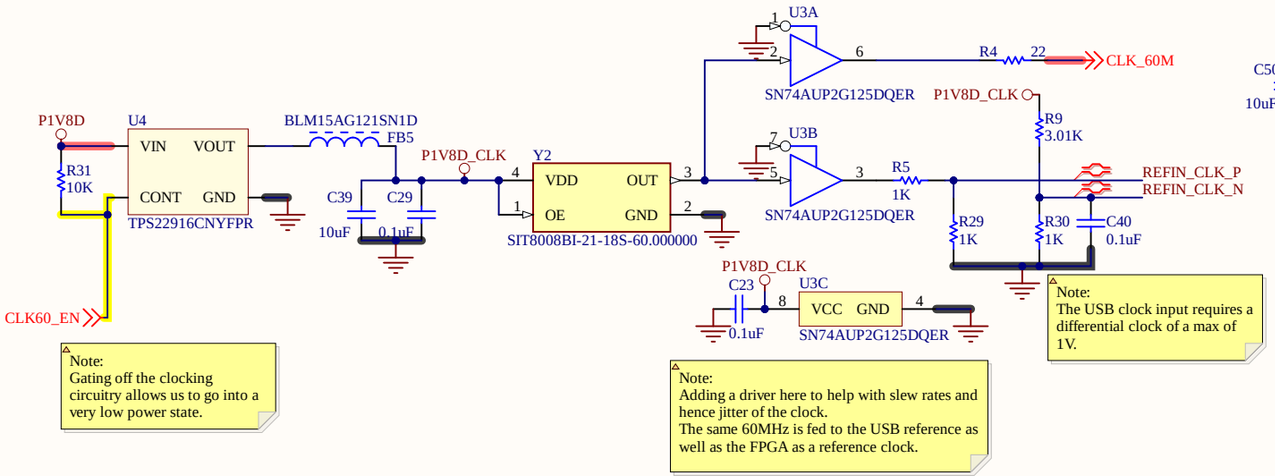
32MB qSPI Flash



USB, AON, Bank 4



Clock



Title:	*tinyCLUNX33_Connectivity*		
Size: B	Number: FPGA	Revision: 3.0	
Date: 21-06-2025	Time: 12:30:44	Sheet 4	of 5
File: FPGA.SchDoc			

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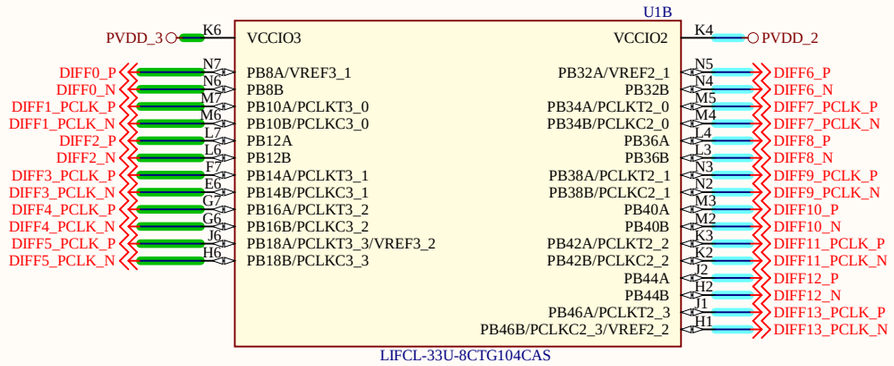
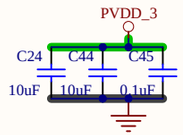
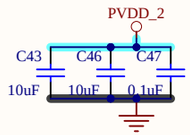
Bank 3: External Interface

Bank 2: External Interface







Layout: Length match all Bank 2 diff pairs with 1mm

Layout: Length match SRAM_CLK to data lanes within 0.1mm

Title:	***tinyCLUNX33_Connectivity***		
Size: B	Number: FPGA_BANKS	Revision: 3.0	
Date: 21-06-2025	Time: 12:30:44	Sheet 5	of 5
File:	FPGA_Bank_2_3_I2C.SchDoc		

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