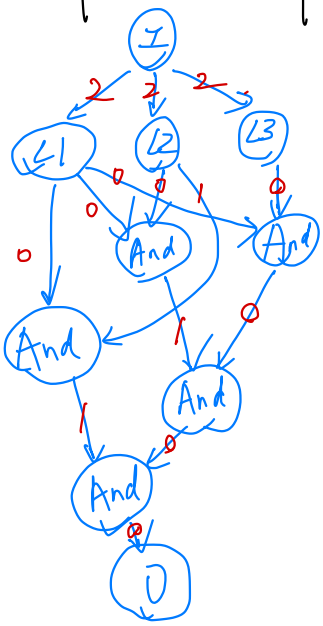
Type 1: And gate as vertices (node)

Inverter gate as Edge.

Example: one expression of SR3



One-hot encoding

Node: 1. Input (Virtual single input) — [0 0 0 1]

2. Literal (# used variables) — [0 0 1 0]

3. And gate — [0 1 0 0]

4. Output — [1 0 0 0]

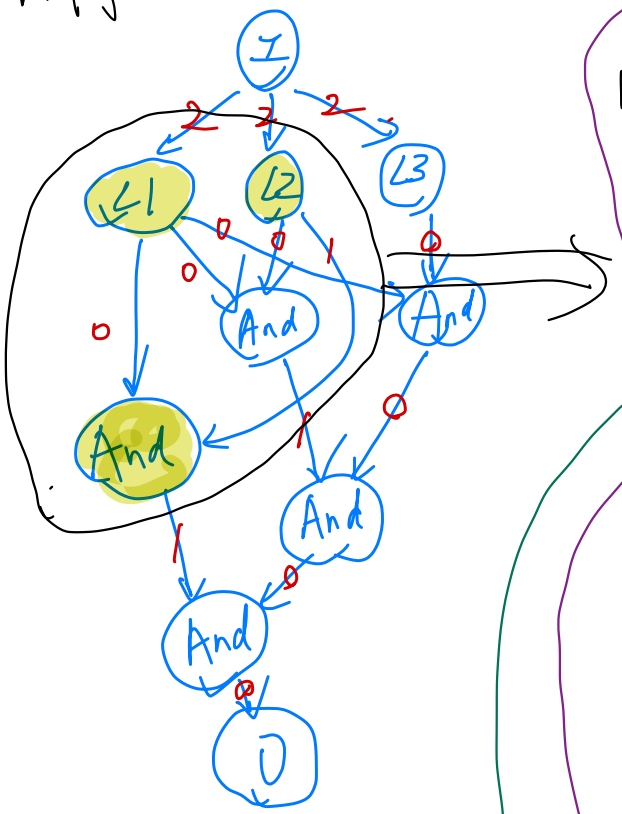
Edge: 0: straight-through — [0 0 1]

1: inverter — [0 1 0]

2. virtual edge — [1 0 0]

(from Input node to Literal node)

Propagation:



$h_1 \in \mathbb{R}^{64}$ (L1) $h_2 \in \mathbb{R}^{64}$ (L2)

0 = [0 0 1] 1 = [0 1 0]

And

$h_3 = 0^{64}$

$(x_1 \wedge \overline{x_2})$

cat h_1 and [0 0 1] $\Rightarrow h_1'$

$h_1' = \text{cat}(h_1, [0\ 0\ 1]) \in \mathbb{R}^{67}$

gated output = sigmoid $(FC(h_1')) \in \mathbb{R}^{64}$

mapper output $= FC(h_1') \in \mathbb{R}^{64}$

$\Downarrow$

$\text{Scaled}(h_1) \in \mathbb{R}^{64}$

$\text{Scaled}(h_2) \in \mathbb{R}^{64}$

$h_{in} = \text{Scaled}(h_1) + \text{Scaled}(h_2)$

$h_3 = GRU(x_3, h_{in})$

$[0\ 1\ 0\ 0]$ Obtained before.

⇓

Updated the hidden state of AND Gate.

Reasons: Inverter:

$gated(h_i) = sigmoid(FC(h_1, [0\ 1\ 0]))$

Non-Inverter:

$gated(h_i) = sigmoid(FC(h_1, [0\ 0\ 1]))$

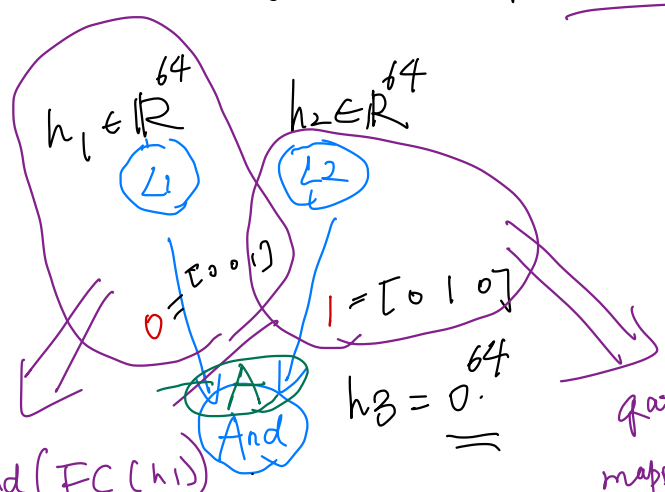
Such one-hot vector can act as Indicator.

Make the hidden state of previous nodes act differently.

Same idea: C-VAE. the class information is also encoded as one-hot vector and concatenated with hidden states.

Type 2: And gate as vertices (node)

Inverter gate as Edge. just Negate the hidden state.



gated(h_1) = sigmoid(FC(h_1))

mapper(h_1) = FC(h_1)

Inverter:

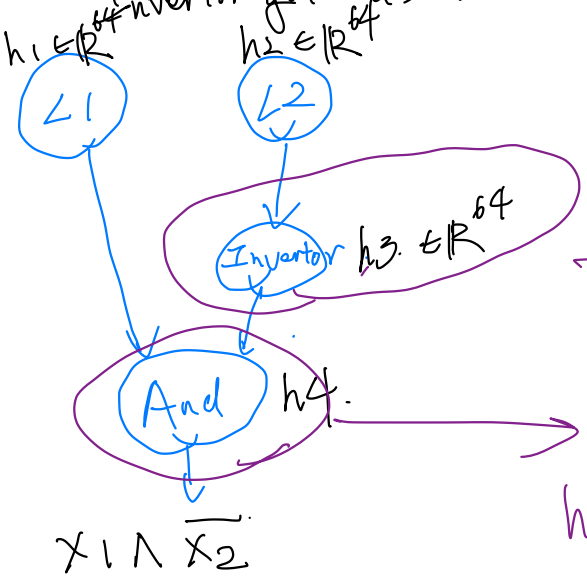
gate(h_2) = sigmoid(FC($-h_2$))

mapper(h_2) = FC($-h_2$)

Type 3 :

And gate

Inverter gate as vertices.



$h_3 = GRU(x_3, h_2)$

$h_4 = GRU(x_4, h_4^{in})$

$h_4^{in} = \sum_{i=1,3} gated(h_i) \odot mapper(h_i)$