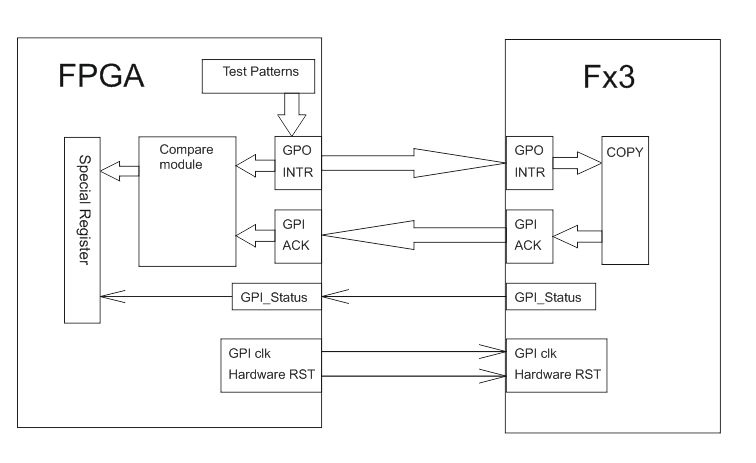
28/08/19

In order to provide full test coverage we have to check connection between FPGA and FX3 chip.

There are several options how to implement such functionality with minimum efforts. FX3 GPIO module are very flexible so we’re going to put it in the simple GPIO mode. This will provide us ability to set any values at input pins of FX3, copy these values to the outputs using special FX3 firmware.



Requirements:

[R-01] FPGA MUST provide clock frequency (40MHz) at the FX3\_PCLK pin

[R-02] FPGA MUST provide reset signal (active high) at the FX3\_RST pin. Duration must be no less than 200us

[R-03] FPGA MUST provide INTR signal (active edge is falling) at the FX3\_GPIO23 to latch test data values in the FX3

[R-04] FPGA MUST latch result values on the falling edge of FX3\_GPIO26

[R-05] FPGA MUST apply at least 4 different test pattern

[R-06] FPGA MUST apply each test pattern at least 1 times

[R-07] FPGA MUST compare test and result values and put “pass” or “fail” to a special register

[R-08] FPGA MUST monitor USB\_CABLE which informs about USB cable connection

[R-09] FPGA MUST check FX3\_GPIO57 pin if USB\_CABLE is ‘1’ for 100us and copy its value to a special register

[R-10] FPGA testbench SHOULD be provided

Table 1. Connection between FPGA and FX3 chip

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| FPGA pin name | FX3 pin name | Function in regular FPGA FW | Direction | Function in test FPGA FW |
| FX3\_DQ[15:0] | GPIO[15:0] | GPIF | IO | GPI[15:0] |
| FX3\_DQ[27:16] | GPIO[44:33] | GPIF | IO | GPO[11:0] |
| FX3\_DQ[31:28] | GPIO[49:46] | GPIF | IO | GPO[15:12] |
| FX3\_PCLK | GPIO[16] | GPIF clock | O | GPI clk |
| FX3\_CSn | GPIO[17] | GPIF CS | O | GPO[16] |
| FX3\_WRn | GPIO[18] | GPIF WR | O | GPI[16] |
| FX3\_OEn | GPIO[19] | GPIF OE | O | GPO[17] |
| FX3\_RDn | GPIO[20] | GPIF RD | O | GPI[17] |
| FX3\_FL\_A | GPIO[21] | GPIF Flag (GPIO) | I | GPO[18] |
| FX3\_FL\_B | GPIO[22] | GPIF Flag (GPIO) | I | GPI[18] |
| FX3\_GPIO23 | GPIO[23] | INTR (GPIO) | O | INTR |
| FX3\_PENDn | GPIO[24] | GPIF PEND | O | GPI[19] |
| FX3\_GPIO25 | GPIO[25] | RST (GPIO) | I | GPO[19] |
| FX3\_GPIO26 | GPIO[26] | GPIO | I | ACK |
| FX3\_FL\_C | GPIO[27] | GPIF Flag (GPIO) | I | GPO[20] |
| FX3\_ADDR1 | GPIO[28] | GPIF ADDR | O | GPI[20] |
| FX3\_ADDR0 | GPIO[29] | GPIF ADDR | O | GPO[21] |
| FX3\_MEM\_CLK | GPIO[53] | SPI CLK | O | GPI[21] |
| FX3\_MEM\_SSN | GPIO[54] | SPI CS | O | GPO[22] |
| FX3\_MEM\_DO\_TXD | GPIO[55] | SPI DO/UART TXD | O | GPI[22] |
| FX3\_MEM\_DI\_RXD | GPIO[56] | SPI DI/UART RXD | I | FX3 Ready |
| FX3\_GPIO57 | GPIO[57] | USB Speed (GPIO) | I | GPI Status |
| FX3\_RST | HW\_RST | Hardware RST | O | Hardware RST |