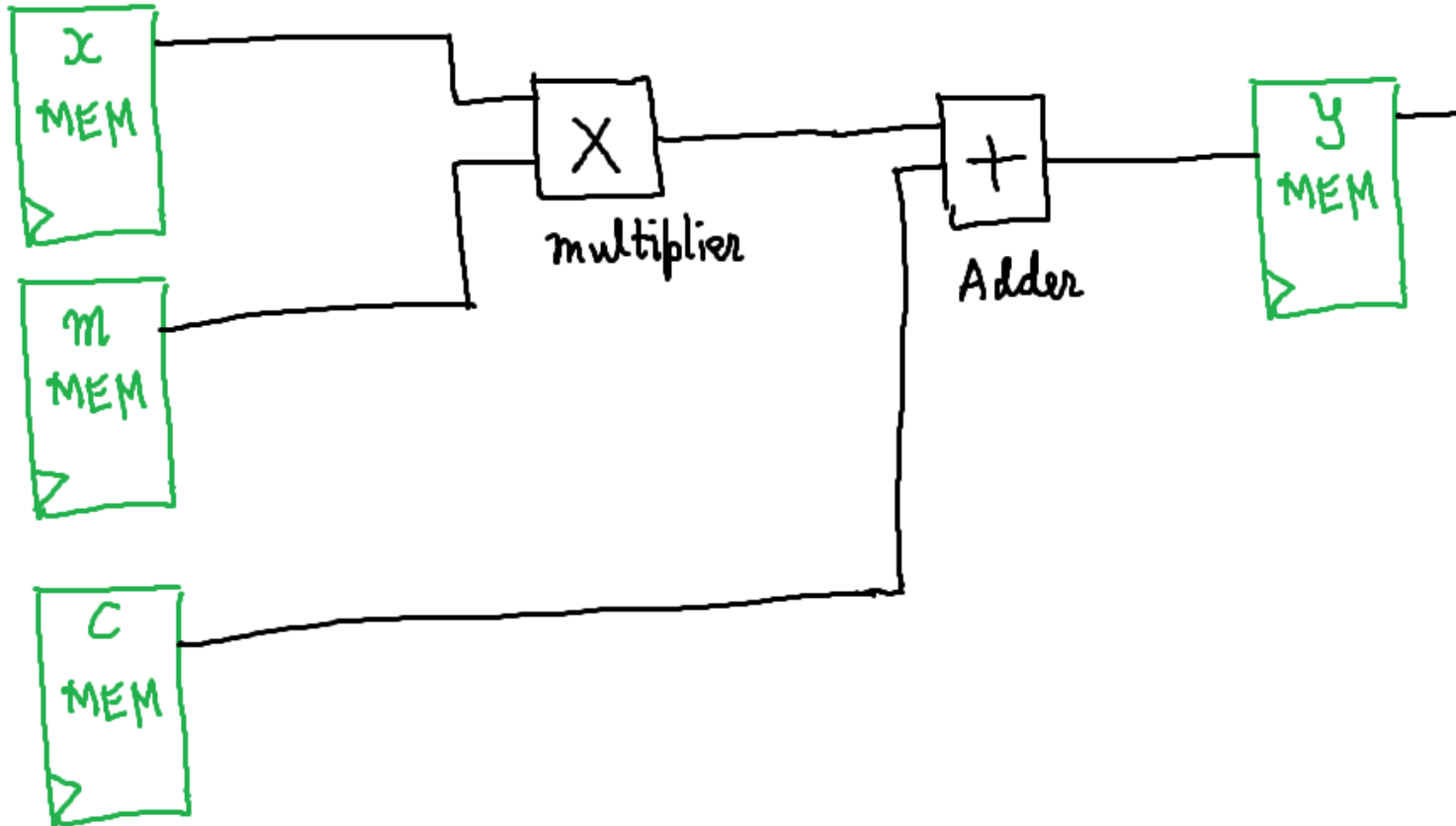


Pipelining and Parallel Processing

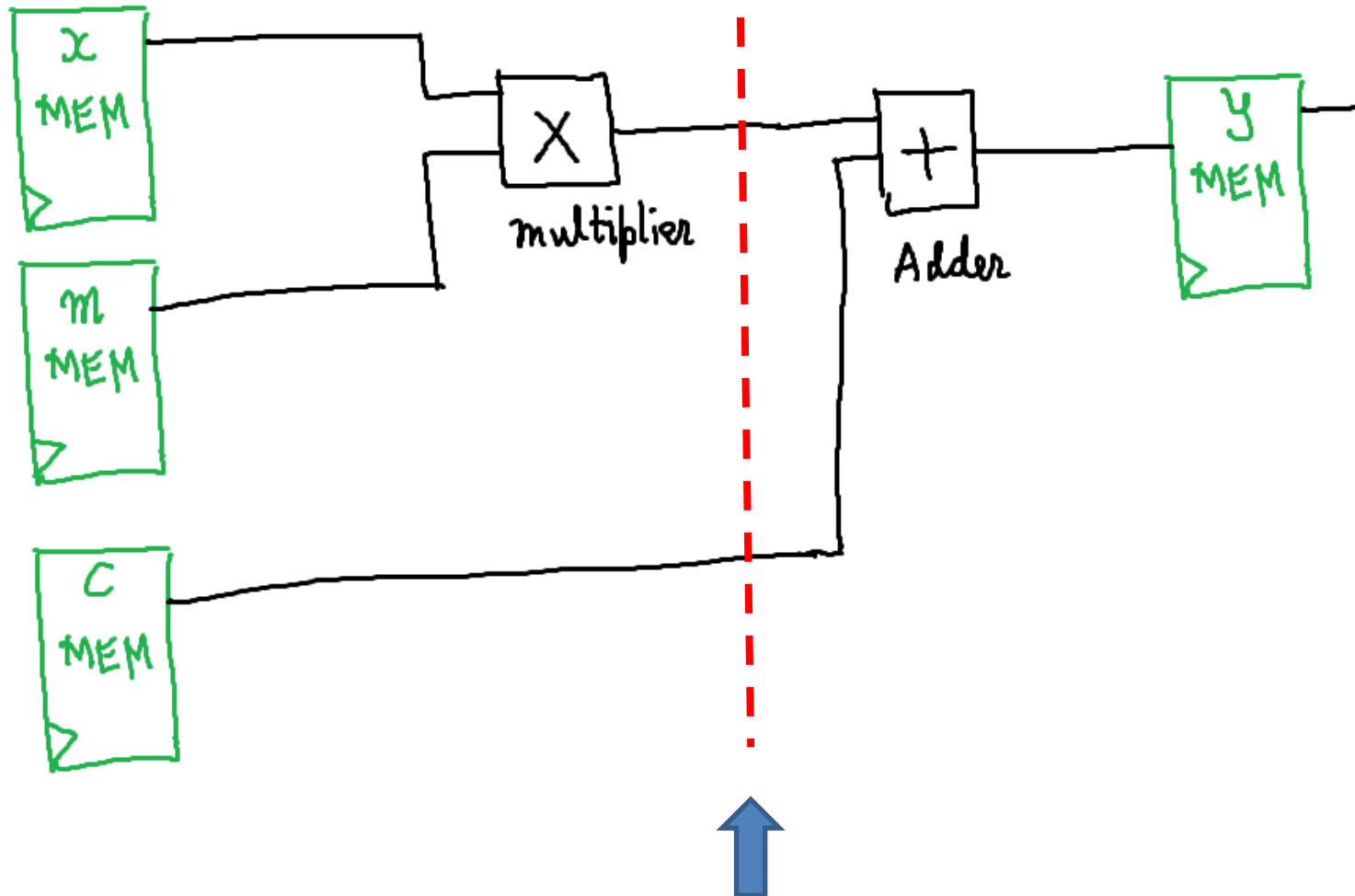
1-Stage (non-pipelined)

$$y_i = (m_i \times x_i) + c_i$$



Decompose into more stages: How?

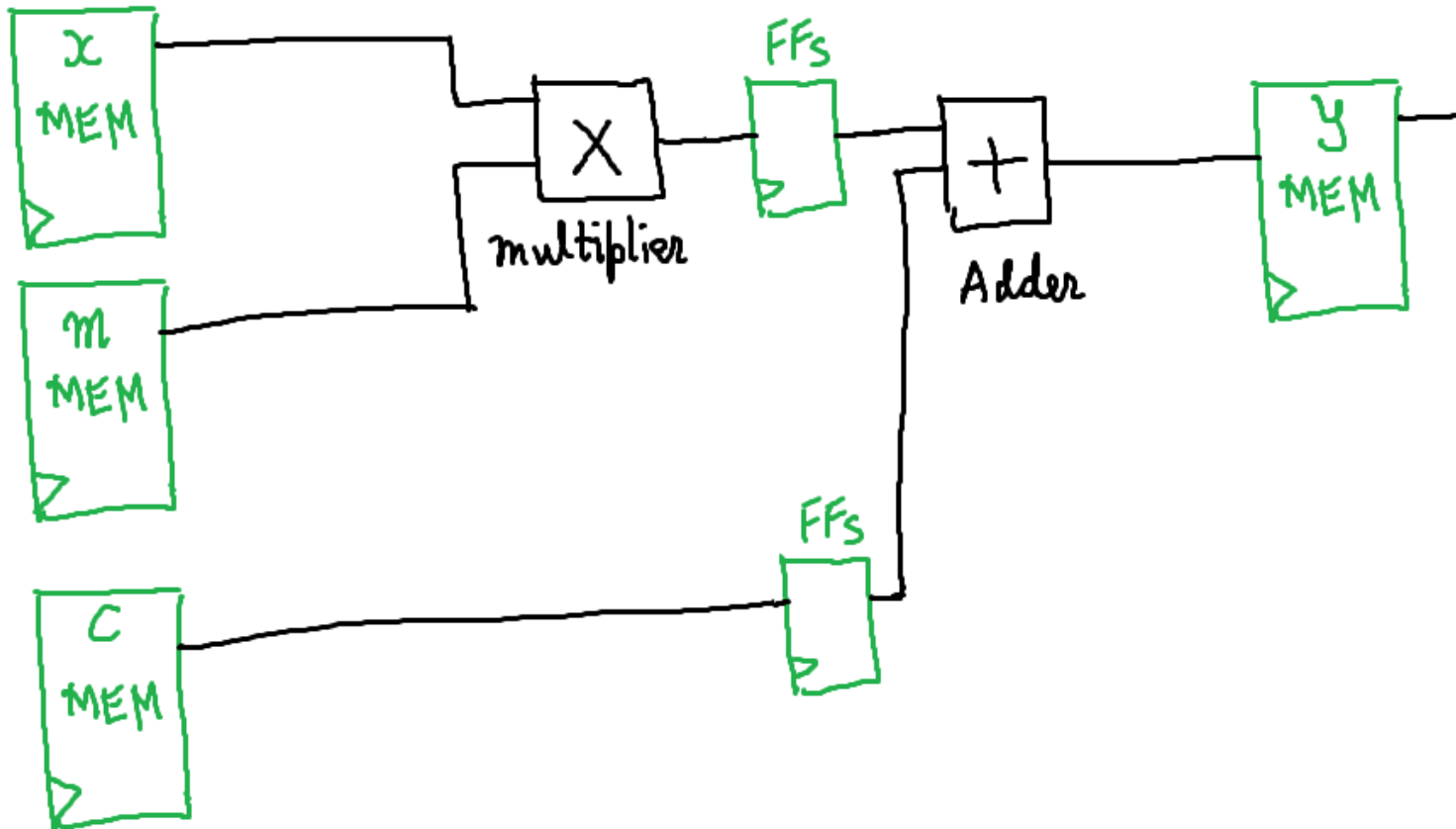
$$y_i = (m_i \times x_i) + c_i$$



Cut here for introducing the
FFs/Register

2-Stage Pipelined

$$y_i = (m_i \times x_i) + c_i$$



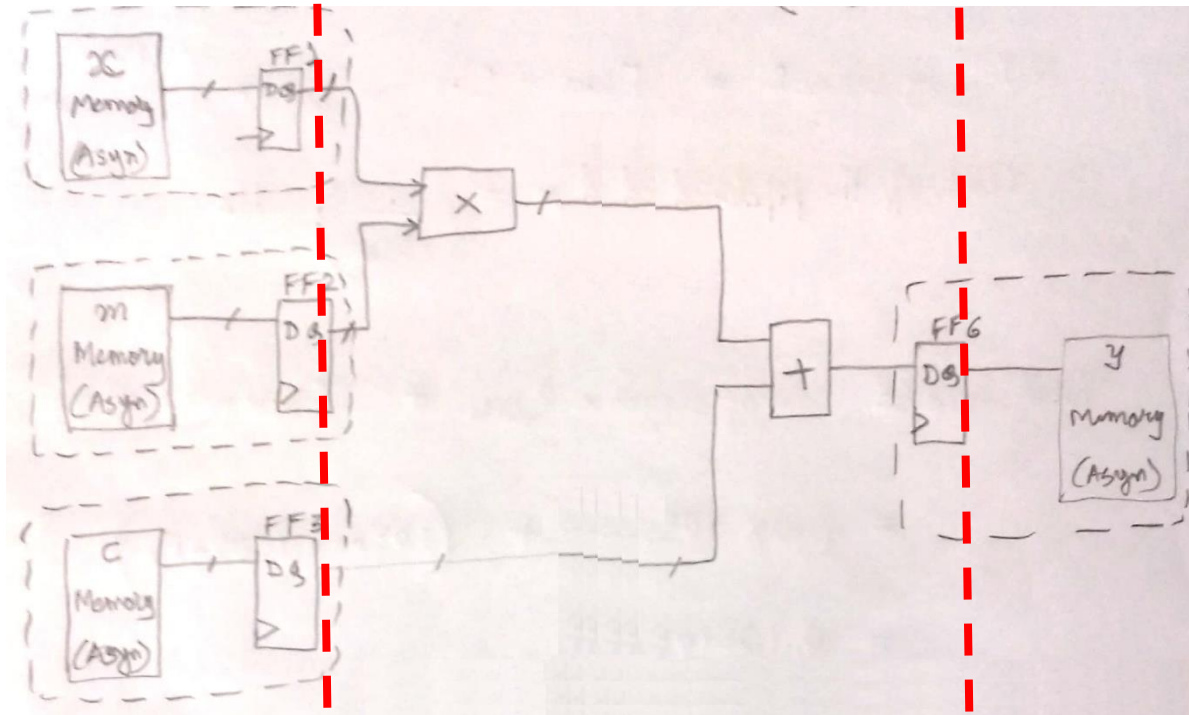
We want to implement

- **Un-pipelined design** (1 stage design)

$$y_i = (m_i \times x_i) + c_i$$

Clock boundary

Data only moves from boundary to boundary when it gets clock edge



Clocked Element
(Could be
Clocked memory
or FF or register

Combinational
cloud

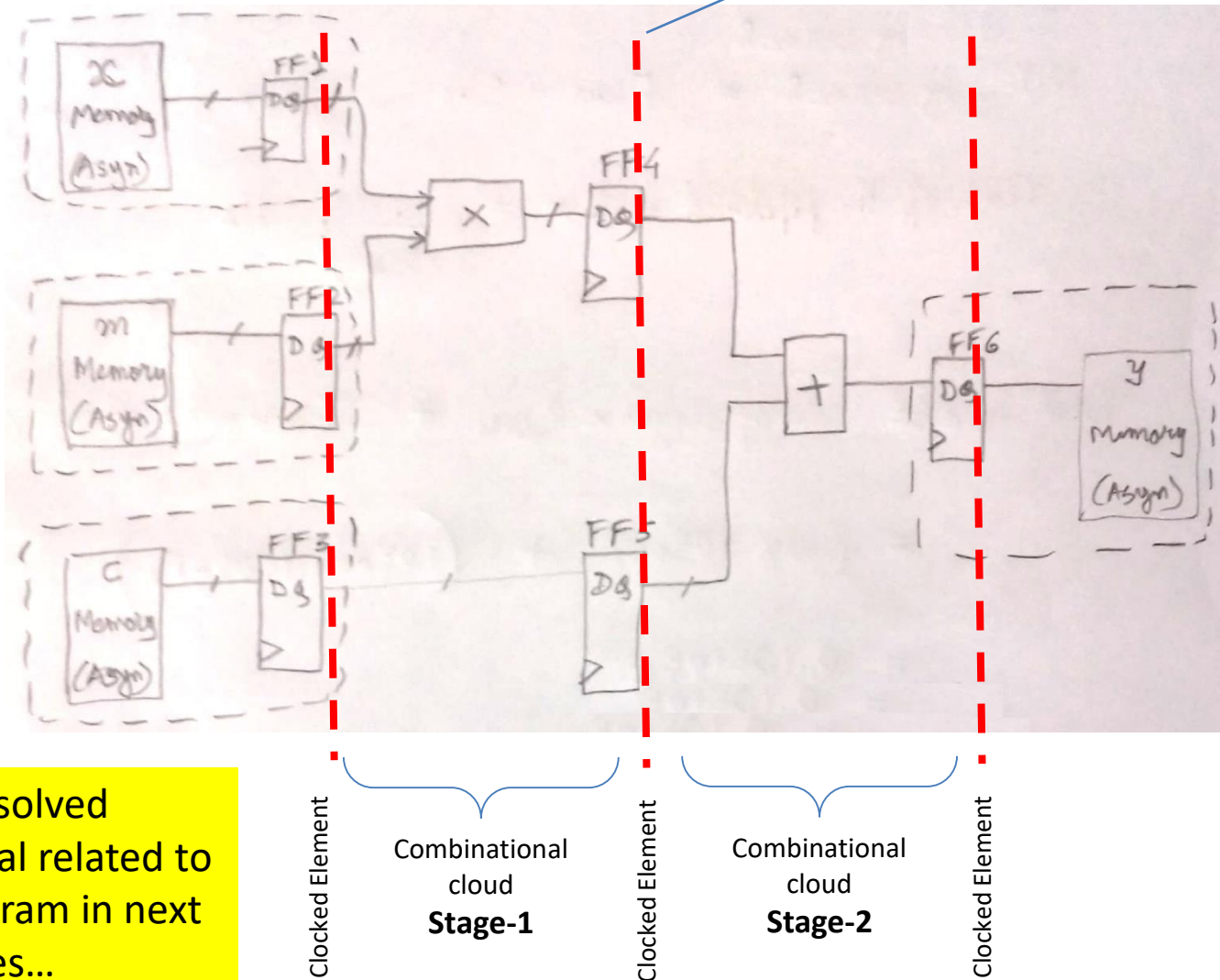
Clocked Element
(Could be
Clocked memory
or FF or register

We want to implement

- **Pipelined design** (2 stage design)

$$y_i = (m_i \times x_i) + c_i$$

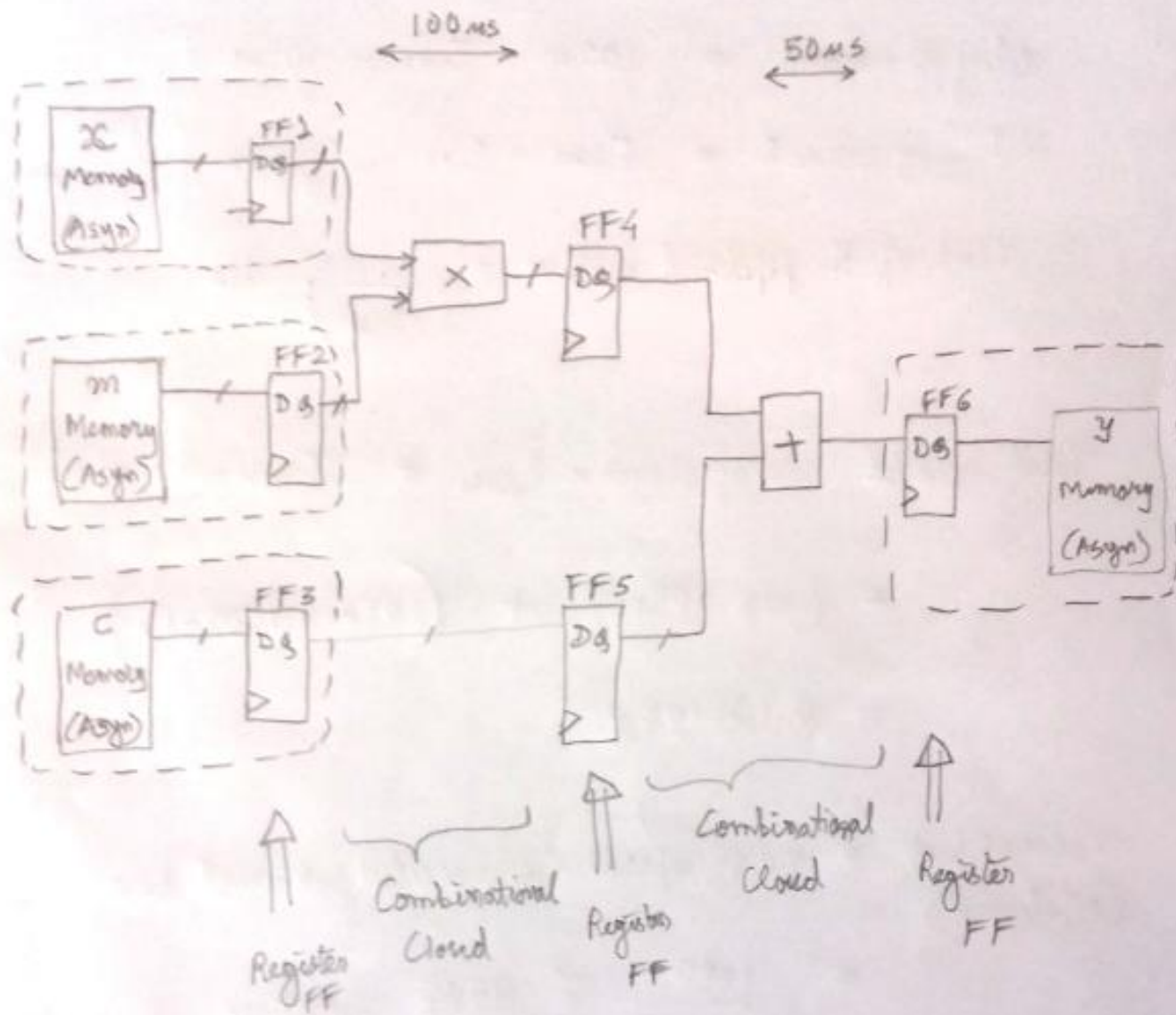
We have deliberately cut the large combinational cloud into two by inserting this clocked elements / FFs



See the solved numerical related to this diagram in next few slides...

Pipelining

FF delay = 5 ns



Let's say we have to do 1000 ($y = mx + c$) operations.

Unpipelined version: Delay = $100\mu s + 50\mu s = 150\mu s$
for Combinational circuit

1 stage design delay = $150\text{ns} + 5\text{ns} = 155\text{ns}$

$$\text{Total delay} = 155 \mu\text{s} \times 1000 = 0.155 \text{ s}$$

2 stage pipelined implementation

$$\left. \begin{array}{l} \text{delay of stage 1} = 100\mu s + 5\mu s = 105\mu s \\ \text{delay of stage 2} = 50\mu s + 5\mu s = 55\mu s \end{array} \right\} \begin{array}{l} T_{\max} = 105\mu s \\ = T_{\text{clock}} \end{array}$$

$$\therefore \text{Clock of the pipelined system} = \left(\frac{1}{105\mu} \right) \text{ Hz}$$

$$\text{Total time} \cong \text{no. of stages} \times T_{\text{clock}} + T_{\text{clock}} \times (\text{no. of operations})$$

$$= (2 \times 105\mu s) + (105\mu s \times (1000 - 1))$$

$$= 0.105105 \text{ s}$$

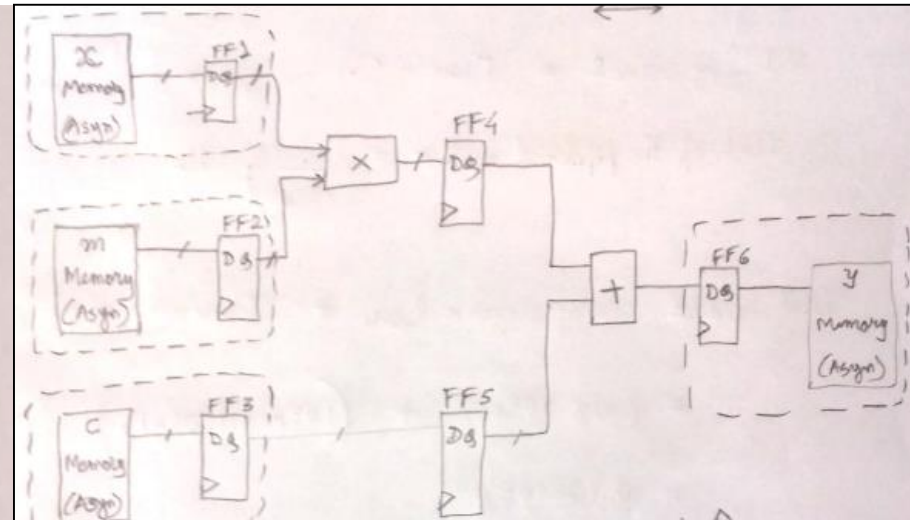
Throughput (pipelined) = no. of operations executed per unit time

$$= \frac{1000}{0.105105} \approx 9514 \frac{\text{operations}}{\text{second}}$$

$$\begin{aligned} \% \text{ improvement in delay} &= \left[\frac{(\text{total time unpipelined} - \text{total time pipelined})}{\text{total time unpipelined}} \right] \times 100 \\ &\approx 32\% \end{aligned}$$

How does data move in the pipe stages.

$x_1 = 1$	$c_1 = 2$	$m_1 = 0.5$
$x_2 = 3$	$c_2 = 1$	$m_2 = 0.9$
$x_3 = 5$	$c_3 = 10$	$m_3 = 2$
$x_4 = 7$	$c_4 = 13$	$m_4 = 1$
$x_5 = 9$	$c_5 = 5$	$m_5 = 0.8$
\vdots	\vdots	\vdots



	Clock1	Clock2	Clock3	Clock4	Clock5	Clock6	Clock7	Clock8
x	1	3	5	7	9
FF1								
m	0.5	0.9	2	1	0.8
FF2								
c	2	1	10	13	5
FF3								
m	-	0.5	2.7	10	7
FF4								
c	-	2	1	10	13
FF5								
y	-	-	2.5	3.7	2.0
FF6								