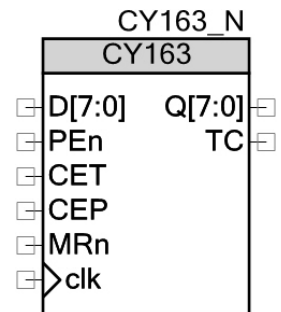


8-bit Binary Counter: Synchronous Reset

CY163 v1.0

Features

- Synchronous reset, counting and loading
- Positive-edge triggered clock
- Selectable load value.
- Simple to deconstruct



General Description

This counter is based on the 74HC163. It is a synchronous pre-settable binary counter with look-ahead carry. Synchronous operation is implemented with positive-edge triggered logic. The counter, Q[7:0] (datapath register A0), may be preset to a load value at inputs D[7:0]. A LOW level at the master reset input (MRn) sets the counter to zero, providing a synchronous clear.

The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output, when enabled, will produce a HIGH output pulse of duration approximately equal to clock cycle.

This component was built as a teaching tool. This classic component's operation is well understood and this datasheet's function is to help understand how the component was built through its deconstruction. It is recommended that you review the CY161 component before attempting this one.

Pin Description

Pin	Type	Function
D[7:0]	inputs	value to be loaded
Pen	input	load enable input (active low)
CET	input	count enable carry input
CEP	input	count enable input
MRn	input	synchronous master reset (active low)
Clk	input	clock input

Pin	Type	Function
Q[7:0]	outputs	counter value
TC	output	terminal count output

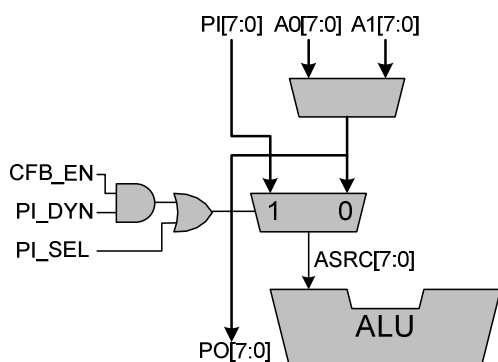
Function Table

Operating Modes	Inputs					Outputs	
	MRn	clk	CEP	CET	PEn	Q	TC
reset	0	↑	x	x	x	0x00	0
load	1	↑	x	x	0	D	Q == 0xff && CET == 1
count	1	↑	1	1	1	Q + 1	Q == 0xff
hold	1	x	0	x	1	Q	Q == 0xff && CET == 1
hold	1	x	x	0	1	Q	0

Deconstructing the Component

This component is a good example of how to route parallel data into the ALU and out of the A0/A1 registers. With three synchronous inputs, it easily fits into the eight available datapath configurations (instructions).

Below is simplified block diagram of the parallel In/Out interface to a datapath.



The parallel out (PO) interface is always available and connects to either A0 or A1. The parallel in (PI) interface must be routed into the left input of the ALU (ASRC). If the PI_SEL bit (CFG15.7) is set, the PI is the permanent input to ASRC. However if instead the PI_DYN bit (CFG17.5) is set, the CFB_EN bit in each datapath instruction determines the ASRC source for that particular instruction. This bit shares function with the single instruction CRC functionality. If PI_DYN is set, CFB_EN serves to select a parallel input to the ALU. If not set, CFB_EN determines if a CRC operation is performed.

For this counter there are four different operations.

- Reset
- Hold
- Load
- Count Up

These four operations need to be implemented with datapath instructions.

Using PSoC Creator, open the CY163 example project and you will see the project schematic (*TopDesign.cysch*). It has a CY163 component connected to input switches, output LEDs, and a clock.

In the Workspace Explorer, click the **Components** tab. Then, right-click on the project and select **Import Component**. Navigate to where the CYCC_SimpleComps library project is, and select the CYCC_CY163_v1_0 component. Click **OK** and the following files are shown for the component:

- Symbol file (cysym)
- Datasheet (pdf)
- Verilog File (v)

Open the symbol file to find a symbol with six inputs and two outputs. It looks like the symbol shown on the first page. There are no additional symbol parameters.

Open the Verilog file and notice that at lines 31 – 38, these definitions were passed to this Verilog file when it was created. The first 25 lines of this header list register usage and the datapath instruction definitions.

There is a need for intermediate signals and this is handled in lines 42 - 45. What follows is the datapath module definition. It was created and inserted by the Datapath Configuration Tool. This information is backward compatible so opening up the Datapath Configuration Tool for this Verilog file results in the following.

C:\Documents and Settings\dvaness\Desktop\Simple_Components\SimpleComponentLibrary.cylib\CY163\CY163.v - Datapath Configuration Tool

File Edit View Tools Help

Configuration: counter

CFG0RAM

Reset	Reg	Binary Value	FUNC	SRCA	SRCB	SHIFT	A0 WR SRC	A1 WR SRC	CFB EN	CI SEL	SI SEL	CMP SEL	Comment
	Reg0	10101000 01000000	XOR	A0	A0	PASS	ALU	NONE	DSBL	CFGA	CFGA	CFGA	Reset A0 = 0
	Reg1	10101000 01000000	XOR	A0	A0	PASS	ALU	NONE	DSBL	CFGA	CFGA	CFGA	Reset A0 = 0
	Reg2	10101000 01000000	XOR	A0	A0	PASS	ALU	NONE	DSBL	CFGA	CFGA	CFGA	Reset A0 = 0
	Reg3	10101000 01000000	XOR	A0	A0	PASS	ALU	NONE	DSBL	CFGA	CFGA	CFGA	Reset A0 = 0
	Reg4	00000000 01001000	PASS	A0	D0	PASS	ALU	NONE	ENBL	CFGA	CFGA	CFGA	Load A0 = pi
	Reg5	00000000 00000000	PASS	A0	D0	PASS	NONE	NONE	DSBL	CFGA	CFGA	CFGA	Null
	Reg6	00000000 01001000	PASS	A0	D0	PASS	ALU	NONE	ENBL	CFGA	CFGA	CFGA	Load A0 = pi
	Reg7	00100000 01000000	INC	A0	D0	PASS	ALU	NONE	DSBL	CFGA	CFGA	CFGA	Count A0 = A0 +1

CFG9

Reset	AMASK Value	A [7]	A [6]	A [5]	A [4]	A [3]	A [2]	A [1]	A [0]	Unused	Comment
	FF	1	1	1	1	1	1	1	1	00000000	

CFG11-10

Reset	CMASK1 Value	CMASK0 Value	C1 [7]	C1 [6]	C1 [5]	C1 [4]	C1 [3]	C1 [2]	C1 [1]	C1 [0]	C0 [7]	C0 [6]	C0 [5]	C0 [4]	C0 [3]	C0 [2]	C0 [1]	C0 [0]	Comment
	FF	FF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

CFG13-12

Reset	Binary Value	CMP SELB	CMP SELA	CI SELB	CI SELA	CMASK1 EN	CMASK0 EN	A MSK EN	DEF SI	SI SELB	SI SELA	Comment
	00000000 00000000	A1_D1	A1_D1	ARITH	ARITH	DSBL	DSBL	DSBL	DEF_0	DEFSI	DEFSI	

CFG15-14

Reset	Binary Value	PI SEL	SHIFT SEL	PI_DYN	MSB SI	F1 INSEL	F0 INSEL	MSB EN	MSB SEL	CHAIN CMSB	CHAIN FB	CHAIN 1	CHAIN 0	Comment
	00100000 00000000	ACC	SL	EN		BUS	BUS	DSBL	BIT0	NOCHN	NOCHN	NOCHN	NOCHN	

CFG17-16

Reset	Binary Value	Unused [15:13]	ADD SYNC	Unused [11:10]	F1 DYN	F0 DYN	F1 CK INV	F0 CK INV	FIFO FAST	FIFO CAP	FIFO EDGE	FIFO ASYNC	EXT CRCPRS	WRK16 CONCAT	Comment
	00000000 00000000	000		00					DP	AX	LEVEL	SYNC	DSBL	DSBL	

Note that although only four operations are needed to be implemented, all 8 of the datapath instructions are used. By judicious selection of their address position and duplication, the logic to control them has been greatly simplified. The PI_DYN bit has been enabled so the CFB_EN bit of each instruction controls the ASRC input to the ALU.

- For the reset instructions A0 is XORed with itself and placed back in A0.
- For the load instructions the parallel input is passed through the ALU and placed in A0. Note that with PI_DYN enabled the load instructions has CFB_EN enabled and the input is from PI.
- For the null instructions A0 is passed through the ALU but not fed to any register. It does nothing.
- For the count instruction A0 is incremented by the ALU and fed back to A0.

When saved, this tool inserts the updated configuration data back into the Verilog file along with an instance of the datapath interface. Just pass the correct signals in to and out of it and you are

done. This counter parameter list may look ominous but only a few parameters have to be entered as shown below.

```
/* input          */ .clk(clk),           //Clock for datapath
/* input [02:00]   */ .cs_addr({MRn, Load, PEn}), //Control for reg selection
/* output         */ .ff0(terminalCount), //TC from Datapath
/* input [07:00]   */ .pi(D[7:0]),        //Parallel data port
/* output [07:00]  */ .po(Q[7:0])         //Parallel data port
```

These parameters do the following:

- Connect a reset signal to the datapath reset circuitry
- Connect a clock signal to the datapath clock circuitry
- Provide three inputs to control the instruction processing
- Connect the “all 1s” flag to an output
- Connect the parallel input to the datapath PI
- Connect the datapath PO to the parallel output

Support

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