Complete ASIC & FPGA Design Services

EXECUTION EXPERIENCE

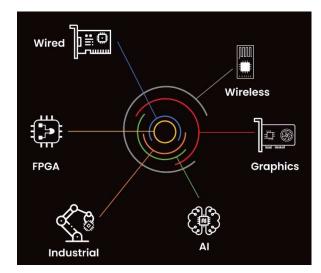
3+ complex SoCs with complex subsystems and partitions All major FPGAs and procssors HW/SW/IP integration

DEEP & WIDE EXPERTISE

SoC RTL/Verification to GDSII FPGA design/prototyping System/SW/HW engineering Multiple domains/applications

EFFECTIVE PROGRAM MANAGEMENT

Hybrid Agile dev model
Highly transparent
communication
Issue escalation mechanism
Risk mitigation planning



- Fast growing provider of premier semiconductor technical solutions
 - Founded in 2018
 - ° 100+ design engineers
- Led by industry veterans with a total experience of 100+ years
- 10+ global major customers served
- Multiple complex SoCs delivered at < 10nm
- Skilled in using all major FPGA and processors

Driven by technology disruptions and a raging pandemic, global majors in the hi-tech industry are looking to scale and outcompete rivals by outsourcing critical pieces of development work to innovative design services partners. Large design services companies are unable to build a high quality pool of resources with specialized skills due to their large overheads and previous generation financial models. As a result, they can only subcontract and act as a distribution channel for niche, specialized smaller firms such as P2F that have built enduring supply chains at the right cost.

Since inception, P2F's expert teams have successfully tapped out tens of complex SoCs in various domains and industry segments for major semiconductor and technology businesses worldwide.

Our engineers are extremely comfortable working across a variety of technology nodes, tools and flows, design tools and techniques, and are skilled at handing off designs without surprises.

P2F provides end to end services for semiconductor design from RTL to GDS-II and sign-off, design verification, library development, DFT, AMS design and FPGA design and development.

P2F's team follows a hybrid execution model that combines both agile and waterfall development models. It gives the team the flexibility to be deployed at any stage without affecting project schedules while meeting aggressive timelines.



SPECIFIC DIFFERENTIATORS

Adjacent area expertise

Custom recipes for quick TAT

with focus on QOR

EDA cloud flow execution

STABLE RESORCE

MODEL

Business continuity and stability

Continuous training and

improvement

Customer needs drive flexibility

FLEXIBLE EXECTION MODEL

Consulting

- On site
- o All timeframes
- o Flexible deployment
- o International support
- o T&M Billing

Turnkey

- On or off site
- o SoW based
- o PM Leadership
- o NRE based billing

Case Studies: 5/7nm Physical Design

DESCRIPTION & DELIVERABLES	PARTITIONS	NODE	COMPLEXITY
Partition closure for Al low power CPU chips	20	5nm	2GHz, ~1.5Mn instances
Partition closure for AI based chips	3	5nm	PCIE Gen5 Subsystem closure
Partition closure for GPU chips	15	5nm	~2Mn instances
Partition closure for Al chips	5	5nm	~2Mn instances
Partition closure for Graphics chips	30	7nm TSMC	~1Mn instances
Partition closure for Modem chips	8	7nm TSMC	~1Mn instances
Partition closure for Modem chips	30+	7nm TSMC	~1Mn instances

Case Studies: FPGA/System Design

DESCRIPTION & DELIVERABLES	TECHNOLOGY & COMPLEXITY		
Flash Emulation Product	4 Xilinx Artix XC7A200T F1156 FPGAs		
	Zynq ZC7045 Controller		
	2 ONFI Lanes / FPGA		
	4G/8G ONFI Lane I/F		
	8 ONFI Lanes / VF		
	8, 8GB DDR3 – ON board (SODIMM)		
Image Processing Platform / DIN Rail PLC	Zynq Dual ARM Cortex-A9 @ 866MHz, Artix-7 FPGA		
Controller	1GB DDR-2, 512MB NAND FLASH		
	1 x 10/100/1000 BASE-T On module,		
	1 x USB 2.0 OTG		
	SD Card, JTAG, SDIO, CAN 2.0, 1 x UART, 1 x I2C		
	4.5-5.5V DC Input, 5W (Max)		
	2 x 100 Pin SAMTEC LSHM-150 connector		
	1 x 80 Pin SAMTEC and 1 X 40 Pin connector		
Machine Vision Platform	Zynq Dual ARM Cortex-A9 @800MHz. ARTIX-7 FPGA		
	Image compression using JPEG2000		
	1GB DDR-3, 512MB NAND FLASH		
	1x10/100/1000 BASE-T on module Ethernet interface		
	1x USB 2.0 OTG on module interface		
	SD card, CAN2.0, I2C, SPI		
	-20 to 70°C operating temperature		
	SMP mode RT Linux for Soft PLC and HMI		
	VxWorks BSP support in AMP and SMP configuration		

