

# **EE 577A- Fall 2021 VLSI SYSTEM DESIGN**

## **Lab2 Report**

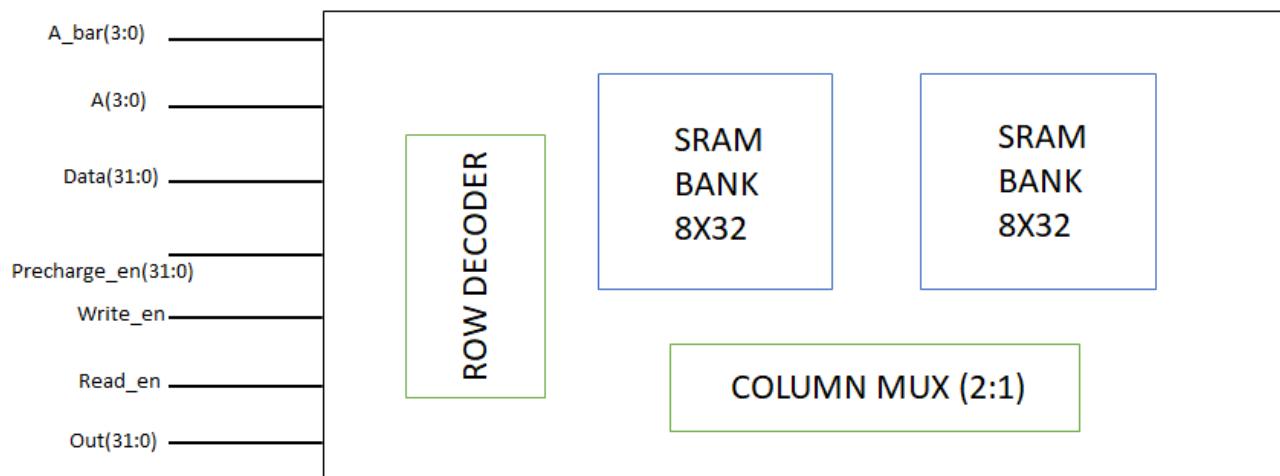
### **512-bit SRAM Array Design**

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**3751474091**

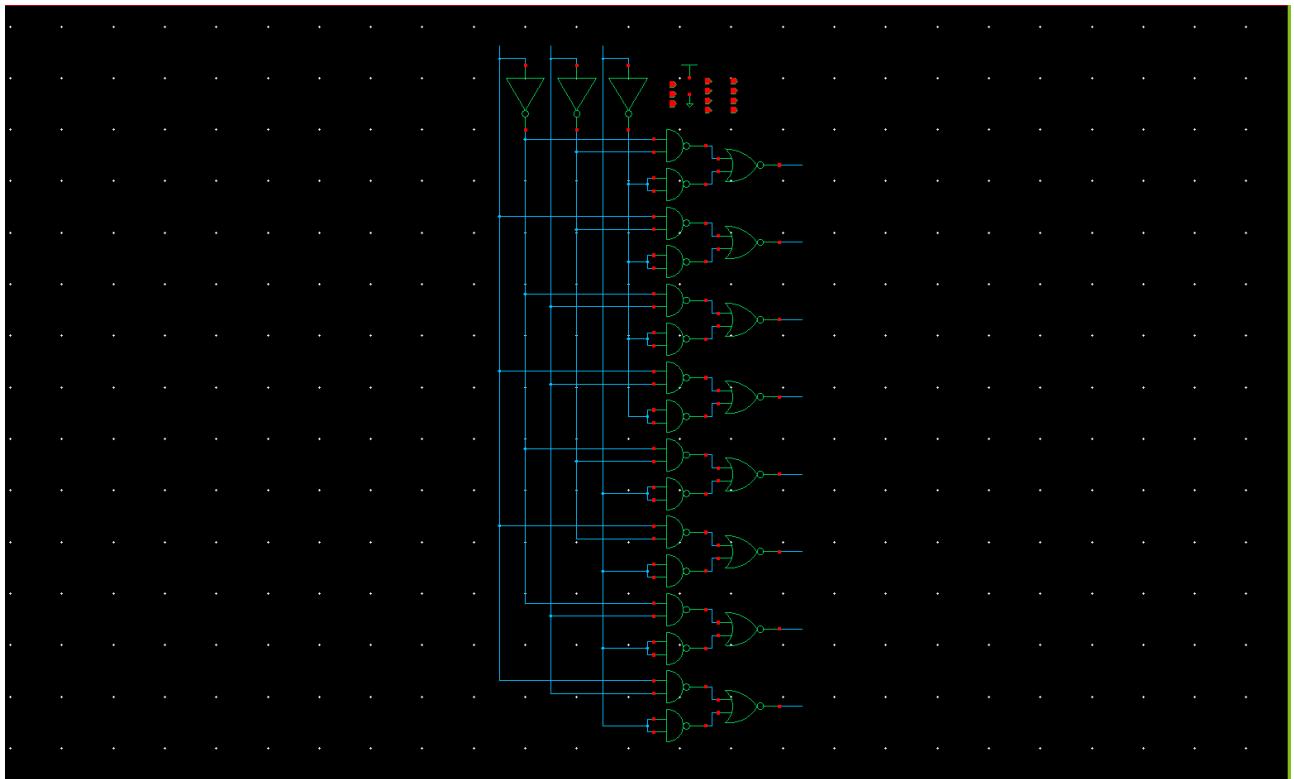
In this lab, we will design a 512-bit SRAM with two 256-bit banks. The word length is 16 bits.



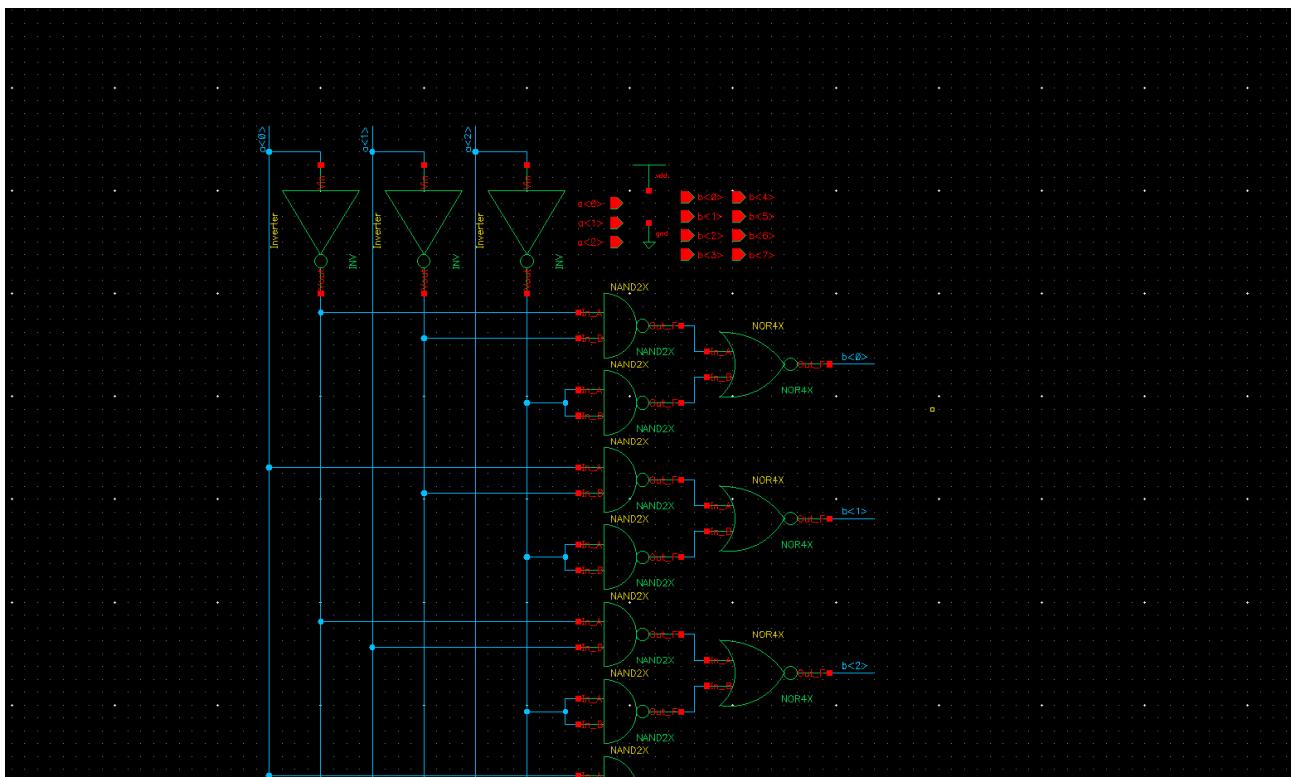
Below is the summary of the input pins:

INPUT	ADDRESS BITS	A[3]-A[0], A_bar[3]-A_bar[0]	Transition time =5ps
INPUT	READ CONTROL	<u>Read_en</u>	Transition time =5ps
INPUT	WRITE CONTROL	<u>Write_en</u>	Transition time =5ps
INPUT	PRECHARGE CONTROL	<u>Precharge_en</u>	Transition time =5ps
INPUT	WRITE DATA BITS	Data[31]-data[0]	Transition time =5ps
INPUT	READ DATA BITS	Out[31]-out[0]	Transition time =5ps

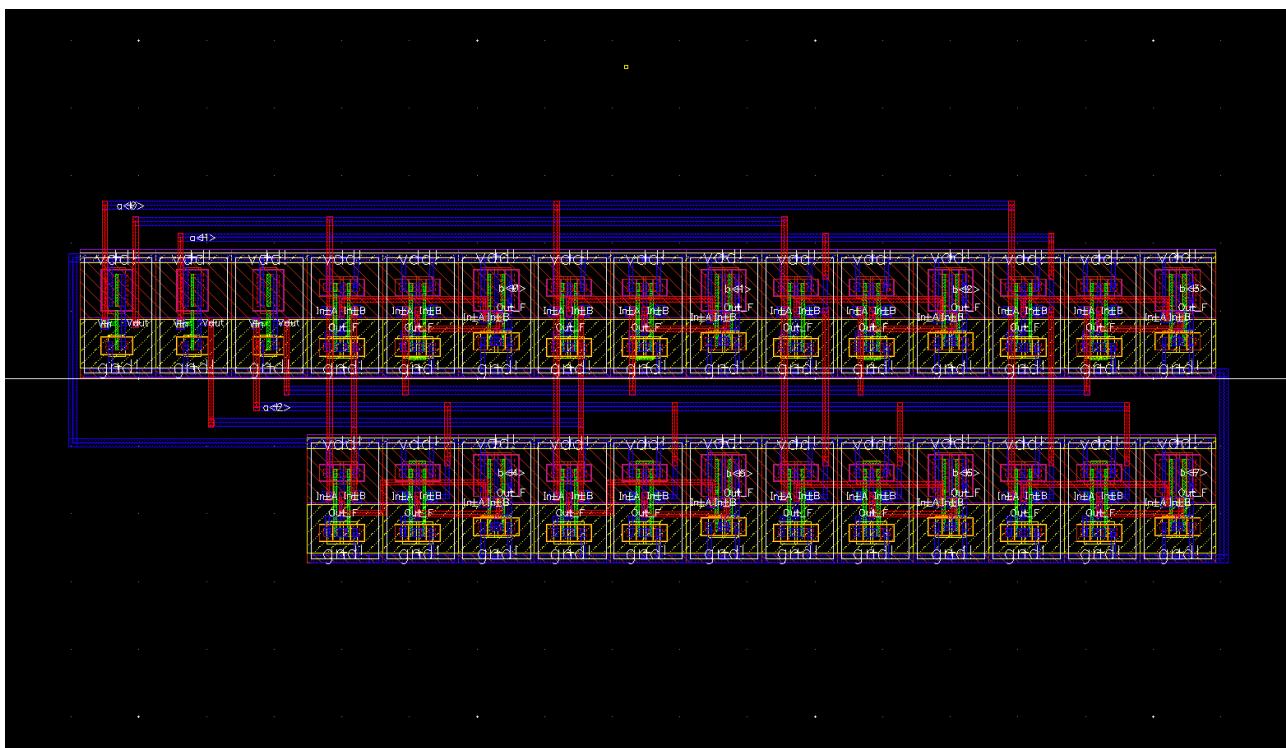
### 3-8 Decoder (Schematic)



The figure below is the pre-decode system for 3-8 decoder.



### 3-8 Decoder (Layout)



PVS 16.15-64b Reports: Done [DRC] DR...

[DRC] DRC

DRC: Cumulative Time CPU = 0 (s) REAL = 0 (s)  
PATTERN\_MATCH: Cumulative Time CPU = 0 (s) REAL = 0 (s)  
DFM FILL: Cumulative Time CPU = 0 (s) REAL = 0 (s)

Total CPU Time : 1 (s)  
Total Real Time : 1 (s)  
Peak Memory Used : 30 (M)  
Total Original Geometry : 264 (3101)  
Total DRC RuleChecks : 562  
Total DRC Results : 0 (0)  
Summary can be found in file Decoder3\_8.sum

ASCII Check

PVS 16.15-64b DRC Results Viewer

File View Options Tools Windows Help

Design Lab1:Decoder3\_8:layout

DRC Cell/Rule Hier Top Cells Rules Show:

Explain Return On Top

Cell/Rule Color Count Level

Total: 0 results in 0 of 562 checks. Total number of non-empty checks is 0.

/home/viter

PVS 16.15-64b Reports: Done [LVS] LV...

[DRC] DRC X [LVS] LVS X

```
#####
# Run Result      : MATCH
#
# Run Summary     : [INFO]   ERC Results: Empty
#                   : [INFO]   Extraction Clean
#
# ERC Summary File: Decoder3_8.sum
# Extraction Report File: Decoder3_8.rep
# Comparison Report File: Decoder3_8.rep.cls
#
#####
Checking in all SoftShare licenses.

PVS Comparison Finished. Thu Sep 23 21:38:04 2021
```

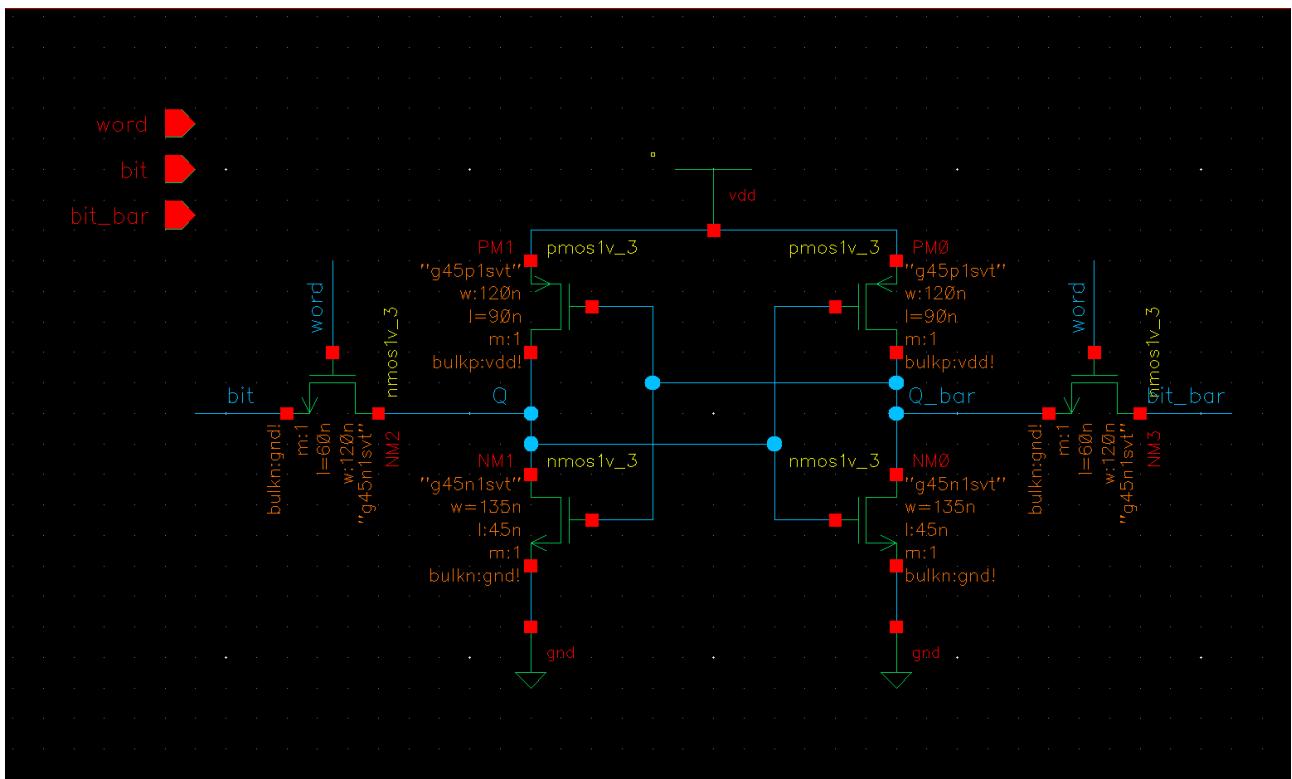
**PVS 16.15-64b LVS Run St...**

ERC Results: **Empty**  
 Extraction Results: **Clean**  
 Comparison Results: **Match**

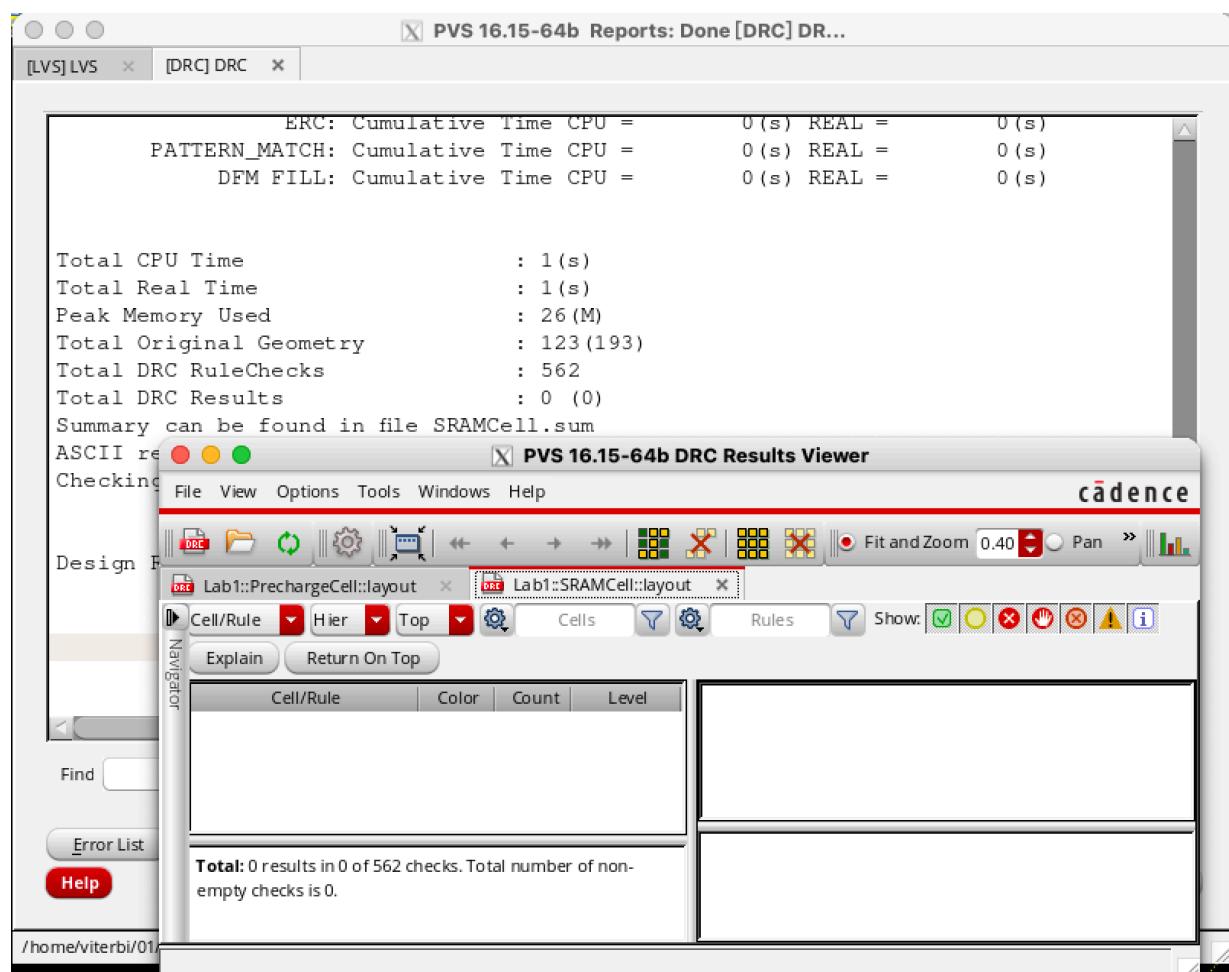
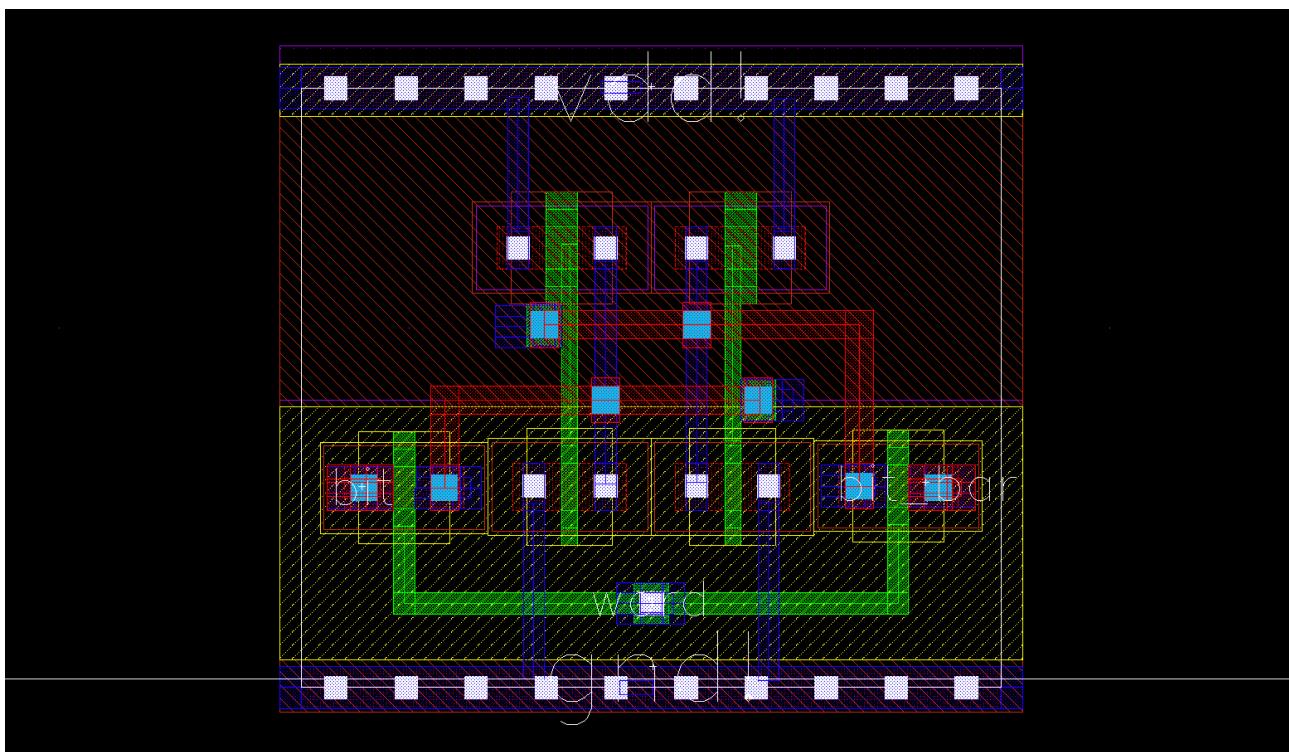
Do you want to start the LVS DE?  Yes  No

/home/viterbi/01/tchueh/work\_gdk045/LVS

## SRAM Cell (Schematic)



## SRAM Cell (Layout)



PVS 16.15-64b Reports: Done [LVS] LV...

[DRC] DRC X [LVS] LVS X

```
#####
# Run Result      : MATCH
#
# Run Summary     : [INFO]  ERC Results: Empty
#                   : [INFO]  Extraction Clean
#
# ERC Summary File : SRAMCell.sum
# Extraction Report File : SRAMCell.rep
# Comparison Report File : SRAMCell.rep.cls
#
#####

```

Checking in all SoftShare licenses.

PVS Comparison Finished. Thu Sep 23 21:47:51 202

ERC Results      **Empty**  
Extraction Results: **Clean**  
Comparison Results: **Match**

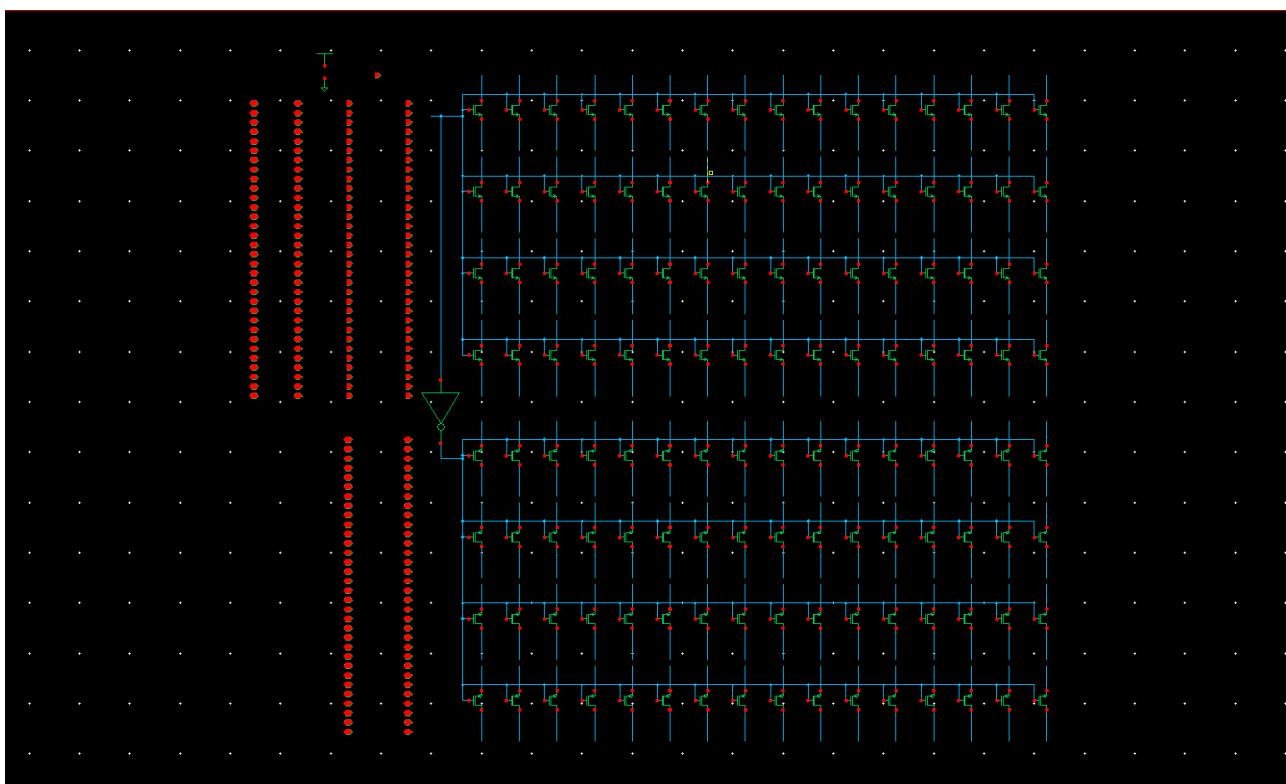
Do you want to start the LVS DE?

Find  Next

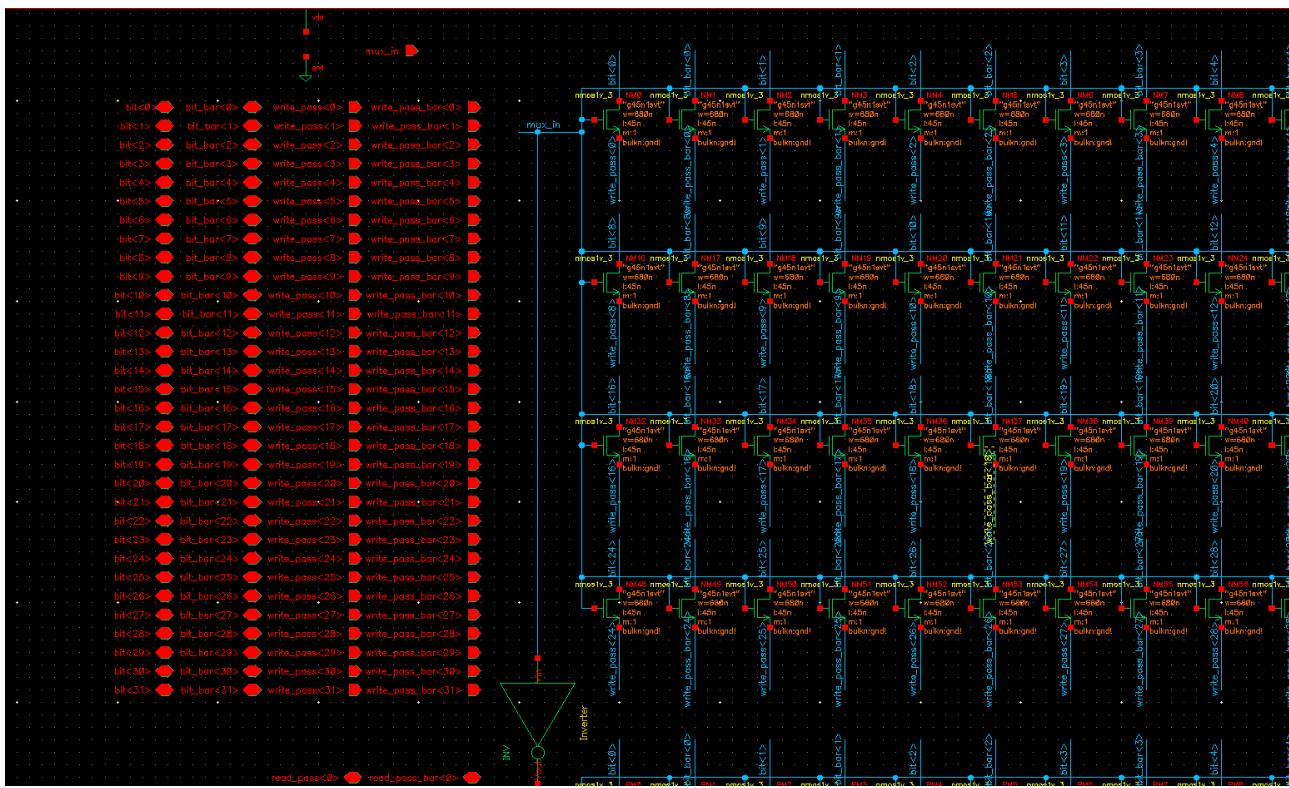
Error List  Help  ReRun  Resubmit  Close Report  Kill

/home/viterbi/01/tchueh/work\_gpdk045/LVS

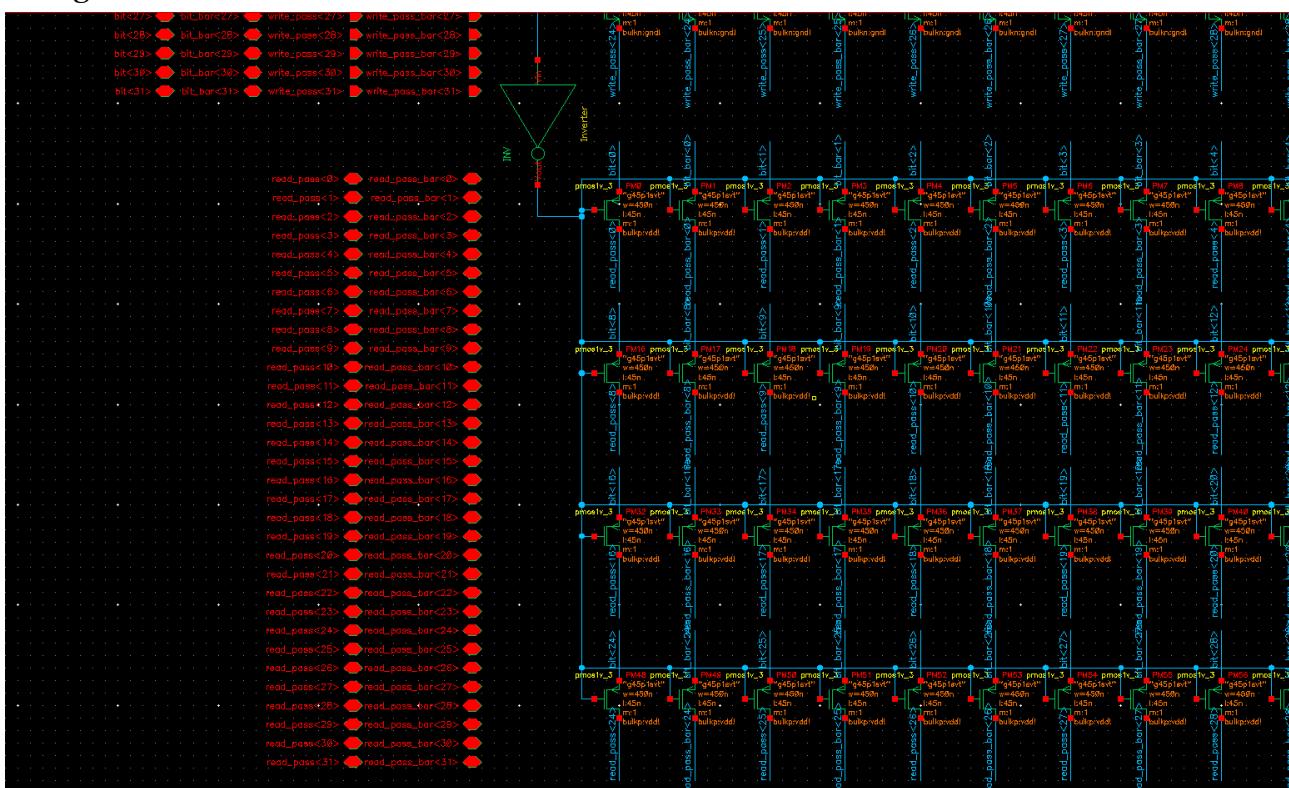
Write/Read MUX (Schematic)



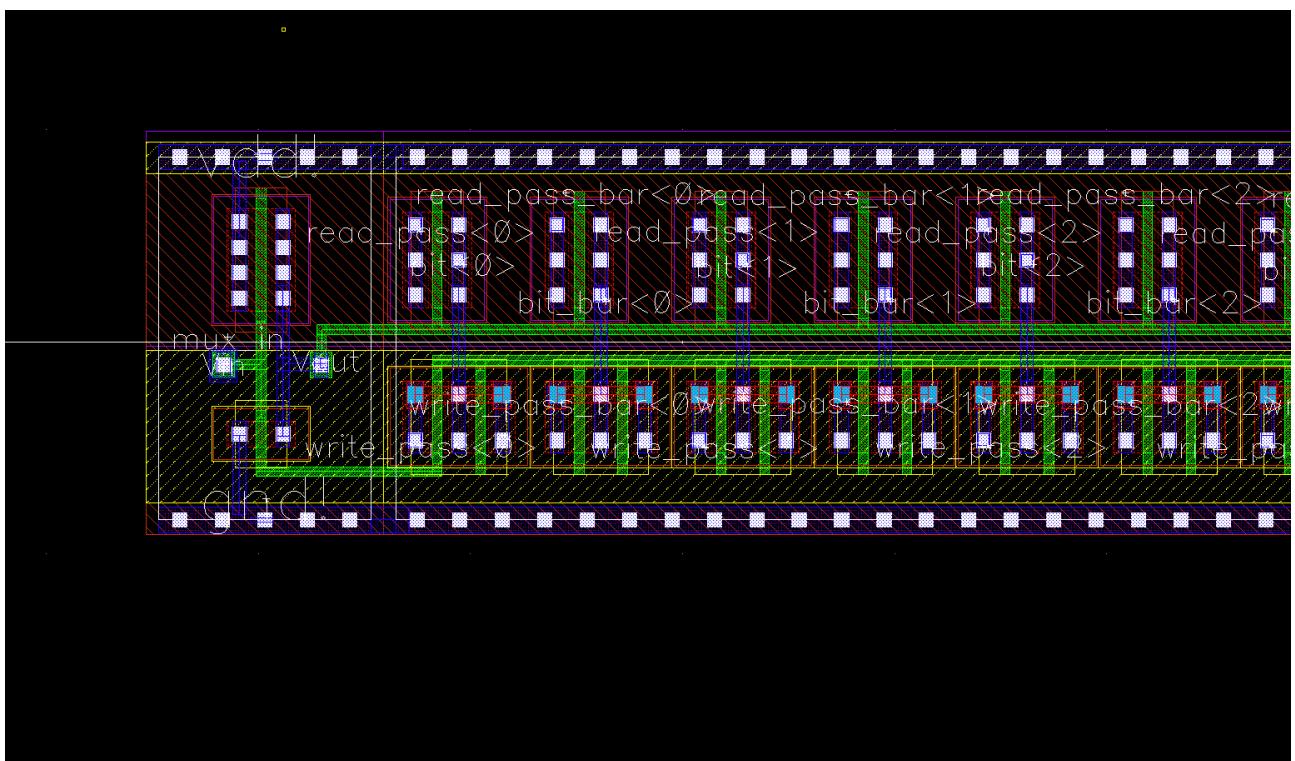
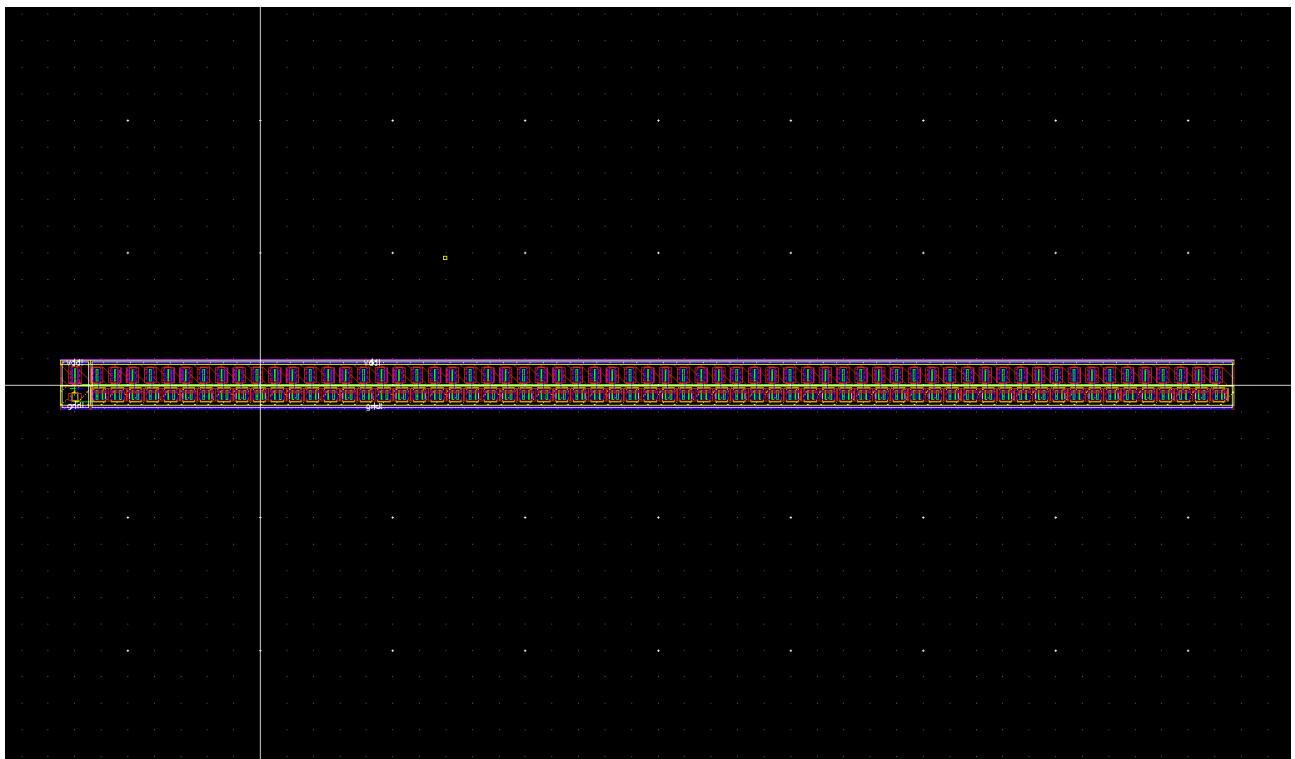
The figure below shows that nMOS pass transistors ( $W = 68\text{nm} / L = 45\text{nm}$ ) is used to design the column write MUX.



The figure below shows that pMOS pass transistors ( $W = 450\text{nm} / L = 45\text{nm}$ ) is used to design the column read MUX.



## Write/Read MUX (Layout)



PVS 16.15-64b Reports: Done [DRC] DR...

[LVS] LVS    [DRC] DRC

```

ERC: Cumulative Time CPU =      0 (s)  REAL =      0 (s)
PATTERN_MATCH: Cumulative Time CPU =      0 (s)  REAL =      0 (s)
DFM FILL: Cumulative Time CPU =      0 (s)  REAL =      0 (s)

Total CPU Time : 1 (s)
Total Real Time : 2 (s)
Peak Memory Used : 34 (M)
Total Original Geometry : 885 (4104)
Total DRC RuleChecks : 562
Total DRC Results : 0 (0)
Summary can be found in file MUX.sum
ASCII report: /home/viterbi/01/tchueh/work_gpdk045/DRC/MUX.sum
Checking
```

**PVS 16.15-64b DRC Results Viewer**

File View Options Tools Windows Help

Design Rule

DXF Lab1:MUX:layout

Cell/Rule Hier Top Cells Rules Show:

Explain Return On Top

Total: 0 results in 0 of 562 checks. Total number of non-empty checks is 0.

PVS 16.15-64b Reports: Done [LVS] LV...

[DRC] DRC    [LVS] LVS

```

#####
#
# Run Result : MATCH
#
# Run Summary : [INFO] ERC Results: Empty
#                : [INFO] Extraction Clean
#                : [INFO] Some Sections Have Been Truncated
#
# ERC Summary File : MUX.sum
# Extraction Report File : MUX.rep
# Comparison Report File : MUX.rep.cls
#
#####

Checking in all SoftShare licenses.

PVS Comparison Finished. Thu Sep 23 22:12:39 202
```

**PVS 16.15-64b LVS Run St...**

ERC Results: **Empty**  
 Extraction Results: **Clean**  
 Comparison Results: **Match**

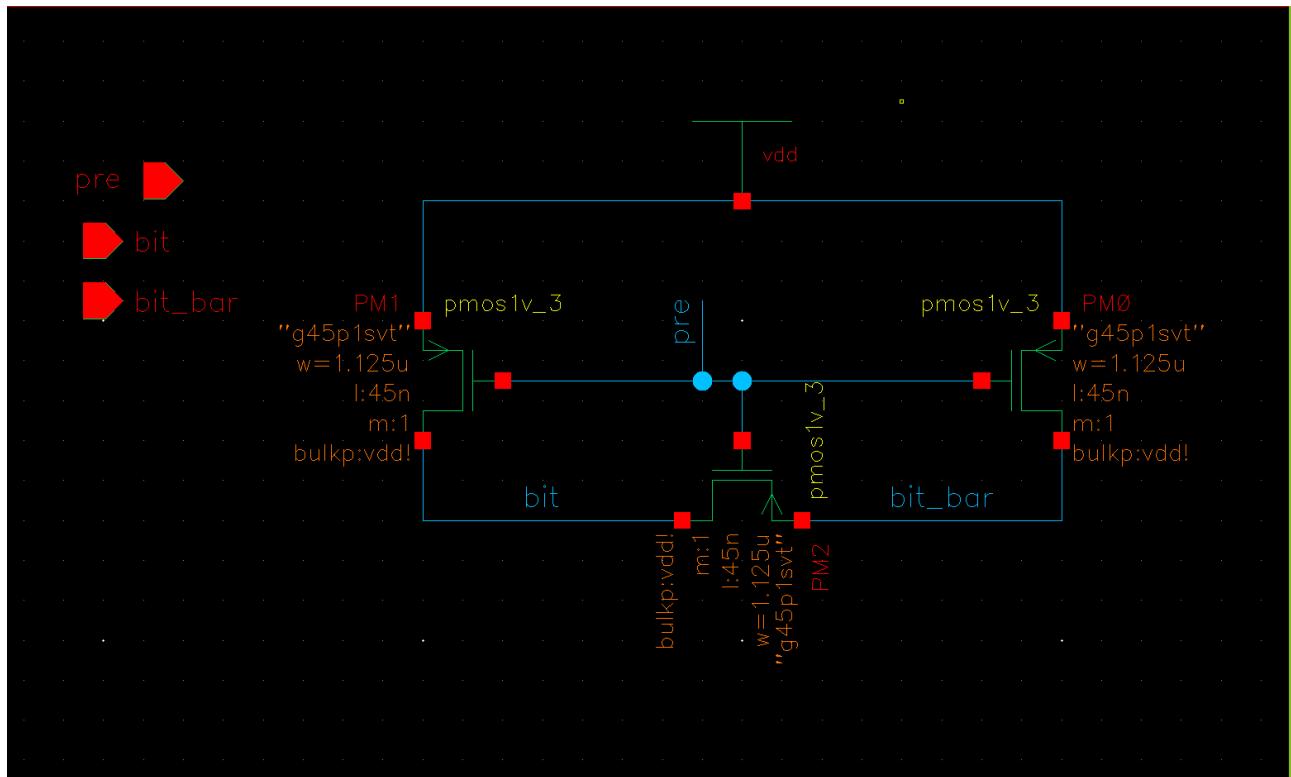
Do you want to start the LVS DE?  Yes  No

Find  Next  ReRun  Resubmit  Close Report  Kill

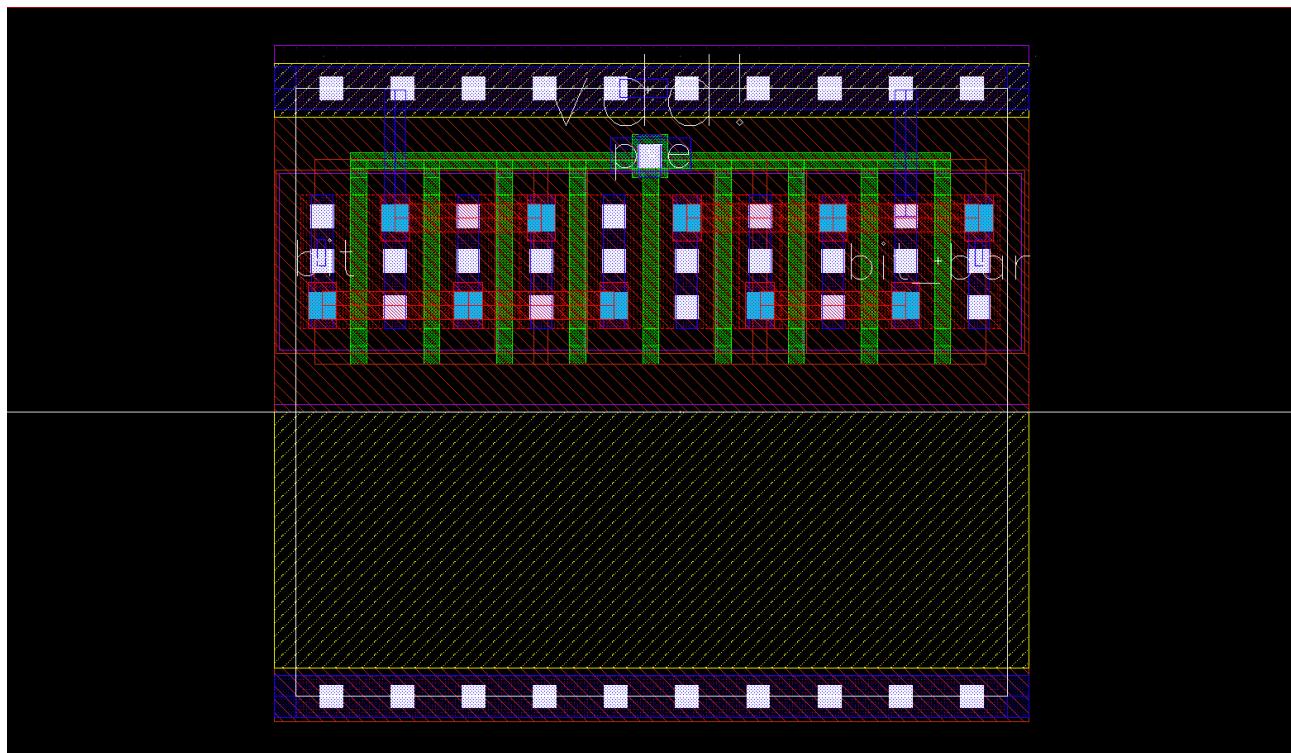
Error List  Help

/home/viterbi/01/tchueh/work\_gpdk045/LVS

Pre-charge (Schematic)



Pre-charge (Layout)



The screenshot shows the Cadence PVS 16.15-64b DRC Results Viewer interface. The title bar reads "PVS 16.15-64b Reports: Done [DRC] DR...". The main window displays the following summary statistics:

	Cumulative Time	CPU =	0 (s)	REAL =	0 (s)
ERC:	Cumulative Time	CPU =	0 (s)	REAL =	0 (s)
PATTERN_MATCH:	Cumulative Time	CPU =	0 (s)	REAL =	0 (s)
DFM FILL:	Cumulative Time	CPU =	0 (s)	REAL =	0 (s)

Below these, detailed metrics are listed:

	:	
Total CPU Time	:	1 (s)
Total Real Time	:	1 (s)
Peak Memory Used	:	26 (M)
Total Original Geometry	:	93 (202)
Total DRC RuleChecks	:	562
Total DRC Results	:	0 (0)

Summary can be found in file PrechargeCell.sum

The interface includes a toolbar with icons for DRC, File, View, Options, Tools, Windows, Help, and various search and filter functions. A status bar at the bottom shows the path "/home/vitek" and the title "PVS 16.15-64b Reports: Done [LVS] LV...".

The screenshot shows a terminal window with the following text output:

```
#####
# Run Result : MATCH
#
# Run Summary : [INFO] ERC Results: Empty
# : [INFO] Extraction Clean
#
# ERC Summary File : PrechargeCell.sum
# Extraction Report File : PrechargeCell.rep
# Comparison Report File : PrechargeCell.rep.cls
#
#####
Checking in all SoftShare licenses.
```

Below the terminal, a message says "PVS Comparison Finished. Thu Sep 23 21:44:20 2021".

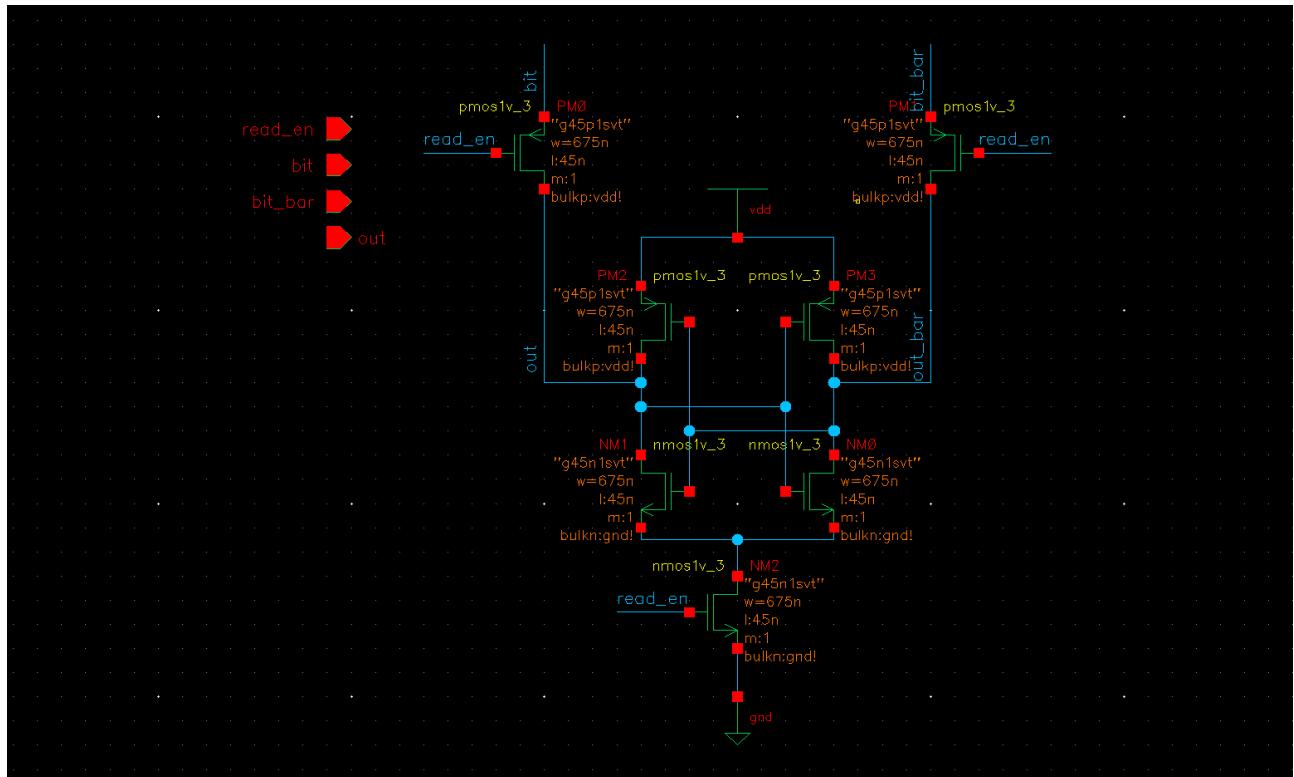
A modal dialog box titled "PVS 16.15-64b LVS Run St..." displays the following results:

Result Type	Status
ERC Results	Empty
Extraction Results	Clean
Comparison Results	Match

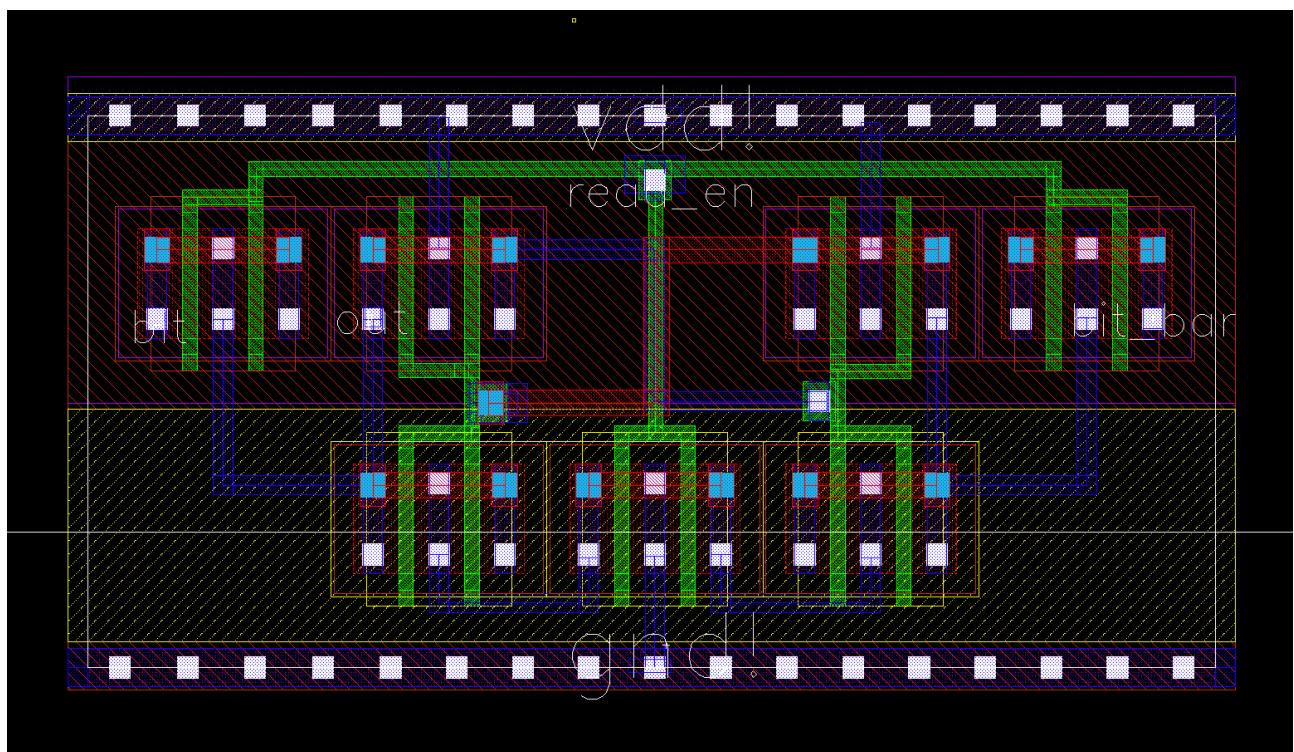
The dialog also contains a question: "Do you want to start the LVS DE?". It has two buttons: "Yes" (highlighted) and "No".

At the bottom of the screen, there are several buttons: Find, Error List, Help, ReRun, ReSubmit, Close Report, and Kill.

## Sense Amp. (Schematic)



## Sense Amp. (Layout)



[LVS] LVS [DRC] DRC

```

ERC: Cumulative Time CPU = 0 (s) REAL = 0 (s)
PATTERN_MATCH: Cumulative Time CPU = 0 (s) REAL = 0 (s)
DFM FILL: Cumulative Time CPU = 0 (s) REAL = 0 (s)

Total CPU Time : 1 (s)
Total Real Time : 1 (s)
Peak Memory Used : 26 (M)
Total Original Geometry : 168 (349)
Total DRC RuleChecks : 562
Total DRC Results : 0 (0)
Summary can be found in file SenseAmpCell.sum
ASCII re: Checking File View Options Tools Windows Help
Design P... DRC Lab1::PrechargeCell::layout Lab1::SRAMCell::layout Lab1::SenseAmpCell::layout
Cell/Rule Hier Top Cells Rules Show Explain Return On Top
Total: 0 results in 0 of 562 checks. Total number of non-empty checks is 0.

```

[DRC] DRC [LVS] LVS

```

#####
# Run Result : MATCH
#
# Run Summary : [INFO] ERC Results: Empty
#                : [INFO] Extraction Clean
#
# ERC Summary File : SenseAmpCell.sum
# Extraction Report File : SenseAmpCell.rep
# Comparison Report File : SenseAmpCell.rep.cls
#
#####

Checking in all SoftShare licenses.

PVS Comparison Finished. Thu Sep 23 21:51:45 2021
```

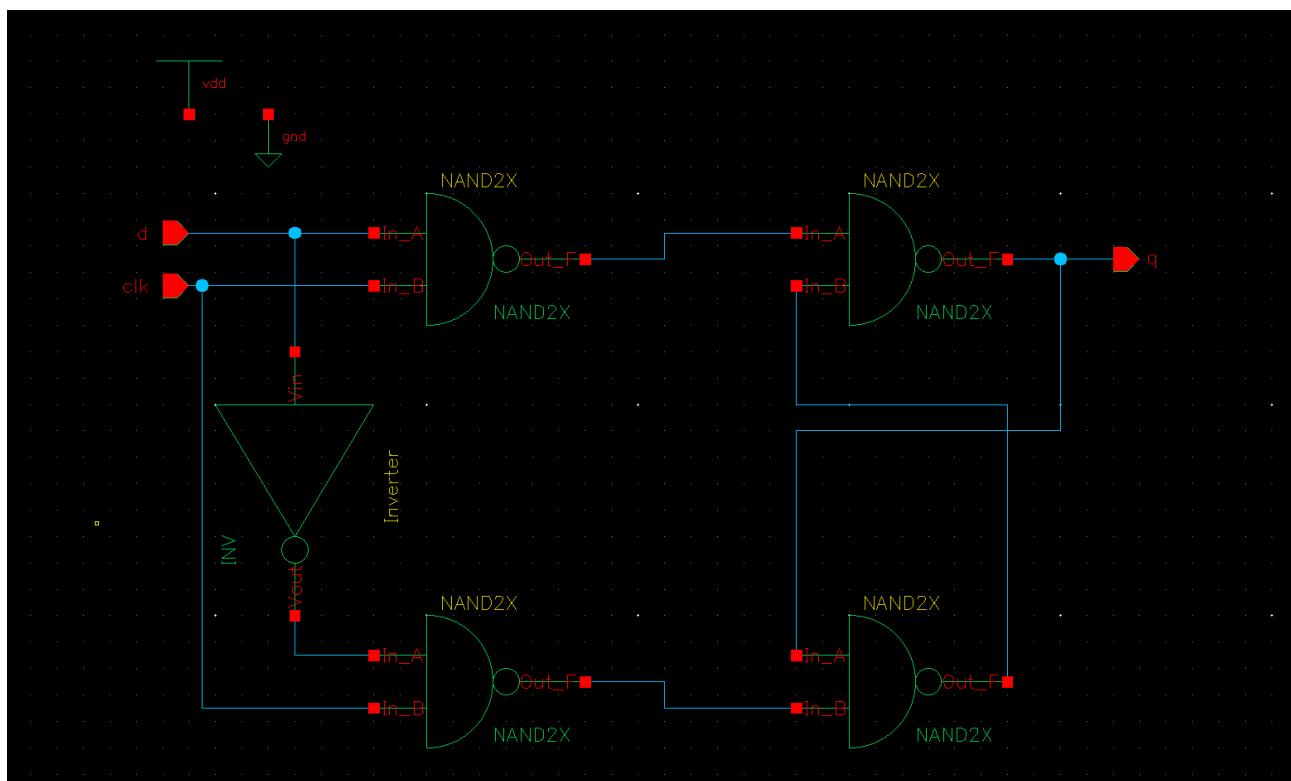


ERC Results **Empty**  
 Extraction Results: **Clean**  
 Comparison Results: **Match**

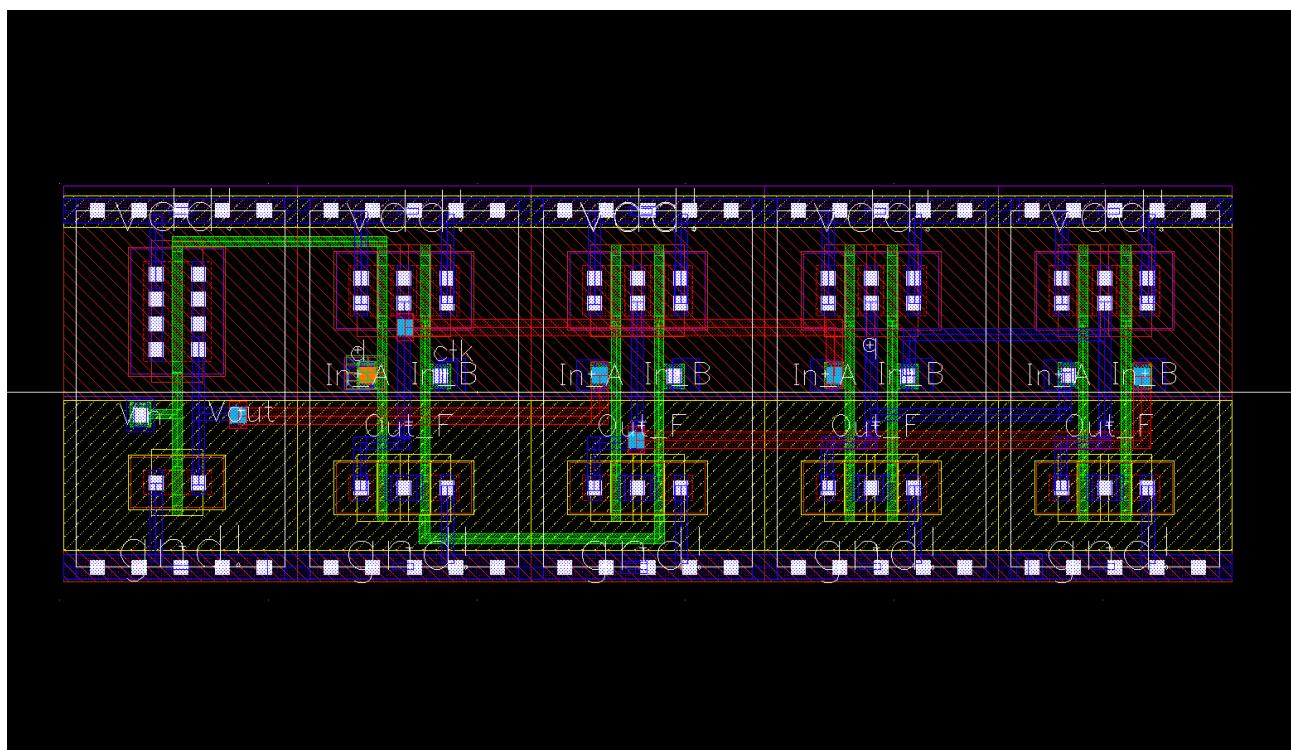
Do you want to start the LVS DE?

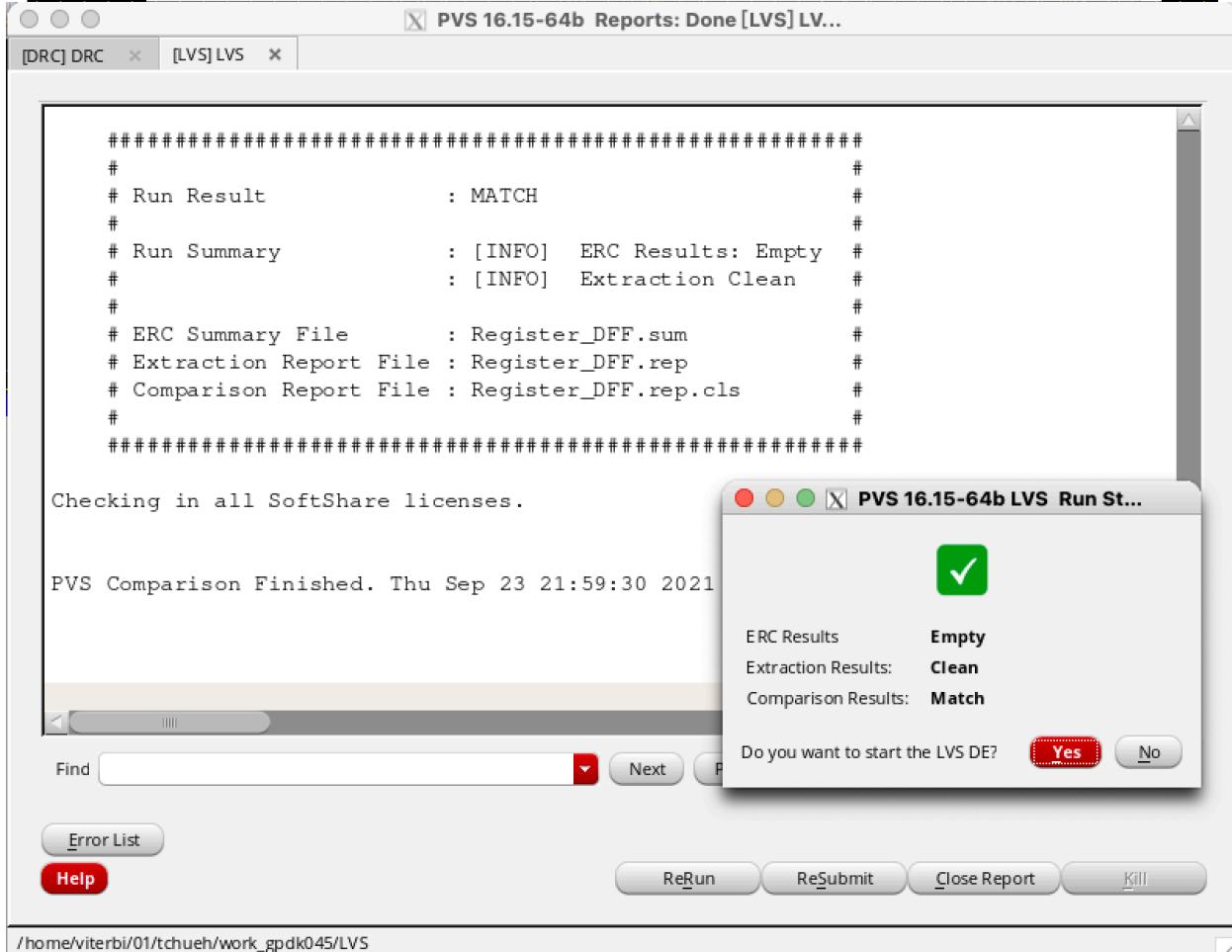
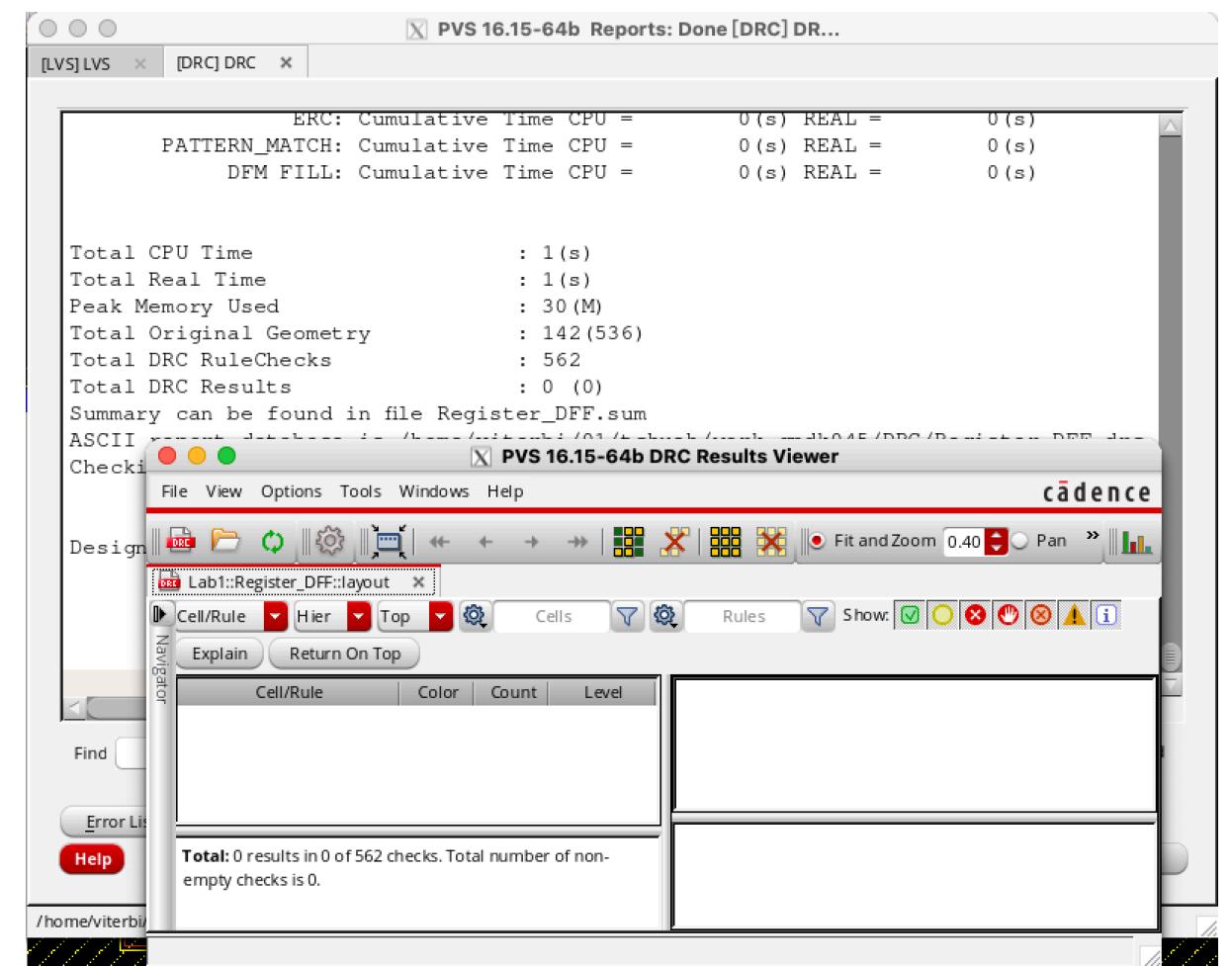
ReRun ReSubmit Close Report Kill

## Register (Schematic)

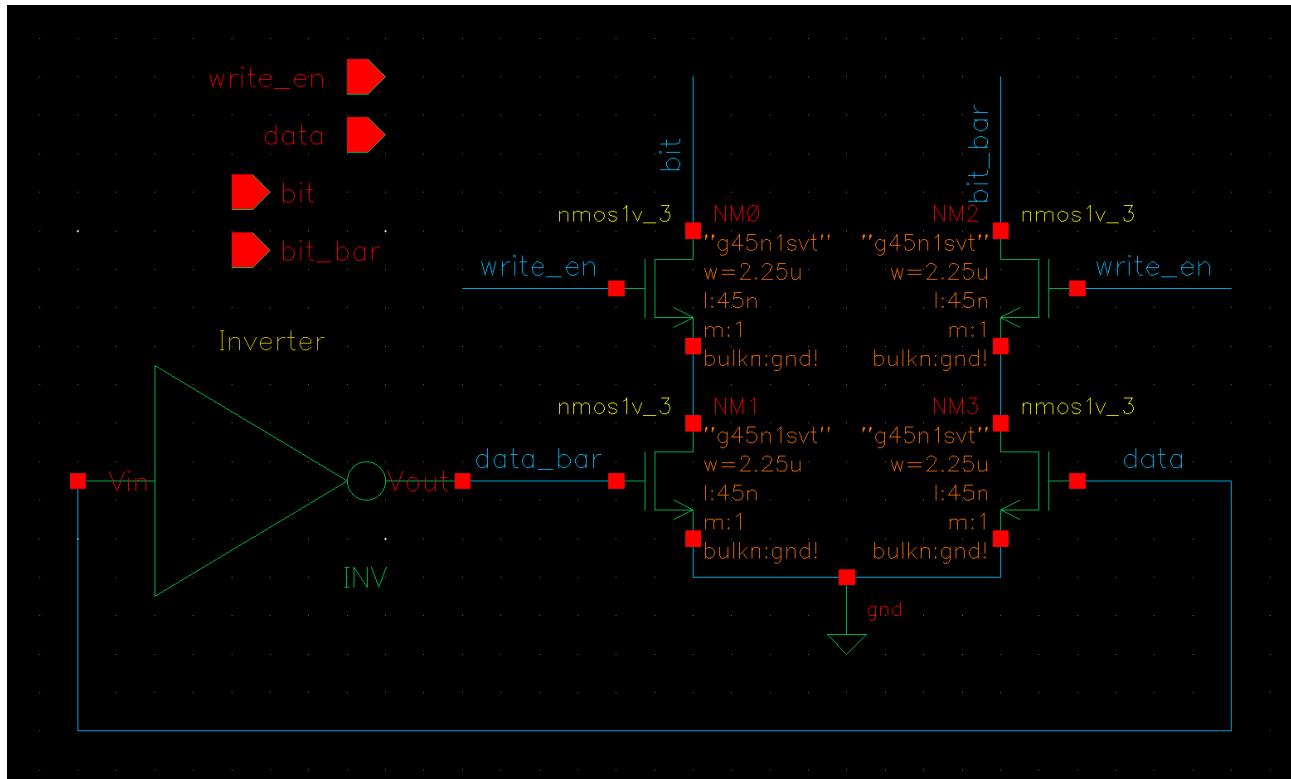


## Register (Layout)

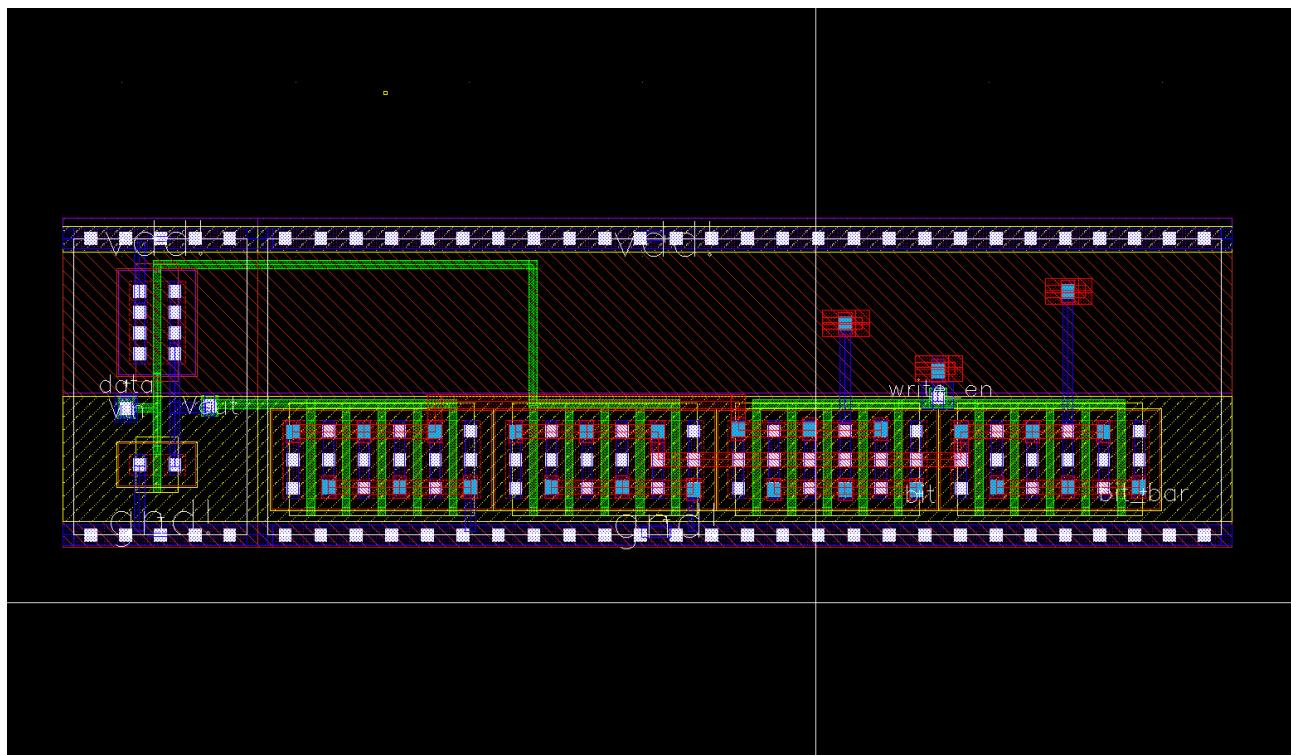




## Write Path (Schematic)



## Write Path (Layout)



PVS 16.15-64b Reports: Done [DRC] DR...

[LVS] LVS    [DRC] DRC

```

ERC: Cumulative Time CPU =      0 (s) REAL =      0 (s)
PATTERN_MATCH: Cumulative Time CPU =      0 (s) REAL =      0 (s)
DFM FILL: Cumulative Time CPU =      0 (s) REAL =      0 (s)

Total CPU Time : 1 (s)
Total Real Time : 1 (s)
Peak Memory Used : 30 (M)
Total Original Geometry : 255 (525)
Total DRC RuleChecks : 562
Total DRC Results : 0 (0)
Summary can be found in file WritePathCell.sum
ASCII re: Checking File View Options Tools Windows Help
Design E DRC Lab1::WritePathCell::layout
Cell/Rule Hier Top Cells Rules Show: Explain Return On Top
Total: 0 results in 0 of 562 checks. Total number of non-empty checks is 0.

```

PVS 16.15-64b Reports: Done [LVS] LV...

[DRC] DRC    [LVS] LVS

```

#####
# Run Result : MATCH
#
# Run Summary : [INFO] ERC Results: Empty
#                : [INFO] Extraction Clean
#
# ERC Summary File : WritePathCell.sum
# Extraction Report File : WritePathCell.rep
# Comparison Report File : WritePathCell.rep.cls
#
#####

Checking in all SoftShare licenses.

PVS Comparison Finished. Thu Sep 23 21:56:10 2015

```

PVS 16.15-64b LVS Run St...

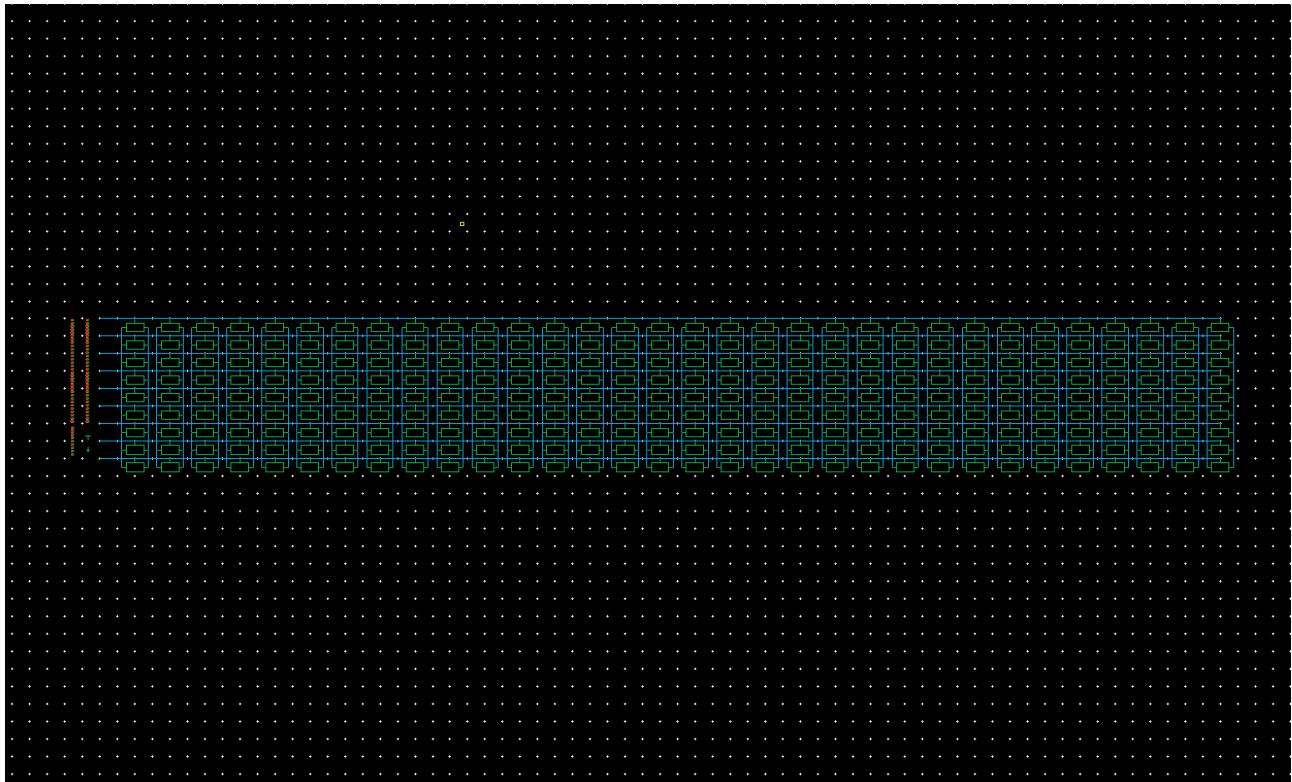
ERC Results	Empty
Extraction Results:	Clean
Comparison Results:	Match

Do you want to start the LVS DE?

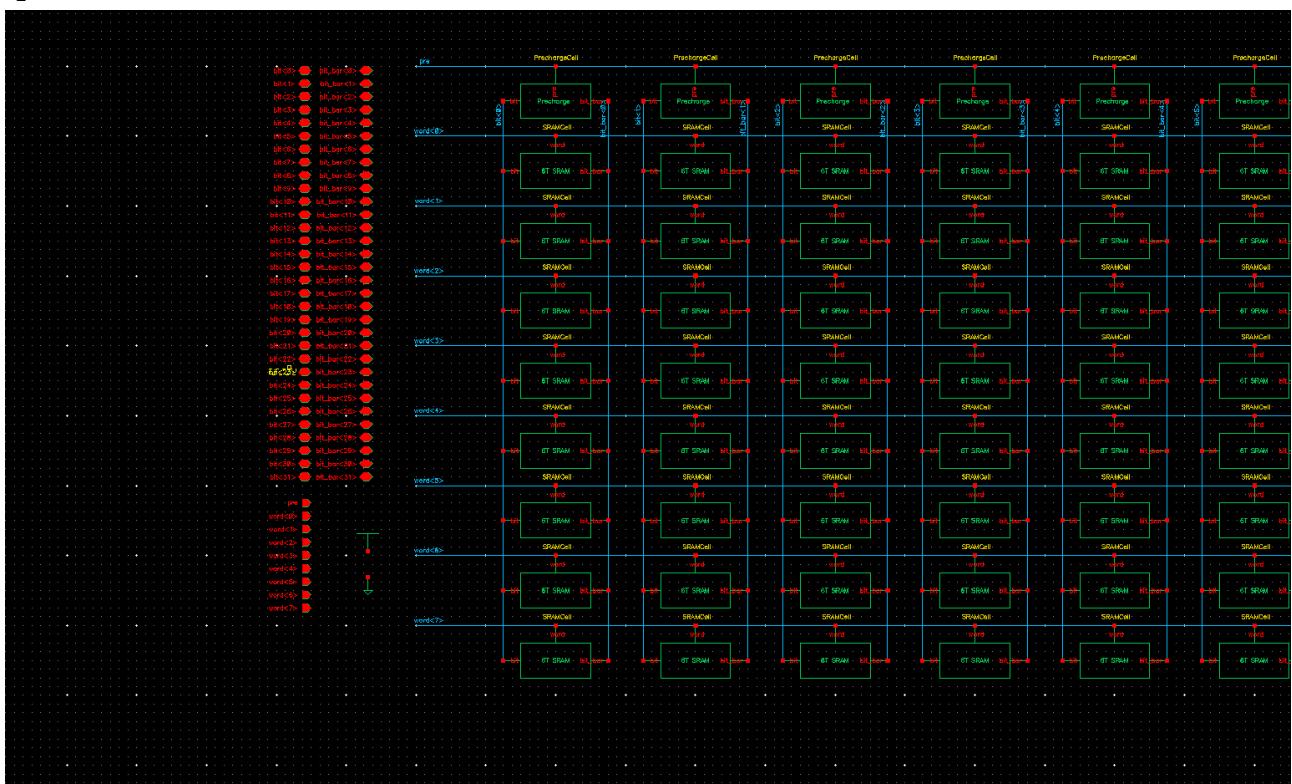
Find    Next    ReRun    Resubmit    Close Report    Kill

Error List    Help

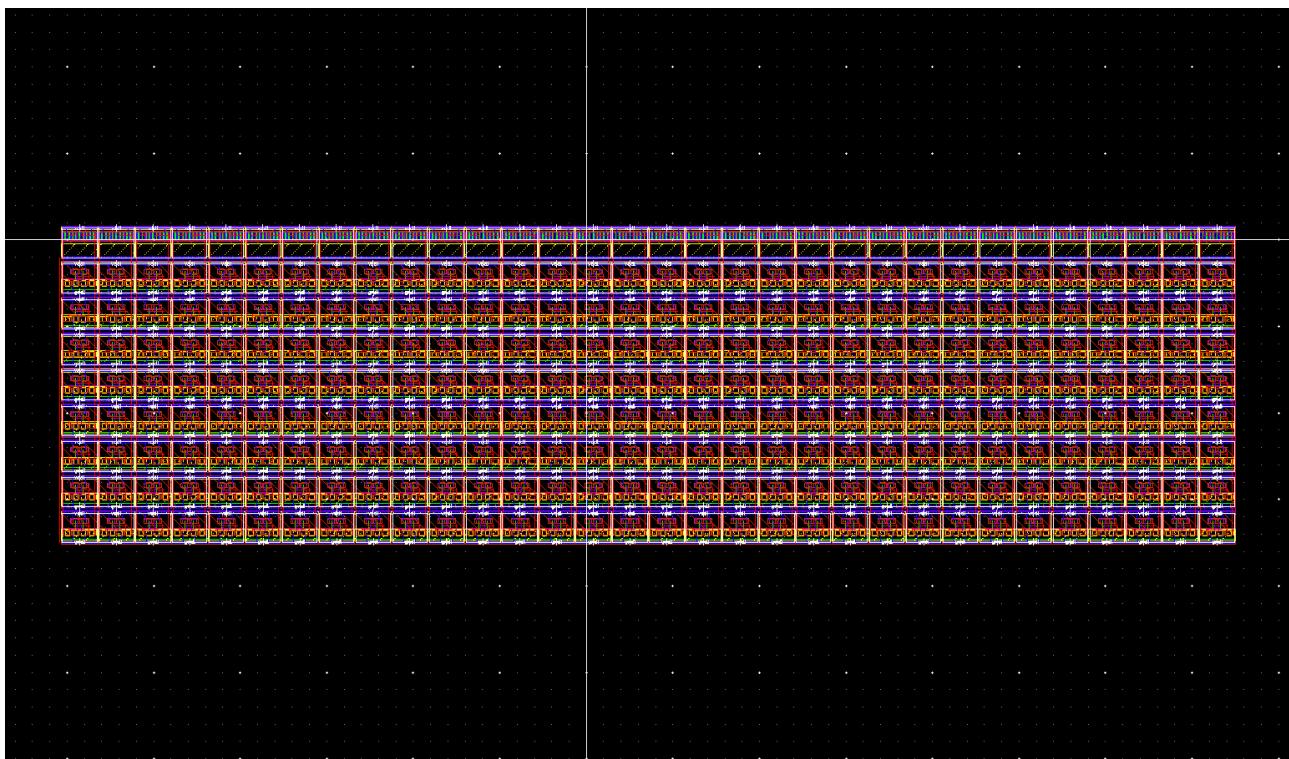
## SRAM 8x32 Bank (Schematic)



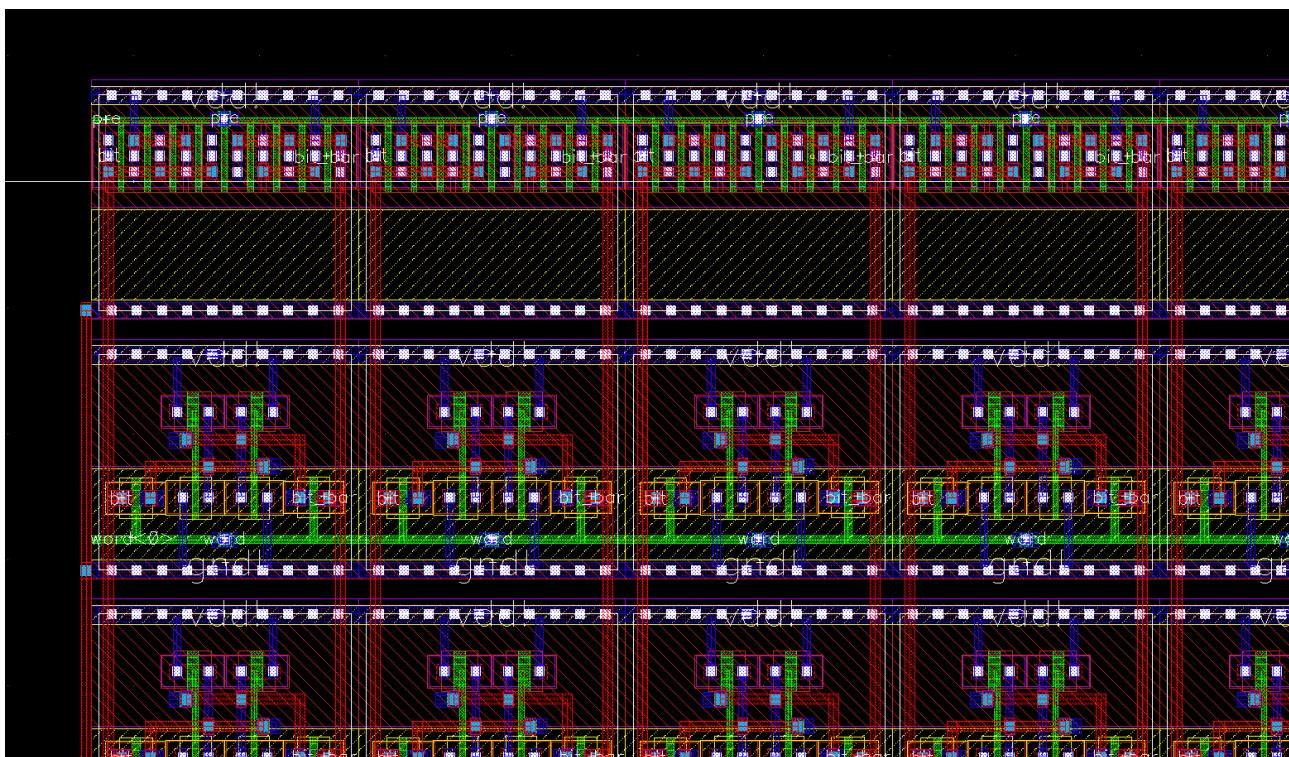
Each 256-bit SRAM bank was constructed with 8 row, 32 columns. The pre-charge was placed at the first row and connected to all the bit line and bit line bars.

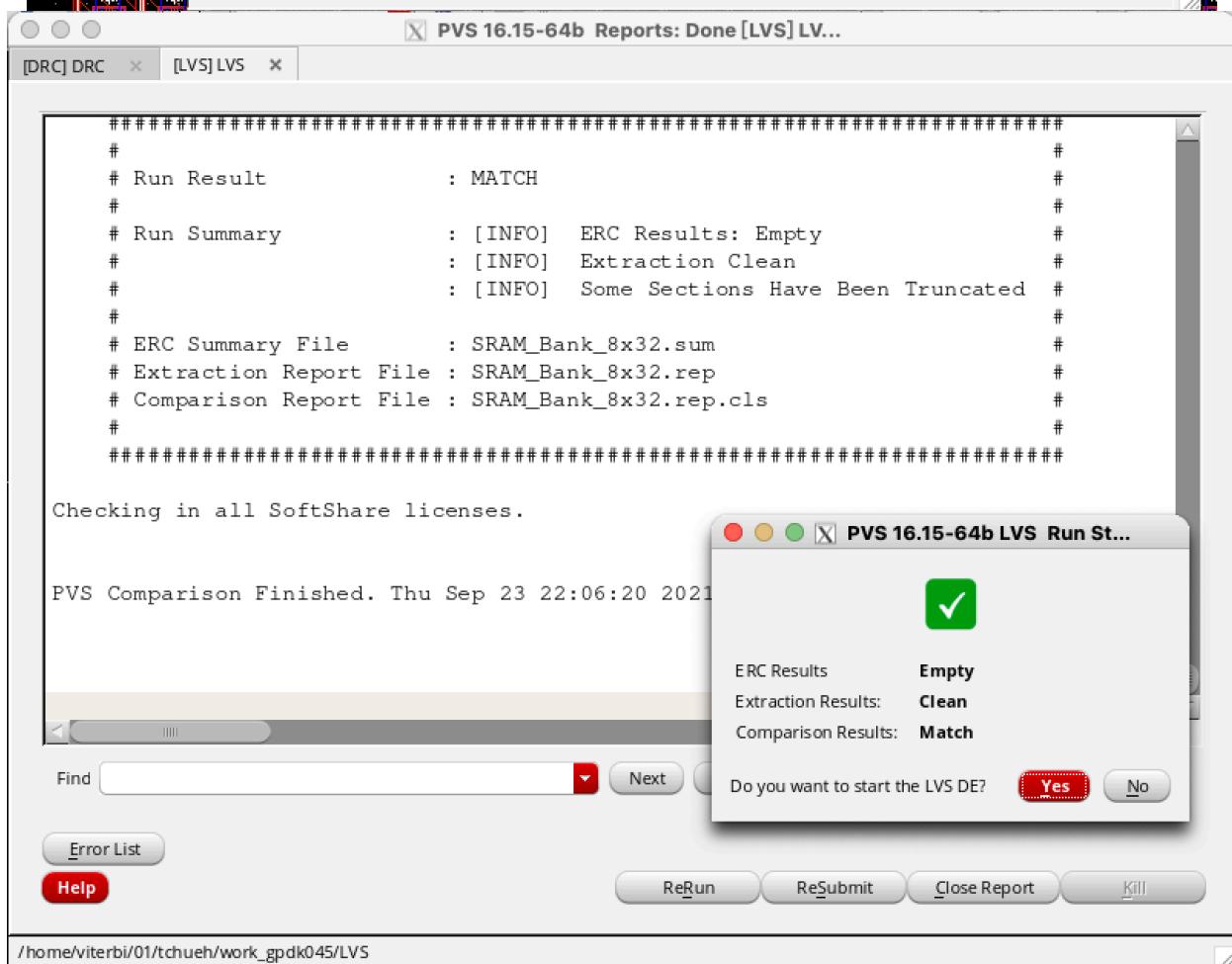
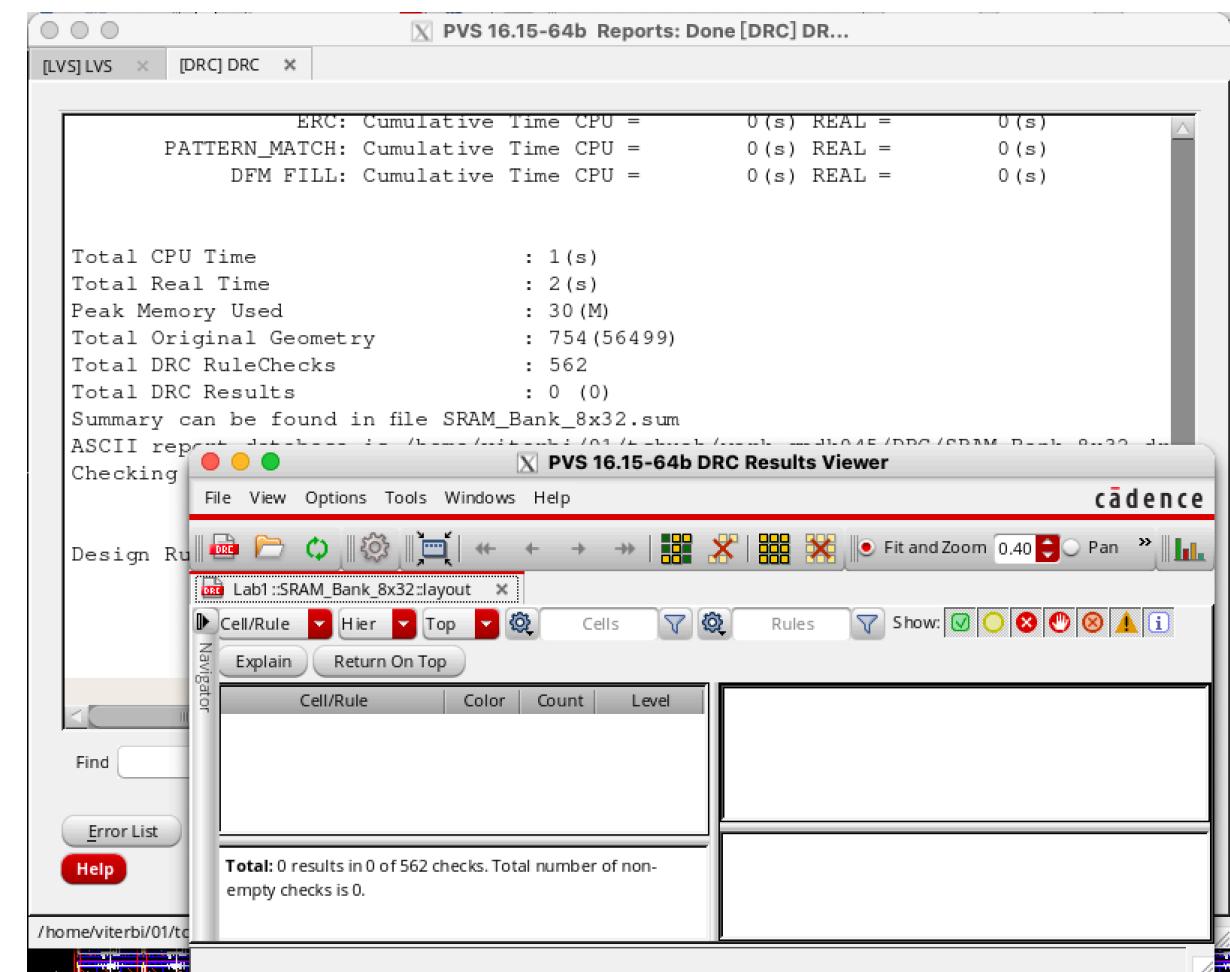


## SRAM 8x32 Bank (Layout)

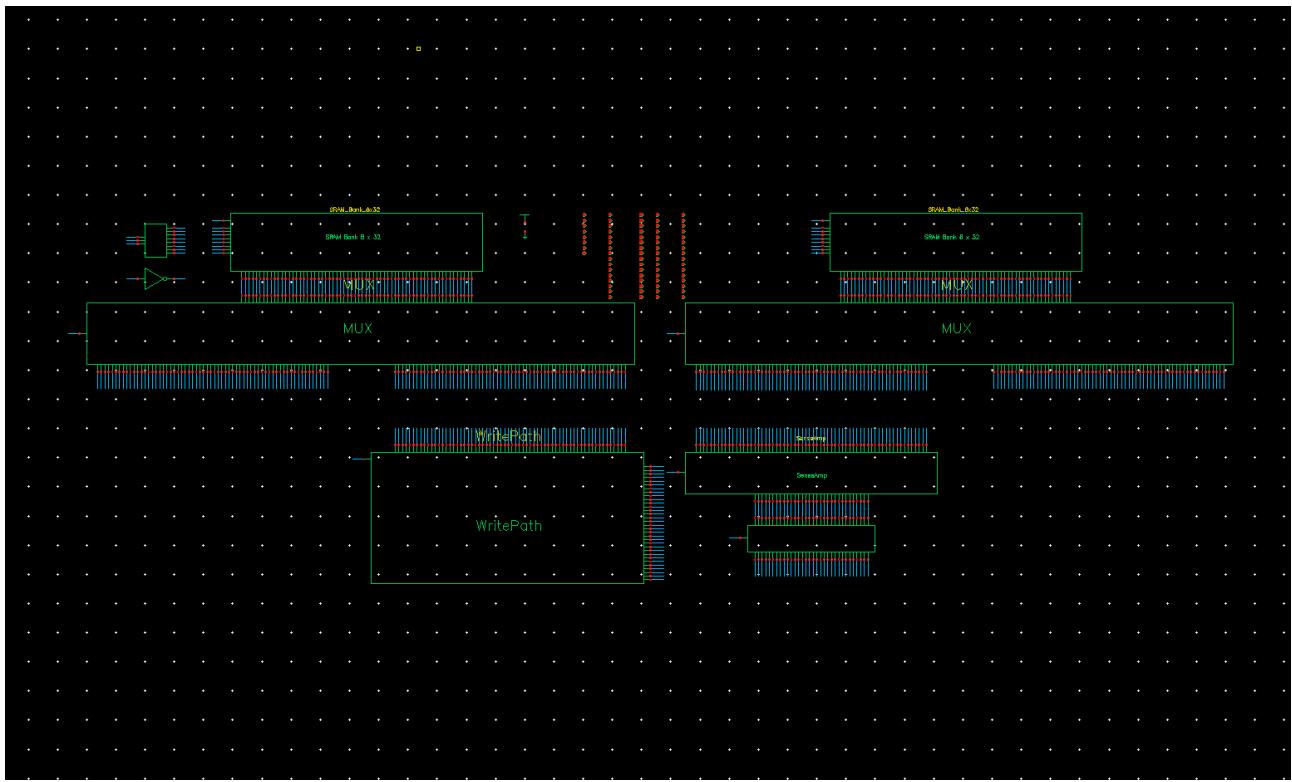


The first row is the pre-charge system and following with 8 SRAM Cells.

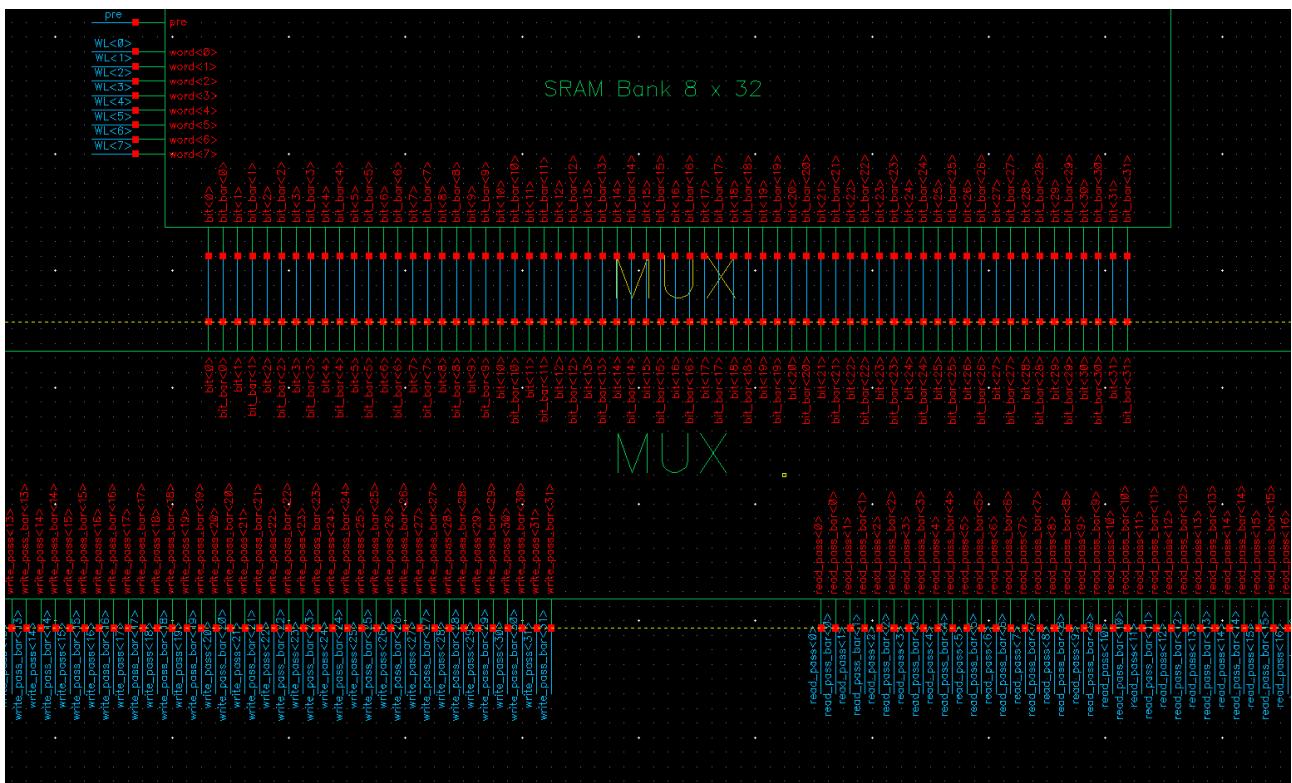




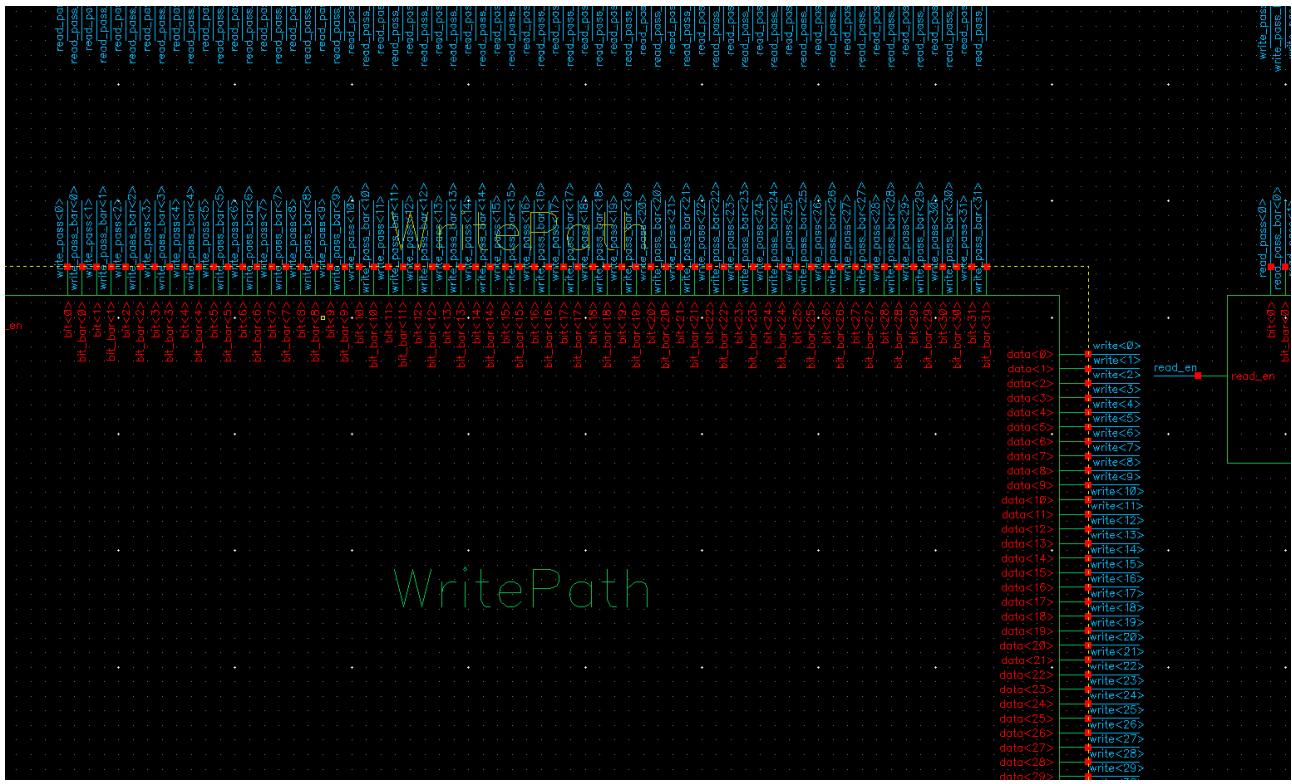
## SRAM 512-bit (Schematic)



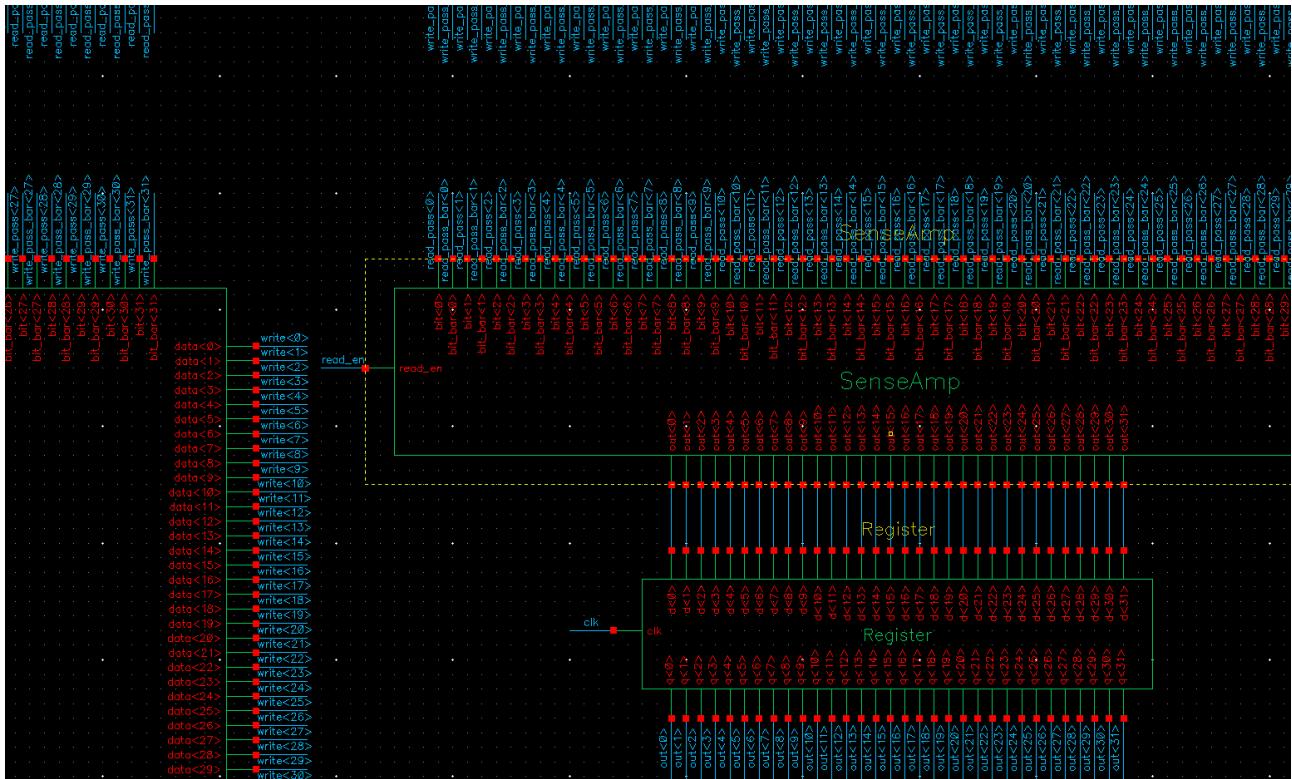
The SRAM Bank is connected to write/read MUX.



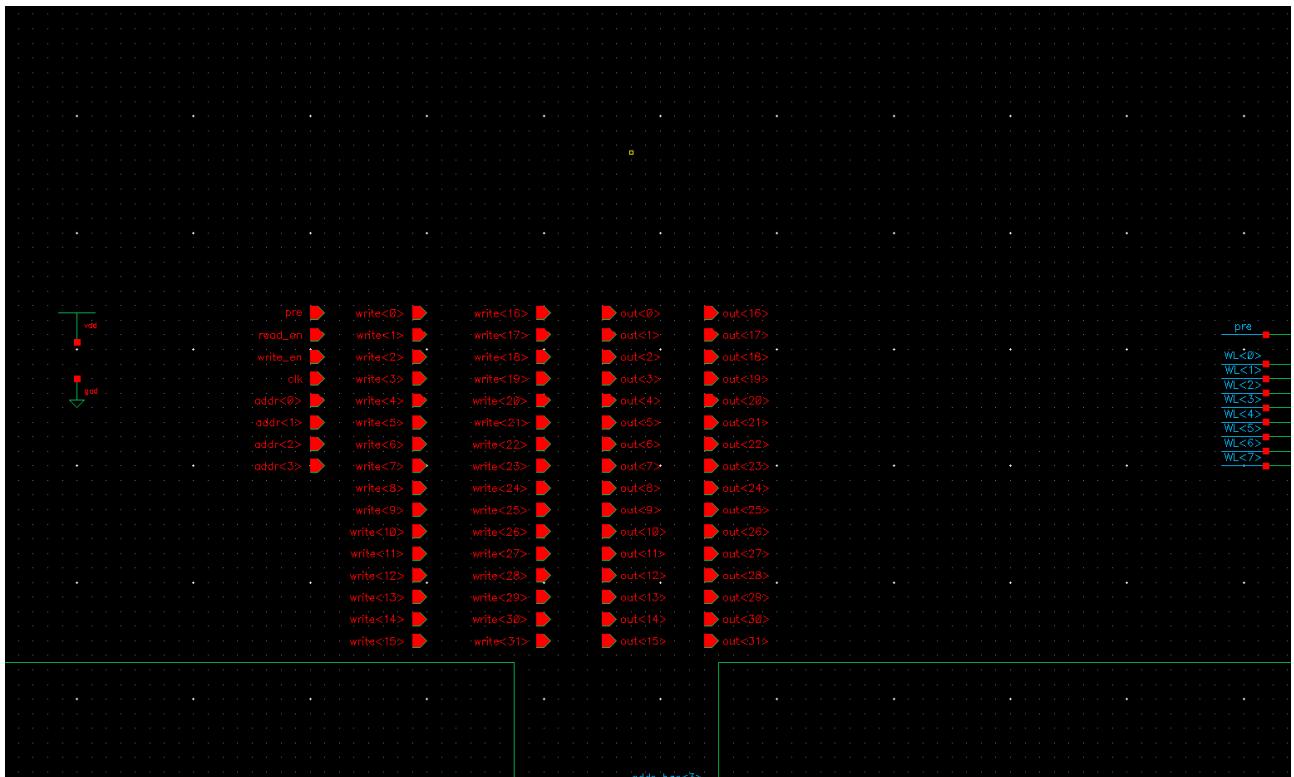
The write\_pass of the MUX is connected to the bit line in Write Path.



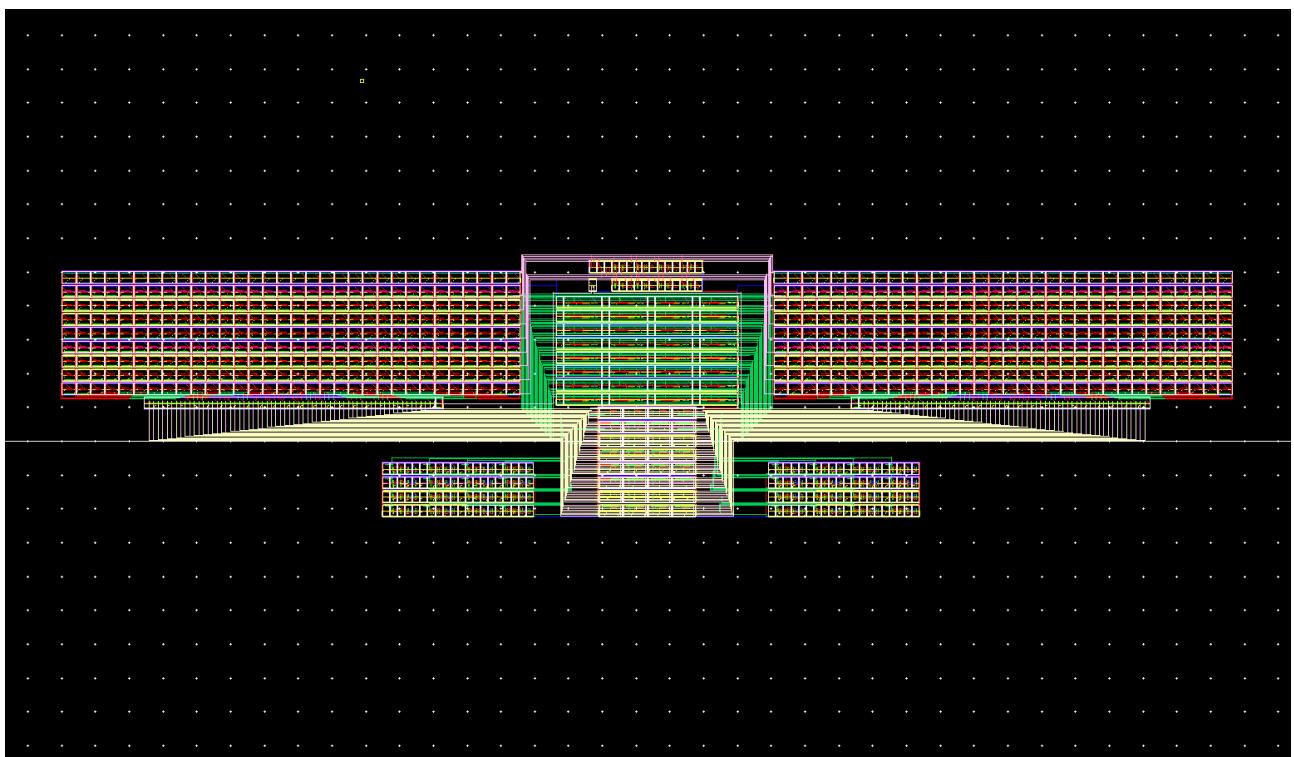
The read\_pass of the MUX is connected to the bit line in Sense Amp.

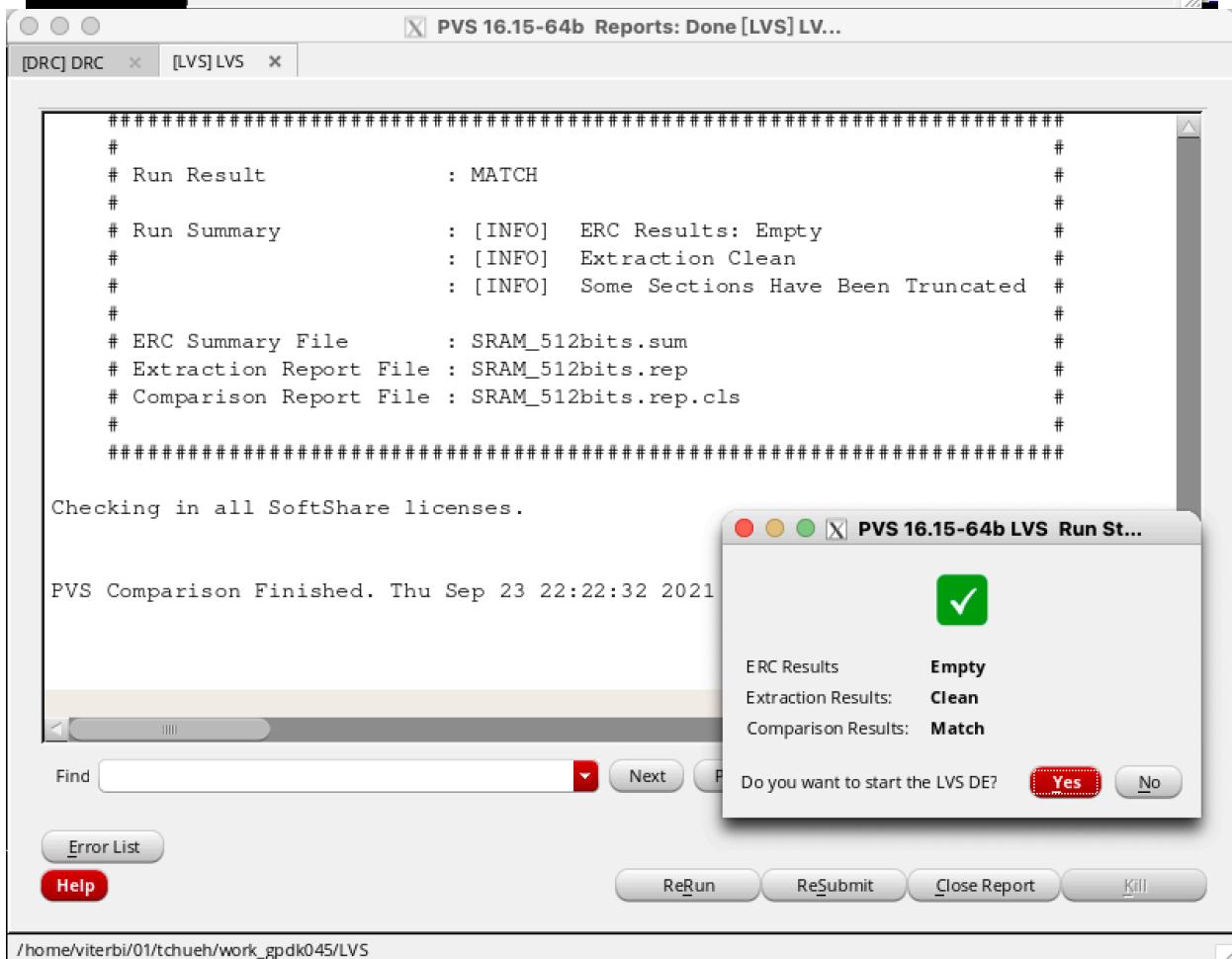
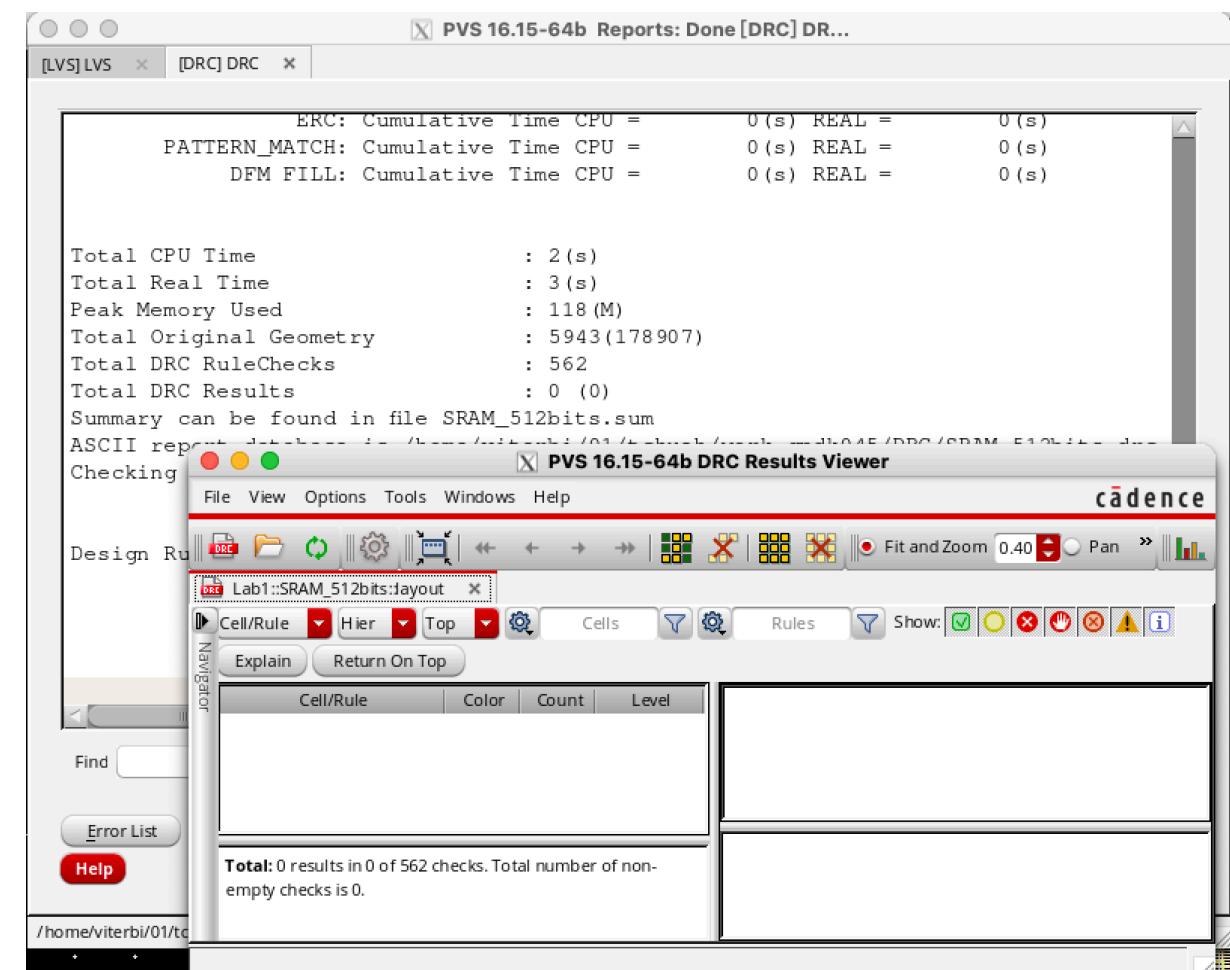


The figure below is the I/O pins of the SRAM 512-bit.

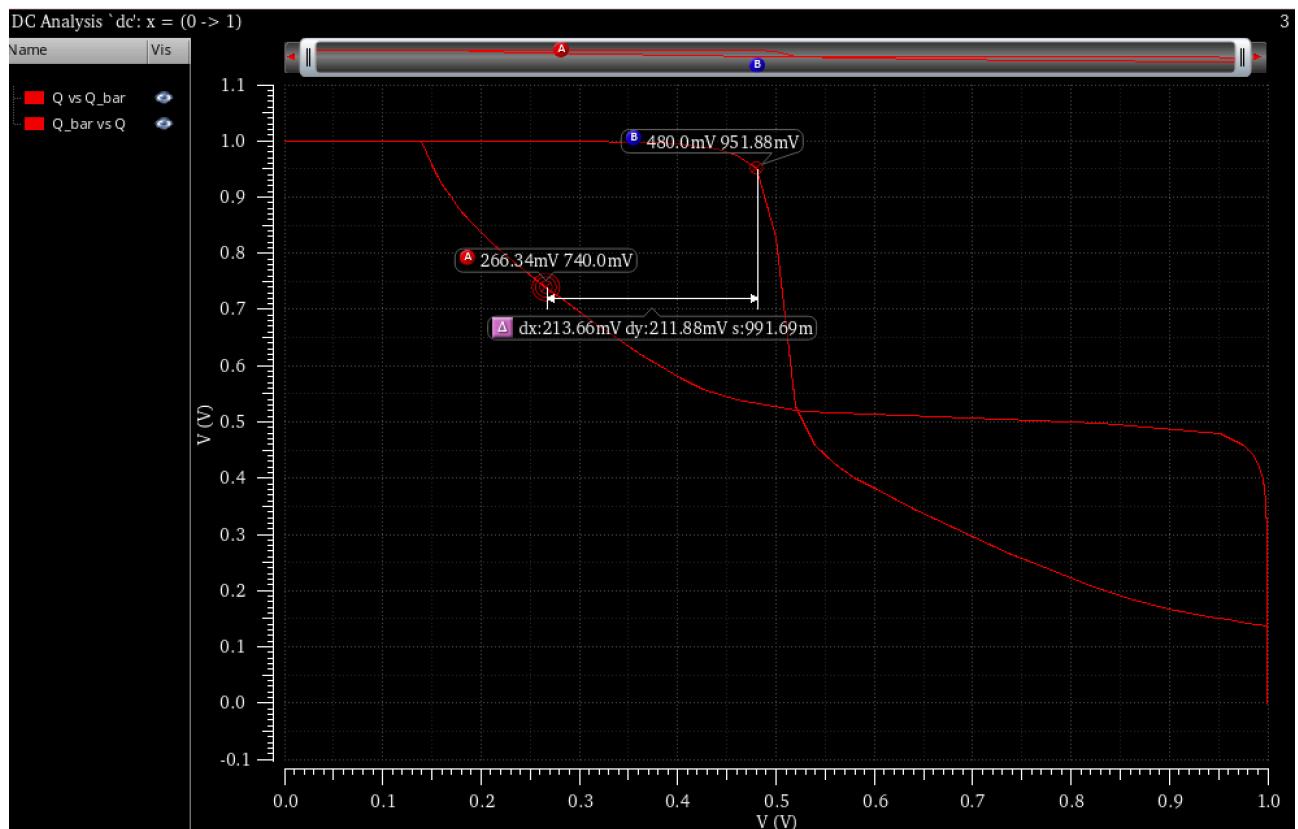


SRAM 512-bit (Layout)

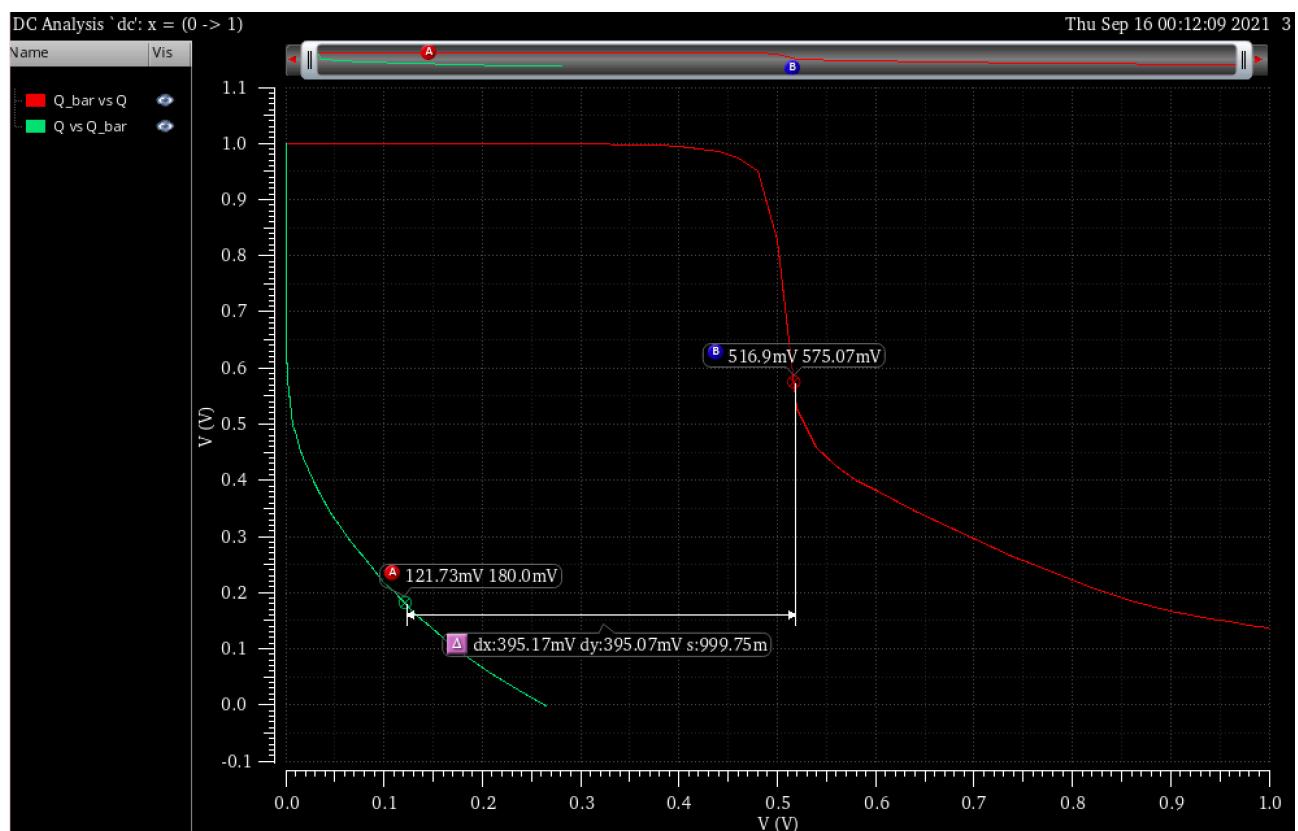




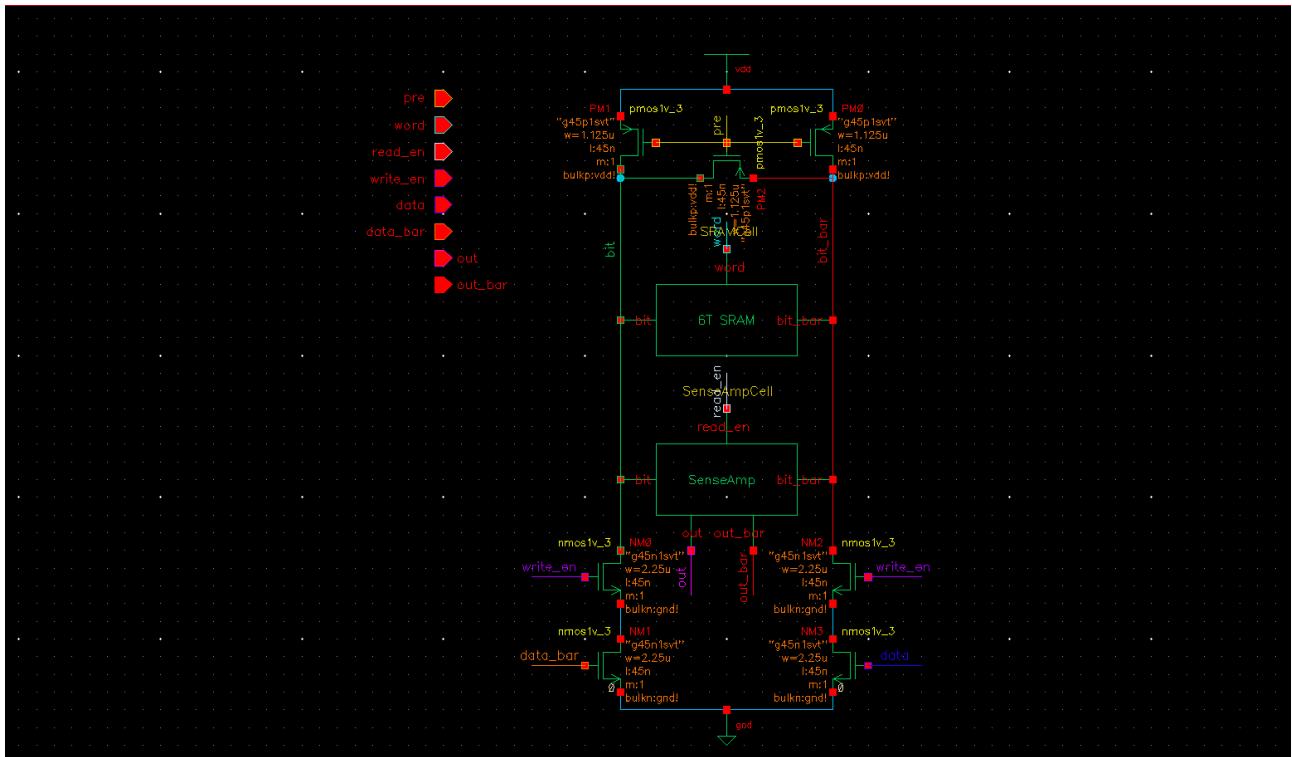
Read SNM is at least 190mV



Write SNM is at least 395mV



## SRAM One Cell (Schematic)



The figure below shows the simulation for the single SRAM Cell with the waveform of the operation Write 1 → Read → 1 → Write 0 → Read 0.



Write 1   Read 1   Write 0   Read 0  
12.57 ps   8.52 ps   11.49 ps   8.52 ps

SRAM operation:

During the write operation, the 32-bit input data will be send to the Write Path. The `addr<3>` is going decide which Memory Bank will save the data. After that, the output of the Write Path (bit / bit\_bar) is pass through the nMOS pass transistors in the MUX and stored in the 256-bit SRAM Bank.

During the read operation, the address we got will decide which word line and which Memory Bank to read from. The Sense Amplifier sense the difference in the bit and bit\_bar when the pMOS pass transistors in the MUX tuns on.

Register at the output controls the information when it is available at the clock edge as the Sense Amplifier sense the difference.

Summary:

Area  $173.325 \times 38.807 = 6726.22328$

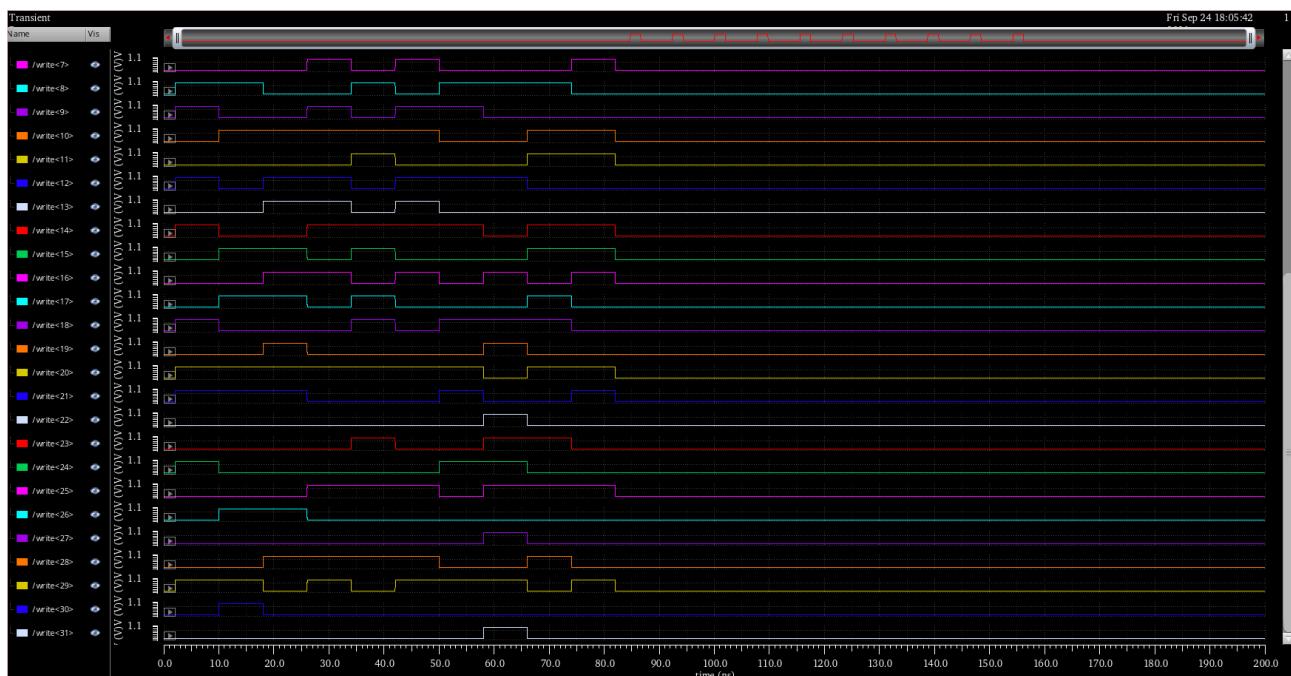
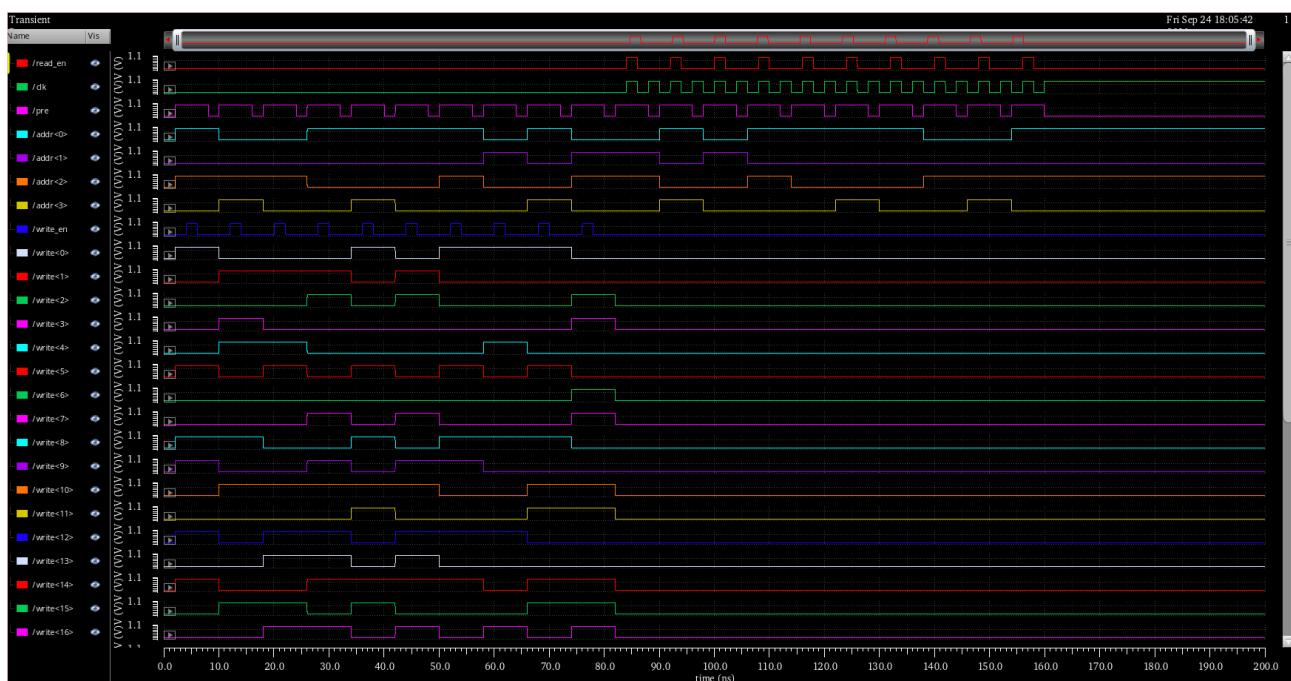
Complete time: 160 ns

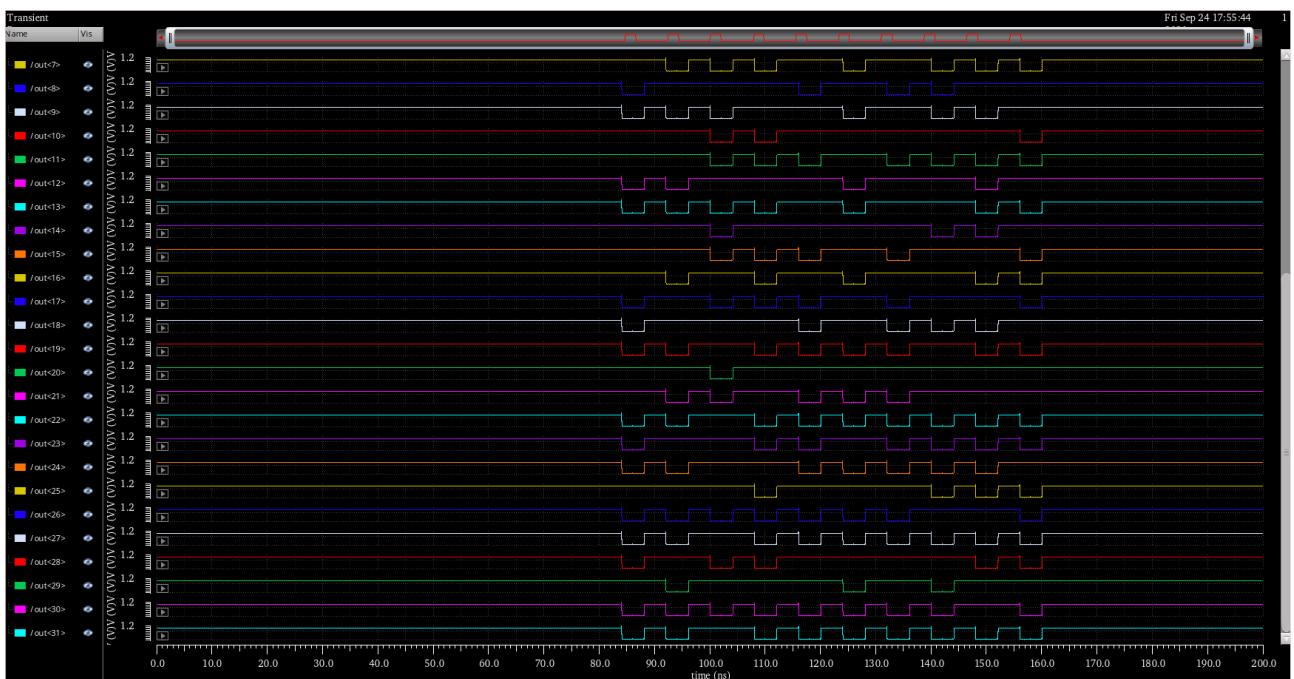
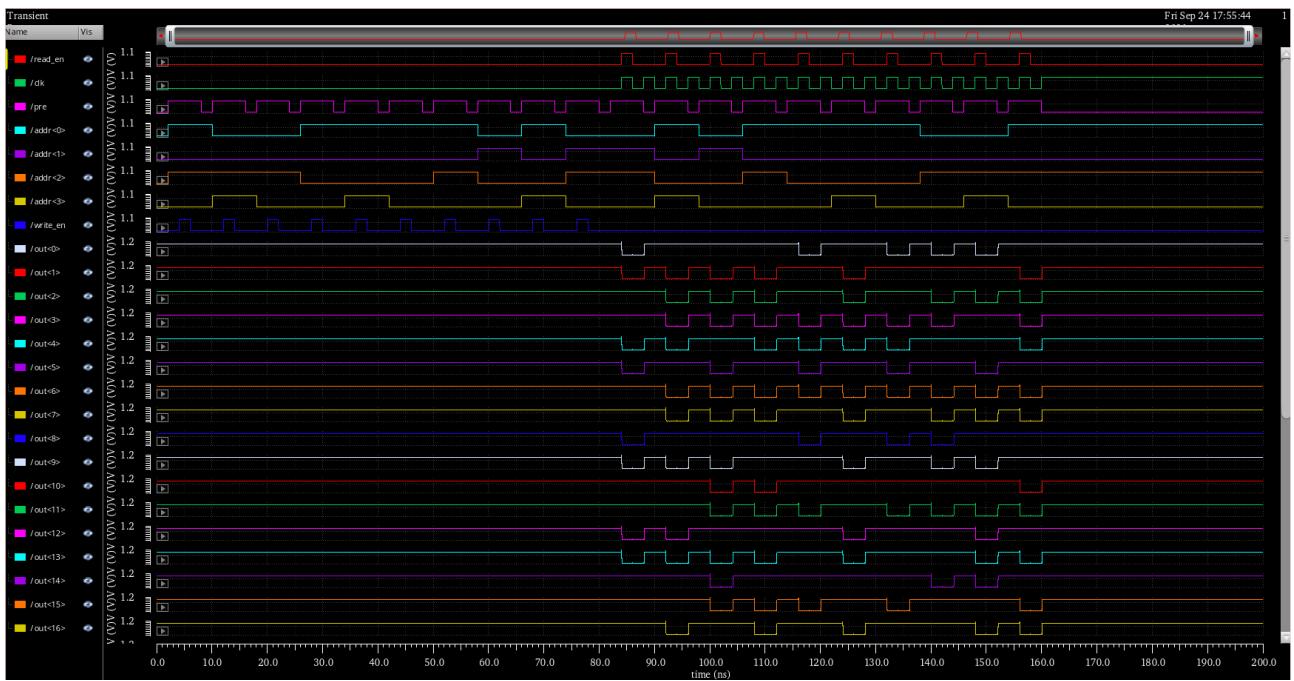
Clock Frequency:  $1/4 \text{ ns} = 250 \text{ MHz}$

Read 10 data values (32 bit each) from a vector file and write into the SRAM in a sequential order starting from the last digit of your USC ID and then read 10 of them in the sequence of your USC ID.

SEQUENCE	A[3]-A[0]	DATA[31]-[0]
0	0100	143B B432
1	0101	2134 5321
2	0111	ABCD 1234
3	0110	2231 CCCC
4	0001	3211 7686
5	0010	ABCD 1111
6	1000	12AB CD91
7	1001	1296 CD21
8	1010	7A5A 6531
9	1100	6432 851A

## SRAM 512-bit (Schematic Waveform)





## SRAM 512-bit (Extracted Waveform)

