

EE 477- Spring 2021 VLSI CIRCUIT DESIGN

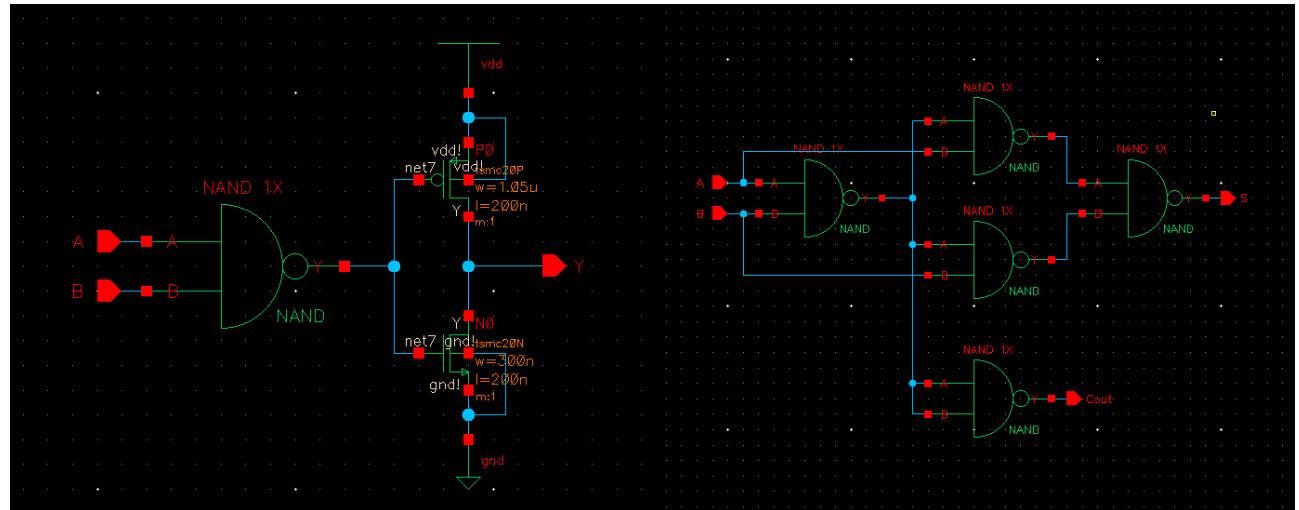
Lab4-1 Report 16-bit Adder & 6x6-bit Multiplier Design

Ti-Shen Chueh

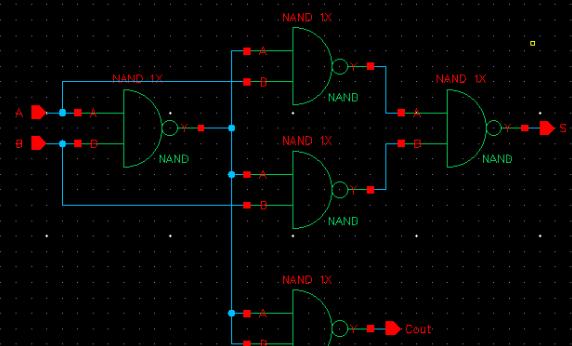
tchueh@usc.edu

3751474091

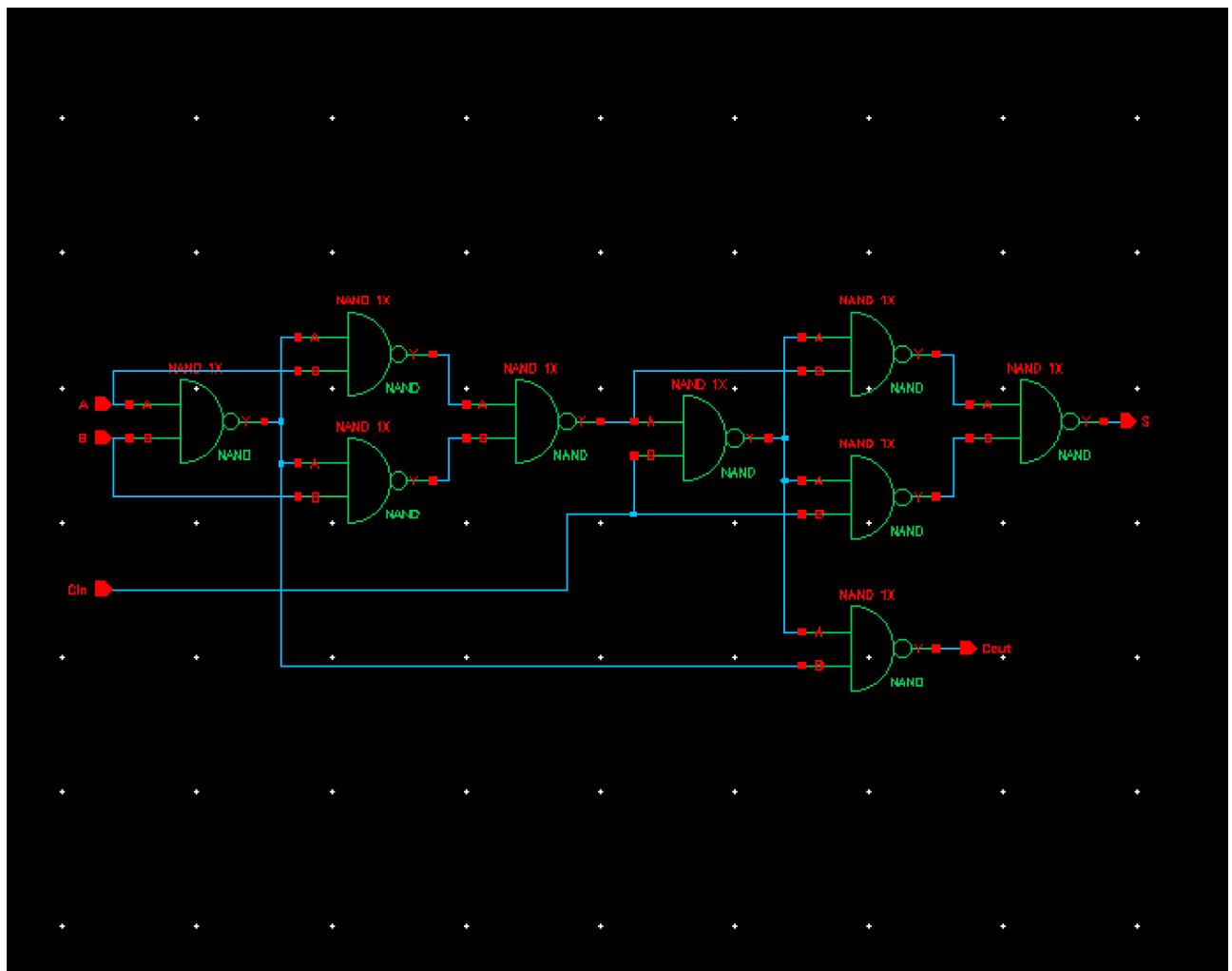
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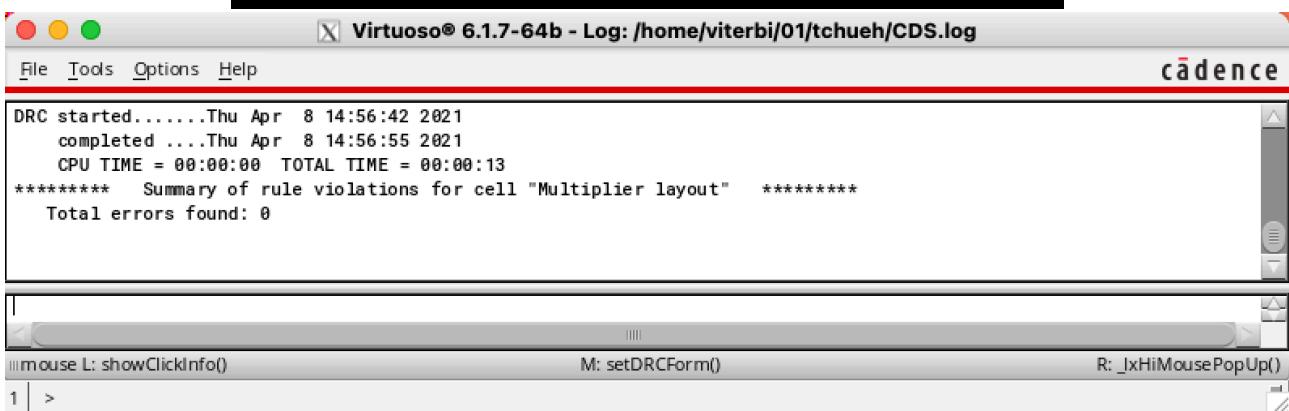
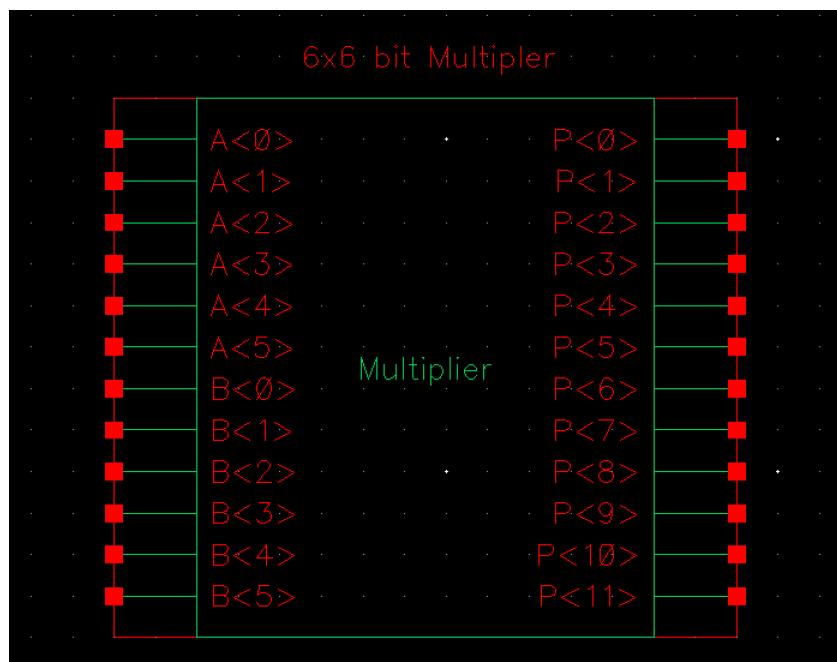
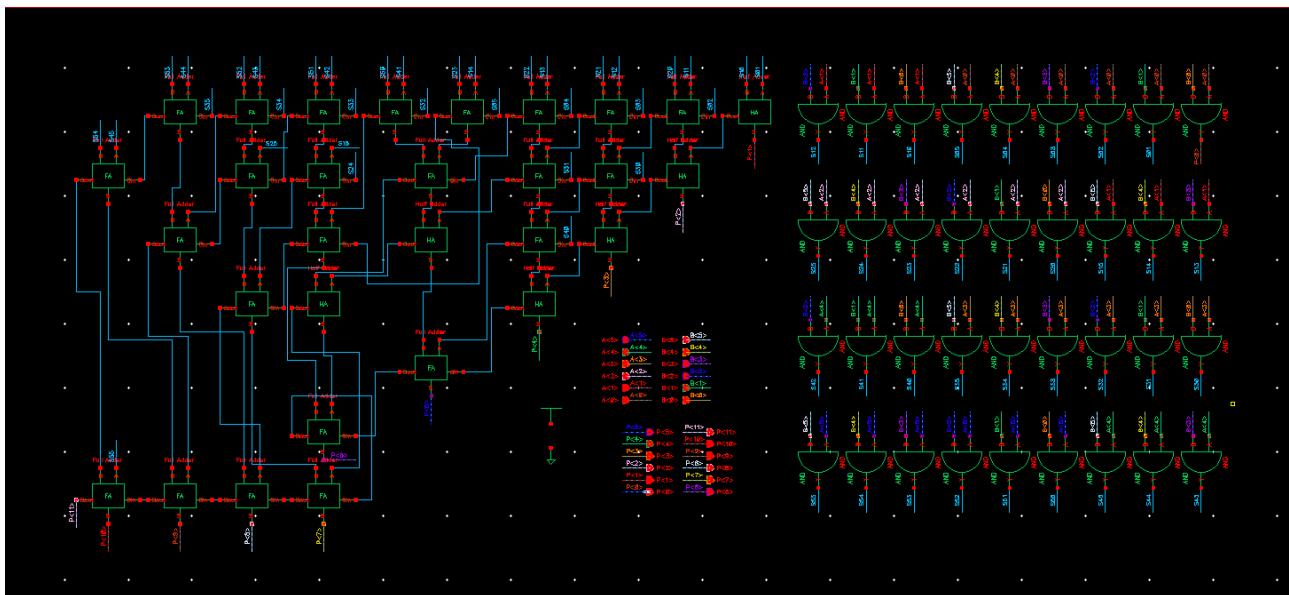
Half adder

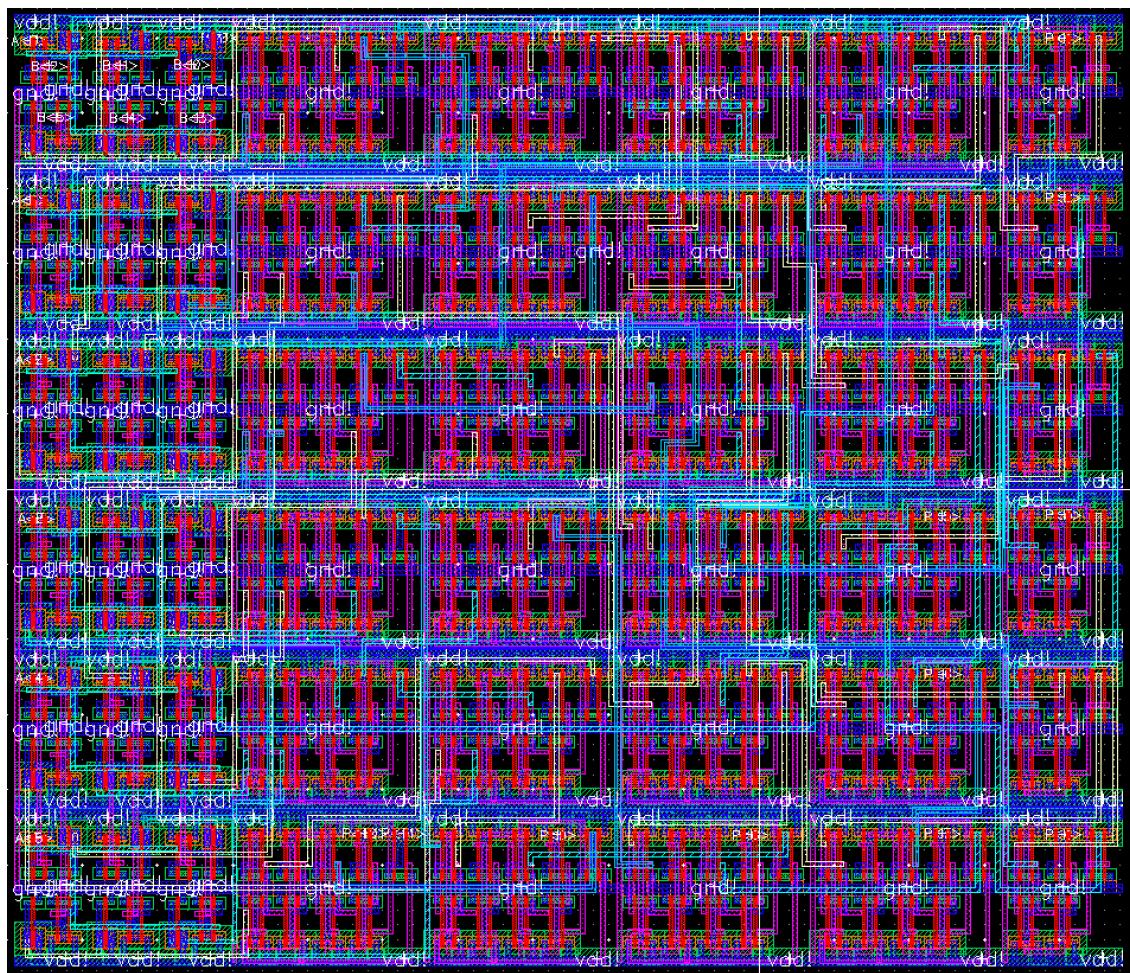


Full Adder

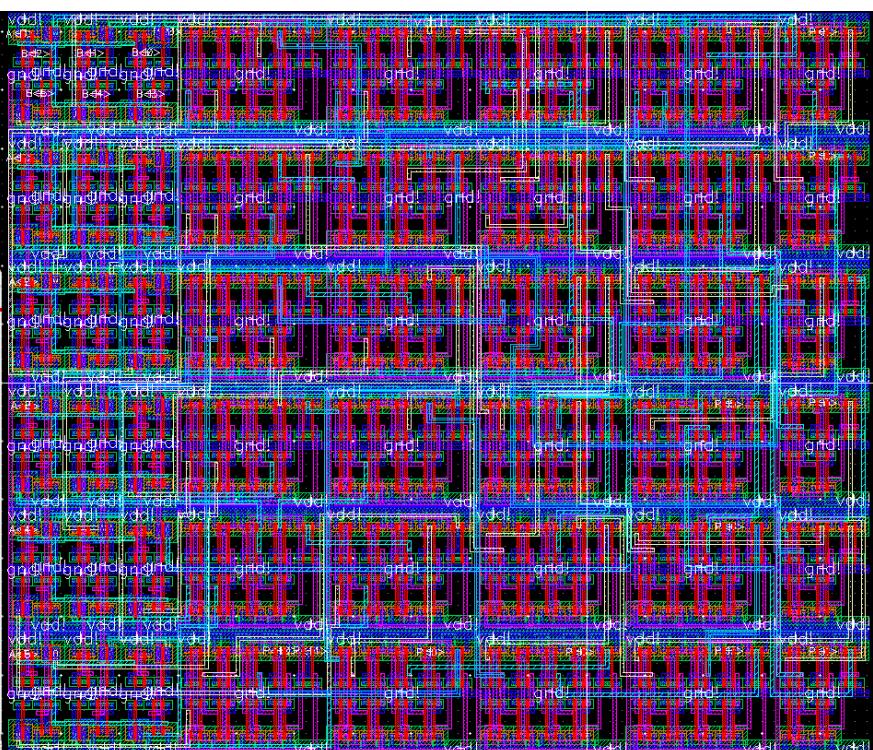
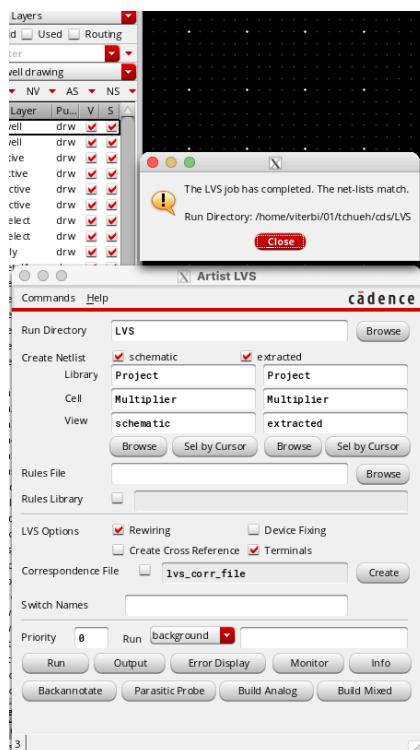


Wallace tree Multiplier

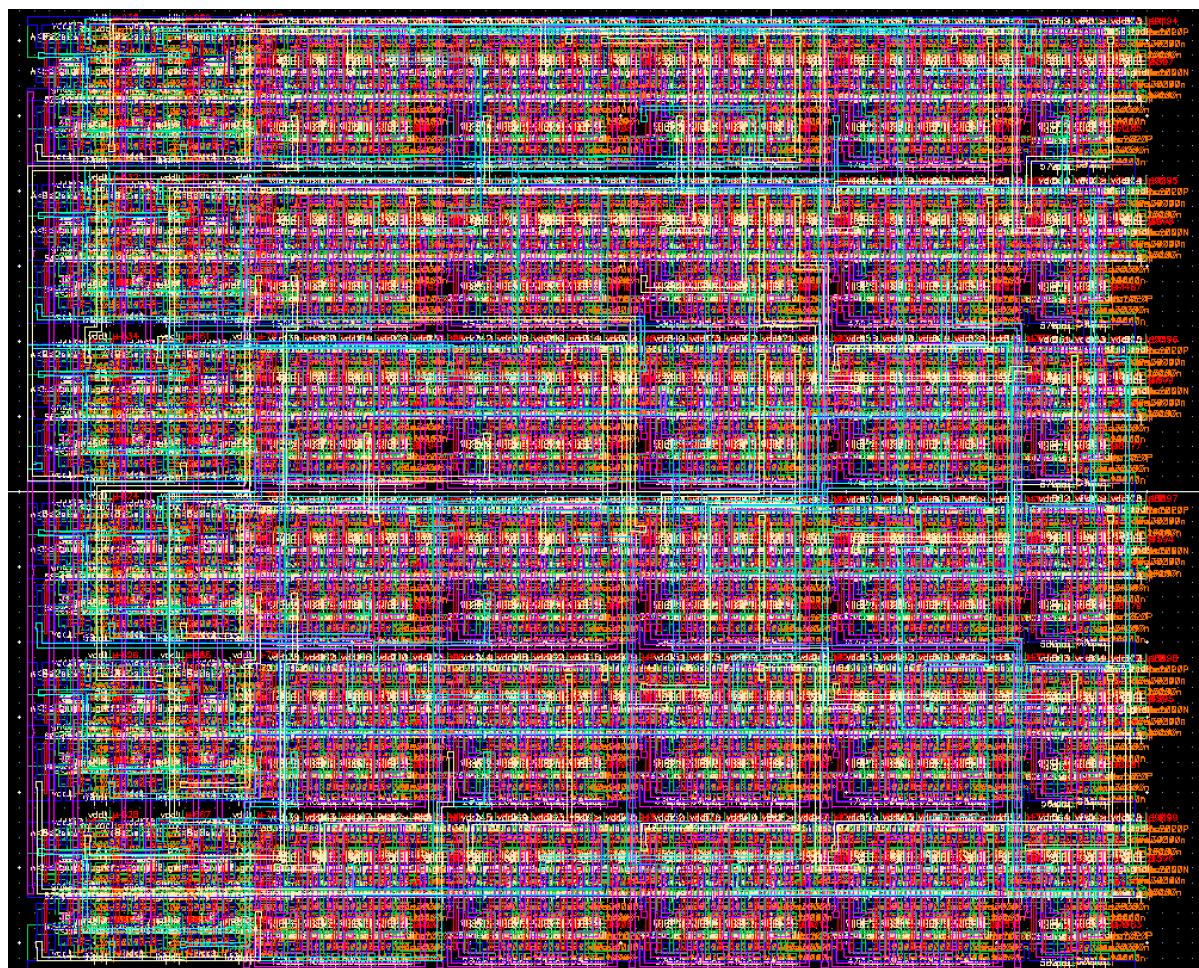
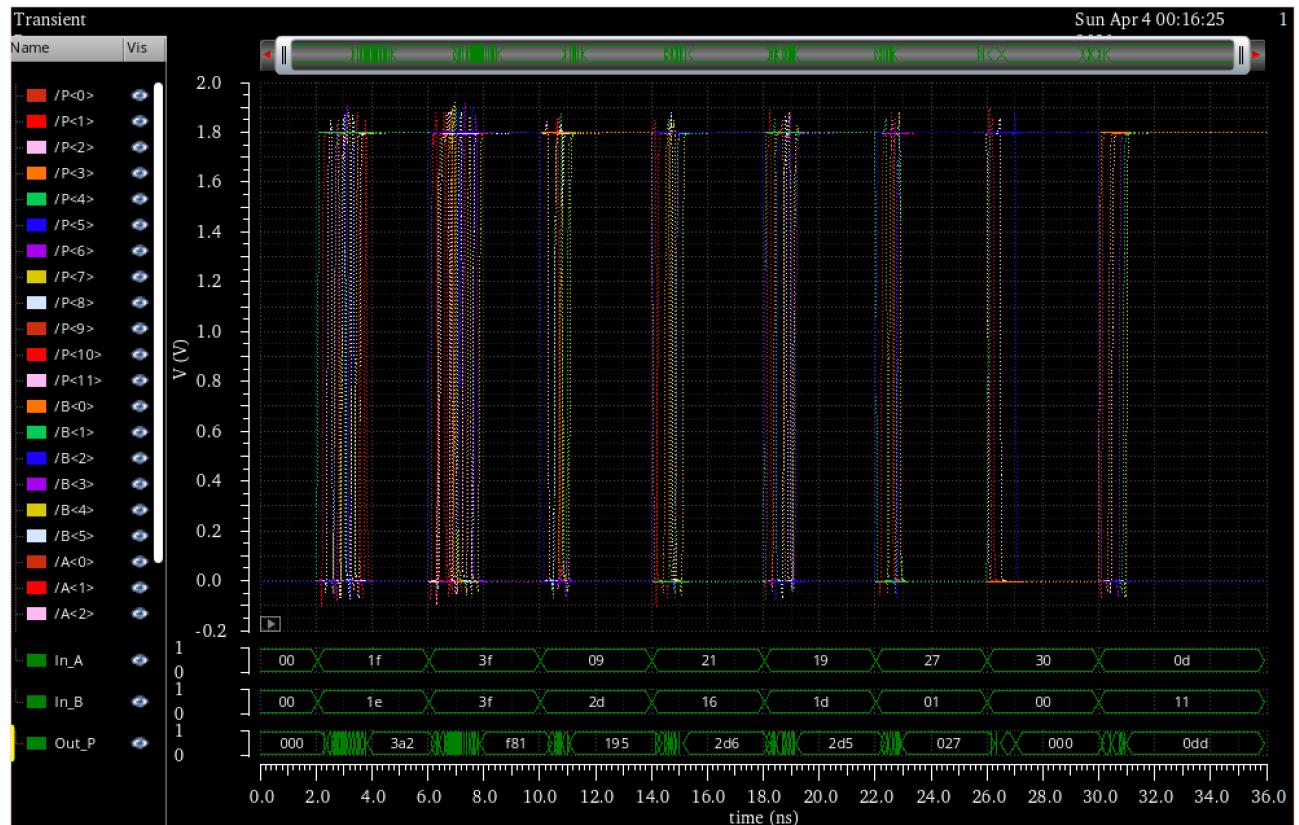




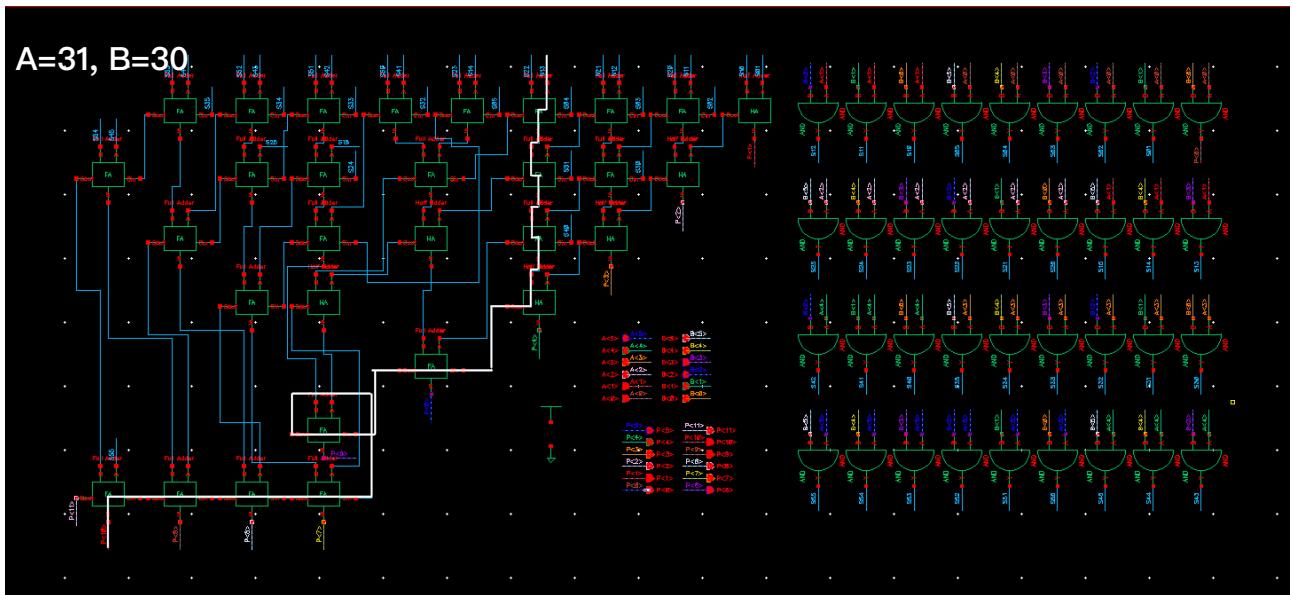
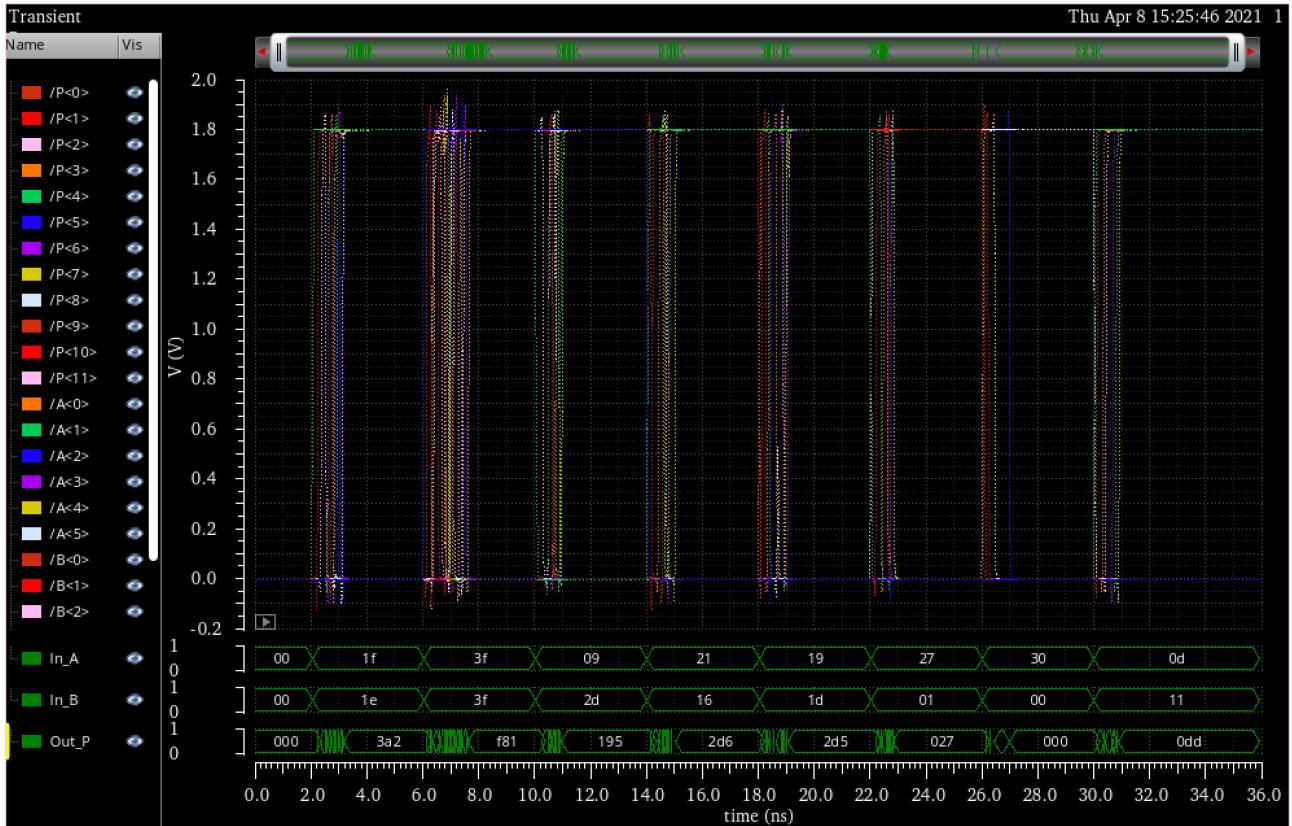
Multiplier Layout



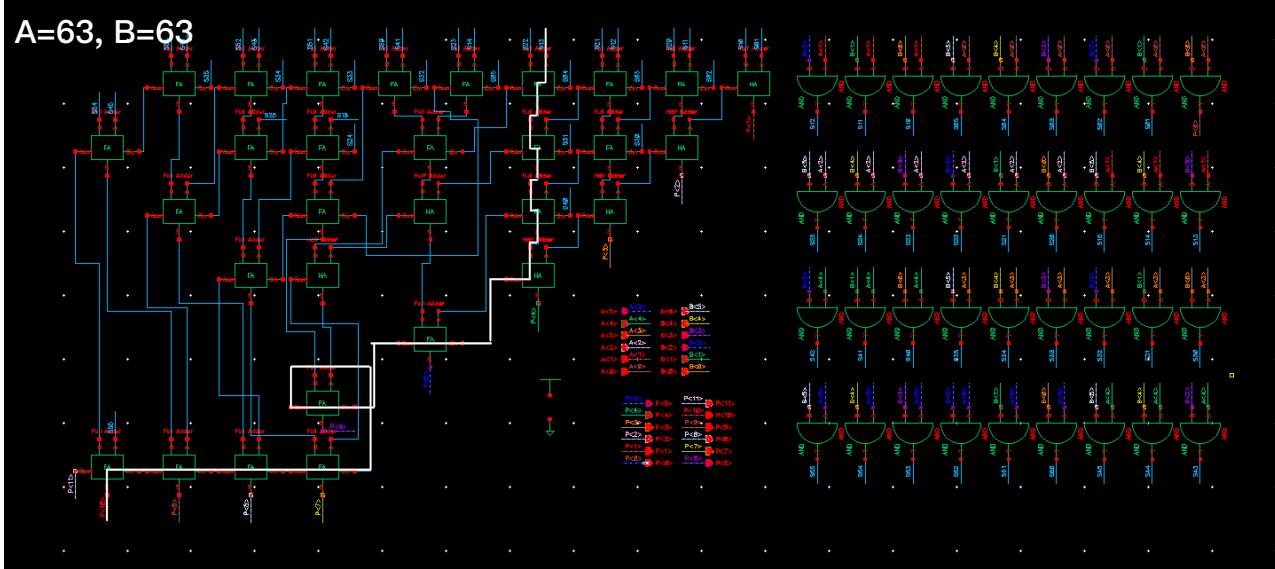
Schematic delay



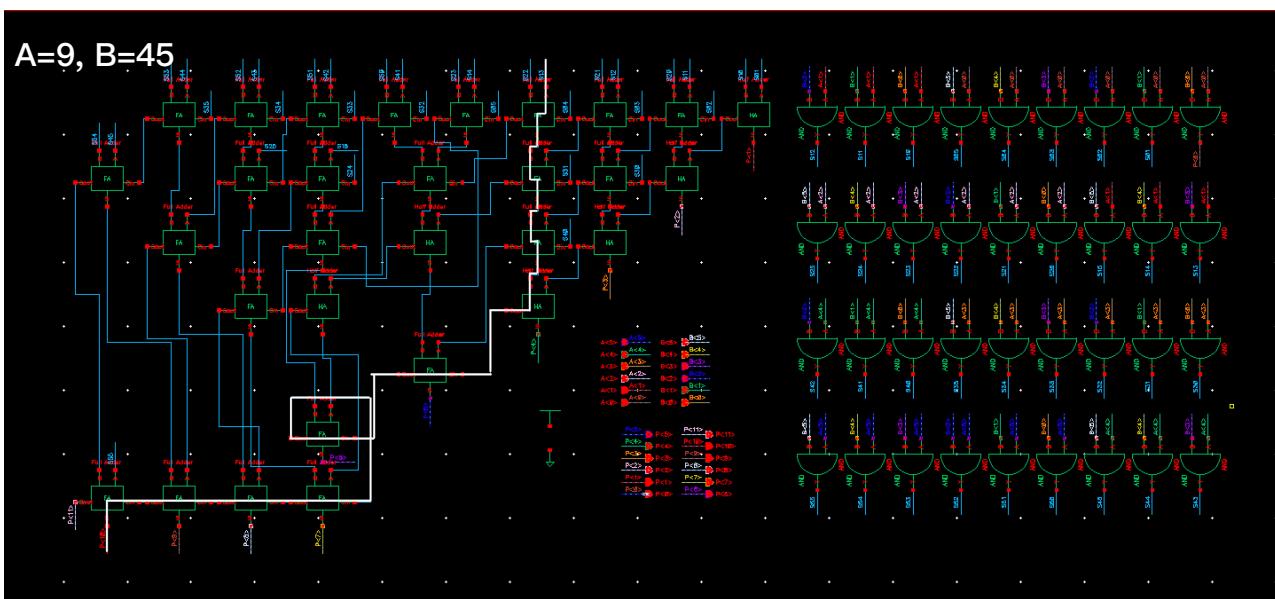
Extracted view delay



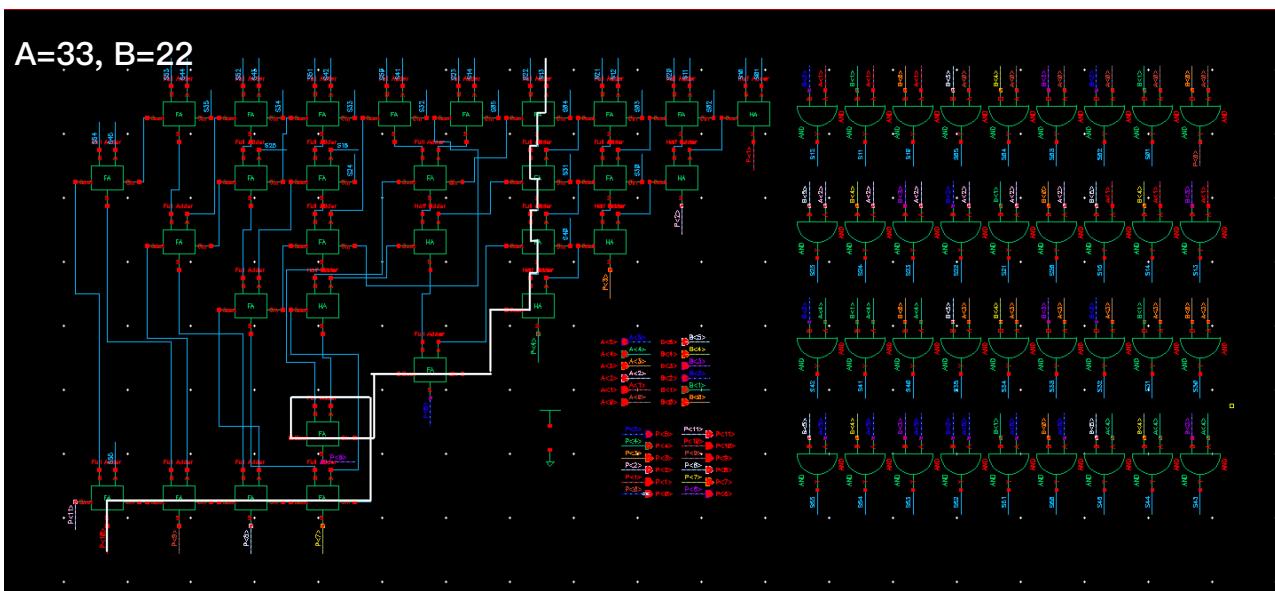
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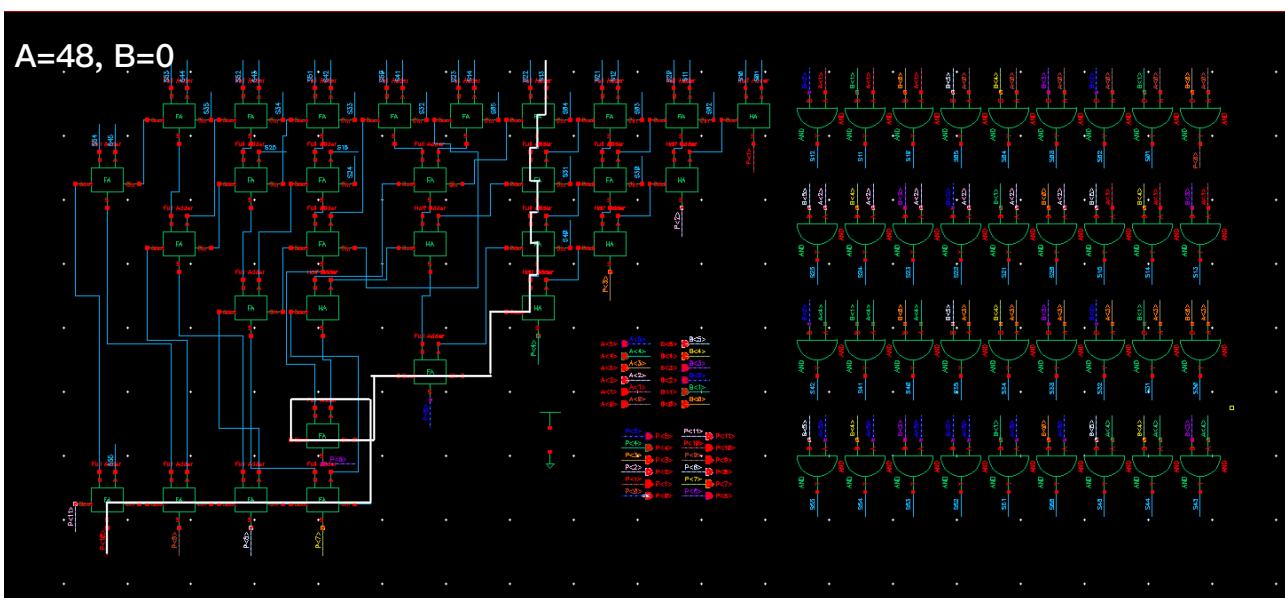
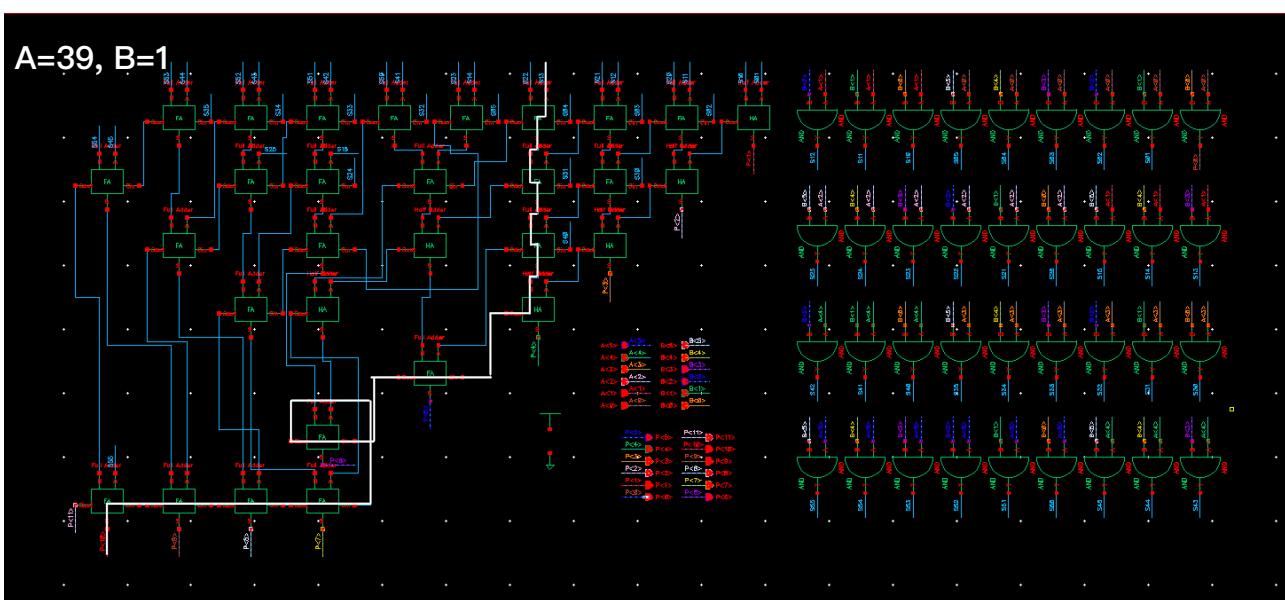
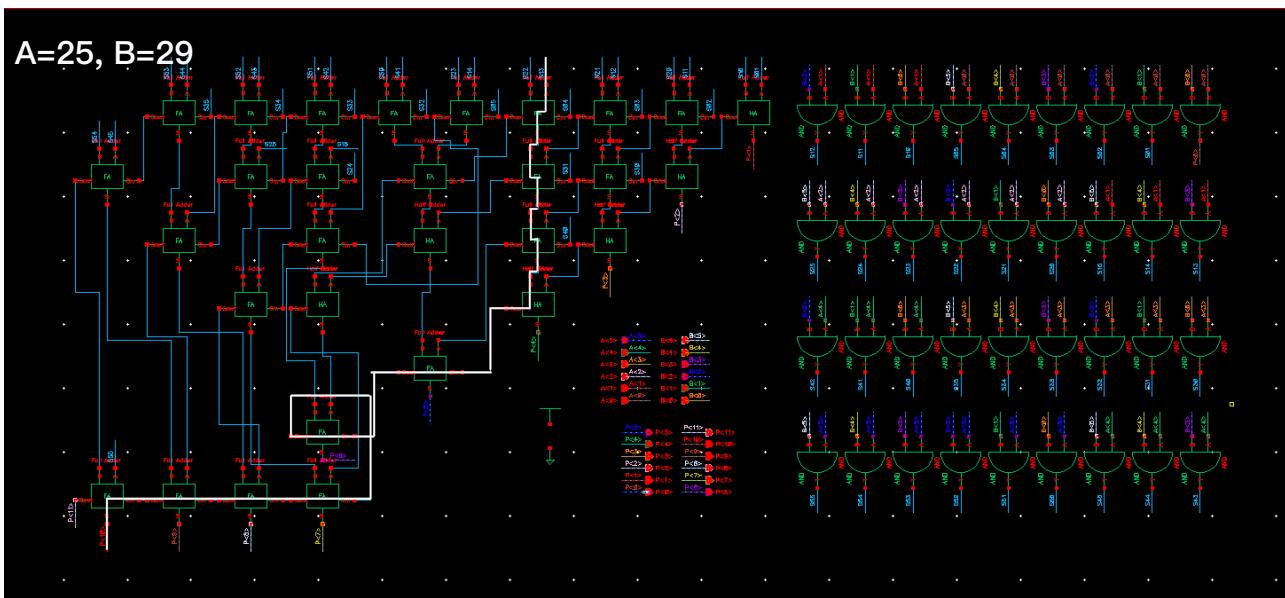


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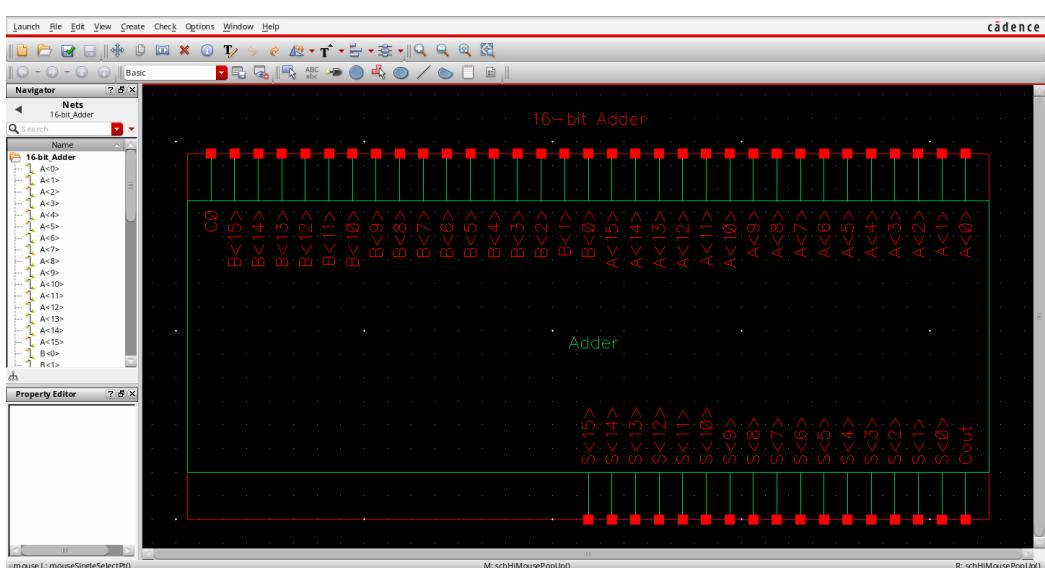
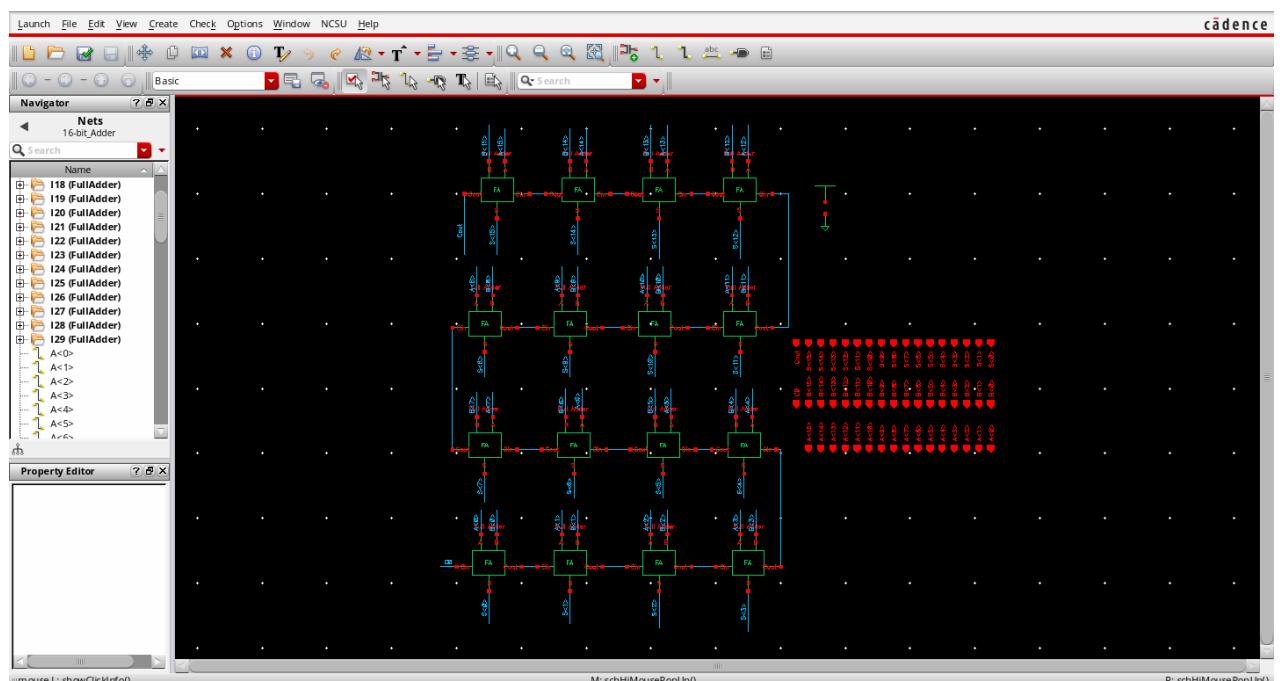
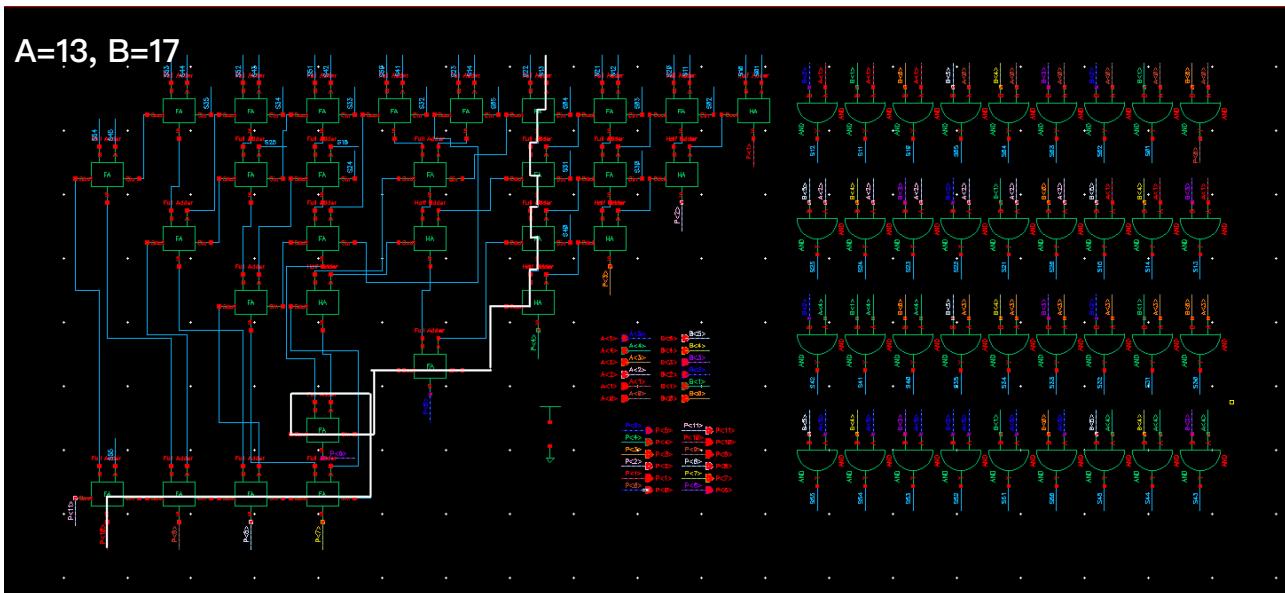


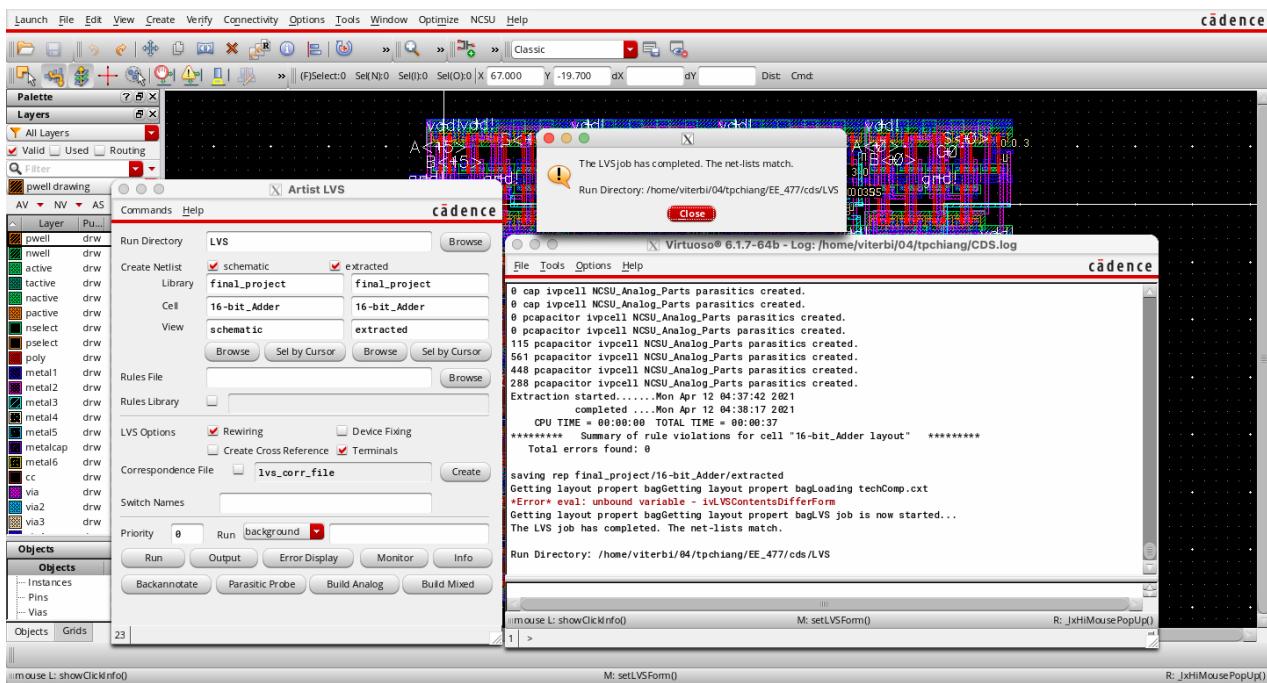
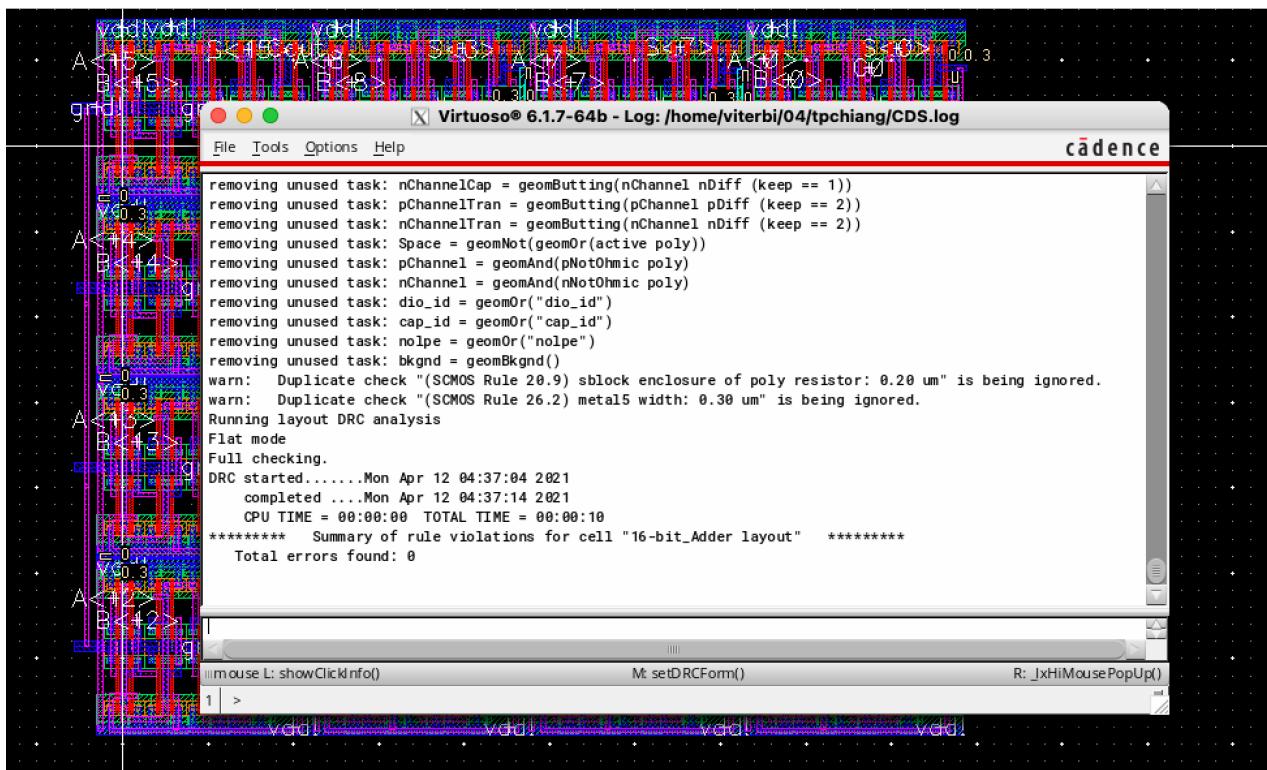
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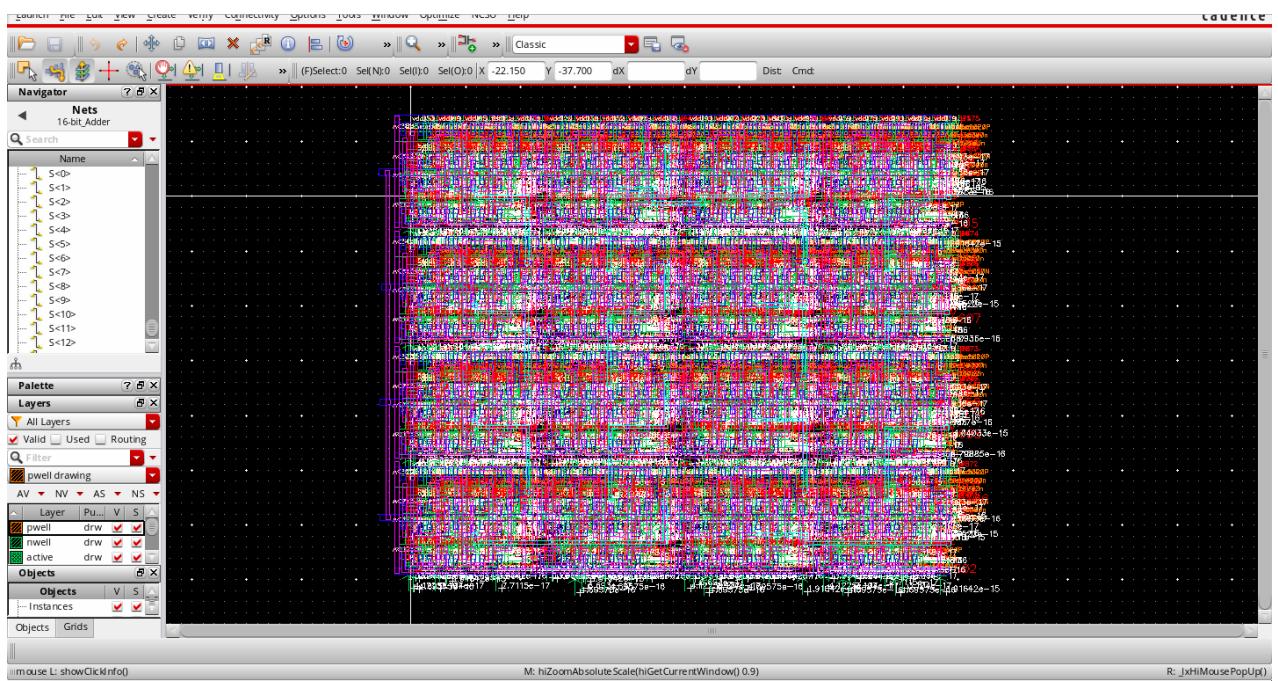
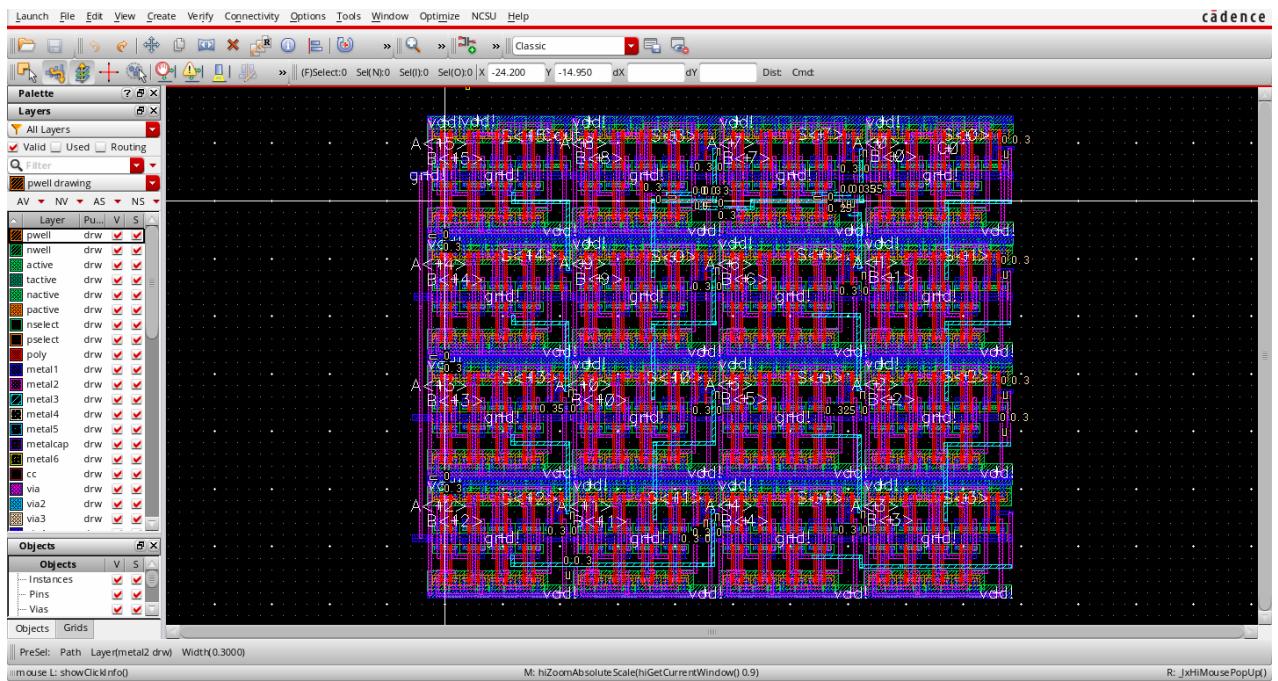




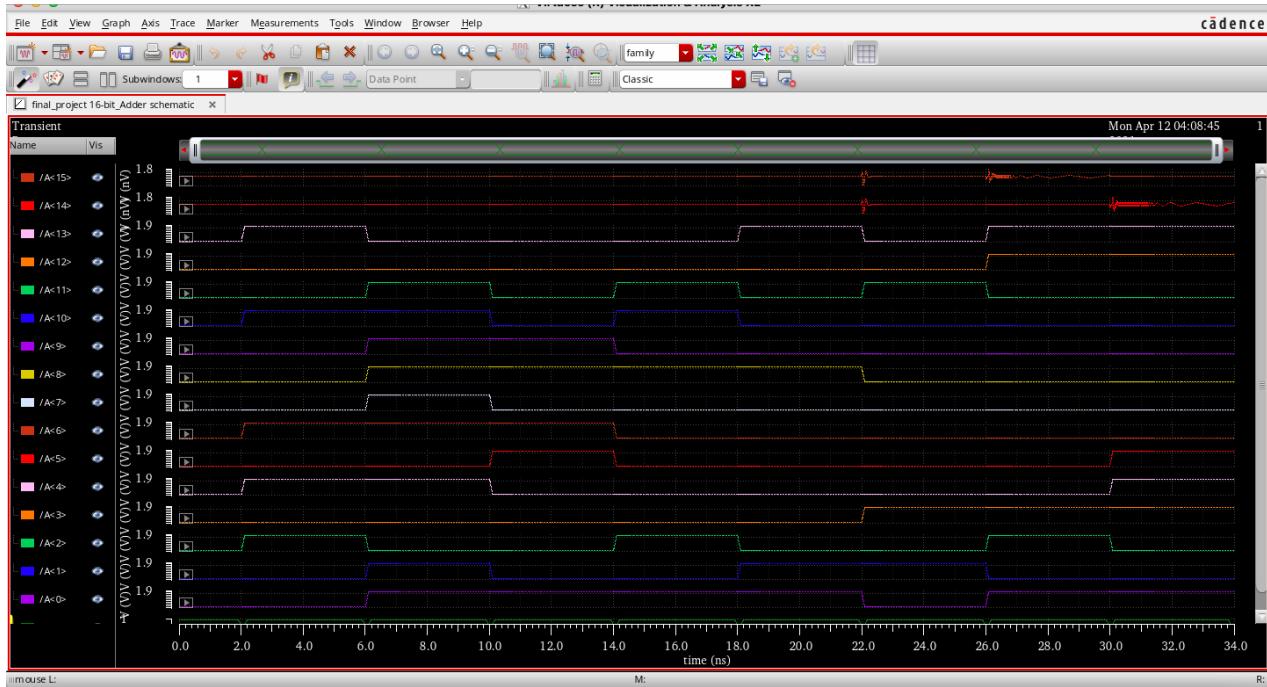
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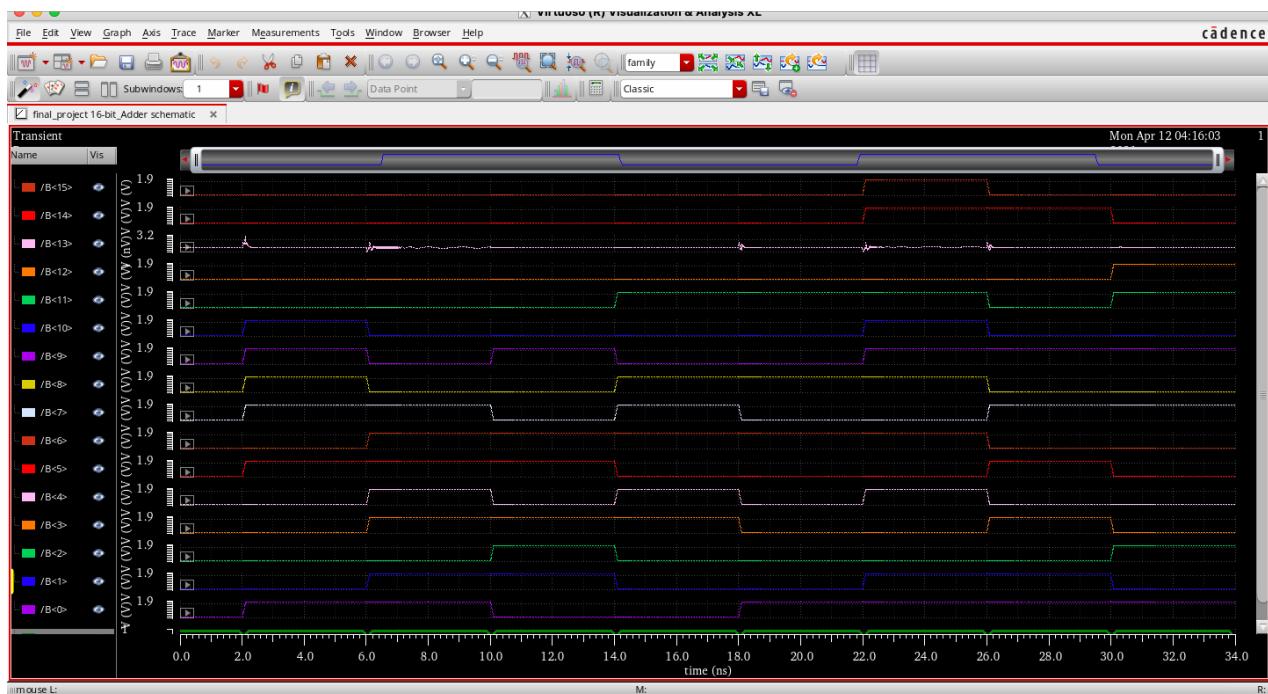


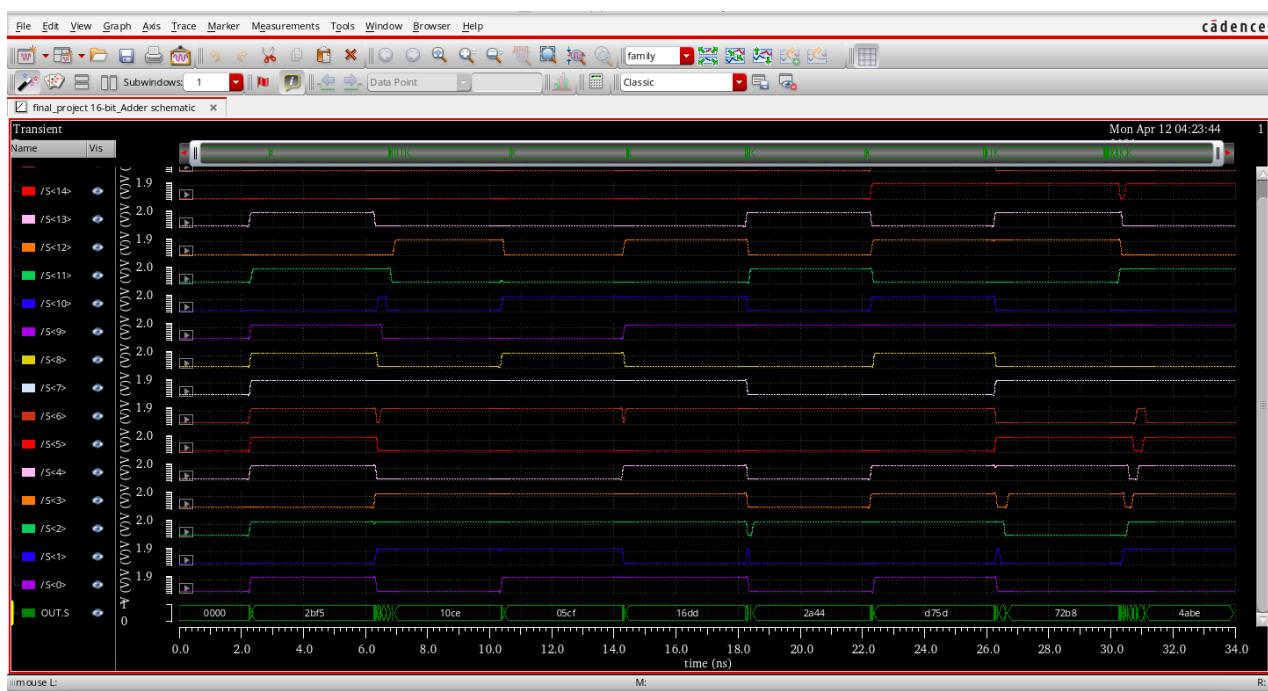
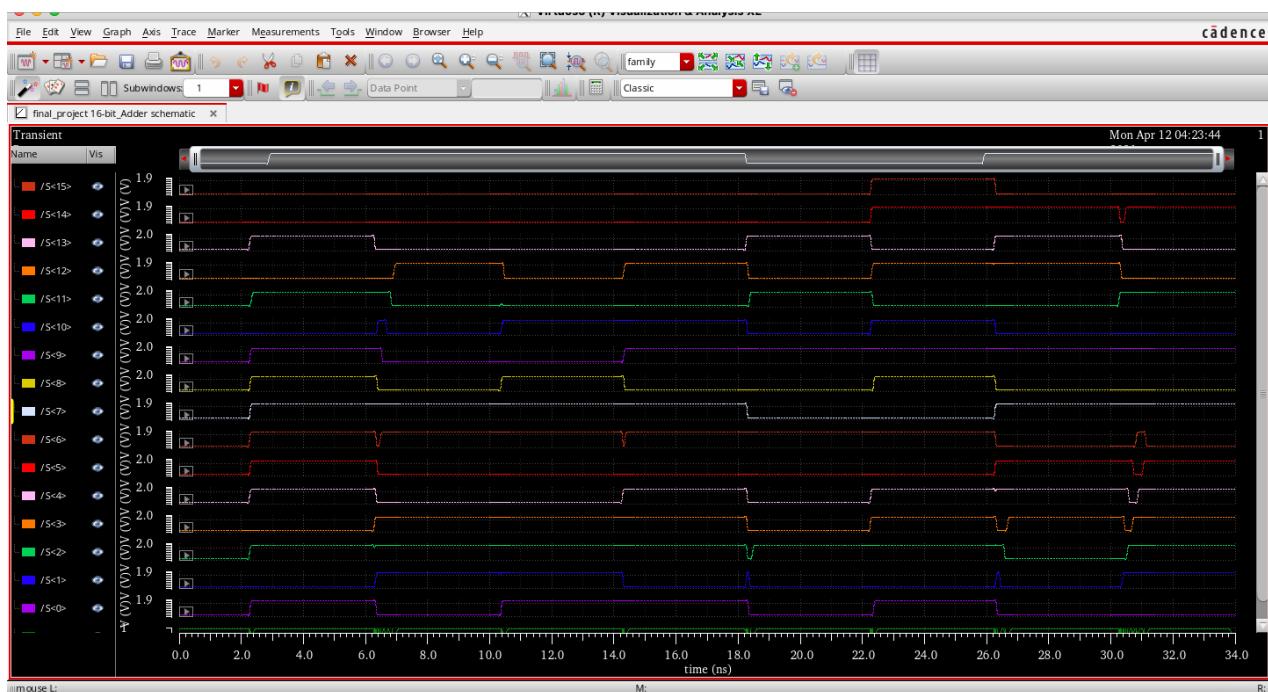


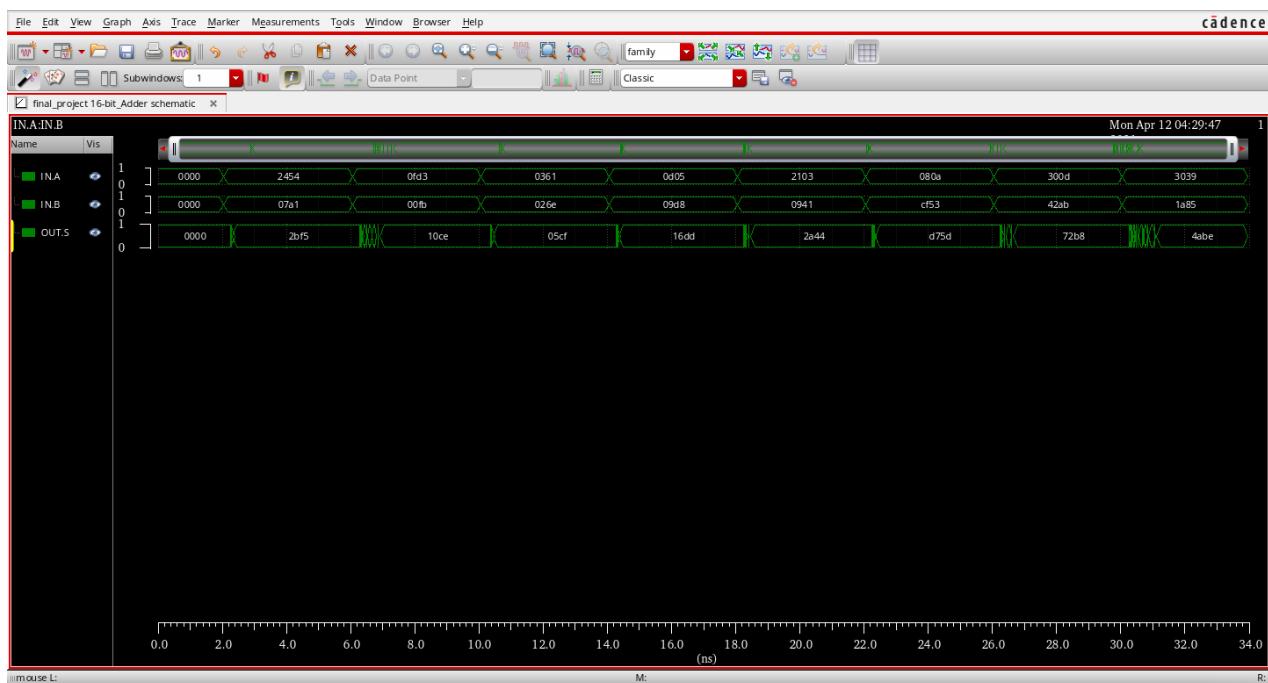


Schematic delay









Extract view delay

