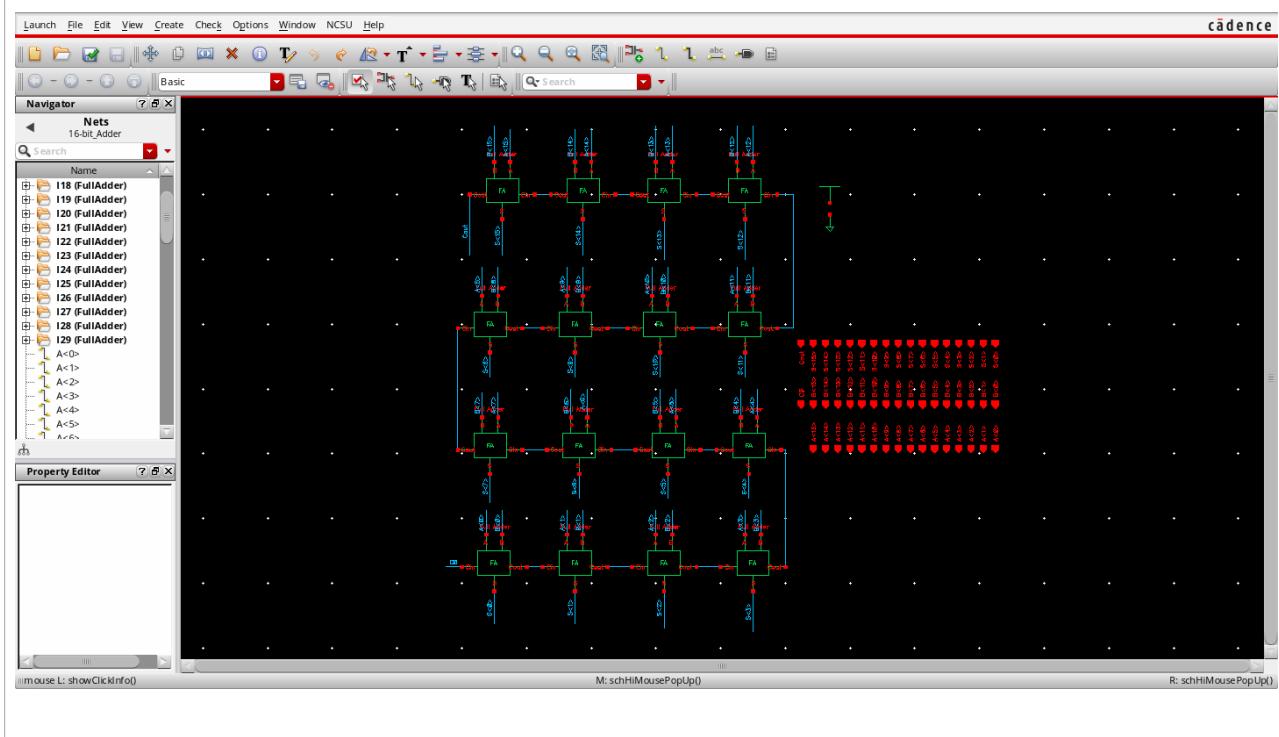
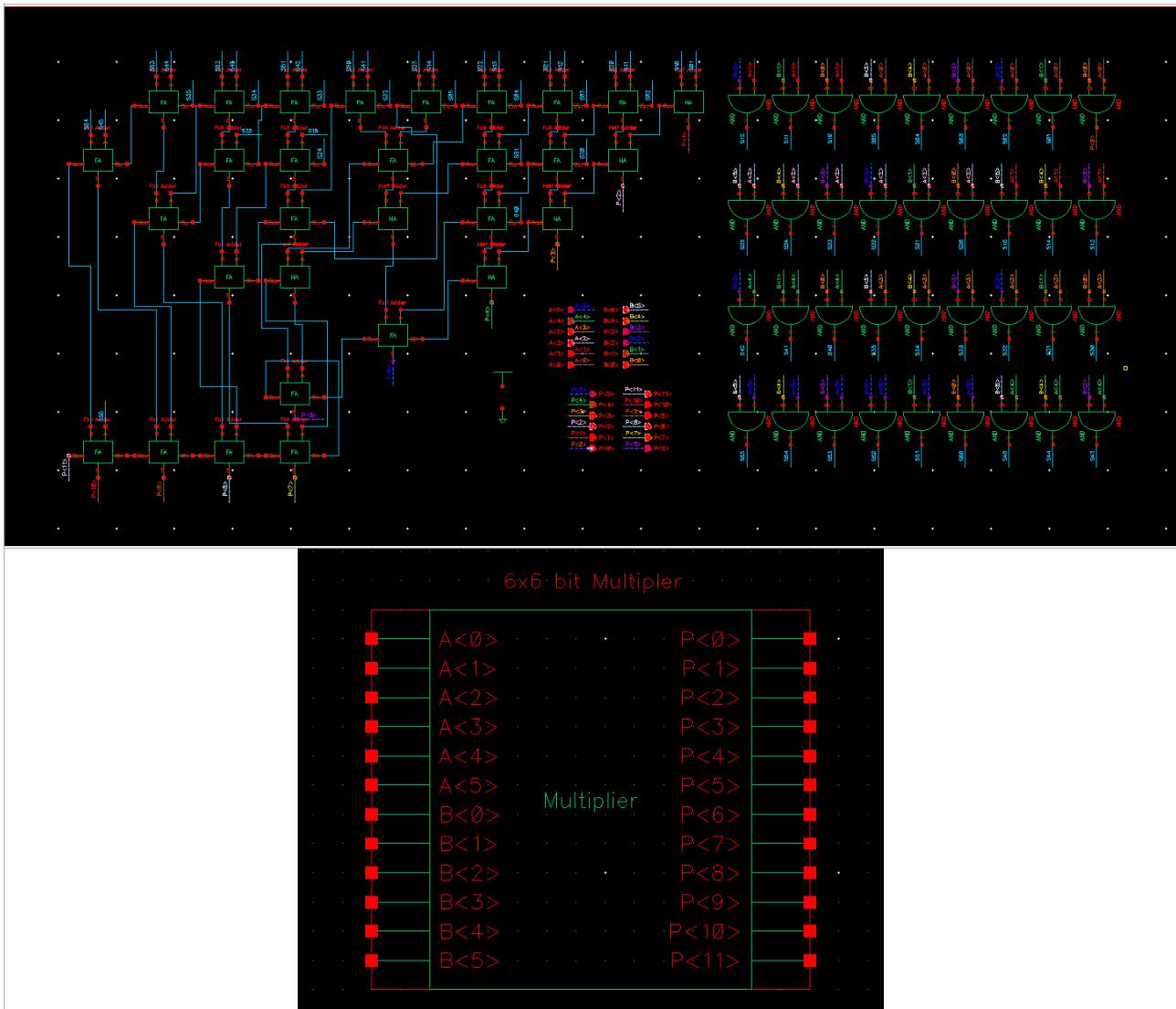
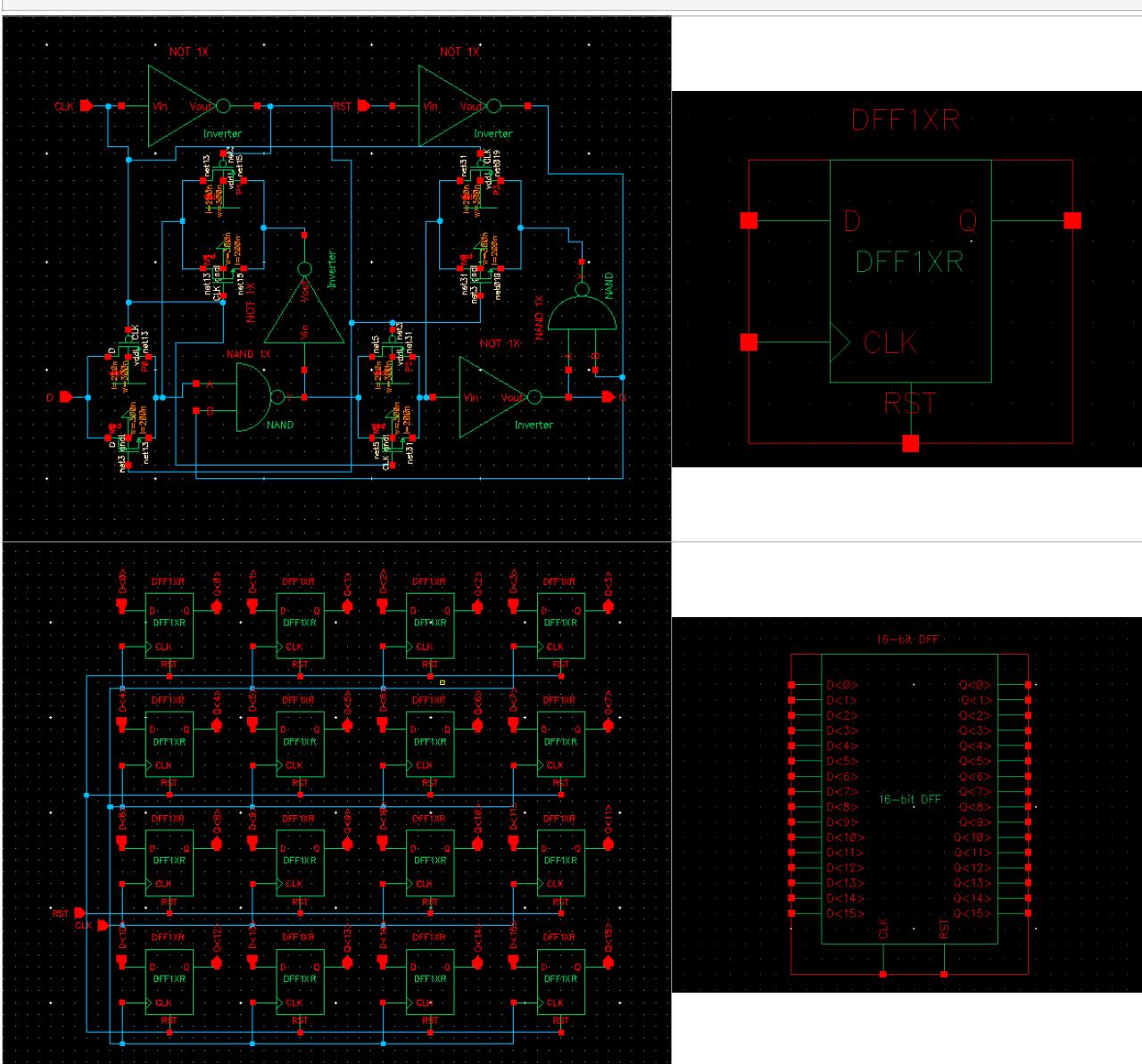
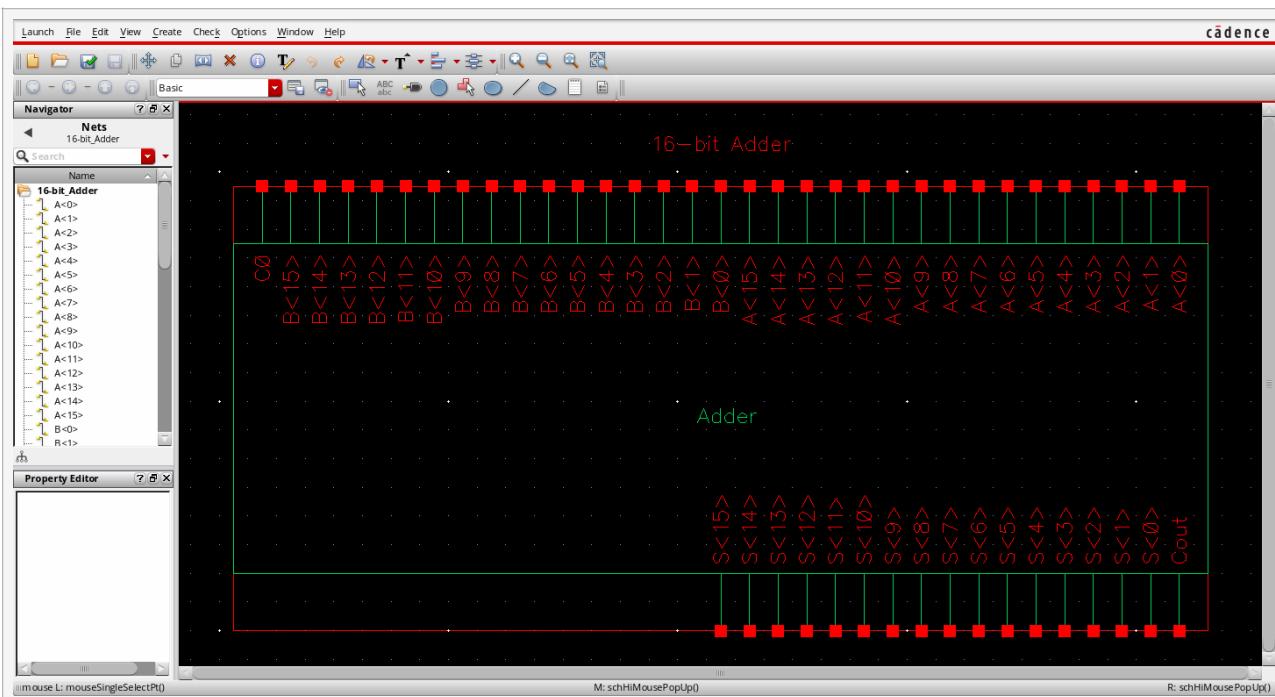
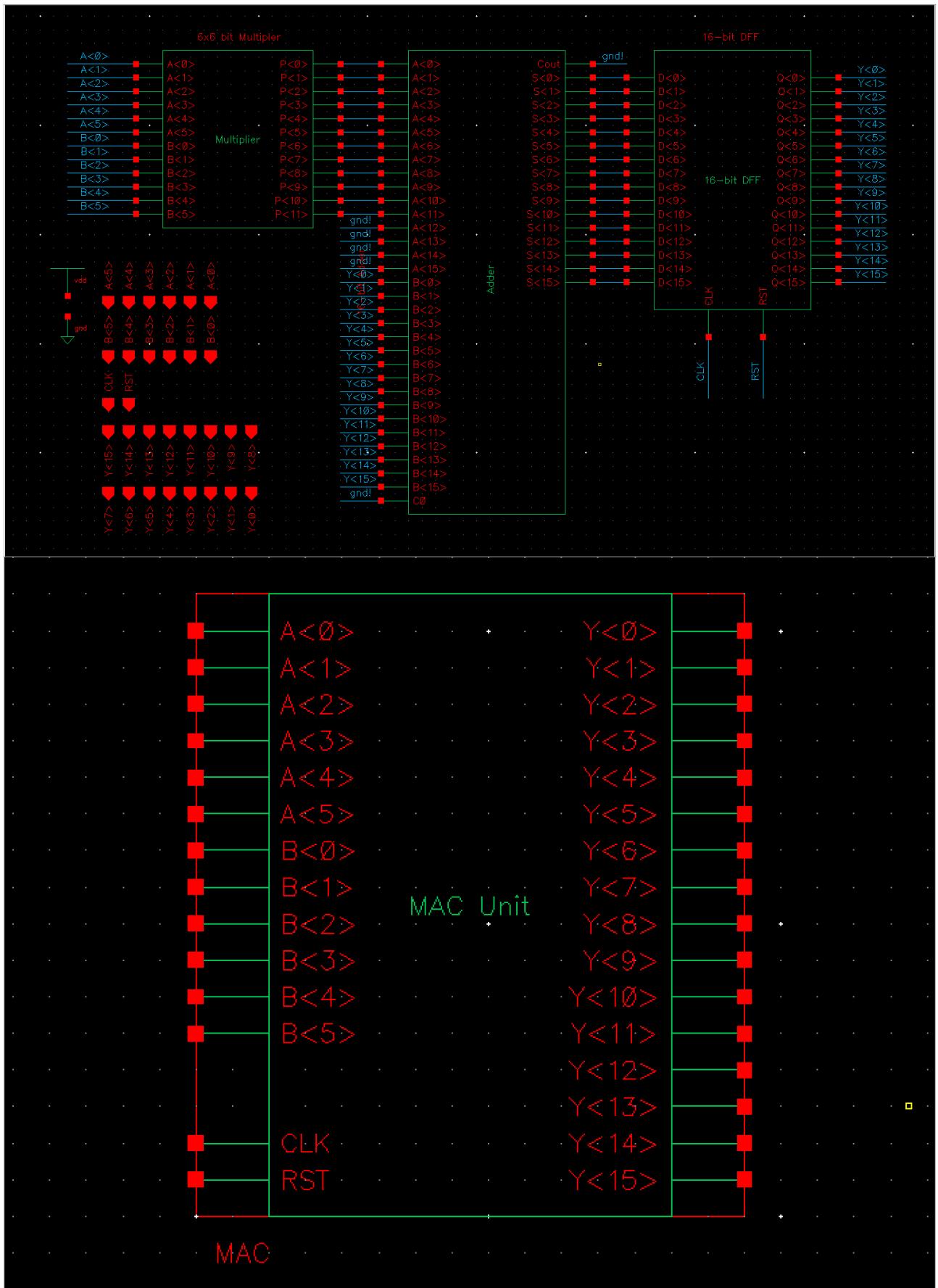
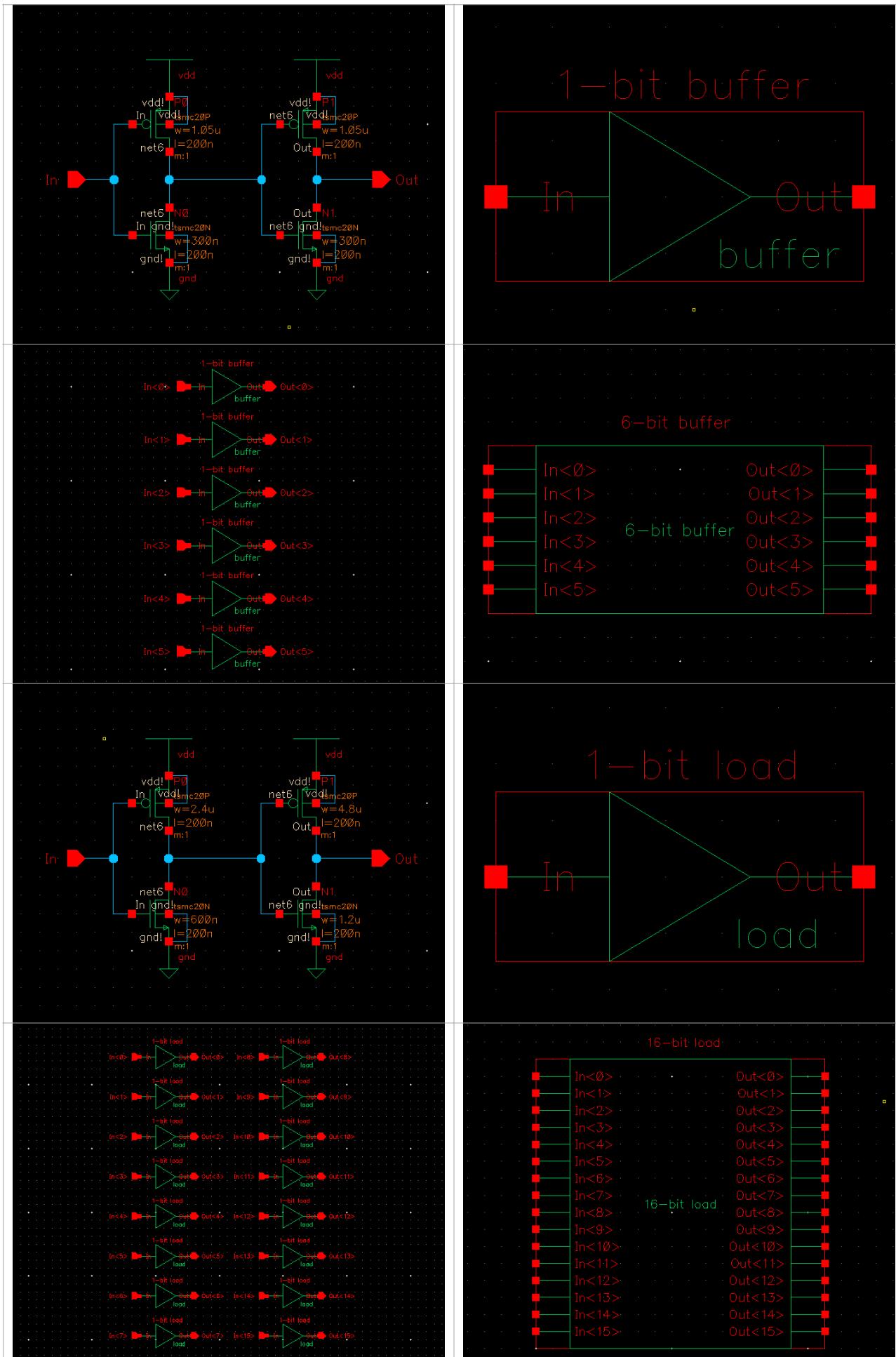


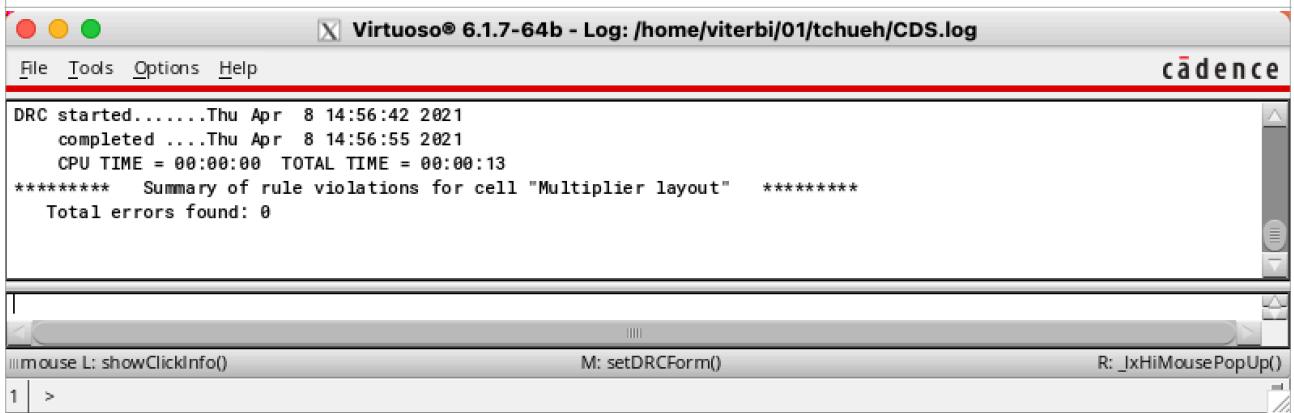
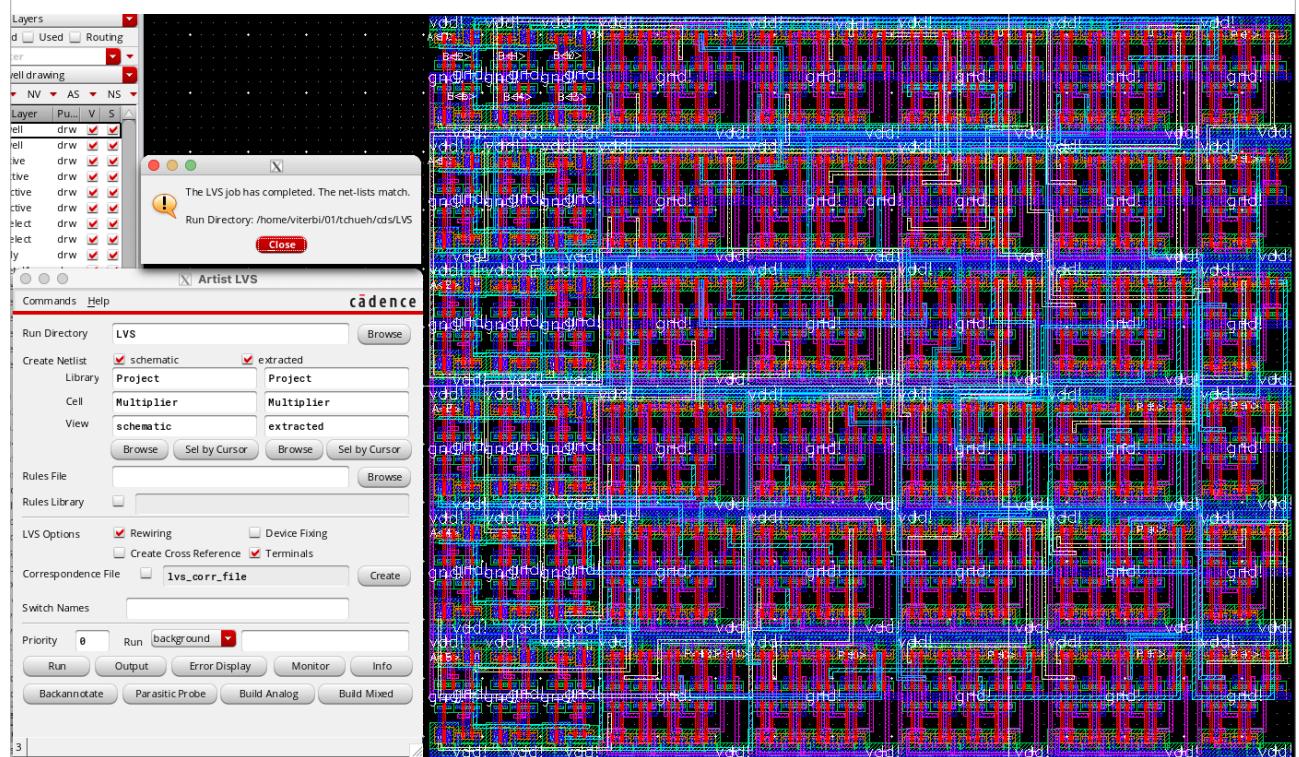
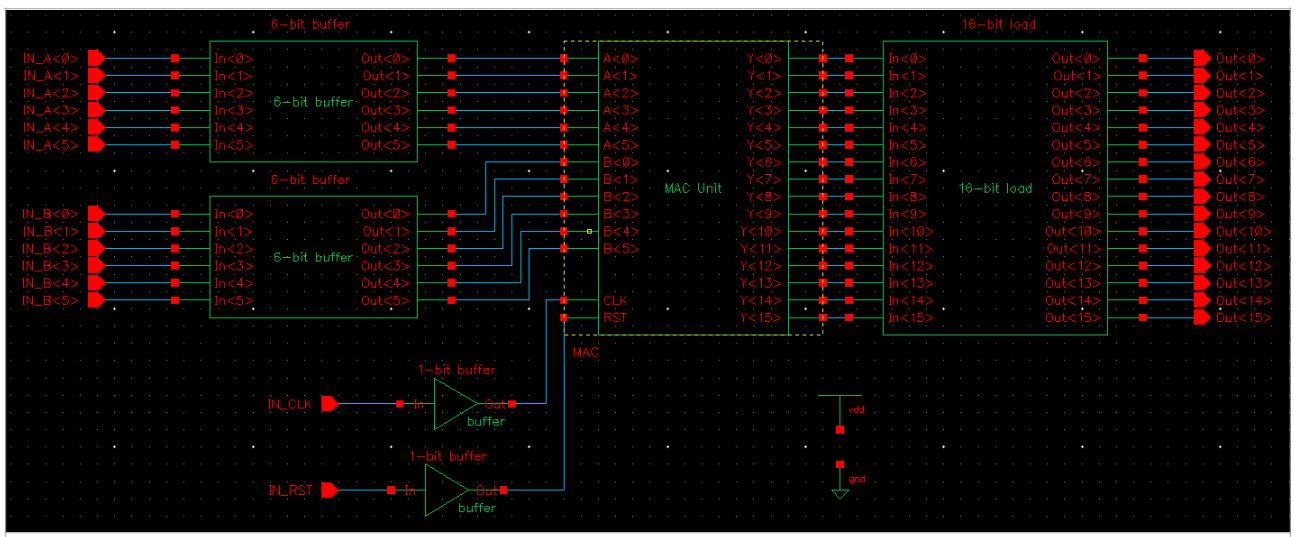
# Ti-Shen Chueh 3751474091



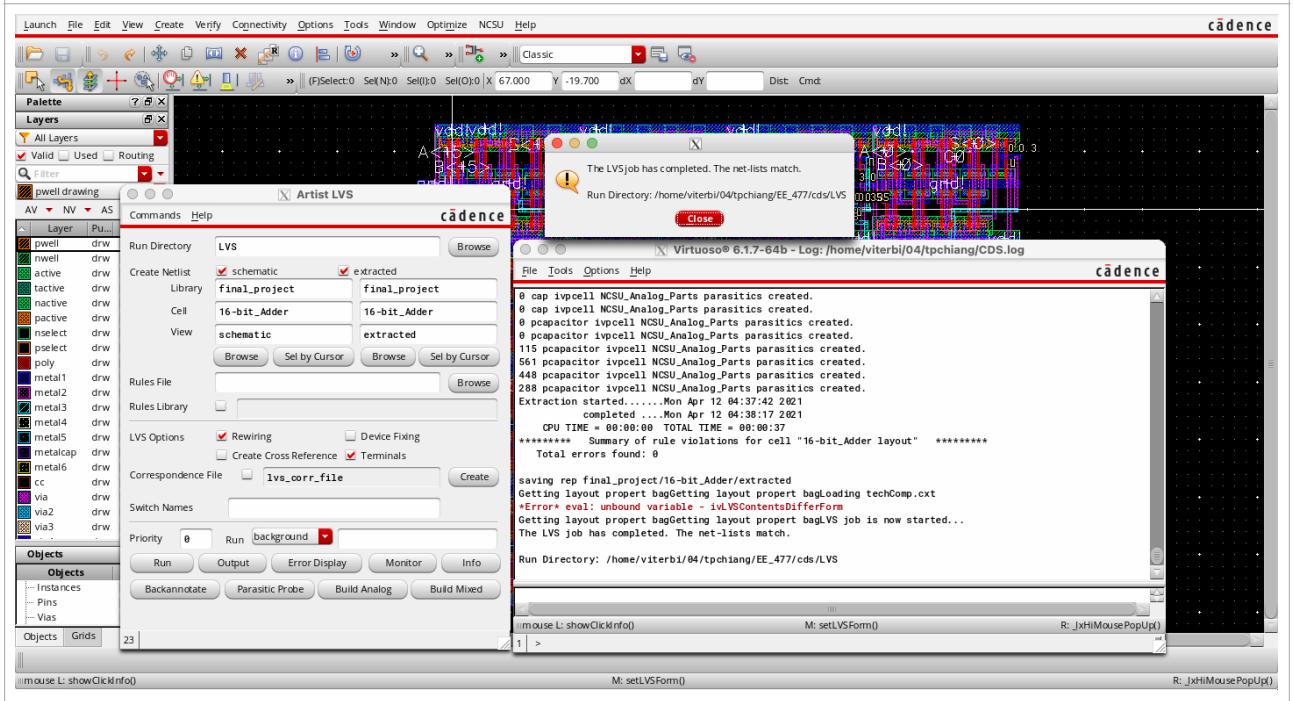
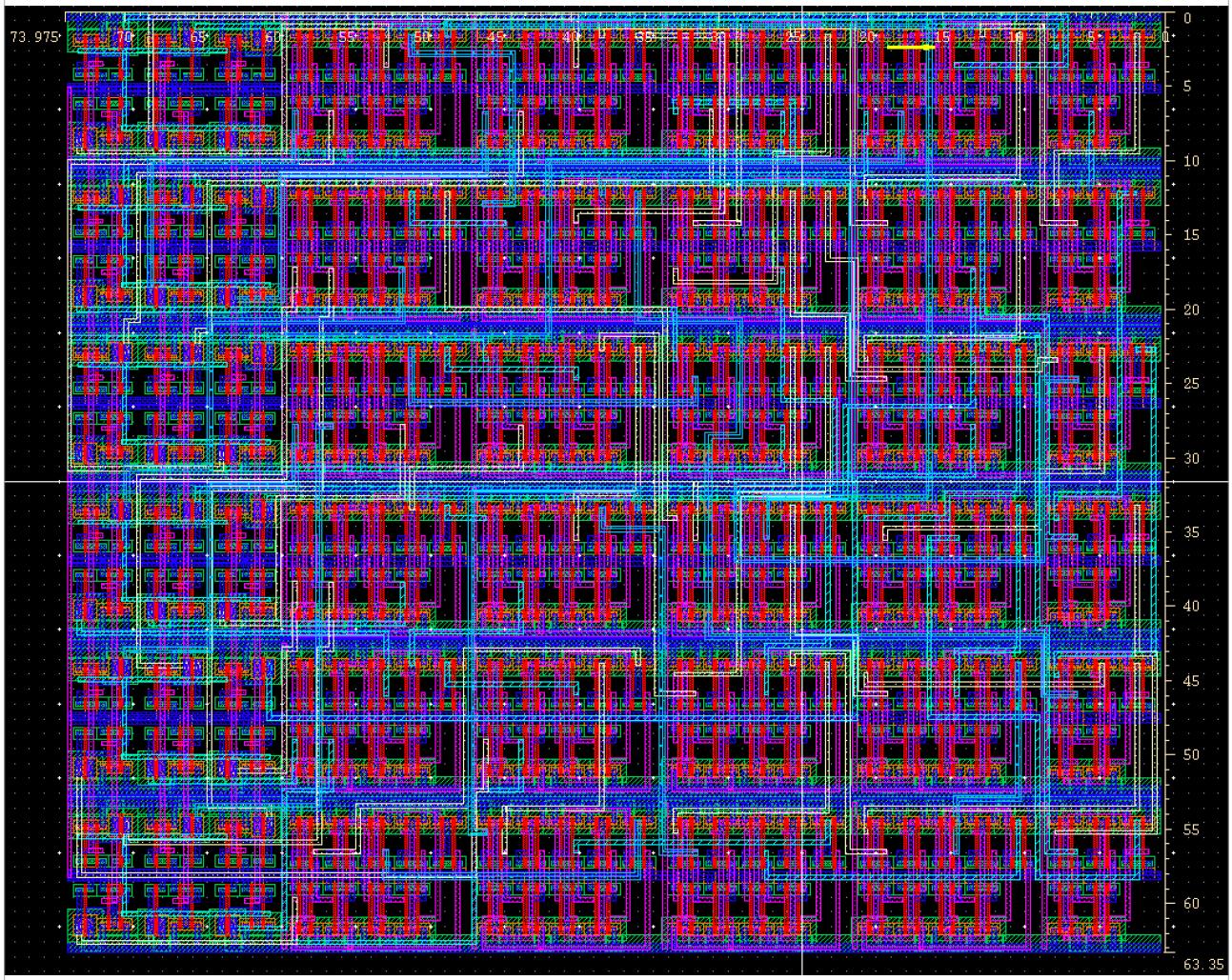


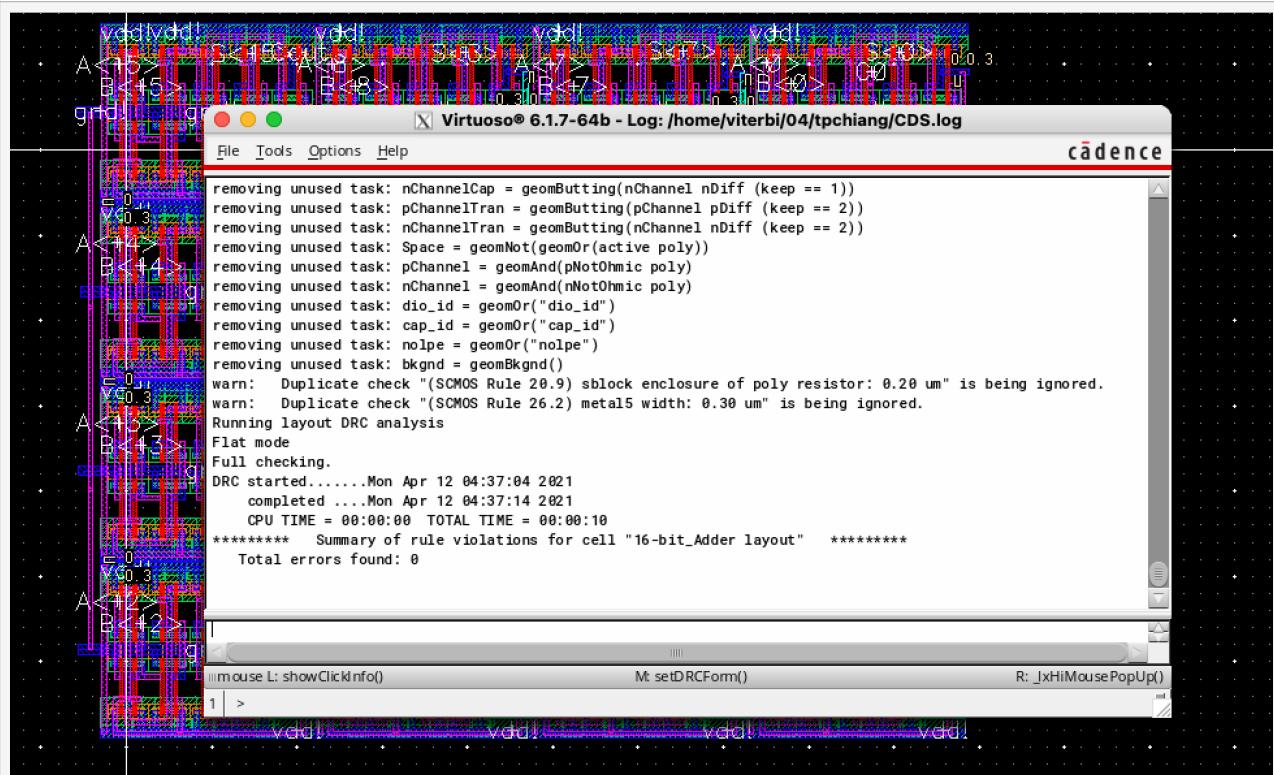




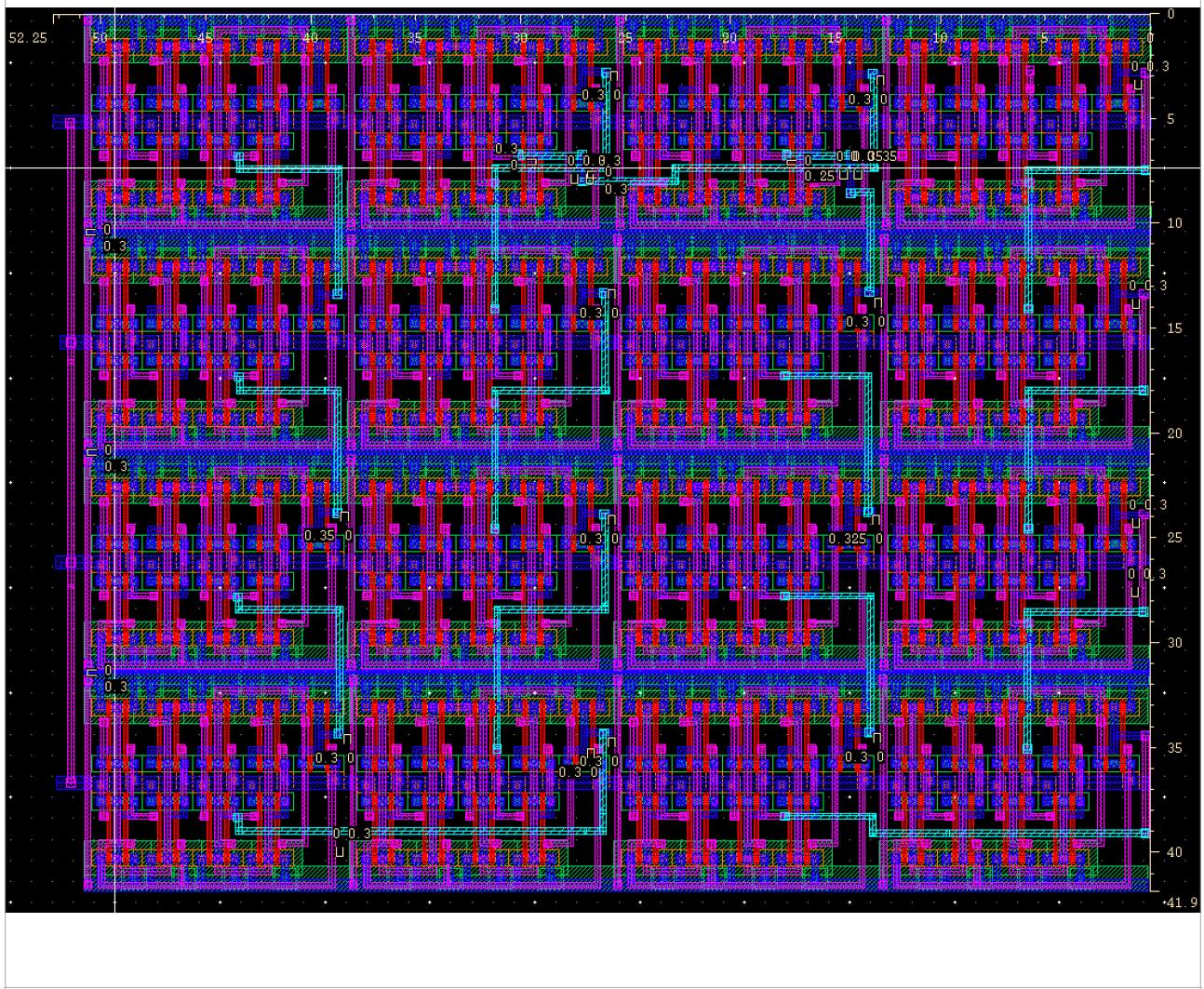


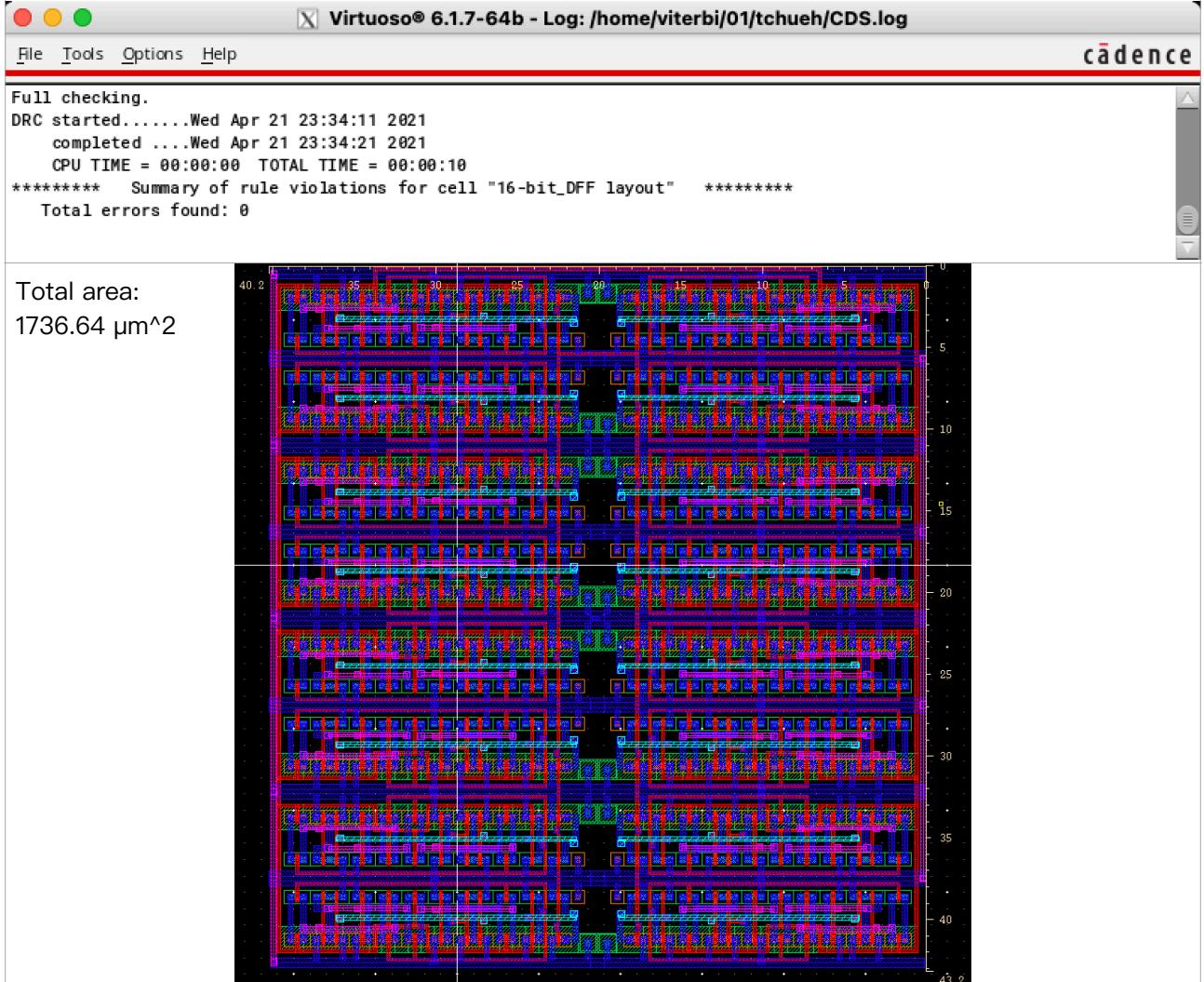
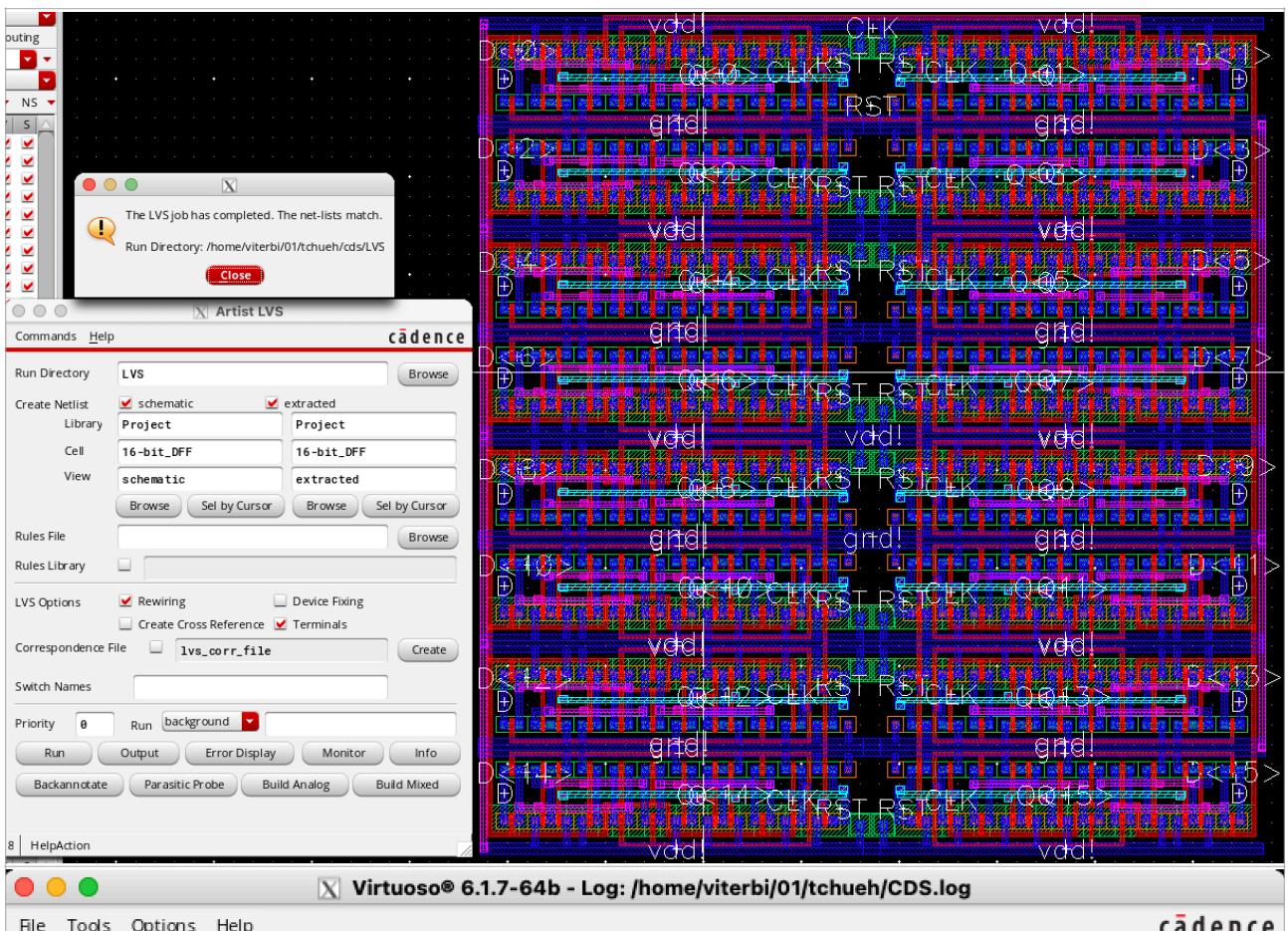
Total area: 4686.32  $\mu\text{m}^2$

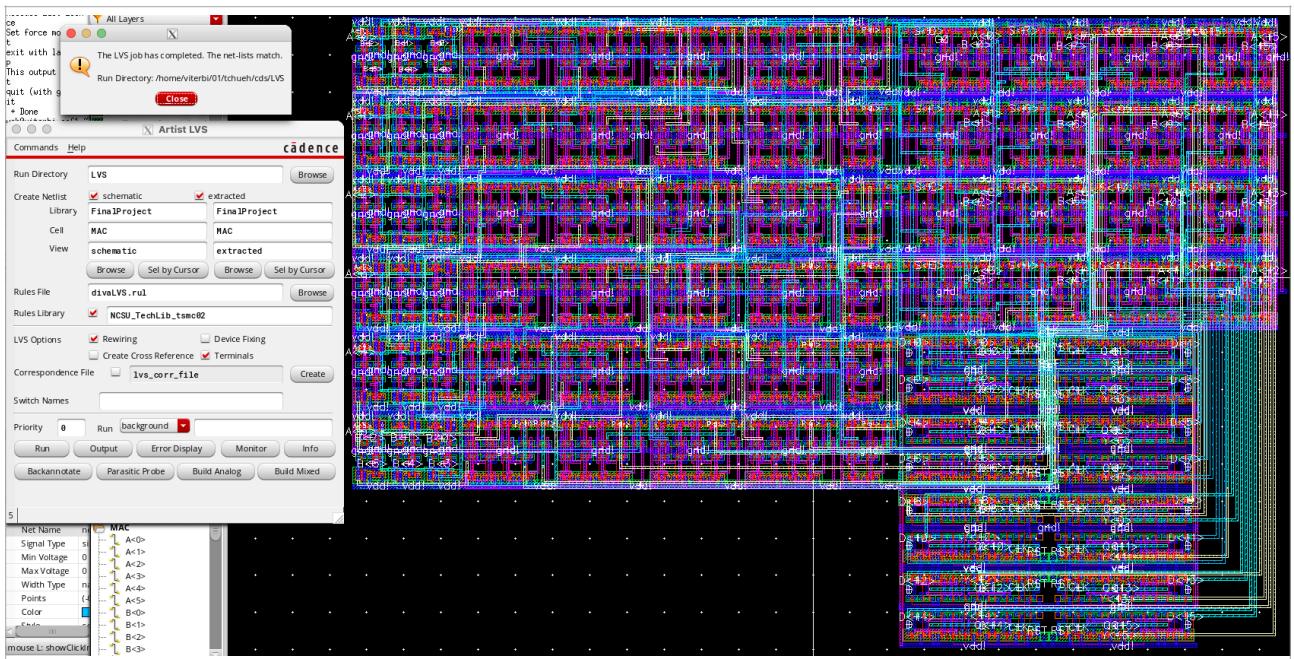




Total area: 2189.275  $\mu\text{m}^2$







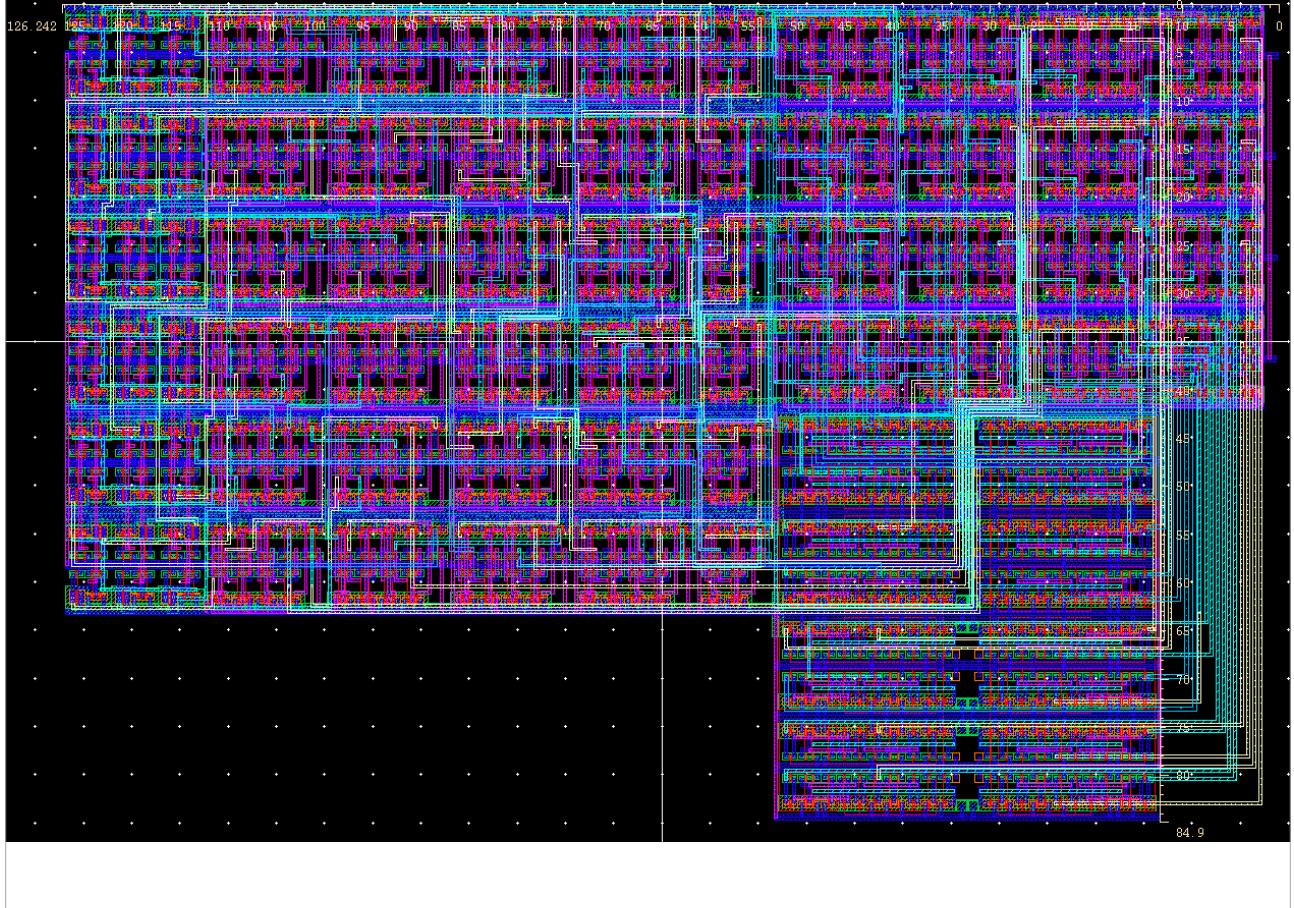
```

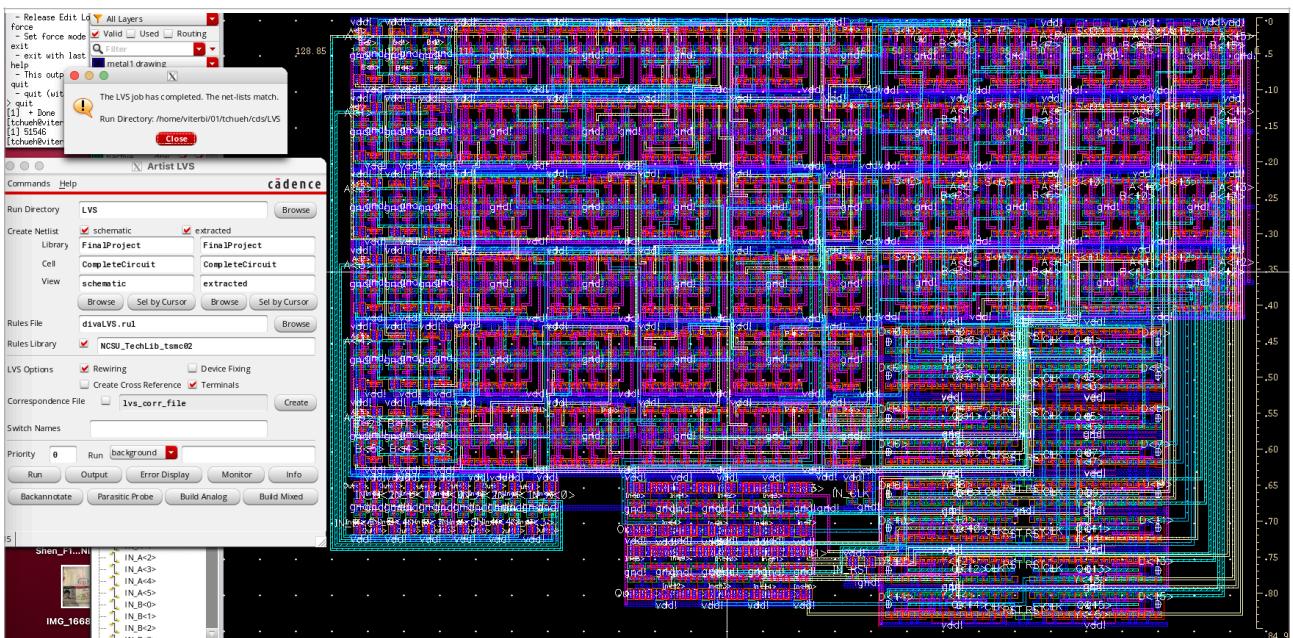
  X  Virtuoso® 6.1.7-64b - Log: /home/viterbi/01/tchueh/CDS.log
File Tools Options Help
cadence

Flat mode
Full checking.
DRC started.....Fri Apr 30 23:03:59 2021
completed ....Fri Apr 30 23:04:11 2021
CPU TIME = 00:00:00 TOTAL TIME = 00:00:12
***** Summary of rule violations for cell "MAC layout" *****
Total errors found: 0

```

Total area: 10717.946  $\mu\text{m}^2$





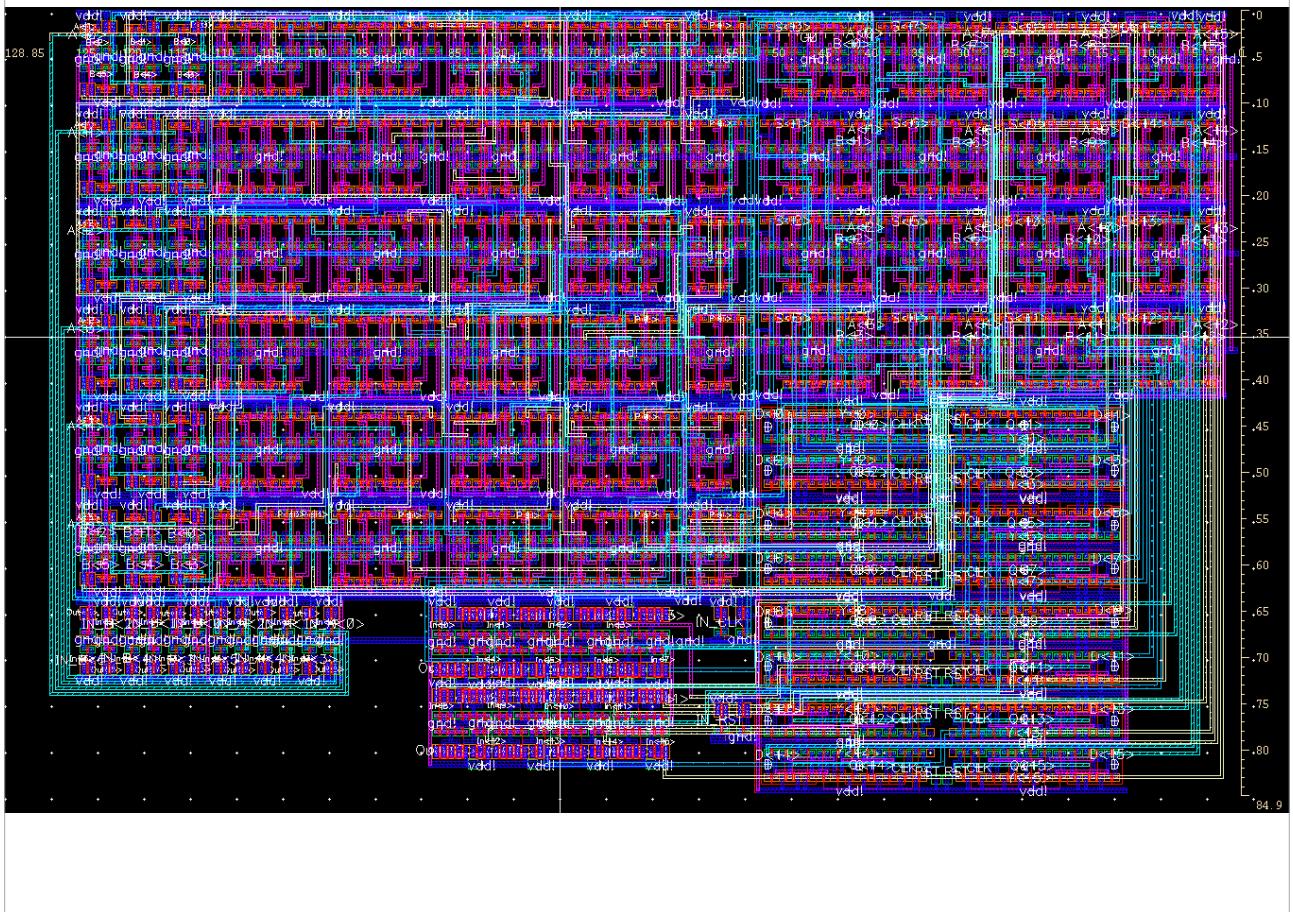
```

Virtuoso® 6.1.7-64b - Log: /home/viterbi/01/tchueh/CDS.log
File Tools Options Help
cadence

DRC started.....Sat May 1 02:33:03 2021
completed ....Sat May 1 02:33:15 2021
CPU TIME = 00:00:00 TOTAL TIME = 00:00:12
***** Summary of rule violations for cell "CompleteCircuit layout" *****
Total errors found: 0

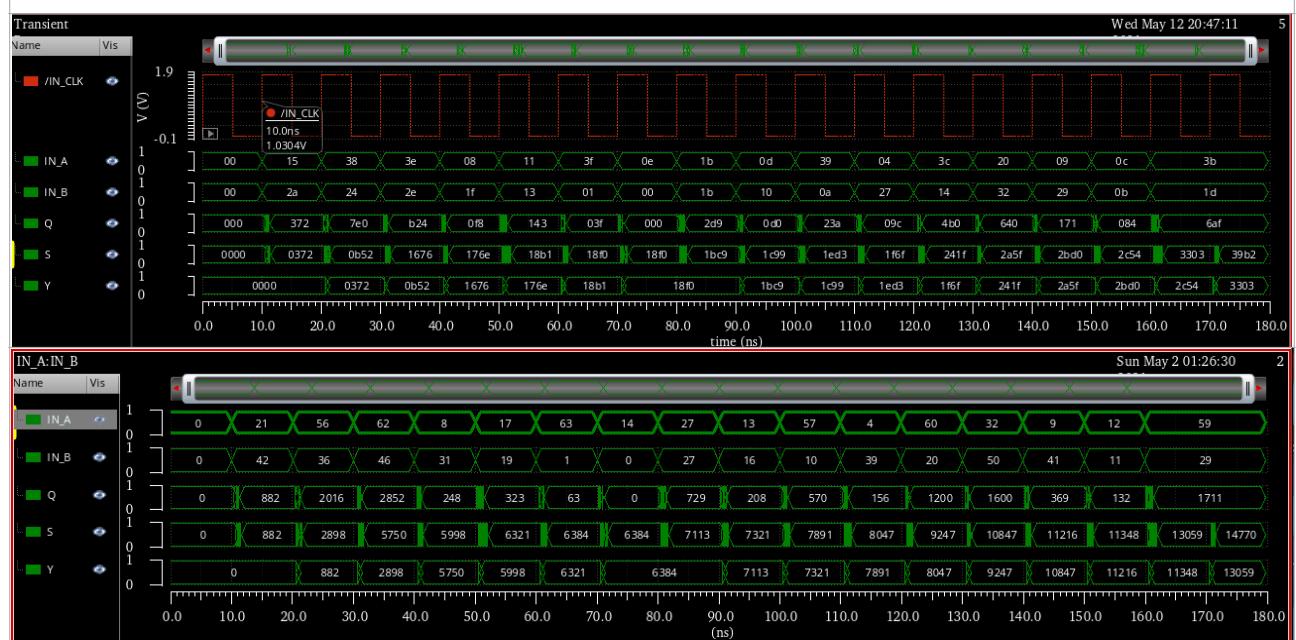
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Total area: 10939.365  $\mu\text{m}^2$



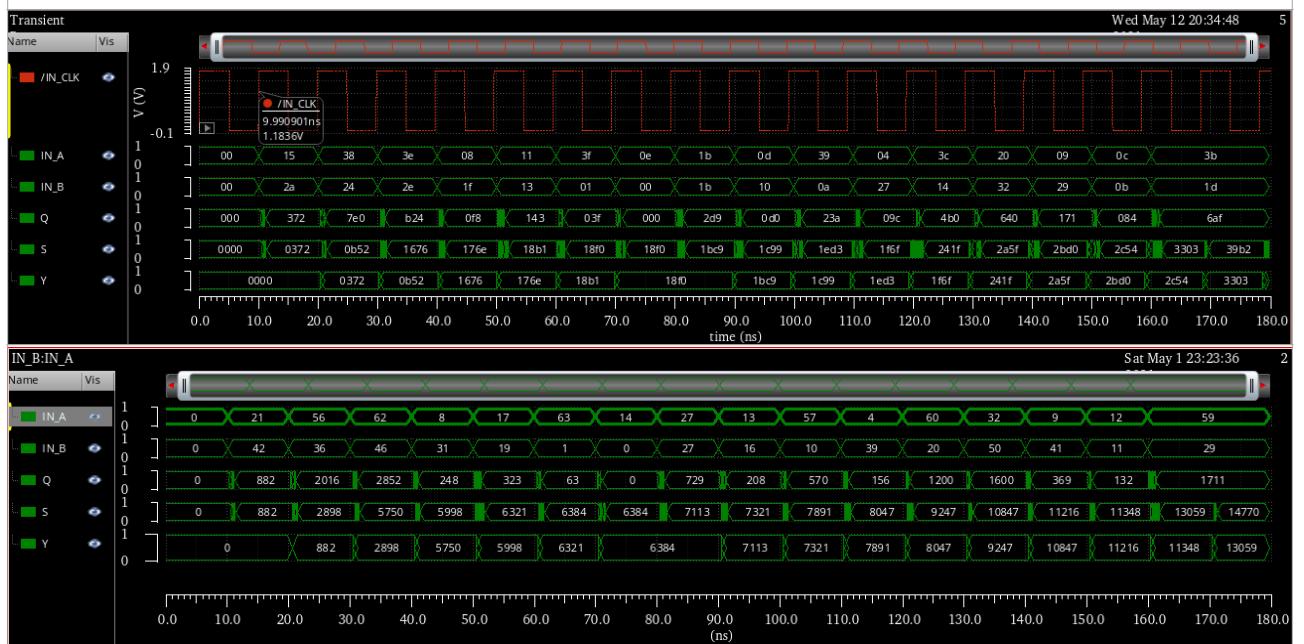
Part-B (a)

SL No.	RST	IN_A	IN_B	Q[11:0]	S[15:0]	Y[15:0]
Initial State>	0	0	0	0	0	0
1	1	21	42	882	882	0
2	1	56	36	2016	2898	882
3	1	62	46	2852	5750	2898
4	1	8	31	248	5998	5750
5	1	17	19	323	6321	5998
6	1	63	1	63	6384	6321
7	1	14	0	0	6384	6384
8	1	27	27	729	7113	6384
9	1	13	16	208	7321	7113
10	1	57	10	570	7891	7321
11	1	4	39	156	8047	7891
12	1	60	20	1200	9247	8047
13	1	32	50	1600	10847	9247
14	1	9	41	369	11216	10847
15	1	12	11	132	11348	11216
16	1	59	29	1711	13059	11348



Part-B (b)

SL No.	RST	IN_A	IN_B	Q[11:0]	S[15:0]	Y[15:0]
Initial State>	0	0	0	0	0	0
1	1	21	42	882	882	0
2	1	56	36	2016	2898	882
3	1	62	46	2852	5750	2898
4	1	8	31	248	5998	5750
5	1	17	19	323	6321	5998
6	1	63	1	63	6384	6321
7	1	14	0	0	6384	6384
8	1	27	27	729	7113	6384
9	1	13	16	208	7321	7113
10	1	57	10	570	7891	7321
11	1	4	39	156	8047	7891
12	1	60	20	1200	9247	8047
13	1	32	50	1600	10847	9247
14	1	9	41	369	11216	10847
15	1	12	11	132	11348	11216
16	1	59	29	1711	13059	11348



### Part-B (c)

SL.No. Initial State>	RST	IN_A	IN_B	Critical Path	Worst-case Delay [ns]
0	0	0	0	-----	-----
1	1	21	42	IN_A/IN_B->S->Q->S->Y	1.39861
2	1	56	36	IN_A/IN_B->S->Q->S->Y	1.29393
3	1	62	46	IN_A/IN_B->S->Q->S->Y	1.53472
4	1	8	31	IN_A/IN_B->S->Q->S->Y	1.25660
5	1	17	19	IN_A/IN_B->S->Q->S->Y	1.86979
6	1	63	1	IN_A/IN_B->S->Q->S->Y	1.57725
7	1	14	0	IN_A/IN_B->S->Q->S->Y	1.53610
8	1	27	27	IN_A/IN_B->S->Q->S->Y	1.53563
9	1	13	16	IN_A/IN_B->S->Q->S->Y	1.44024
10	1	57	10	IN_A/IN_B->S->Q->S->Y	1.35920
11	1	4	39	IN_A/IN_B->S->Q->S->Y	1.55750
12	1	60	20	IN_A/IN_B->S->Q->S->Y	1.77940
13	1	32	50	IN_A/IN_B->S->Q->S->Y	1.18230
14	1	9	41	IN_A/IN_B->S->Q->S->Y	1.24320
15	1	12	11	IN_A/IN_B->S->Q->S->Y	1.34500
16	1	59	29	IN_A/IN_B->S->Q->S->Y	1.91020













Part-B (d)

Performance Matrices	Value	Unit
Final Area (A-b-v)	$128.85 \times 84.9 = 10939.365$	( $\mu\text{m} \times \mu\text{m}$ )
No of Metal Layer used in Layout	Metal 1, Metal 2, Metal 3, Metal 4, and Metal 5	
Maximum Worst-case Delay (IN_A/IN_B to S)	1.91020	ns
Maximum achievable Clock Frequency	$1/9.9\text{ns} = 101.01$	MHz
Final Area $\times$ Delay (clock period)	$10939.365 \times 1.91020 = 20896.37502$	$\mu\text{m}^2 \text{ns}$