EE 477- Spring 2021 VLSI CIRCUIT DESIGN

Lab4-2 Report
12-bit Multiply-Accumulator (MAC) Unit Design

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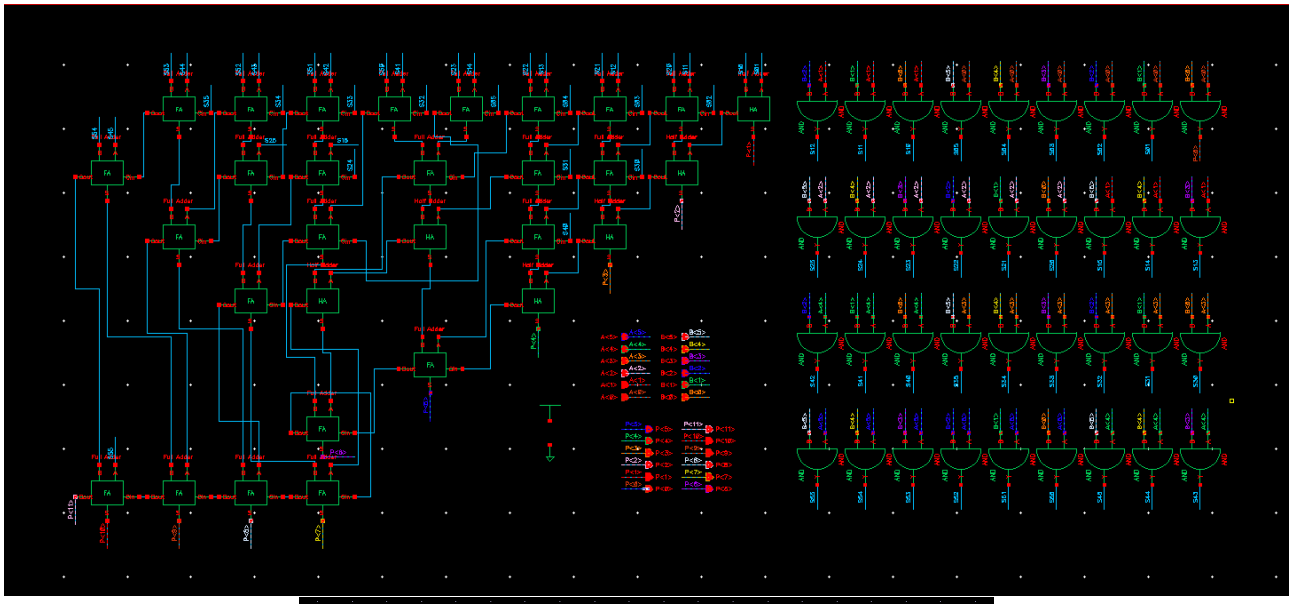
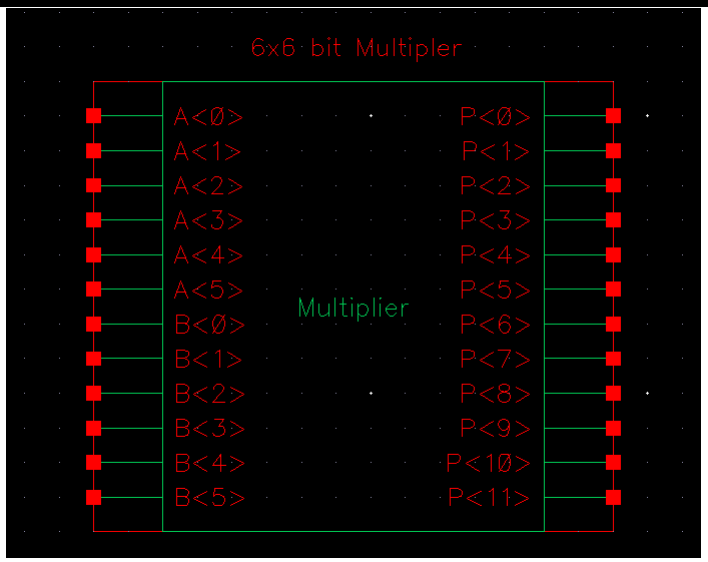
3751474091




6x6 bit Multipler
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A<2>
A<3>
A<4>
A<5>
B<0>
B<1>
B<2>
B<3>
B<4>
B<5>
Multiplier
P<0>
P<1>
P<2>
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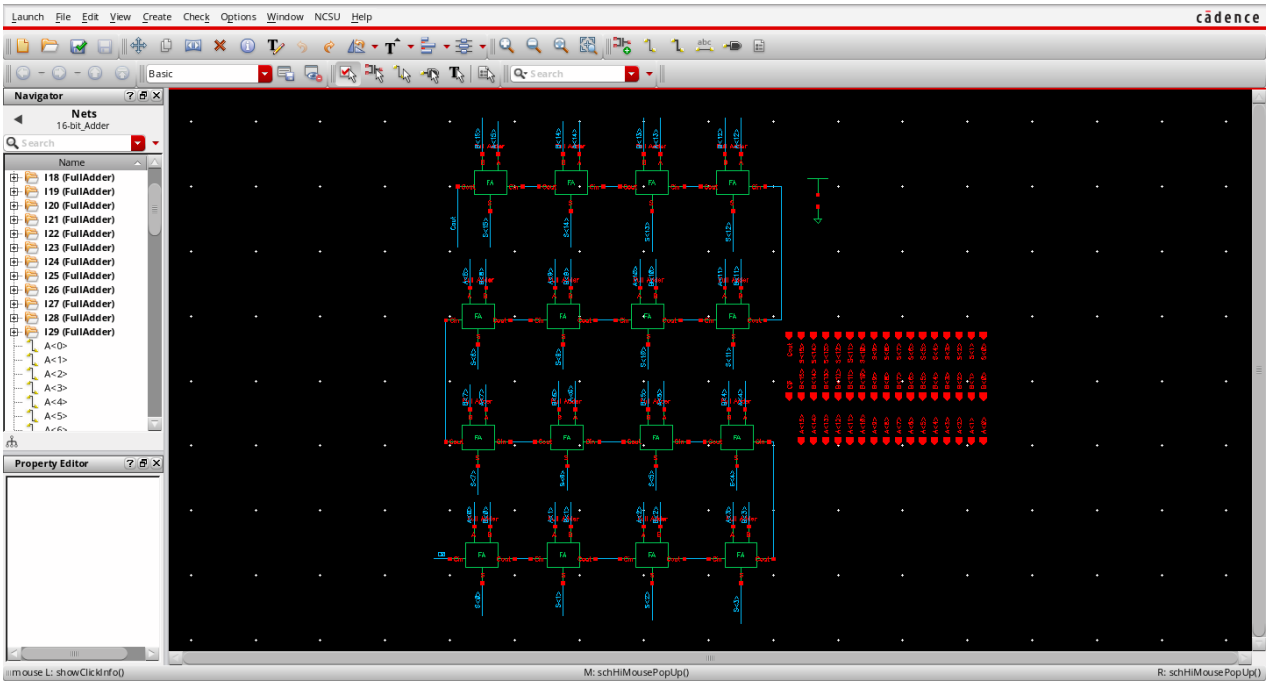
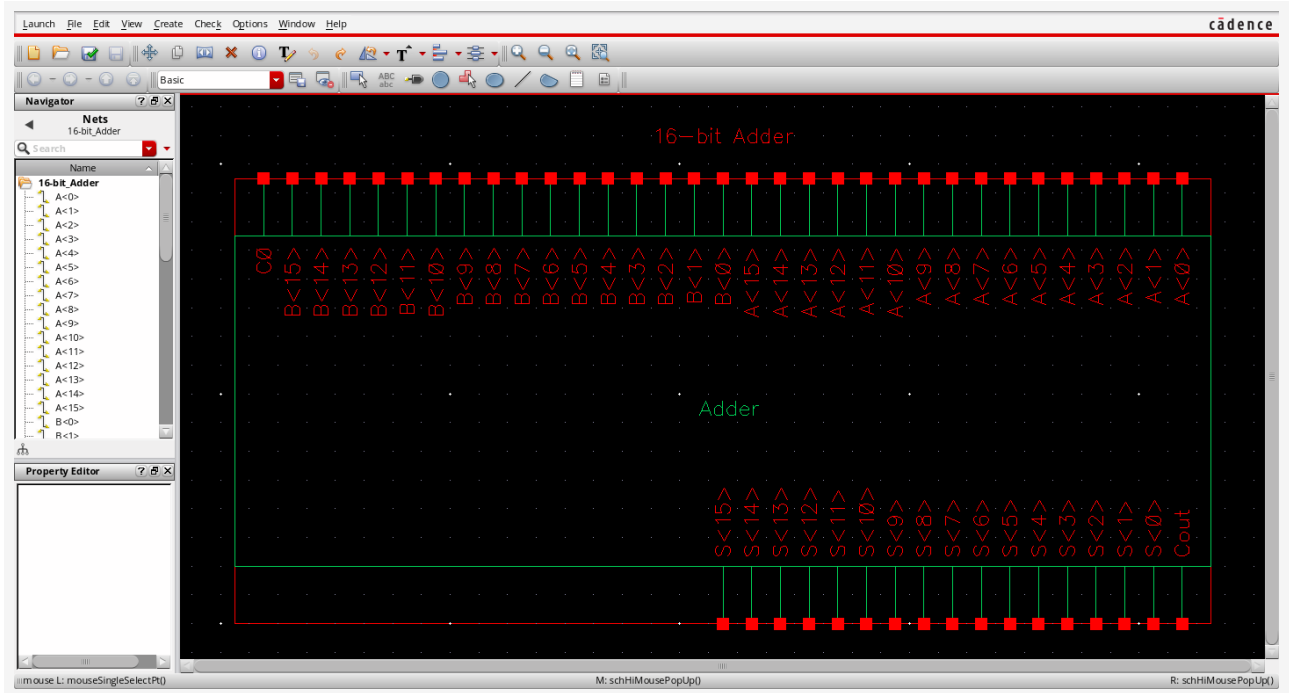
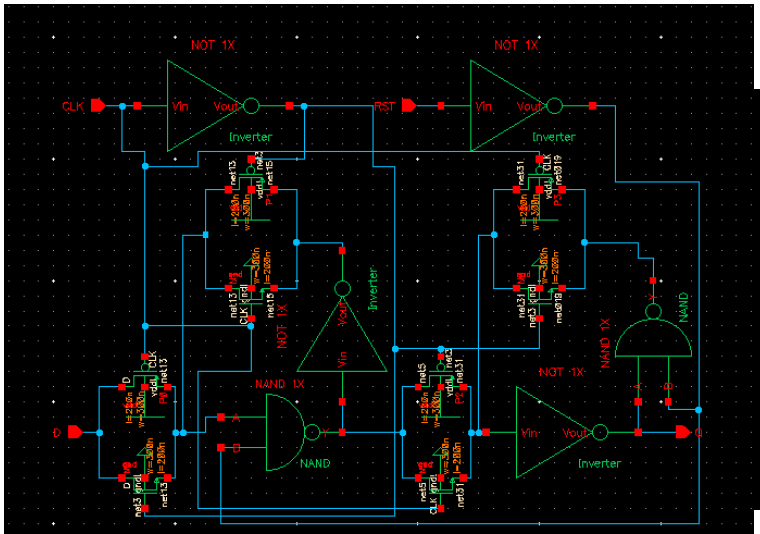
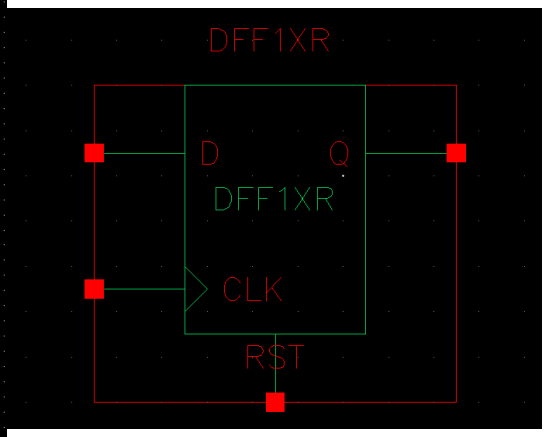
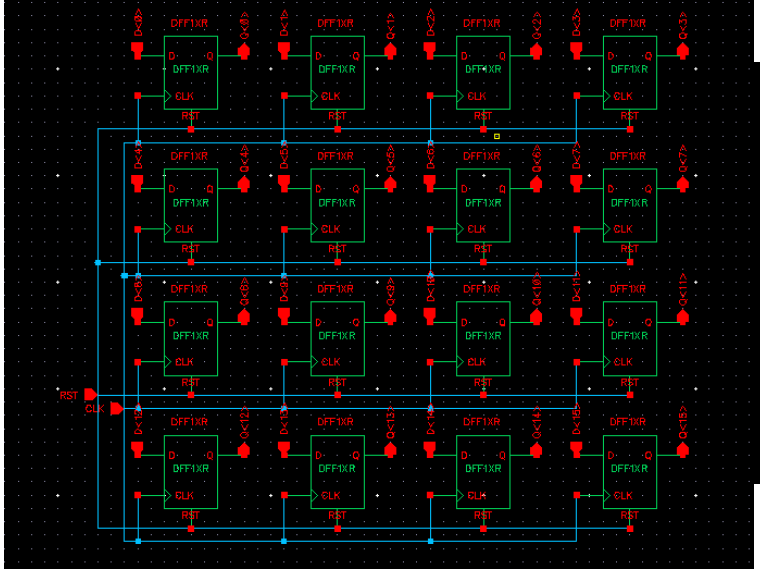
P<7>
P<8>
P<9>
P<10>
P<11>

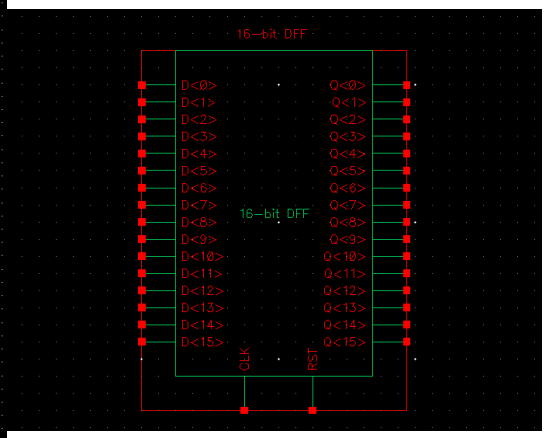

Launch File Edit View Create Check Options Window NCSU Help
cadence
Navigator
Nets
16-bit_Adder
Property Editor


Launch File Edit View Create Check Options Window Help
cadence
Navigator
Nets
16-bit_Adder
Name
16-bit_Adder
Property Editor
16-bit Adder
C0
B<15> B<14> B<13> B<12> B<11> B<10> B<9> B<8> B<7> B<6> B<5> B<4> B<3> B<2> B<1> B<0>
A<15> A<14> A<13> A<12> A<11> A<10> A<9> A<8> A<7> A<6> A<5> A<4> A<3> A<2> A<1> A<0>
Adder
S<15> S<14> S<13> S<12> S<11> S<10> S<9> S<8> S<7> S<6> S<5> S<4> S<3> S<2> S<1> S<0> Cout
mouse L: mouseSingleSelectPt()
M: schHiMousePopUp()
R: schHiMousePopUp()


NOT 1X
NOT 1X
CLK
RST
Vin
Vout
Inverter
Inverter
NAND 1X
NAND
NOT 1X
NAND 1X
NAND
Inverter
D
Q


DFF1XR
D
Q
DFF1XR
CLK
RST


DFF1XR
D
Q
CLK
RST


16-bit DFF
D<0>
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D<2>
D<3>
D<4>
D<5>
D<6>
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D<8>
D<9>
D<10>
D<11>
D<12>
D<13>
D<14>
D<15>
Q<0>
Q<1>
Q<2>
Q<3>
Q<4>
Q<5>
Q<6>
Q<7>
Q<8>
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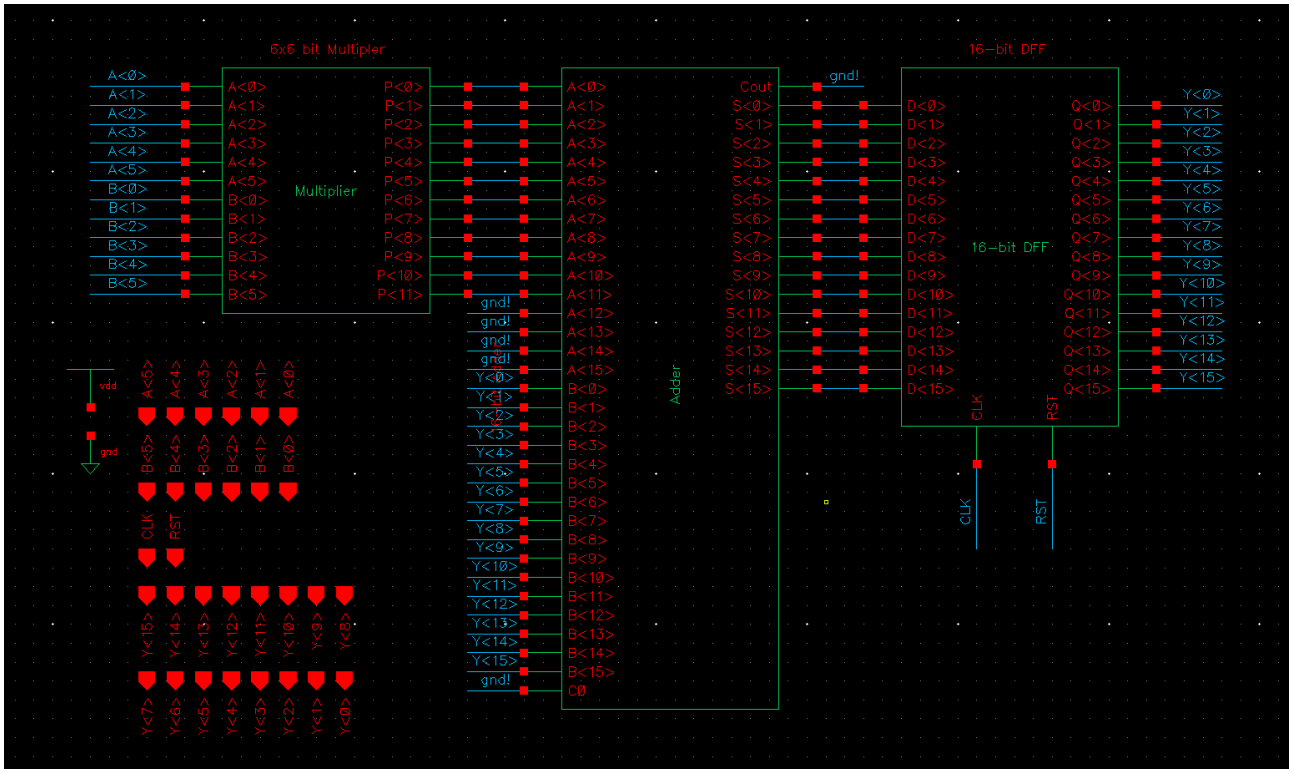
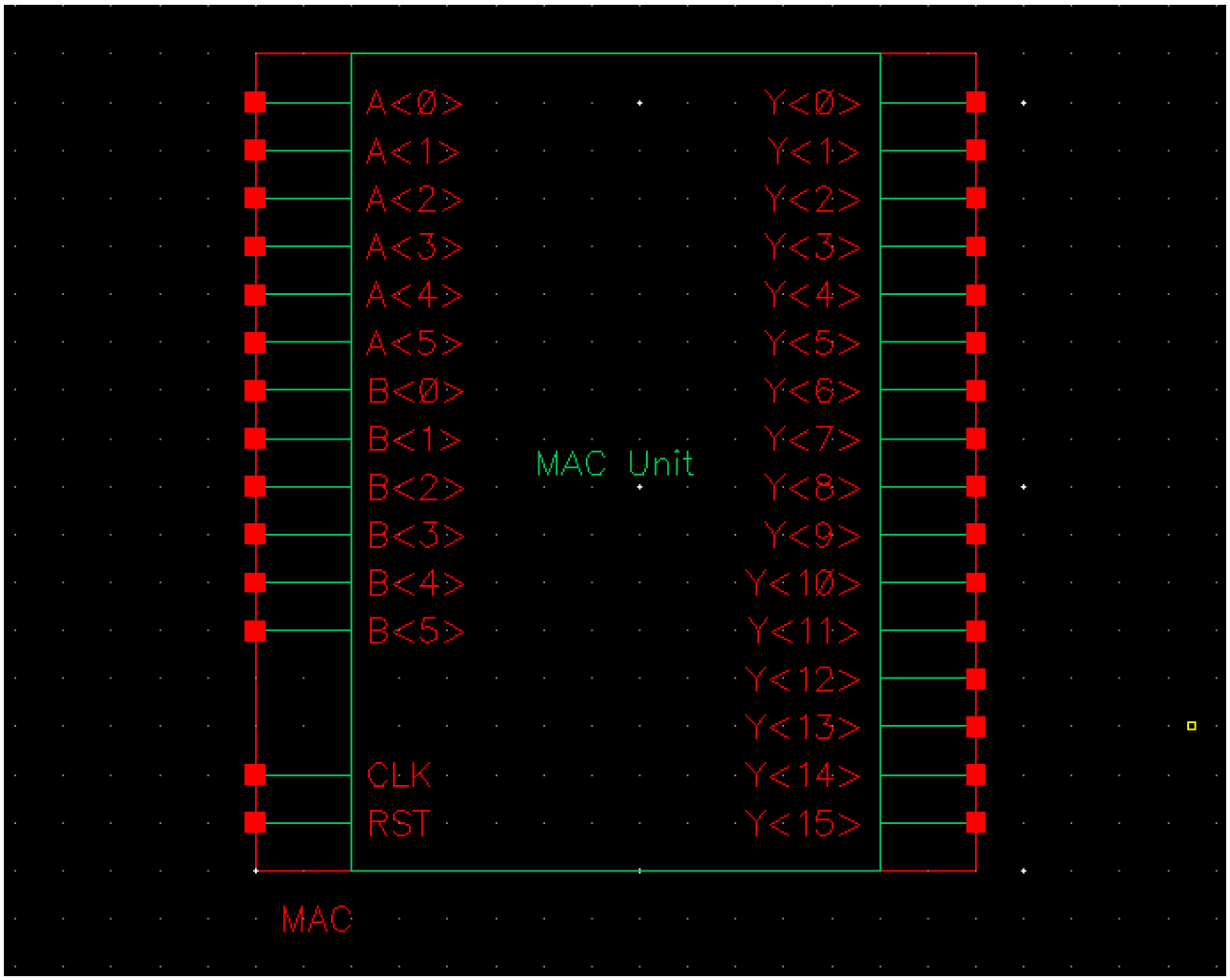
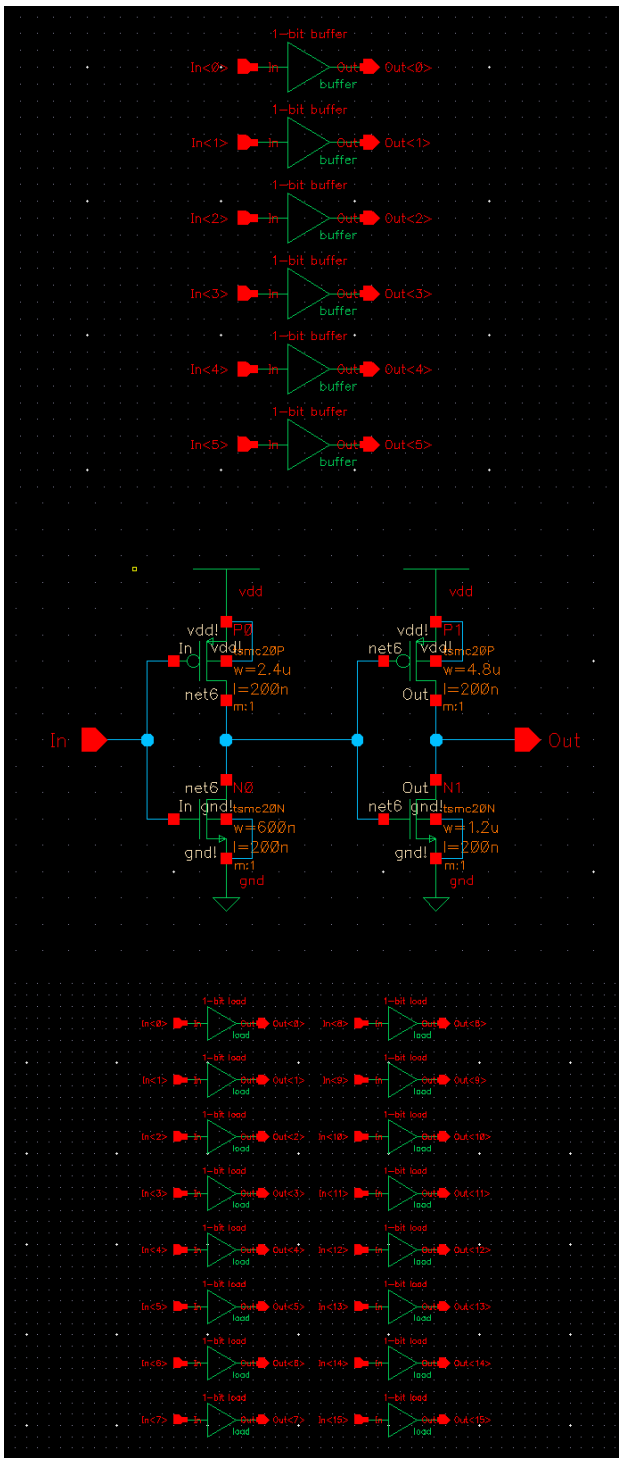
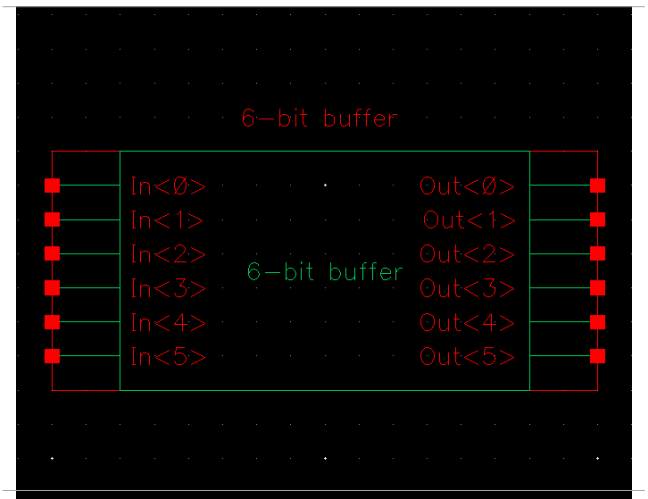
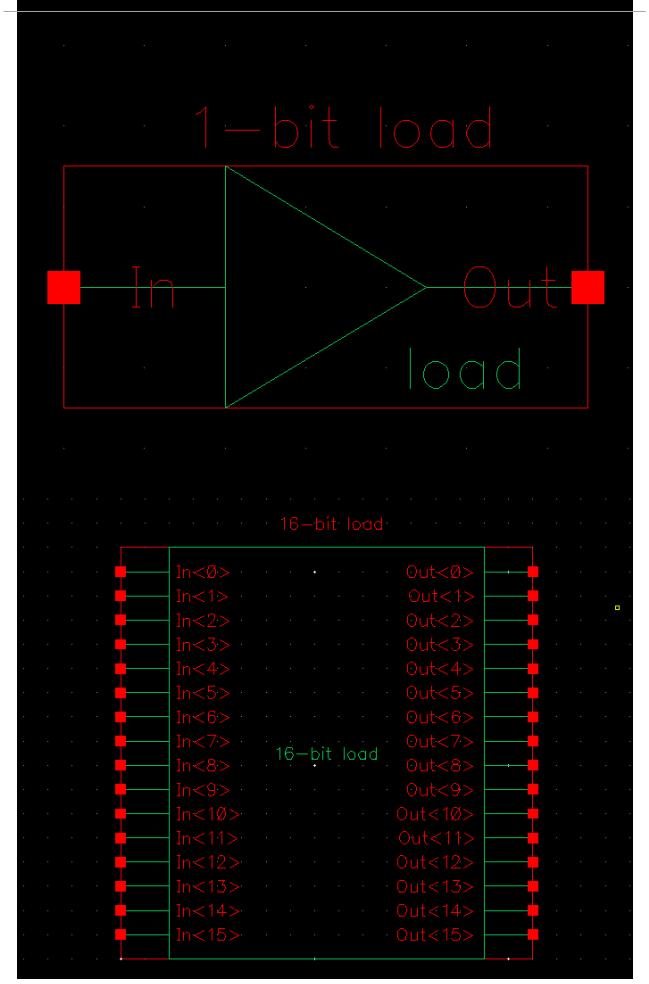
Q<11>
Q<12>
Q<13>
Q<14>
Q<15>
16-bit DFF
CLK
RST


6x6 bit Multiplier
Multiplier
16-bit DFF
16-bit DFF
Adder
gnd!
Cout
CLK
RST
vdd
gnd


MAC Unit
MAC
A<0>
A<1>
A<2>
A<3>
A<4>
A<5>
B<0>
B<1>
B<2>
B<3>
B<4>
B<5>
CLK
RST
Y<0>
Y<1>
Y<2>
Y<3>
Y<4>
Y<5>
Y<6>
Y<7>
Y<8>
Y<9>
Y<10>
Y<11>
Y<12>
Y<13>
Y<14>
Y<15>


1-bit buffer
In<0>
Out<0>
In<1>
Out<1>
In<2>
Out<2>
In<3>
Out<3>
In<4>
Out<4>
In<5>
Out<5>
buffer
vdd
vdd!
P0
P1
In
Out
net6
w=2.4u
w=4.8u
l=200n
m:1
N0
N1
gnd!
w=600n
w=1.2u
gnd
1-bit load
load


6-bit buffer
In<0>
In<1>
In<2>
In<3>
In<4>
In<5>
Out<0>
Out<1>
Out<2>
Out<3>
Out<4>
Out<5>
6-bit buffer


1-bit load
In
Out
load
16-bit load
In<0>
In<1>
In<2>
In<3>
In<4>
In<5>
In<6>
In<7>
In<8>
In<9>
In<10>
In<11>
In<12>
In<13>
In<14>
In<15>
Out<0>
Out<1>
Out<2>
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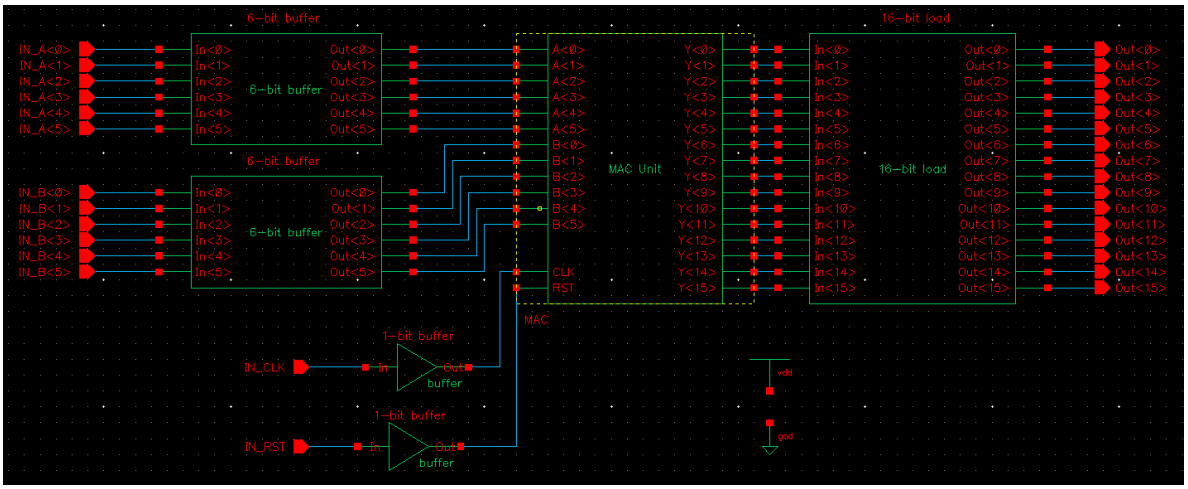
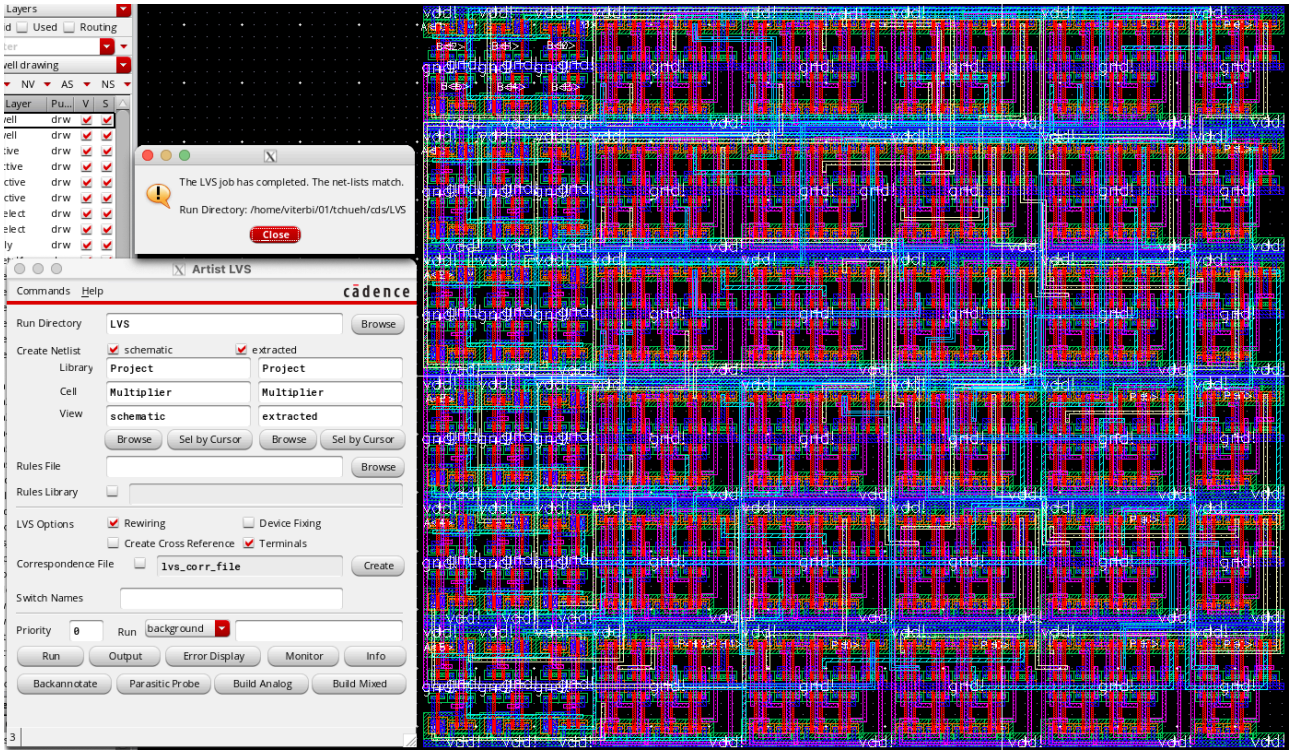
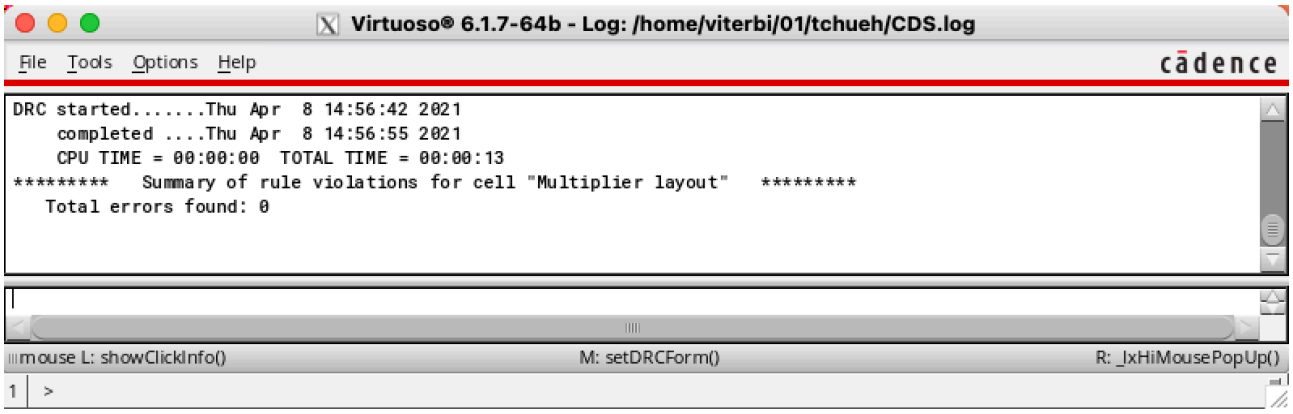
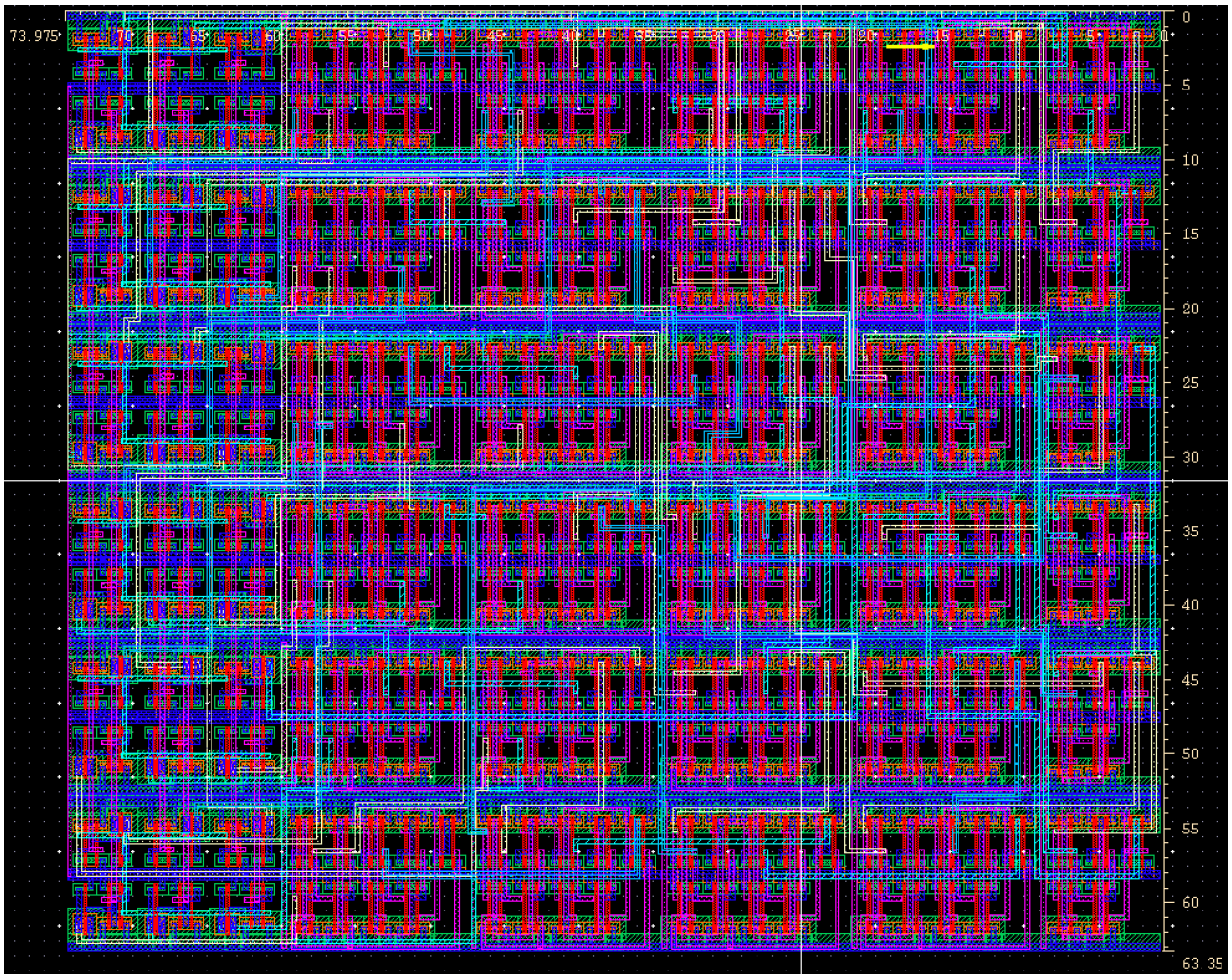
Out<4>
Out<5>
Out<6>
Out<7>
Out<8>
Out<9>
Out<10>
Out<11>
Out<12>
Out<13>
Out<14>
Out<15>
16-bit load

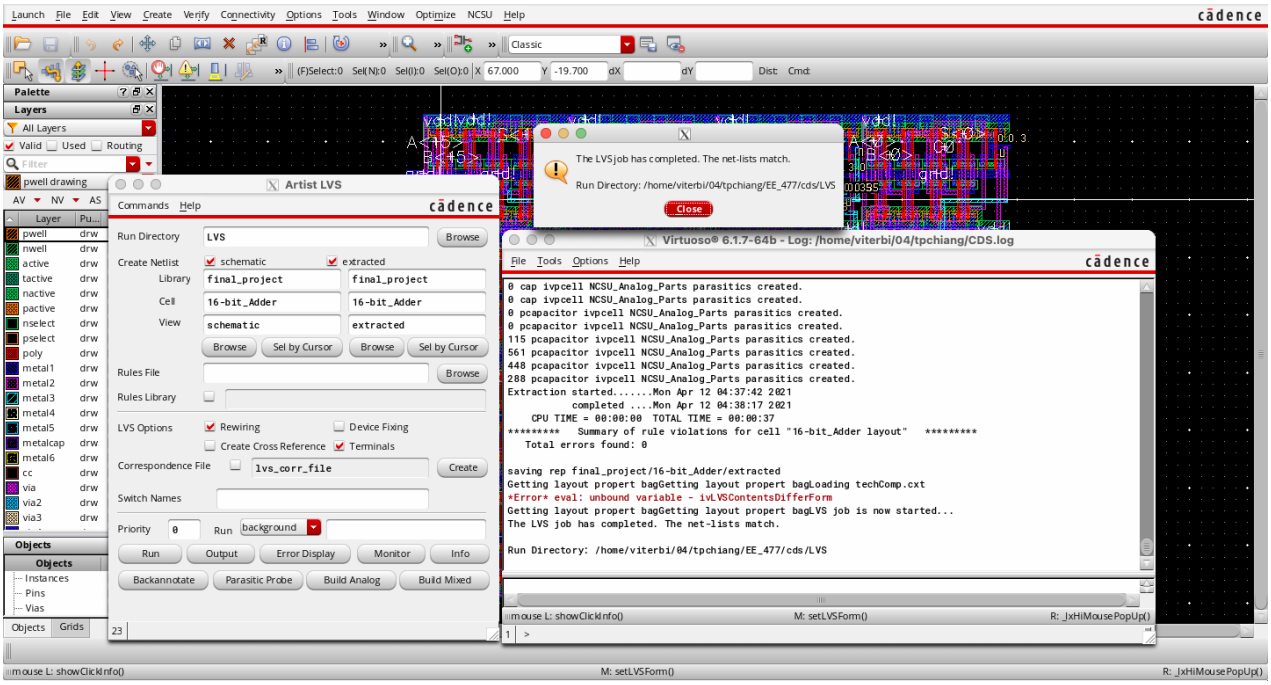

6-bit buffer
IN_A<0>
IN_A<1>
IN_A<2>
IN_A<3>
IN_A<4>
IN_A<5>
IN_B<0>
IN_B<1>
IN_B<2>
IN_B<3>
IN_B<4>
IN_B<5>
MAC Unit
CLK
RST
MAC
16-bit load
IN_CLK
IN_RST
1-bit buffer
buffer
vdd
gnd

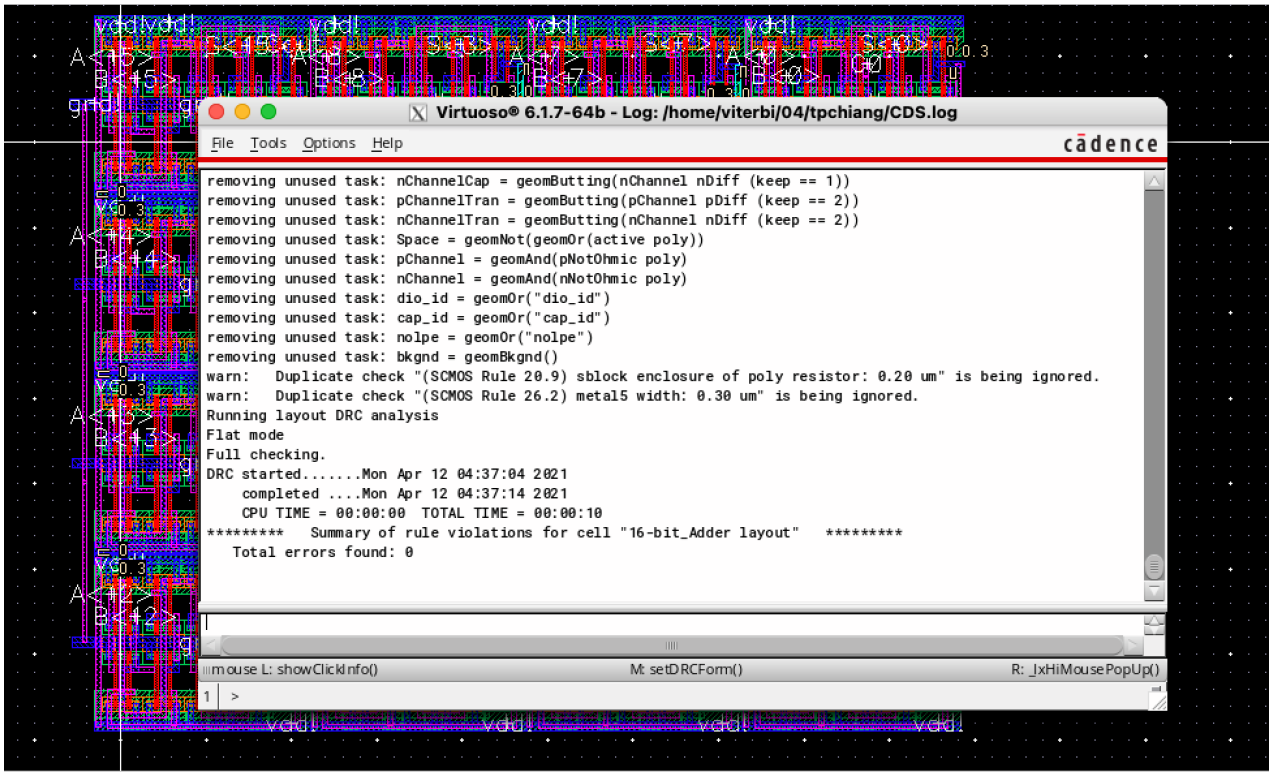

The LVS job has completed. The net-lists match.
Run Directory: /home/viterbi/01/tchueh/cds/LVS
Close
Artist LVS
Commands Help
cadence
Run Directory
LVS
Browse
Create Netlist
schematic
extracted
Library
Project
Cell
Multiplier
View
schematic
extracted
Sel by Cursor
Rules File
Rules Library
LVS Options
Rewiring
Device Fixing
Create Cross Reference
Terminals
Correspondence File
lvs_corr_file
Create
Switch Names
Priority
Run
background
Run
Output
Error Display
Monitor
Info
Backannotate
Parasitic Probe
Build Analog
Build Mixed


Virtuoso® 6.1.7-64b - Log: /home/viterbi/01/tchueh/CDS.log
File Tools Options Help
cadence
DRC started.....Thu Apr 8 14:56:42 2021
completed ....Thu Apr 8 14:56:55 2021
CPU TIME = 00:00:00 TOTAL TIME = 00:00:13
********* Summary of rule violations for cell "Multiplier layout" *********
Total errors found: 0
mouse L: showClickInfo()
M: setDRCForm()
R: _lxHiMousePopUp()
1 >

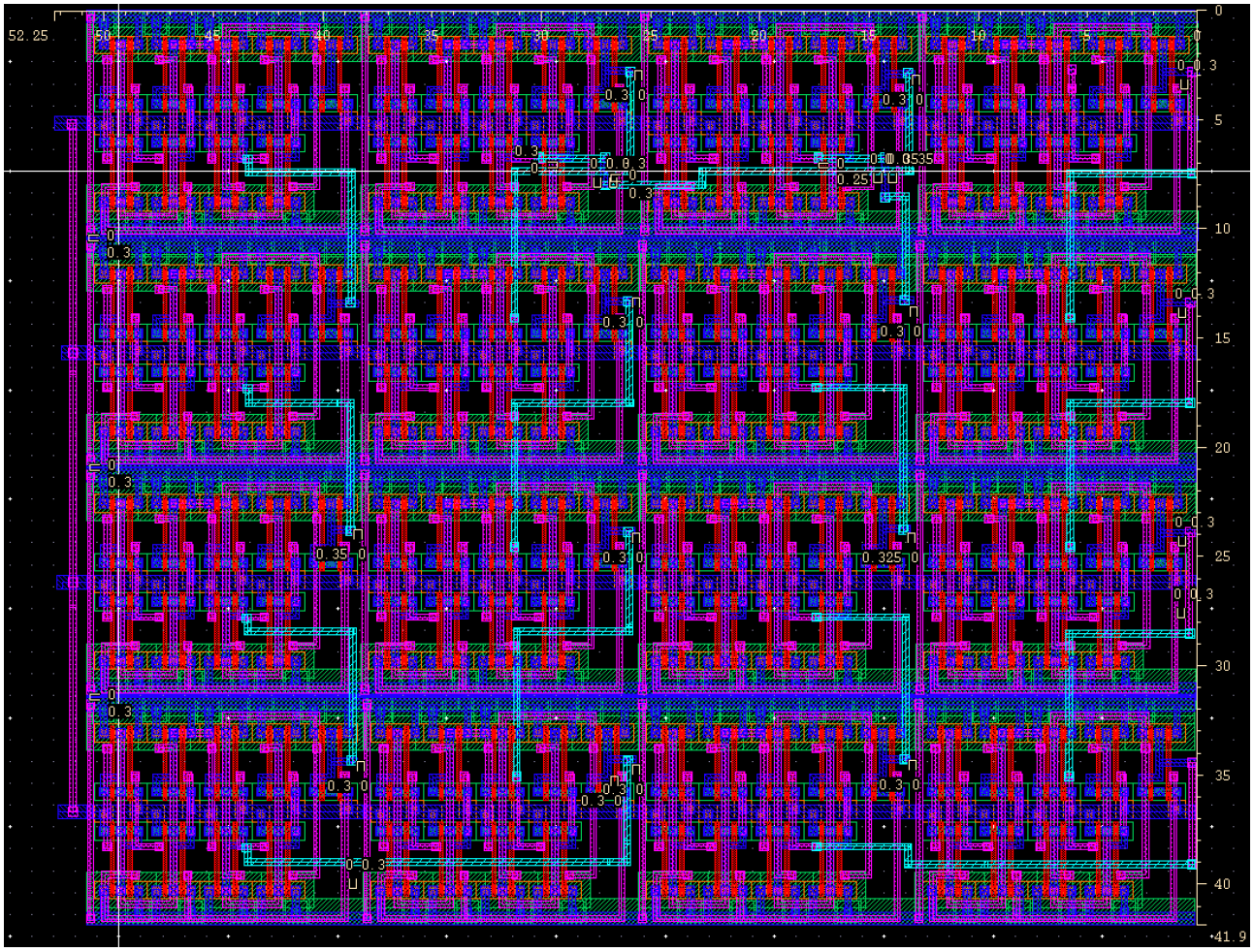
Total area: 4686.32 µm^2

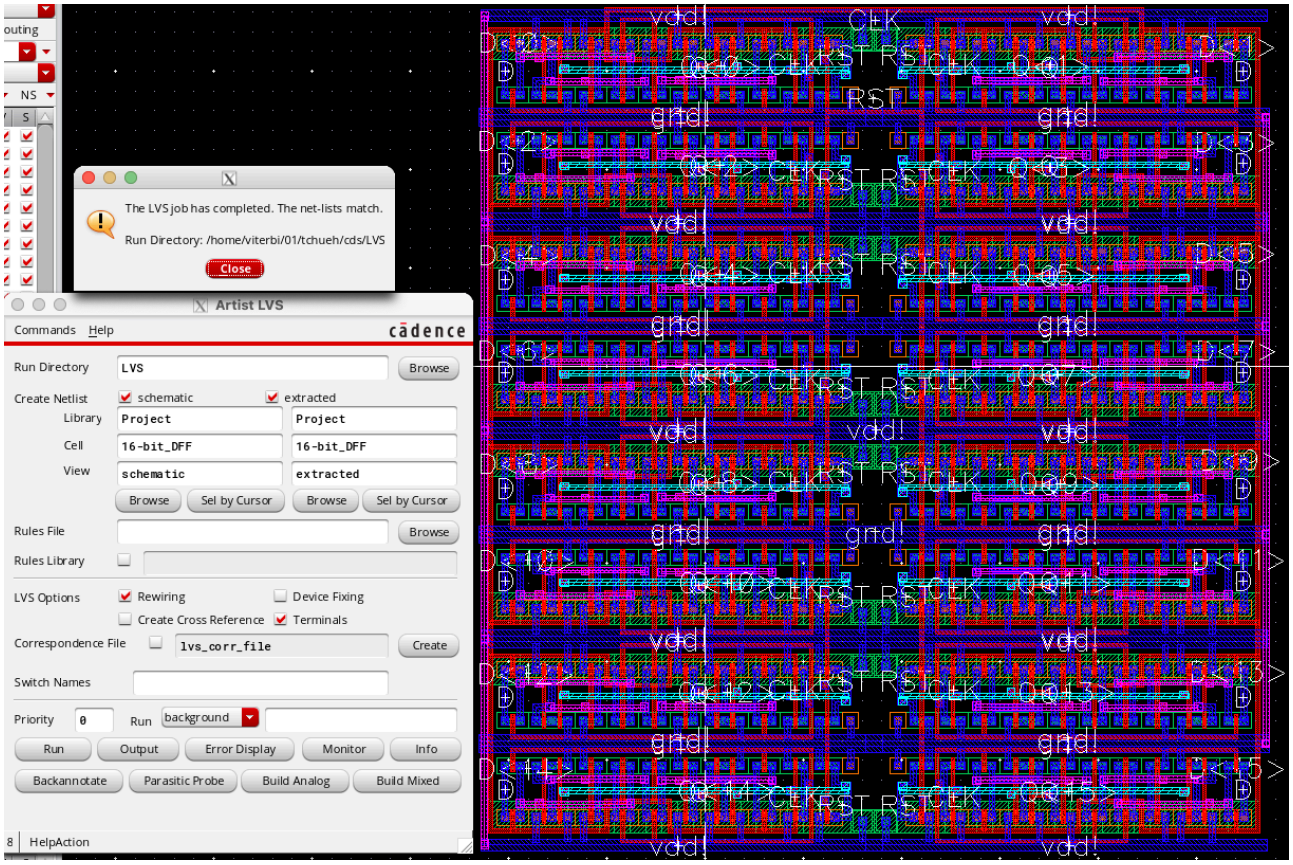




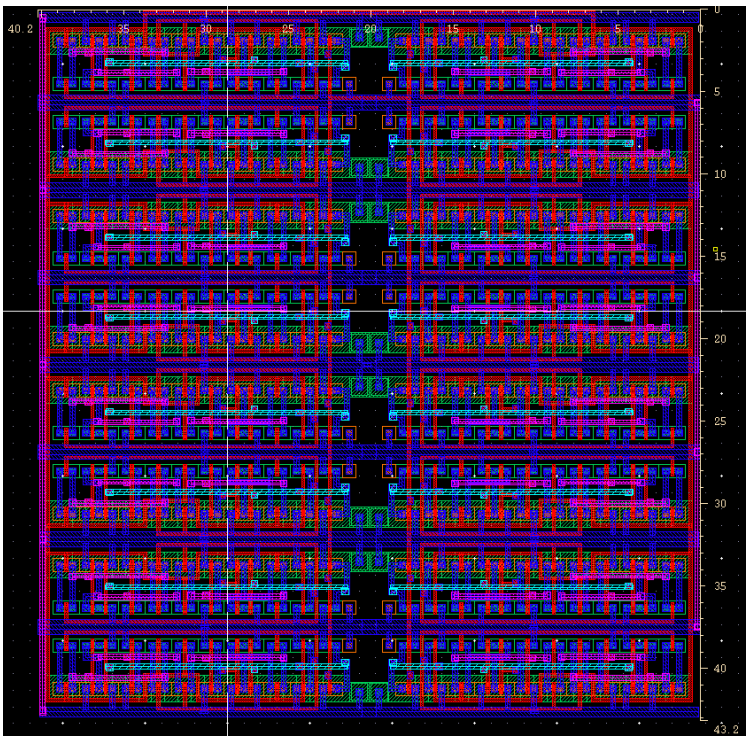


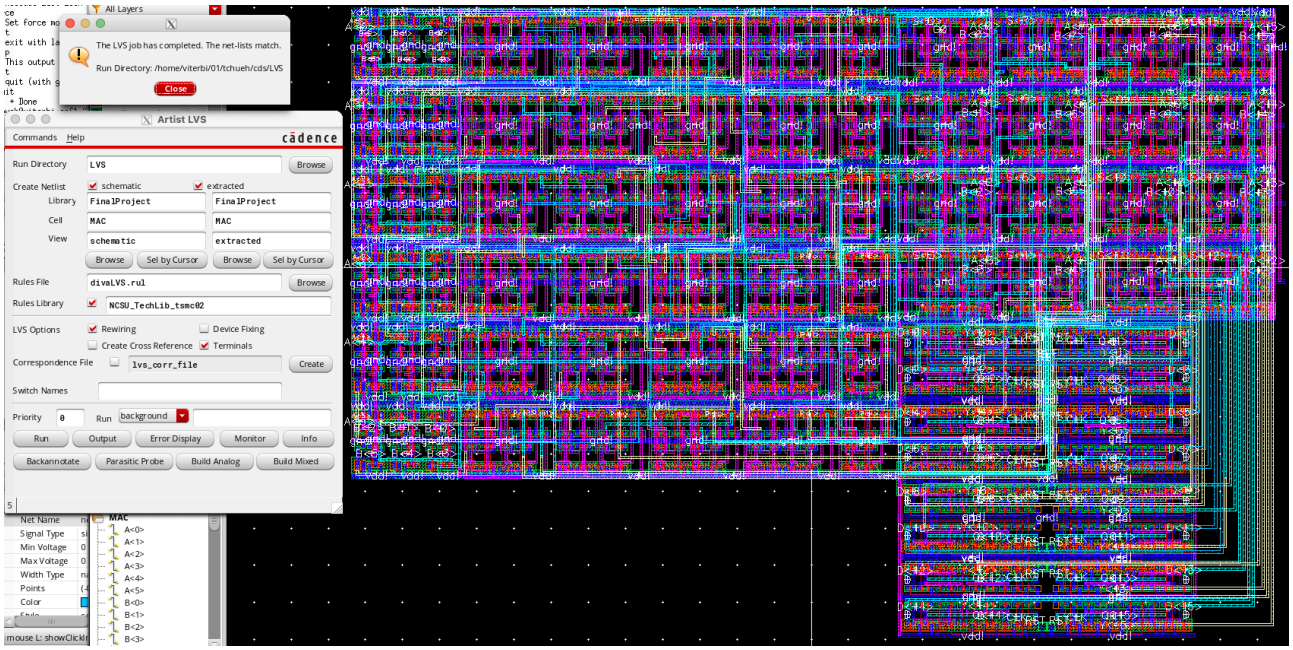
Total area: 2189.275 μm^2

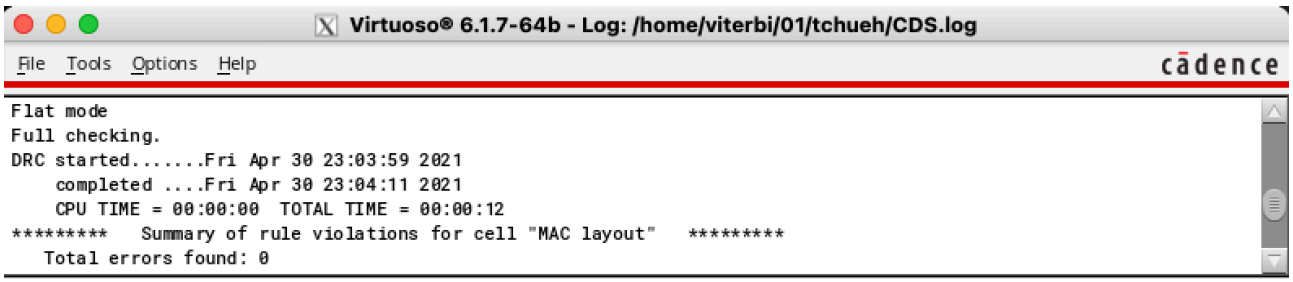




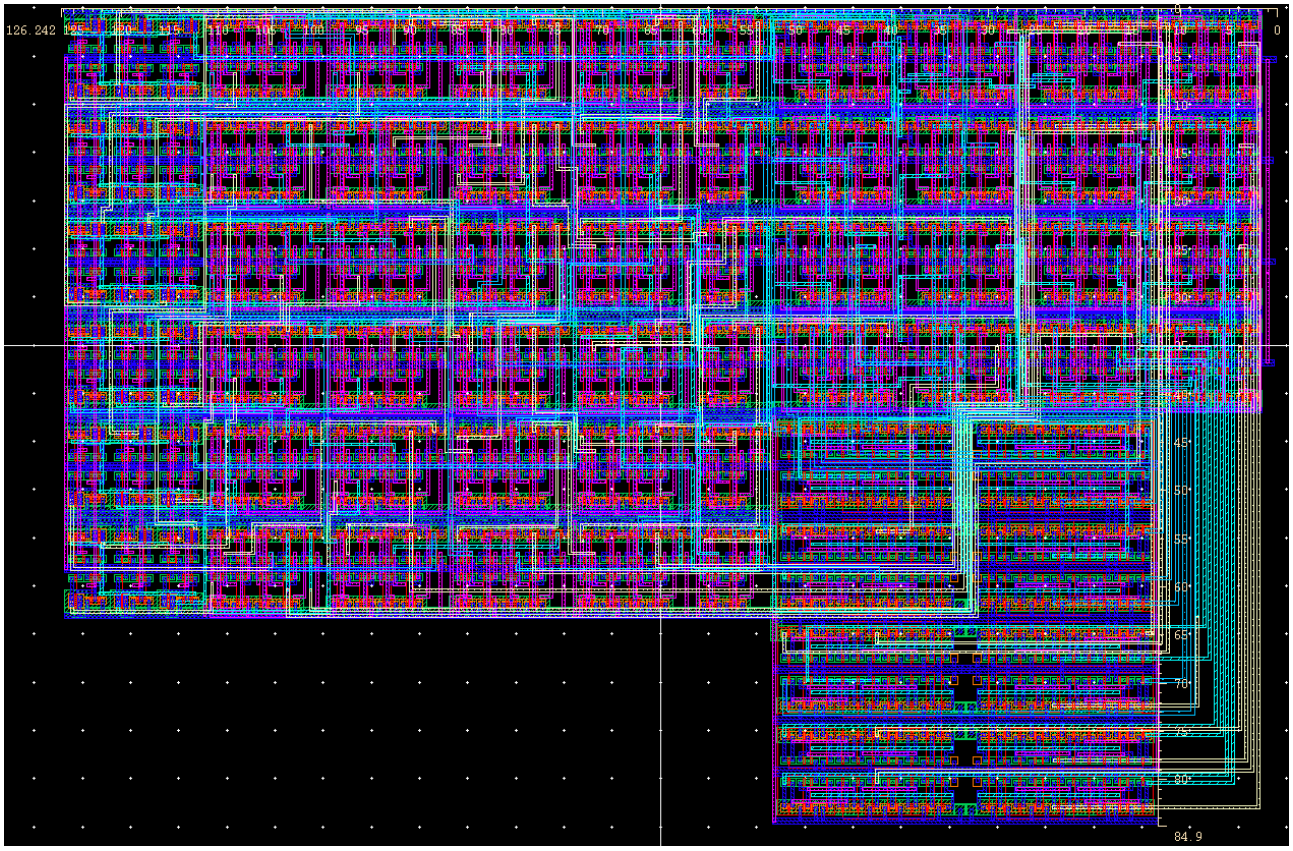
Total area: 1736.64 µm^2

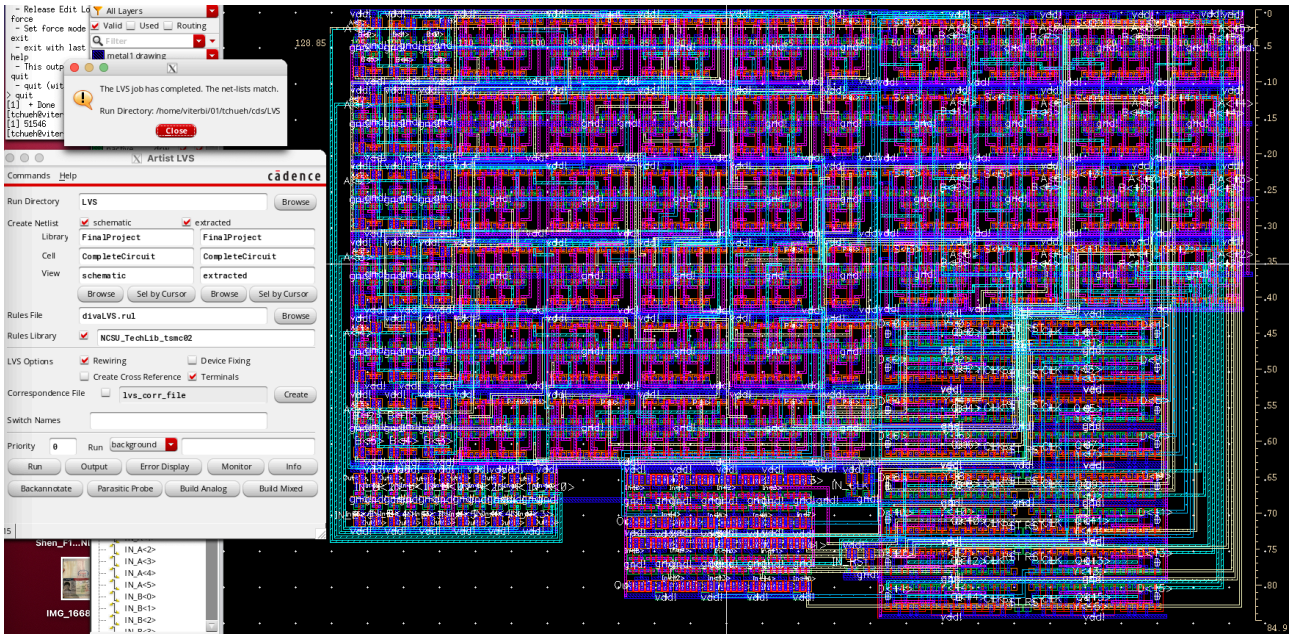




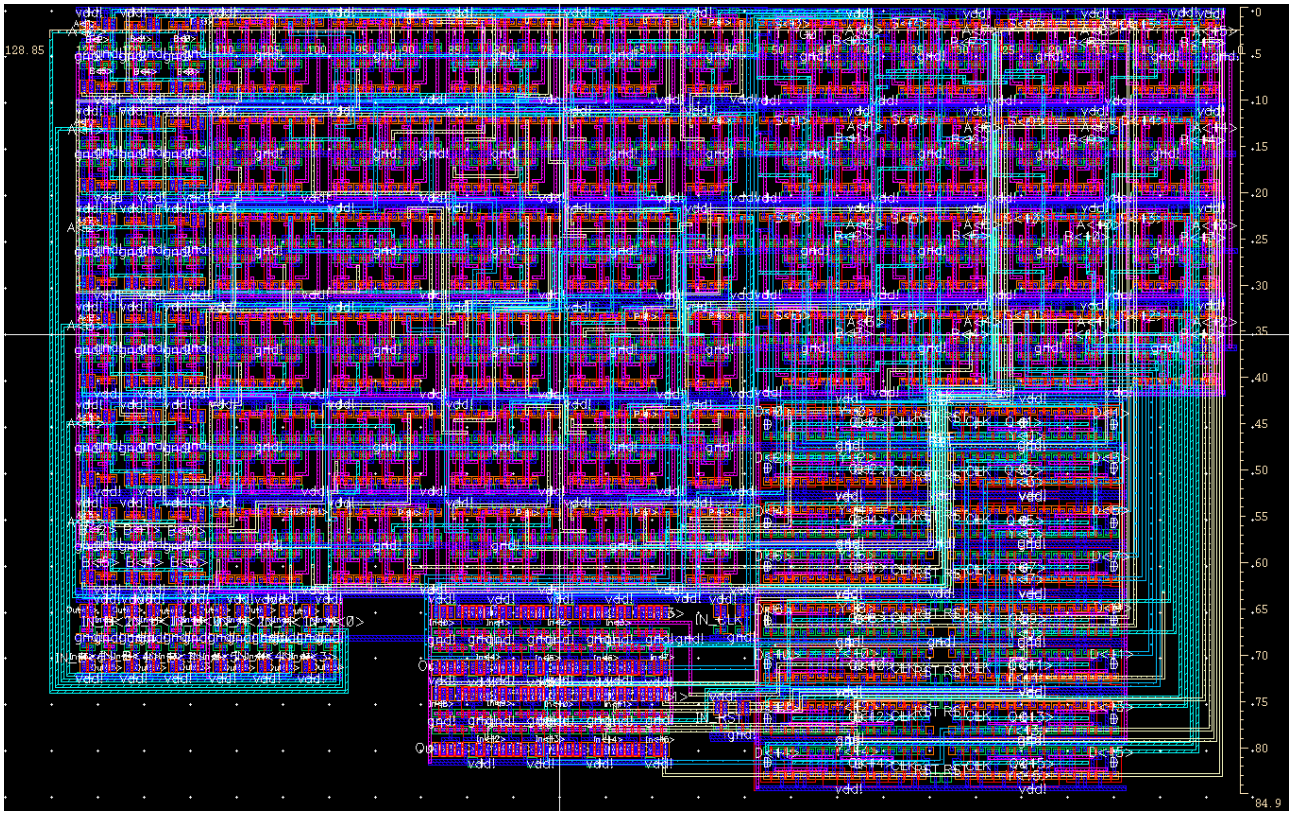


Total area: 10717.946 µm^2



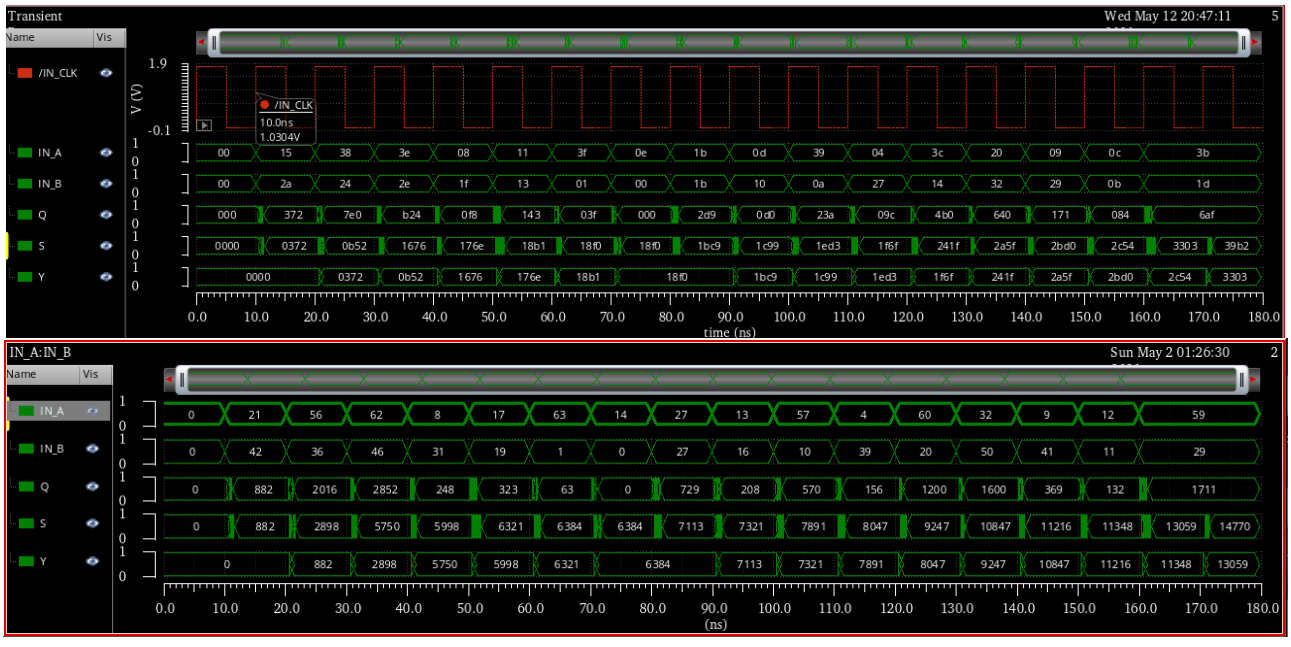


Total area: 10939.365 μm^2



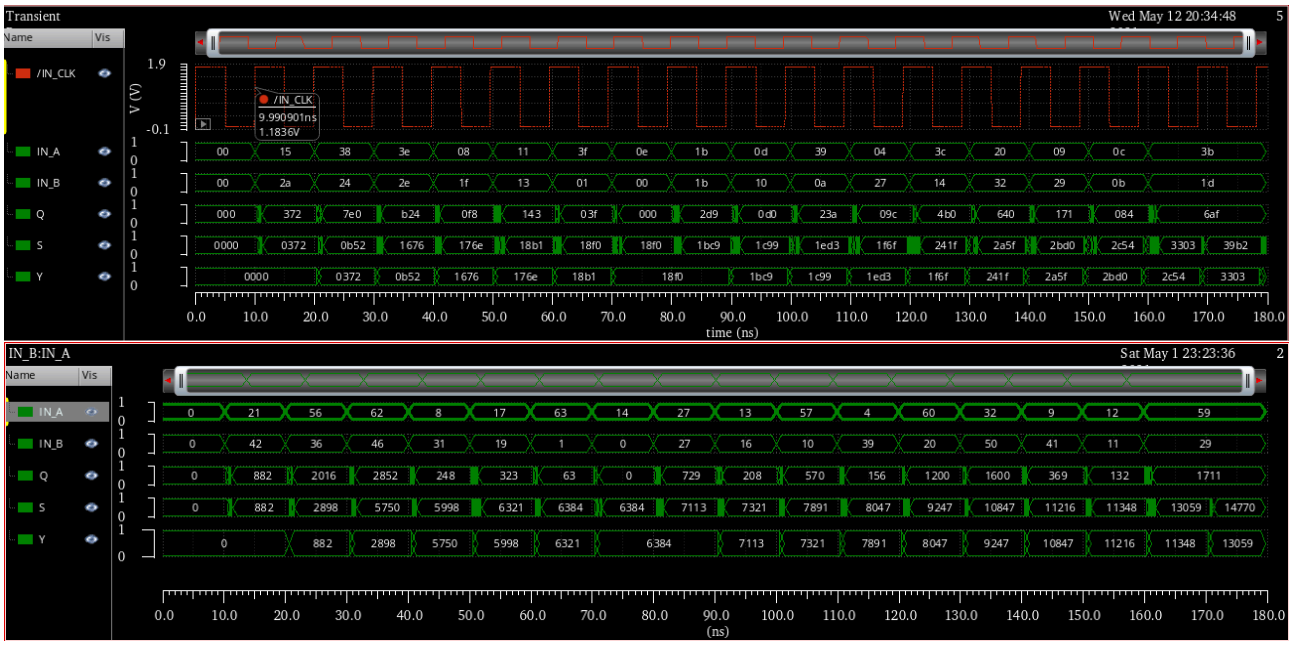
Part-B (a)

SL No.	RST	IN_A	IN_B	Q[11:0]	S[15:0]	Y[15:0]
Initial State>	0	0	0	0	0	0
1	1	21	42	882	882	0
2	1	56	36	2016	2898	882
3	1	62	46	2852	5750	2898
4	1	8	31	248	5998	5750
5	1	17	19	323	6321	5998
6	1	63	1	63	6384	6321
7	1	14	0	0	6384	6384
8	1	27	27	729	7113	6384
9	1	13	16	208	7321	7113
10	1	57	10	570	7891	7321
11	1	4	39	156	8047	7891
12	1	60	20	1200	9247	8047
13	1	32	50	1600	10847	9247
14	1	9	41	369	11216	10847
15	1	12	11	132	11348	11216
16	1	59	29	1711	13059	11348



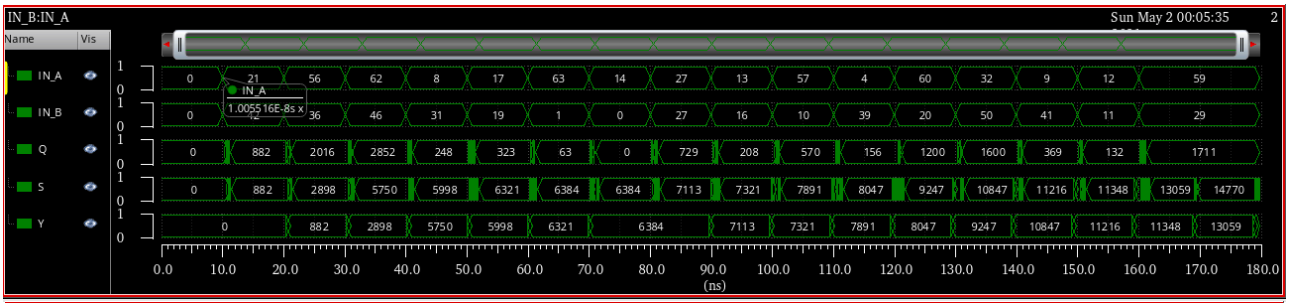
Part-B (b)

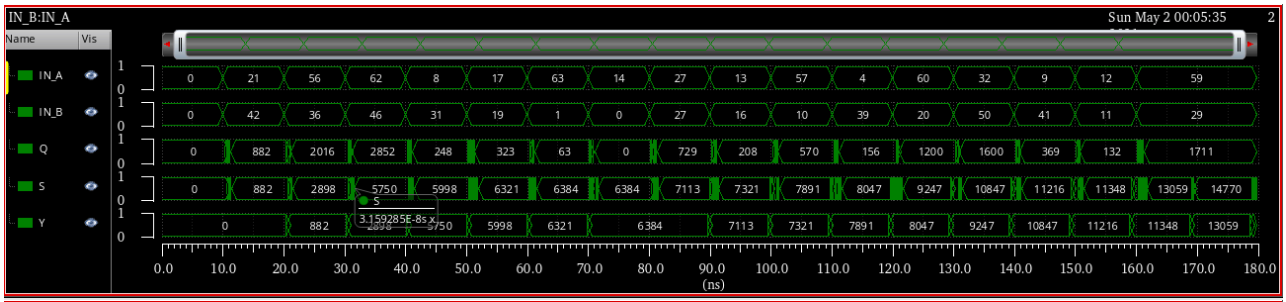
SL No.	RST	IN_A	IN_B	Q[11:0]	S[15:0]	Y[15:0]
Initial State>	0	0	0	0	0	0
1	1	21	42	882	882	0
2	1	56	36	2016	2898	882
3	1	62	46	2852	5750	2898
4	1	8	31	248	5998	5750
5	1	17	19	323	6321	5998
6	1	63	1	63	6384	6321
7	1	14	0	0	6384	6384
8	1	27	27	729	7113	6384
9	1	13	16	208	7321	7113
10	1	57	10	570	7891	7321
11	1	4	39	156	8047	7891
12	1	60	20	1200	9247	8047
13	1	32	50	1600	10847	9247
14	1	9	41	369	11216	10847
15	1	12	11	132	11348	11216
16	1	59	29	1711	13059	11348

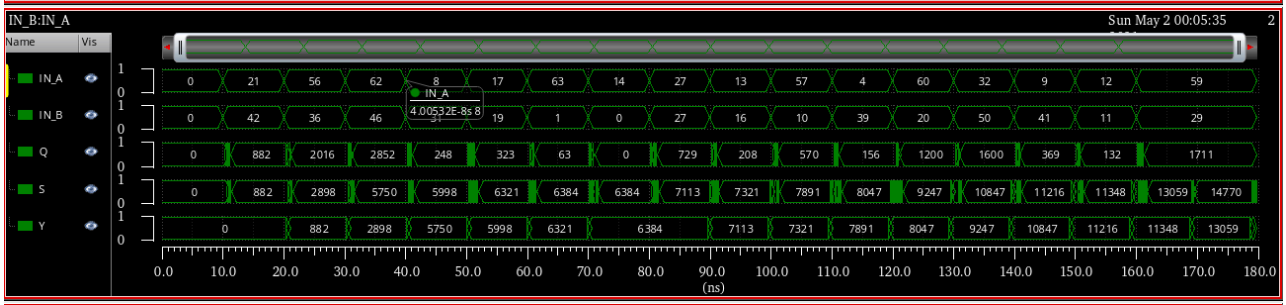


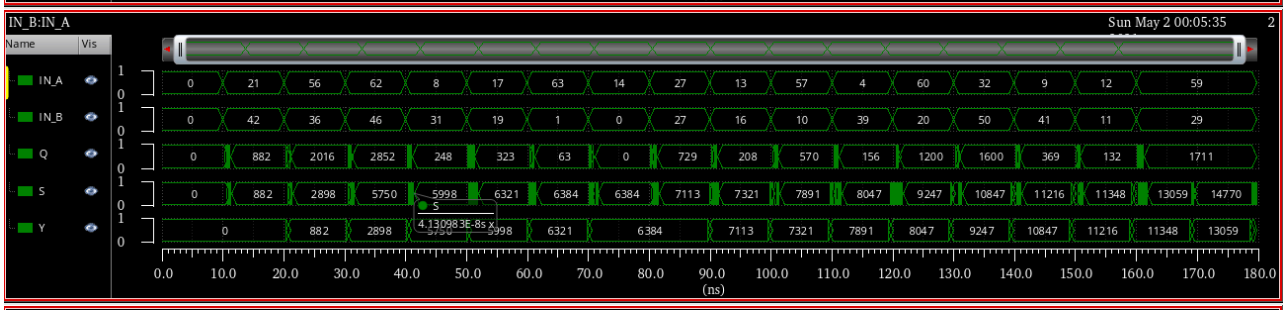
Part-B (c)

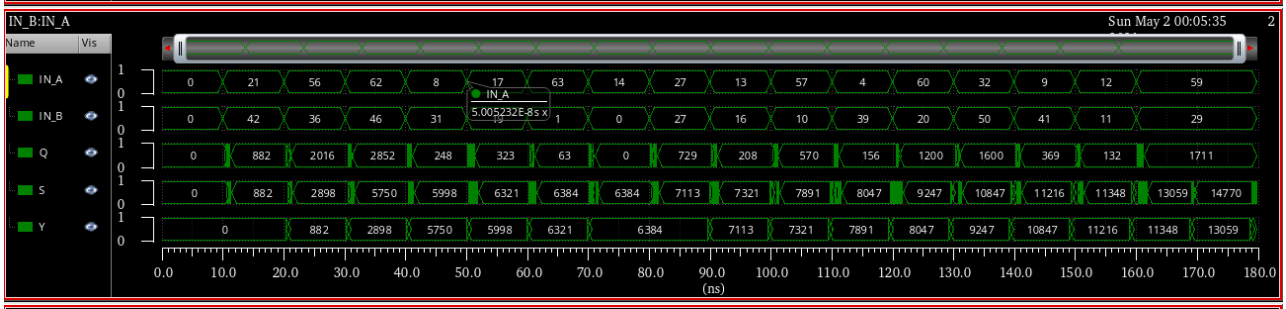
SL No.	RST	IN_A	IN_B	Critical Path	Worst-case Delay [ns]
Initial State>	0	0	0	----	----
1	1	21	42	IN_A/IN_B -> S -> Q -> S -> Y	1.39861
2	1	56	36	IN_A/IN_B -> S -> Q -> S -> Y	1.29393
3	1	62	46	IN_A/IN_B -> S -> Q -> S -> Y	1.53472
4	1	8	31	IN_A/IN_B -> S -> Q -> S -> Y	1.25660
5	1	17	19	IN_A/IN_B -> S -> Q -> S -> Y	1.86979
6	1	63	1	IN_A/IN_B -> S -> Q -> S -> Y	1.57725
7	1	14	0	IN_A/IN_B -> S -> Q -> S -> Y	1.53610
8	1	27	27	IN_A/IN_B -> S -> Q -> S -> Y	1.53563
9	1	13	16	IN_A/IN_B -> S -> Q -> S -> Y	1.44024
10	1	57	10	IN_A/IN_B -> S -> Q -> S -> Y	1.35920
11	1	4	39	IN_A/IN_B -> S -> Q -> S -> Y	1.55750
12	1	60	20	IN_A/IN_B -> S -> Q -> S -> Y	1.77940
13	1	32	50	IN_A/IN_B -> S -> Q -> S -> Y	1.18230
14	1	9	41	IN_A/IN_B -> S -> Q -> S -> Y	1.24320
15	1	12	11	IN_A/IN_B -> S -> Q -> S -> Y	1.34500
16	1	59	29	IN_A/IN_B -> S -> Q -> S -> Y	1.91020




IN_B:IN_A
Sun May 2 00:05:35
Name
Vis
IN_A
IN_B
Q
S
Y
S
3.159285E-8 s
(ns)


IN_B:IN_A
Sun May 2 00:05:35
Name
Vis
IN_A
IN_B
Q
S
Y
IN_A
4.00532E-8 s
(ns)


IN_B:IN_A
Sun May 2 00:05:35
Name
Vis
IN_A
IN_B
Q
S
Y
S
4.130983E-8 s
(ns)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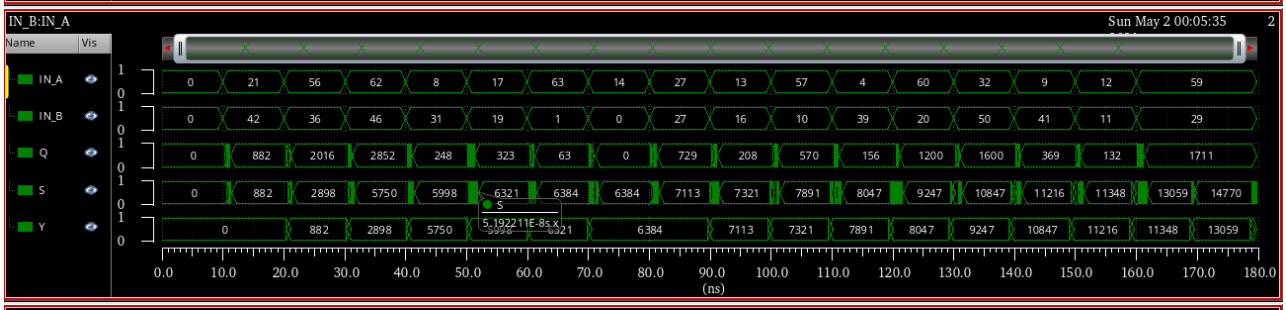
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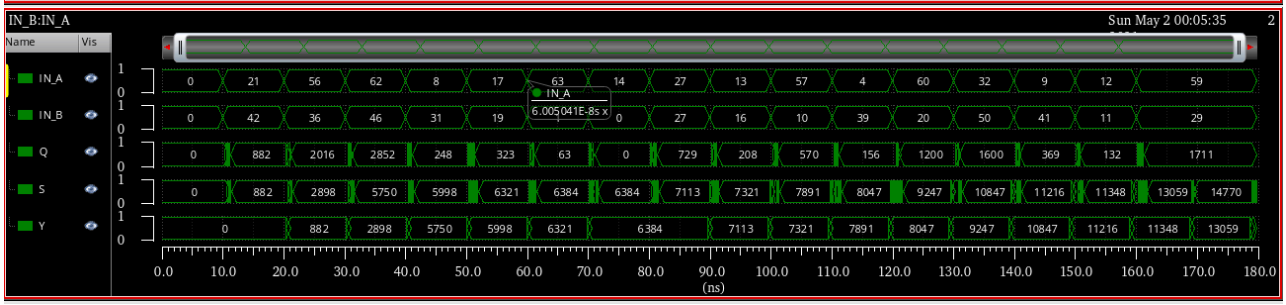
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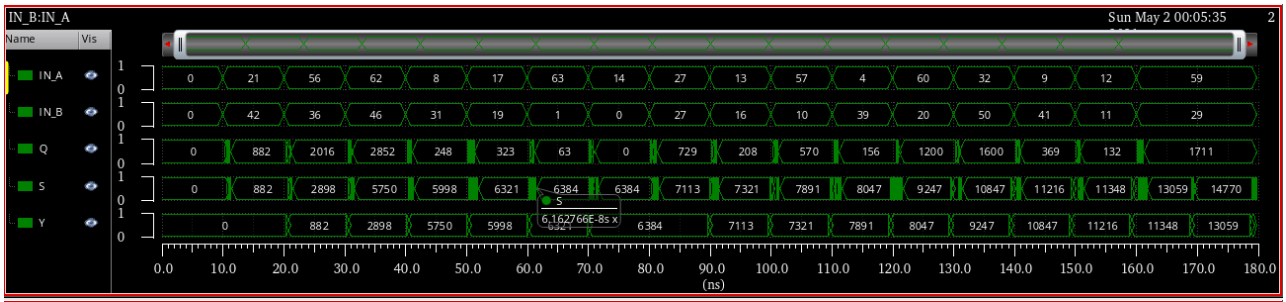
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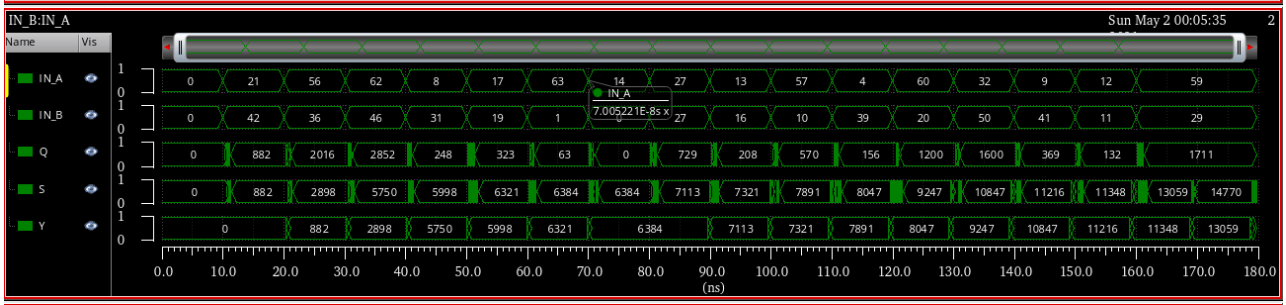
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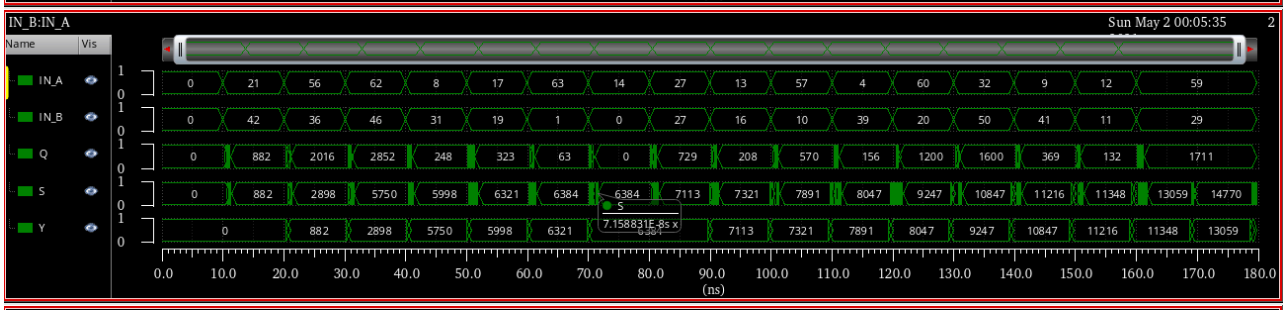
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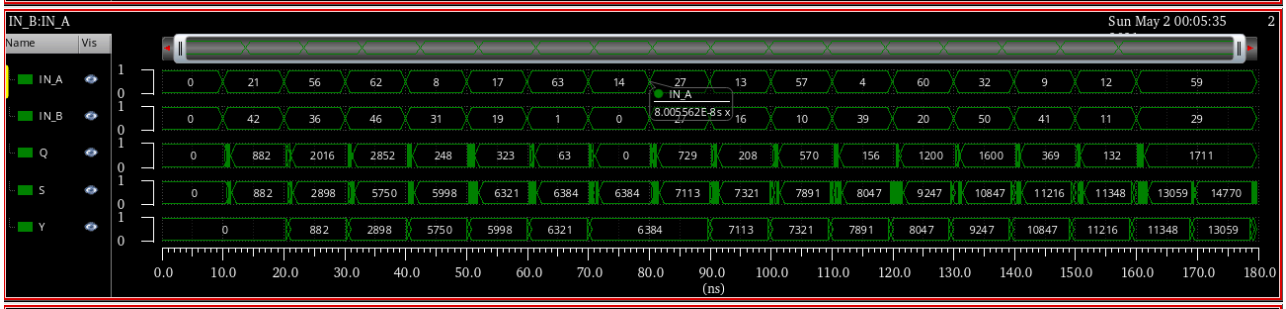
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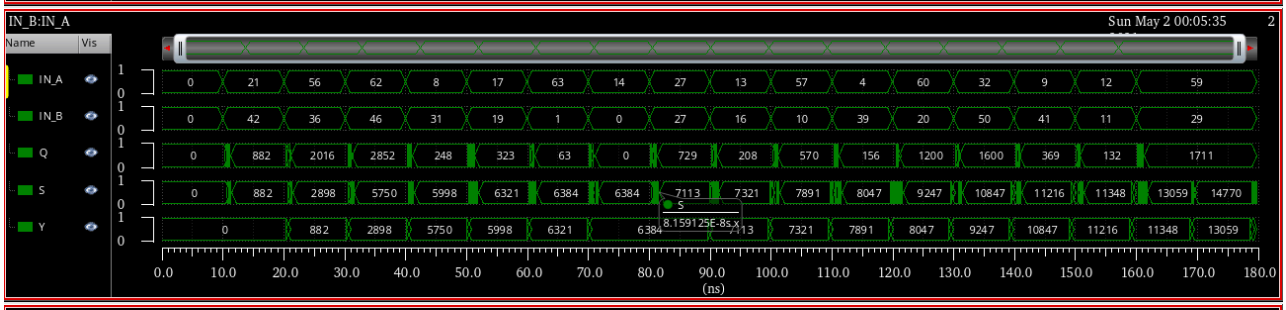
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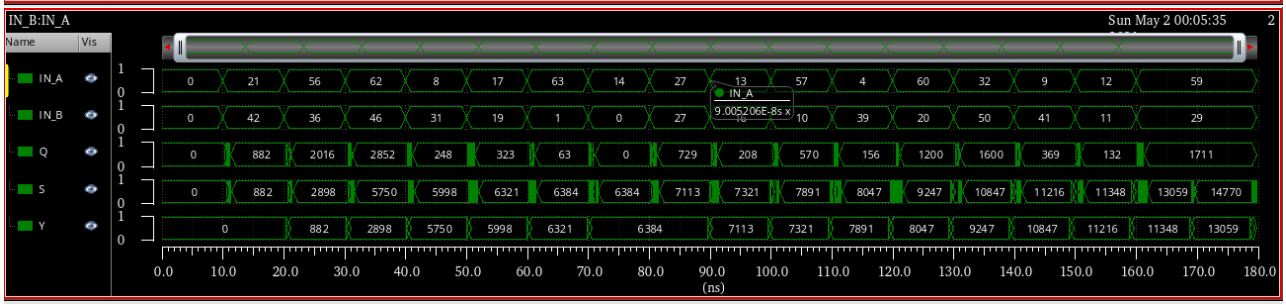
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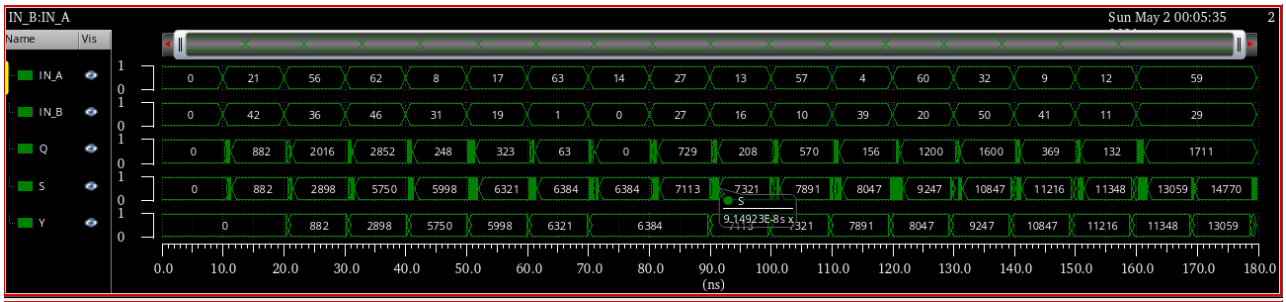
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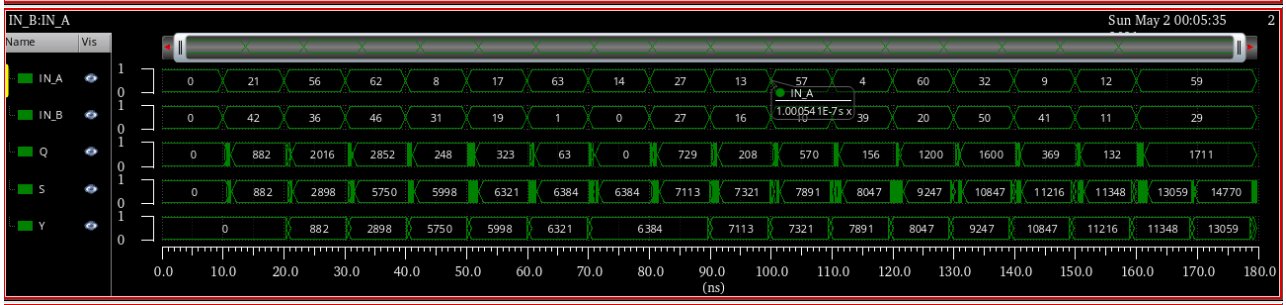
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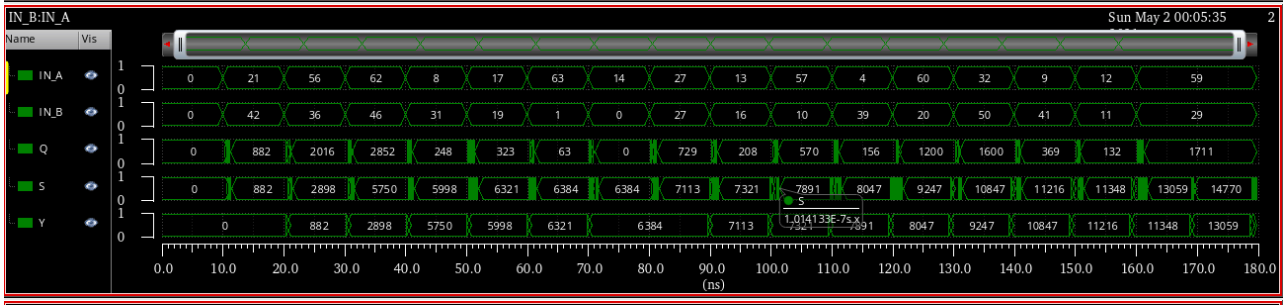
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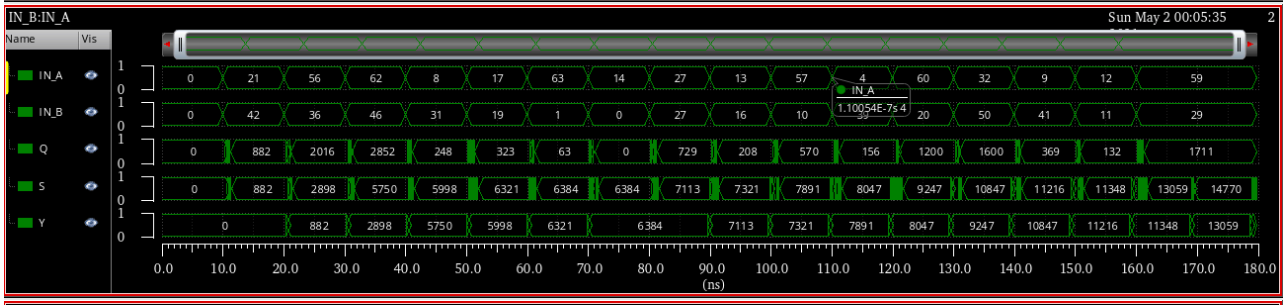
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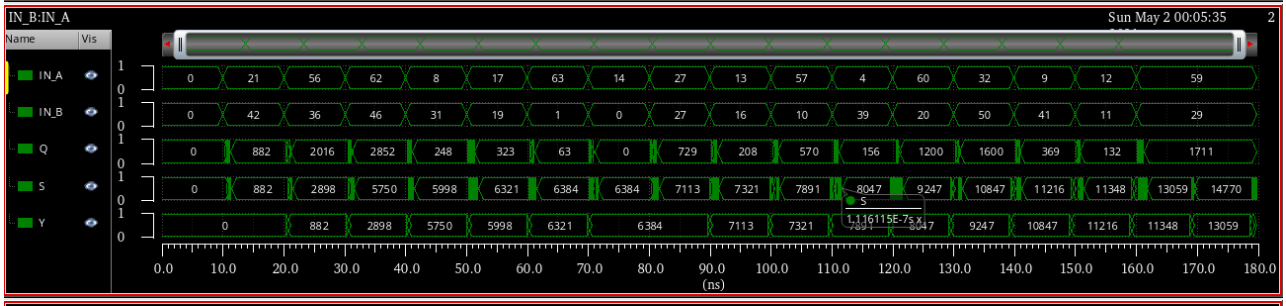
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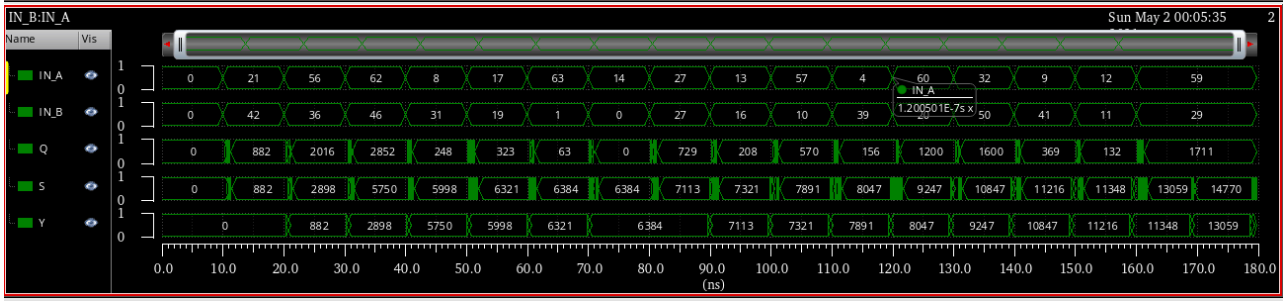
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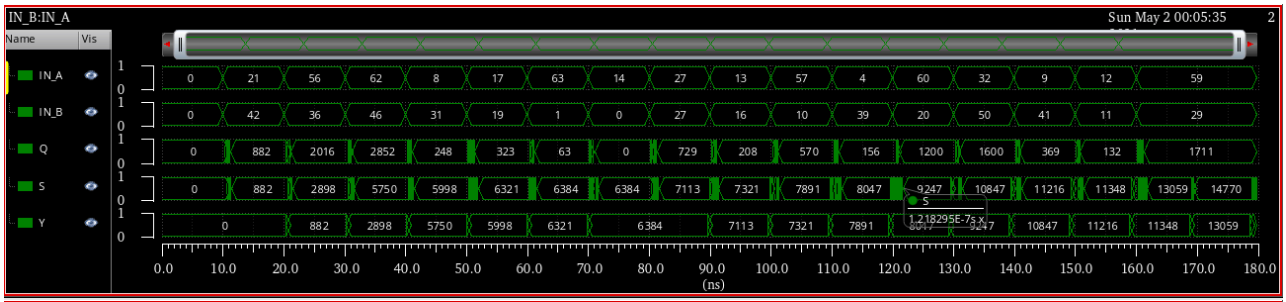
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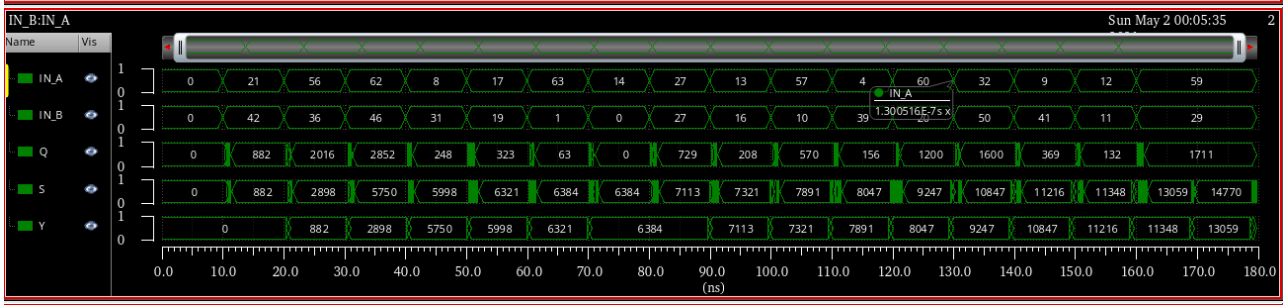
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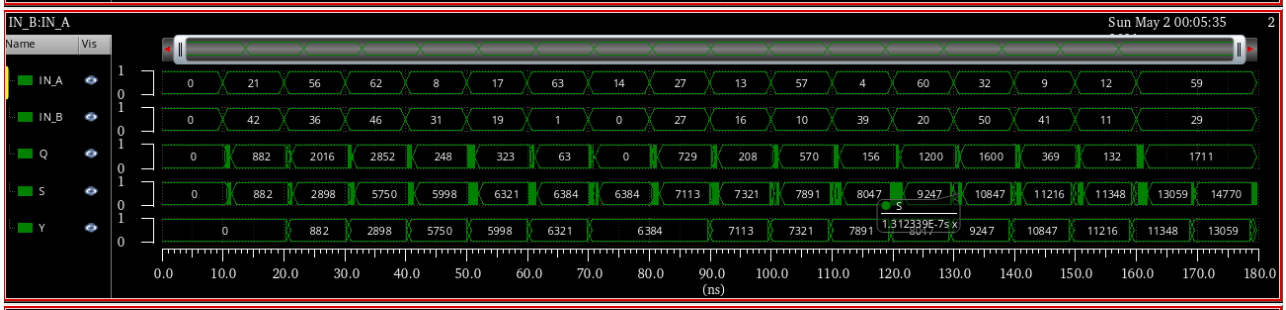
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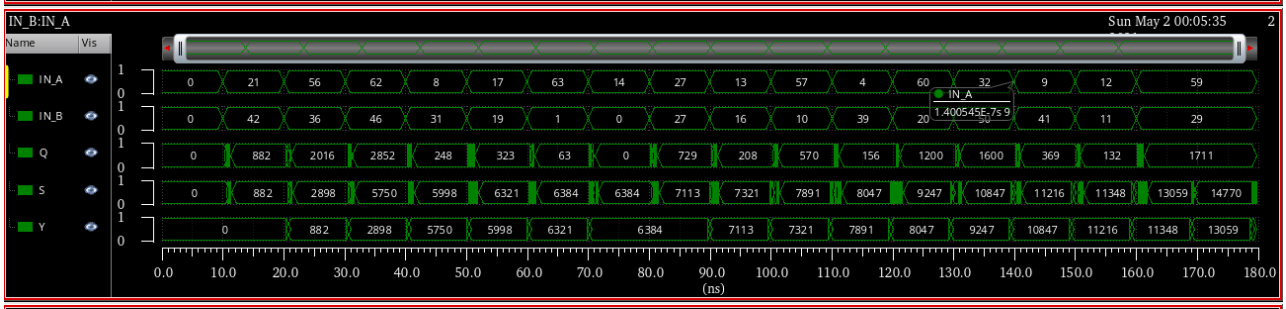
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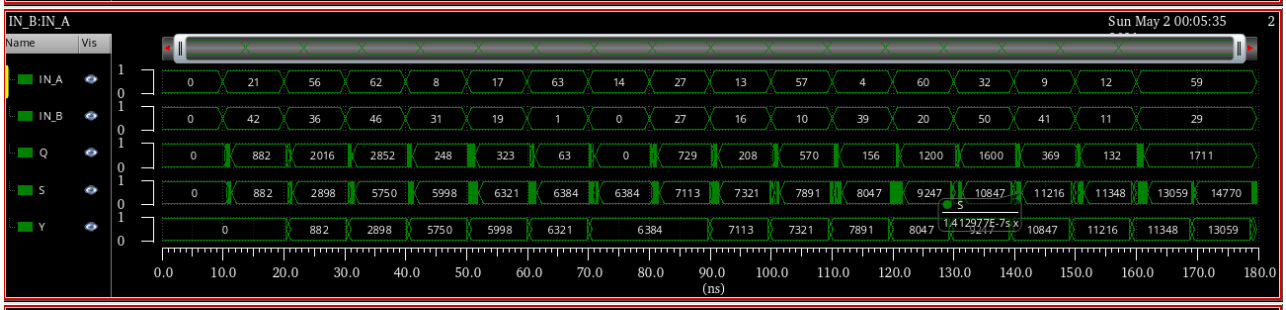
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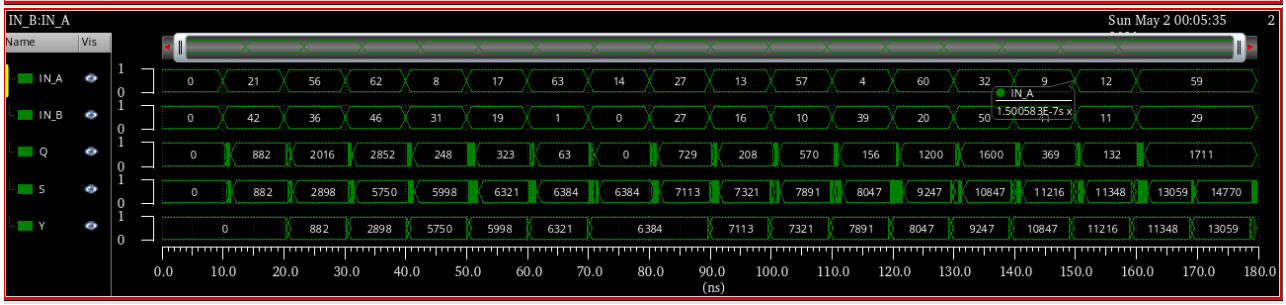
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(ns)

Part-B (d)

Performance Matrices	Value	Unit
Final Area (A-b-v)	128.85*84.9 = 10939.365	(µm×µm)
No of Metal Layer used in Layout	Metal 1, Metal 2, Metal 3, Metal 4, and Metal 5	
Maximum Worst-case Delay (IN_A/IN_B to S)	1.91020	ns
Maximum achievable Clock Frequency	1/9.9ns = 101.01	MHz
Final Area × Delay (clock period)	10939.365*1.91020 = 20896.37502	$\mu m^2 ns$