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RISC vs CISC

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RISC and CISC are two different ways of designing computer processors.

- RISC uses a small set of simple, fixed-size instructions designed to execute in a single clock cycle.
- CISC includes a larger set of instructions, many of which are complex and can perform multiple operations (e.g., memory access and computation) in a single instruction.
- CISC instructions often require multiple clock cycles.
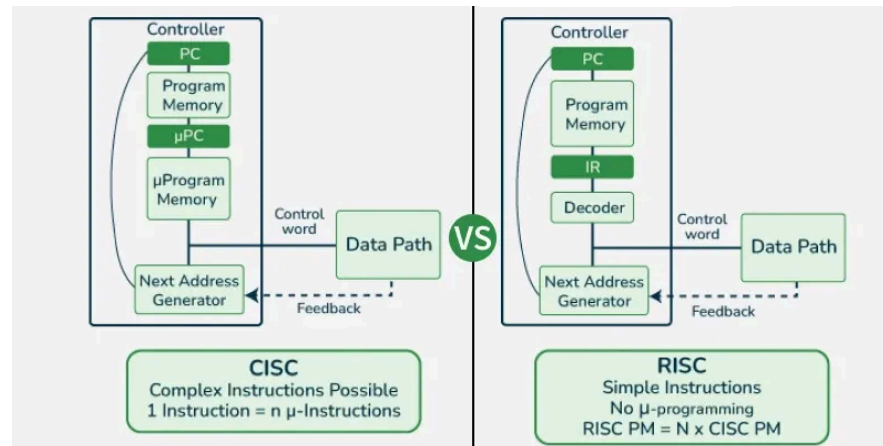
Reduced Instruction Set Architecture (RISC)

RISC simplifies processor design by using a small, uniform set of instructions. Each instruction performs a basic operation (e.g., load, compute, store) and is designed to execute in a single clock cycle, enabling efficient pipelining and simpler hardware.

Characteristics of RISC

- Simpler instruction, hence simple instruction decoding.
- Instruction comes in the form of one word.
- An instruction takes a single clock cycle to get executed.

- More general-purpose registers for register-to-register operations.
- Simple Addressing Modes.
- Optimized for pipelining due to uniform instruction size and simplicity.

Complex Instruction Set Architecture (CISC)

CISC reduces the number of instructions a program needs by using a large set of complex, variable-length instructions. A single instruction can perform multiple operations (e.g., load, compute, and store), which may take multiple clock cycles.

Characteristics of CISC

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decoding.
- Instructions are larger than one-word size.
- Instruction may take more than a single clock cycle to get executed.
- Less number of general-purpose registers as operations get performed in memory itself.
- Complex Addressing Modes.

CPU Performance of RISC and CISC

Both approaches try to increase the CPU performance

$$CPU\ Time = \frac{Seconds}{Program} = \frac{Instructions}{Program} \times \frac{Cycles}{Instructions} \times \frac{Seconds}{Cycle}$$

CPU Time

- **RISC:** Reduce the cycles per instruction at the cost of the number of instructions per program.
- **CISC:** The CISC approach attempts to minimize the number of instructions per program but at the cost of an increase in the number of cycles per instruction.

Earlier when programming was done using assembly language, a need was felt to make instruction do more tasks because programming in assembly was tedious and error-prone due to which CISC architecture evolved but with the uprise of high-level language dependency on assembly reduced RISC architecture prevailed.

Example:

Suppose we have to add two 8-bit numbers:

- **CISC approach:** There will be a single command or instruction for this like ADD which will perform the

task.

- **RISC approach:** Here programmer will write the first load command to load data in registers then it will use a suitable operator and then it will store the result in the desired location.

So, add operation is divided into parts i.e. load, operate, store due to which RISC programs are longer and require more memory to get stored but require fewer transistors due to less complex command.

Comparison Table

RISC and CISC are two processor designs, here is a comparison table between them:

RISC	CISC
Small and simple instruction set	Large and complex instruction set
Fixed-length instructions	Variable-length instructions
Usually 1 cycle per instruction	Multiple cycles per instruction

RISC	CISC
More general-purpose registers	Fewer registers
Simple and limited addressing modes	Complex and many addressing modes
Larger code size (more instructions)	Smaller code size (fewer instructions)
Simple hardware, easier pipelining	Complex hardware, harder pipelining
Examples: ARM, RISC-V, MIPS	Examples: x86, Intel 80386

Suggested Quiz   6 Questions

RISC instructions are generally:

(A) Complex and slow

(B) Single-cycle and fixed length

C   Variable length and multi-cycle

D   Hardwired in cache

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