3rd Sem (CST)

DECEMBER 2024

307/4(N)

3105181

COMPUTER SYSTEM ORGANIZATION

Time Allowed: 3 Hours *Full Marks: 60*

Answer to Question No. 1 of Group A must be written in the main answer script. In Question No. 1, out of 2 marks for each MCQ, 1 mark is allotted for right answer and 1 mark is allotted for correct explanation of the answer.
Answer any Five (05) Questions from Group-B.

GROUP-A

1. Choose the correct answer from the given alternatives and explain your answer (any ten): 2×10=20

   i. The instruction, MOV AX, [2500H] is an example of
   a) immediate addressing mode.
   b) direct addressing mode.
   c) indirect addressing mode.
   d) register addressing mode.

   ii. In a virtual memory system, which of the following can improve the efficiency of address translation?
   a) Larger page size
   b) Smaller page size
   c) Use of Translation Lookaside Buffer (TLB)
   d) Increased RAM size

   iii. Develop a simple assembly language program to add two numbers stored in registers AX and BX, and store the result in CX. Which of the following best represents the steps?
   a) MOV AX, BX; ADD CX, AX
   b) MOV CX, AX; ADD CX, BX
   c) MOV AX, CX; ADD AX, BX
   d) MOV BX, CX; ADD AX, CX

   iv. Which of the following is a challenge that arises in a RISC pipeline architecture?
   a) Hazard detection and resolution
   b) Fetching multiple instructions per cycle
   c) Reducing the instruction set
   d) Supporting a large instruction set

   v. If a floating-point number uses 8 bits for the exponent and 23 bits for the mantissa, what is the precision limit for numbers represented by this format?
   a) Approximately 16 decimal digits
   b) Approximately 6-7 decimal digits
   c) Approximately 12 decimal digits
   d) Approximately 3-4 decimal digits

vi. What is the hit ratio in cache memory?
a) Ratio of cache size to main memory size
b) Number of cache hits divided by total memory accesses
c) Ratio of cache misses to total memory accesses
d) Ratio of cache speed to main memory speed

vii. In Intel 8086, which addressing mode uses the combination of a register and a displacement value?
a) Immediate Addressing
b) Direct Addressing
c) Register Indirect Addressing
d) Base-Indexed Addressing

viii. What is the main characteristic of the Von-Neumann architecture?
a) Separate memory for data and instructions
b) Shared memory for data and instructions
c) No memory hierarchy
d) Direct connection between CPU and memory

ix. Which of the following is responsible for address sequencing in a microprogrammed control unit?
a) Instruction Register
b) Control Memory
c) Arithmetic Logic Unit
d) Program Counter

x. What is the word size of the Intel 8086 microprocessor?
a) 8-bit
b) 16-bit
c) 32-bit
d) 64-bit

xi. In a pipeline architecture, which stage comes immediately after Instruction Fetch?
a) Decode
b) Execute
c) Memory Access
d) Write Back

xii. What is the function of cache memory in a computer system?
a) To store the operating system
b) To store frequently accessed data
c) To increase the size of RAM
d) To serve as backup storage

xiii. Which of the following micro-operations can combine two binary values?
a) Arithmetic micro-operation
b) Shift micro-operation
c) Logic micro-operation
d) Memory transfer

xiv. Which of the following is NOT a valid step in Booth's multiplication algorithm?
a) Add multiplicand
b) Shift right
c) Invert the result
d) Subtract multiplicand

GROUP-B
Answer any Five (05) questions.

2. Explain Von Neumann architecture. Discuss the various types of Addressing Modes of Intel 8086. 4+4
3. Explain Restoring Division Algorithm for Unsigned Integer. Multiply the (-9) with (-13) using booth's algorithm. 4+4
4. Explain 8086 internal architecture. Explain different types of interrupts. 5+3
5. Calculate the number of page faults for the following reference string with frame size as 3 by using a) LRU and FIFO page replacement algorithm. 5,0,2,1,0,3,0,2,4,*3,0,3,2,1,3,0,1,5.* 4+4
6. Compare between direct mapped, set associative and associative cache. Differentiate between write through and write back cache. https://www.wbscteonline.com 5+3

7. Differentiate between fixed point and floating-point representation. Represent -75 as 8-bit 2's complement number. What is Direct Memory Access(DMA)? 3+2+3
8. Explain Pipelining. Discuss different kinds of hazard occurs in pipelining. 3+5
9. Short Note (any two): 4+4
   a) Vector Processor
   b) RISC Pipeline
   c) Cache hit and cache miss