JANUARY 2024

COMPUTER SYSTEM ORGANIZATION

Time Allowed: 2.5 Hours *Full Marks: 60*

Answer to Question No. 1 of Group A must be written in the main answer script.
In Question No. 1, out of 2 marks for each MCQ, 1 marks is allotted for right answer and 1 marks is allotted for correct explanation of the answer.
Answer any Five (05) Questions from Group-B.

GROUP-A

1. Choose the correct answer from the given alternatives and explain your answer (any ten): 2x10=20

i) Von Neumann architecture is based on_____.
a) SISD b) SIMD c) MISD d) MIMD

ii) Example for zero address instructions is _____.
a) push b) load A c) move R1, A d) store x.

iii) What is the full form of TLB ?
a) Translation Loop Buffer b) Translation Look- aside Buffer c) Time Loop Block d) None

iv) What is Page Map Table ?
a) It maps the virtual addresses to physical addresses
b) It maps physical addresses to virtual addresses
c) It maps the virtual addresses to Logical addresses
d) Support all the above

v) The result of **MOV AL, 65** is to store
a) 0100 0010 in AL b) 42H in AL c) 40H in AL d) 0100 0001 in AL

vi) Which of the following is page fault?
a. Page fault occurs when a program accesses a page of another program
b. Page fault occurs when a program accesses a page in main memory
c. Page fault occurs when there is an error in particular page
d. Page fault occurs when a program accesses a page which is not present in main memory

vii) Which of the following are the two main components of the CPU?
a) CU and registers b) Registers and main memory c) CU and ALU d) Registers and ALU.

viii) The term that provides simultaneous data processing tasks are_____.
a) parallel processing b) array processing c)vector processing d) distributed processing.

ix) A 16 x 8 Organisation of memory cells, can store upto _____
a) 256 bits b) 1024 bits c) 512 bits d) 128 bits

x) A processor can access a memory location by 32 bits. Then find the total memory size if all memory locations are available to the processor.
a. 4 GB
b. 4 Gb
c. 2 GB
d. 4 MB

xi) Data transfer from Cache Memory to Processor is _____

a) Word by Word b) Block by Block c) Block by Word d) Word by Block

xii)) In which of the following term the performance of cache memory is measured?

a. Chart ratio
b. Hit ratio
c. Cache ratio
d. Data ratio

xiii) Which of these is NOT involved in the case of a memory write operation?

a) Data bus b) MDR c) MAR d) PC

xiv) Which of the following memory unit communicates directly with the CPU?

a. Auxiliary memory
b. Main memory
c. Secondary memory
d. None of the above

xv) A computer system supports 2^{46} logical addresses and 2^{11} addresses per page. How many pages can be represented in secondary memory (virtual memory address space) ?

a) 35 b) 2^{35} c) 2^{25} d) 2^{57}

GROUP-B

Answer any Five (05) questions.

2. a) Draw the Von Neumann basic structure and mark all its components.
   b) Draw and explain the BUS architecture of a digital computer ? 4+4

3. a) Explain the basic instructions cycle with appropriate diagram.
   b) Write the Zero address instructions to evaluate the arithmetic statement X= (A+B) *(C+D) 4+4

4. a) Write the difference between Minimum Mode and Maximum Mode in 8086 Microprocessor.
   b) Explain with example any four addressing modes available in 8086 microprocessors. 4+4

5. a) Write the different cache mapping techniques and explain it.
   b) A typical computer system cache memory access time is 8 ns and its main memory access time is 80 ns. If hit ratio is 90%, what is the average memory access time? 4+4

6. a) Write the difference between CISC & RISC Architecture.
   b) Write short notes on any one: i) DMA ii) Virtual Memory 4+4

7. a) What is biased exponent of floating-point number?
   b) Discuss in detail the architecture of 8086 microprocessor along with pin configuration diagram. 2+6

8. a) Explain the different groups of computers according to Flynn's classification.
   b) Write down the IEEE-754 format for single and double precision numbers? 4+4

9. a) Describe the concept of Pipeline and its types?
   b) Write the different types of pipeline hazards. 4+4
