//2022//

////short////

1.How control unit controls other units?
>>A CU typically uses a **binary decoder** to convert coded instructions into timing and control signals that direct the operation of the other units.
2. Give an example of a 4 bit, 8bit, 16-bit, and 32 bit microprocessor.
>>A PC or Macintosh has a **32-bit microprocessor**; microwave ovens generally have an **8-bit processor**, and a TV remote control is likely to use a **4-bit processor**. The average late-model car includes about a dozen **16-bit microprocessors.**
3. What is Bus?
>>A bus is a fundamental component of computer architecture, providing a pathway for the transfer of data, addresses, and control signals between the various components of the system, ensuring that they can communicate effectively.
4. What is MAR and MDR?
>>The MAR holds the address of the next item of data that is needed by the processor. The MDR holds data that is either to be passed to the data bus or has just been received from the data bus.
5. What is register?
A **register** is a small, fast storage unit within the CPU that temporarily holds data, instructions, or memory addresses that are actively being processed.
6. What is interrupt?
>>An **interrupt** is a signal that causes the CPU to temporarily halt its current execution and redirect its attention to handle an event, such as hardware or software requests.
7. What is non-volatile memory?
>>Non-volatile memory (NVM) is a type of computer memory that retains stored information even after power is removed.
8. What is logical address?
>>A **logical address**, also known as a **virtual address**, is an address generated by the CPU during the execution of a program. It is the address seen by the process and is relative to the program's address space.
9. Which is an error-detecting code?
>>Error-detecting codes are a sequence of numbers generated by specific procedures for detecting errors in data that has been transmitted over computer networks.
10. What is the logic shift?
>>A **logical shift** is a **bitwise operation** that shifts all the bits of its operand.
11. What type of device converts digital signal into a form that is intelligible to the user?
>> An **output device** reverses the process, translating the digitized signals into a form intelligible to the user.
12. Define clock rate.
>>It is a **measure of how fast a computer's central processing unit (CPU) can execute instructions**
13. Which memory stores instruction which is required to start a computer?
>>The memory that stores the instructions required to start a computer is called ROM (Read-Only Memory).

14. What is the RAID system?

>>**RAID (redundant array of independent disks) is a way of storing the same data in different places on multiple hard disks or solid-state drives (SSDs) to protect data in the case of a drive failure**

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15. at are the three main elements of the control unit?

>> The main elements of the control unit are the decoder, timer/clock, and control logic circuits.

16. w**hat is Cache memory? what is control memory address?**

>>Cache memory is a small, high-speed storage area in a computer that stores frequently accessed data and instructions.

The Control memory address register specifies the address of the micro-instruction. The Control memory is assumed to be a ROM, within which all control information is permanently stored.

17.What is the 2's complement representation of -67?

- **>>67** in binary (8-bit) = **01000011**.
- **-67** in 2's complement (8-bit) = **10111101**

18.What is clock signal in COA?

>>In computer organization and architecture, a **clock signal is an electrical pulse that serves as the timing reference for transmission of data**.

19. USB is a bus?

>> Yes, **USB (Universal Serial Bus)** is indeed a type of **bus**. Specifically, it is a **serial bus** that is widely used for connecting various peripherals to a computer or other host devices.

20. What do you mean by the write-back policy?

>>The **write-back policy** is a **cache memory management strategy** used in computer systems to manage the process of writing data from the **cache** back to the **main memory (RAM)**. In this policy, data is **written to the main memory only when it is evicted from the cache**, not immediately after a write operation occurs in the cache.

21.Wat is RISC Pipeline?

>>The **RISC (Reduced Instruction Set Computing) pipeline** refers to the process of executing instructions in a **RISC-based processor** through multiple stages, where each stage performs a specific part of the instruction execution.

22. That size of MUXs are needed?

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