UG-5664ASYDF01

Evaluation Kit User Guide

Writer:

Email:

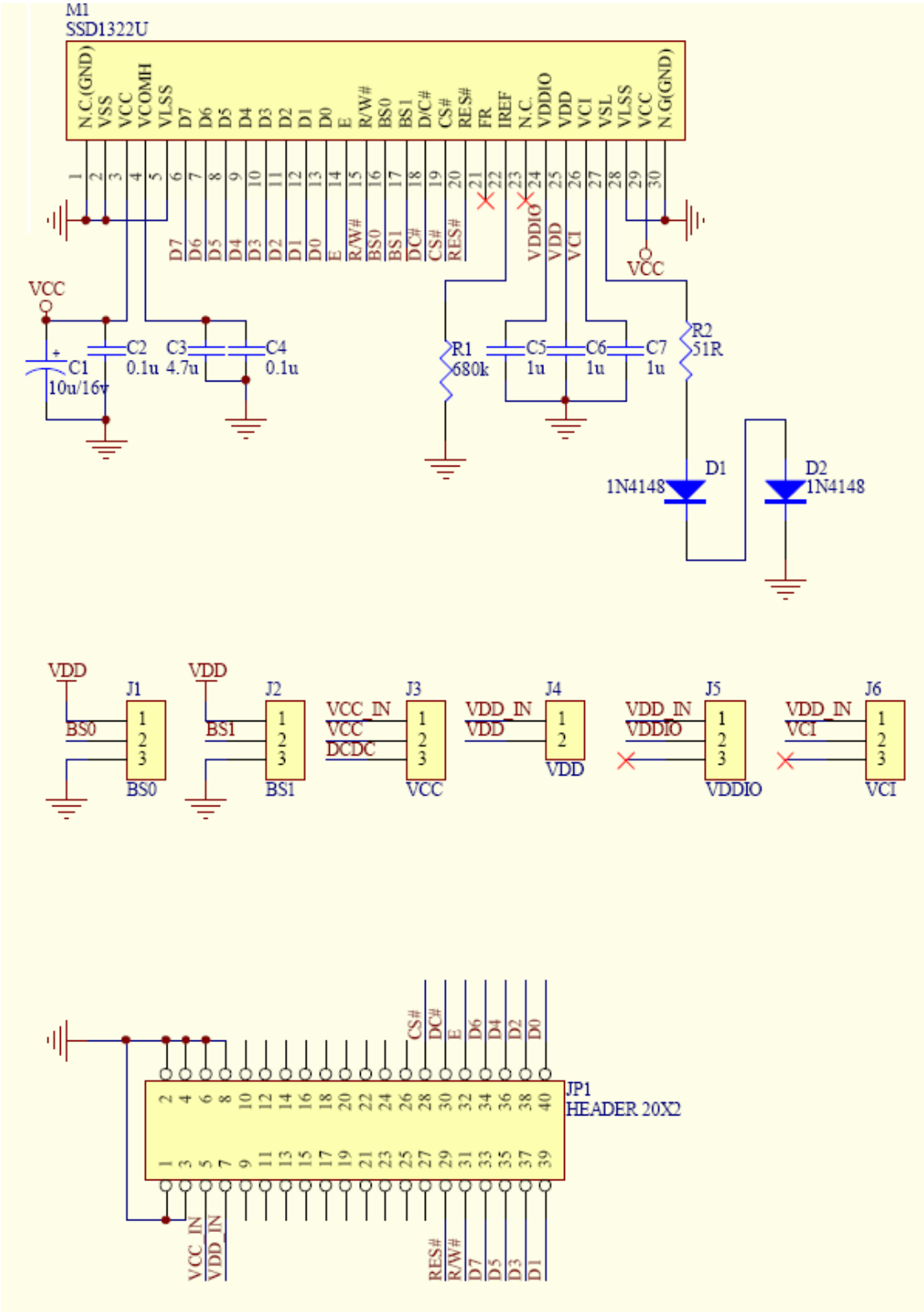
Version: Preliminary

Contents

1.REVISION HISTORY

Date	Page	Contents	Version
200X/XX/XX		Preliminary	Preliminary 0.0

2.EVK Schematic



3.Symbol define

D0-D7：These pins are bi-directional data bus connecting to the MCU data bus.
Unused pins are recommended to tie LOW. (Except for D2 pin in SPI mode)

E/RD#：This pin is MCU interface input.
When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected.
When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected.
When serial interface is selected, this pin E(RD#) must be connected to V_{SS}.

W/R# : This pin is read / write control input pin connecting to the MCU interface.
When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW.
When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected.
When serial interface is selected, this pin R/W (WR#) must be connected to V_{SS}.

D/C# : This pin is Data/Command control pin connecting to the MCU.
When the pin is pulled HIGH, the content at D[7:0] will be interpreted as data.
When the pin is pulled LOW, the content at D[7:0] will be interpreted as command.

RES# : This pin is reset signal input.
When the pin is pulled LOW, initialization of the chip is executed.
Keep this pin pull HIGH during normal operation.

CS# : This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

BS0/BS1 : These pins are MCU interface selection input. See the following table:

BS[1:0]	Bus Interface Selection
00	4 line SPI
01	3 line SPI
10	8-bit 8080 parallel
11	8-bit 6800 parallel

VCC : This is the most positive voltage supply pin of the chip. It can be supplied externally or generated internally by using internal DC-DC voltage converter.

VDD : This is a voltage supply pin. It must be connected to external source.

VDDIO : Power supply for interface logic level. It should be matched with the MCU interface voltage level.

VCI : Low voltage power supply.
V_{CI} must always be equal to or higher than V_{DD} and V_{DDIO}.

VSS : This is a ground pin. It also as a reference for the logic pins and the OLED driving voltages. It must be connected to external ground.

NC : These pins should be left open individually.

4.TIMMING CHARACTERISTICS

4.1 80-Series MPU parallel Interface

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Table 1 80-Series MPU parallel Interface Timing Characteristics

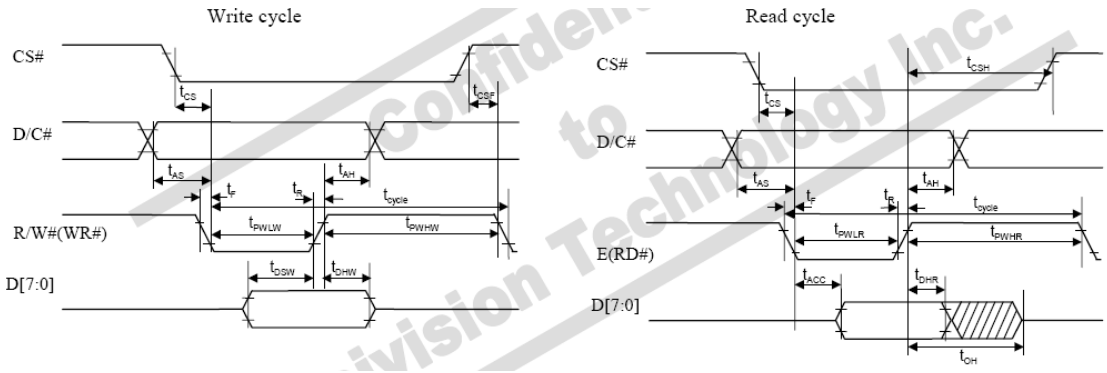


Figure 1 80-Series MPU parallel Interface Timing Diagram

4.2 6800-Series MPU parallel Interface

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Table 1 80-Series MPU parallel Interface Timing Characteristics

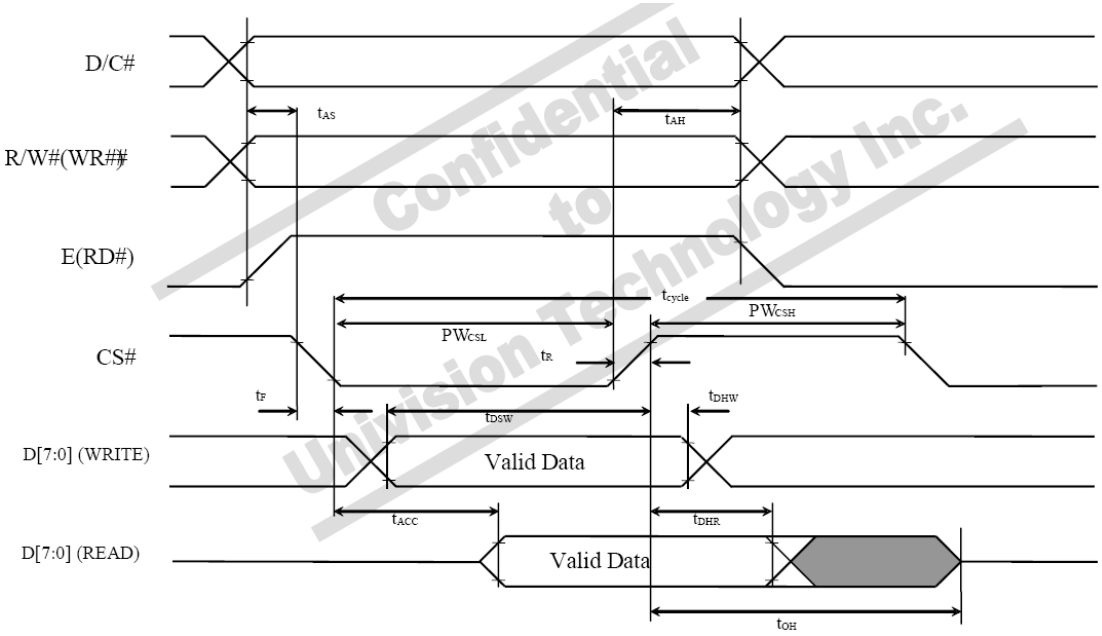


Figure 1 80-Series MPU parallel Interface Timing Diagram

4.3 SPI(4-wire)-Series MPU parallel Interface

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Table 1 SPI(4-wire)-Series MPU parallel Interface Timing Characteristics

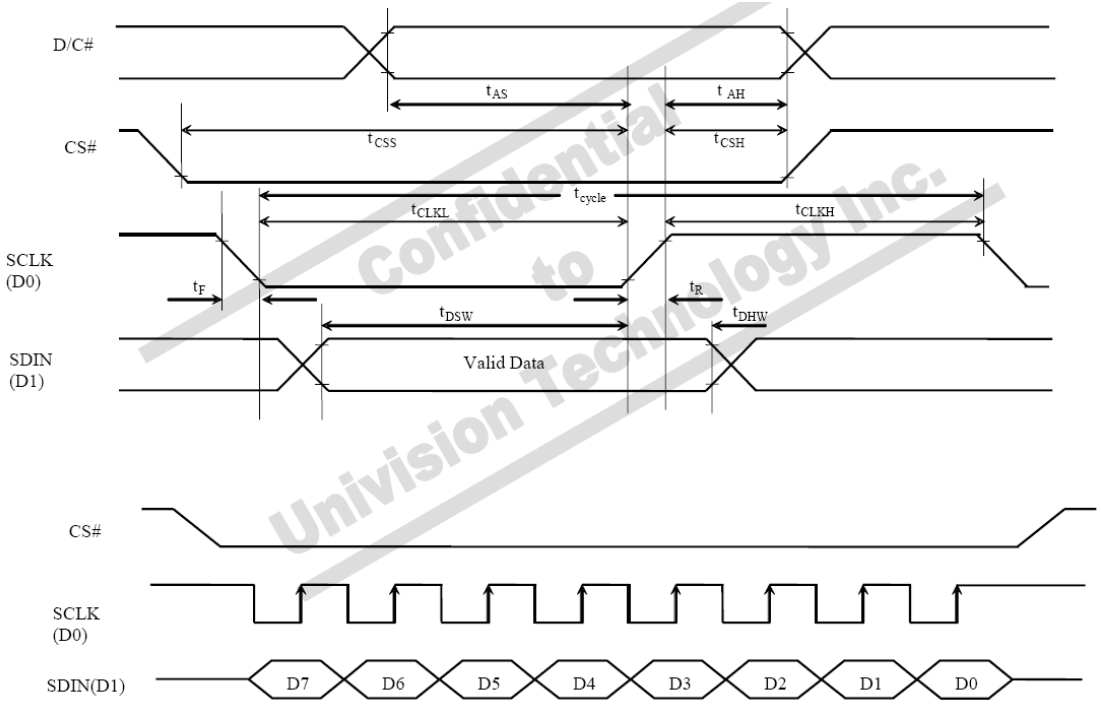


Figure 1 SPI(4-wire)-Series MPU parallel Interface Timing Diagram

4.4 SPI(3-wire)-Series MPU parallel Interface

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Table 1 SPI(3-wire)-Series MPU parallel Interface Timing Characteristics

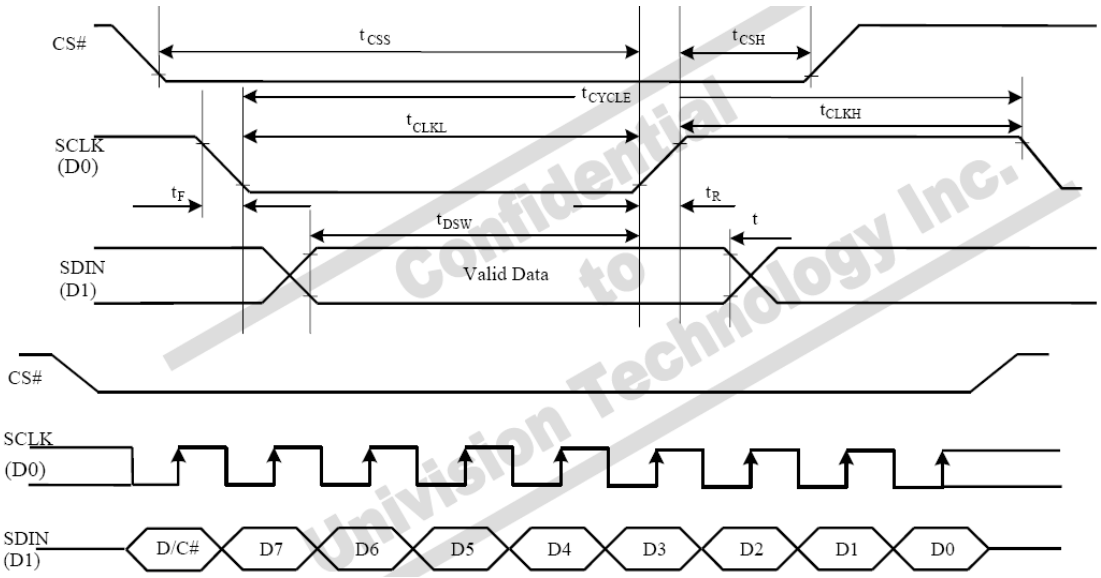


Figure 1 SPI(4-wire)-Series MPU parallel Interface Timing Diagram

5.EVK use introduction

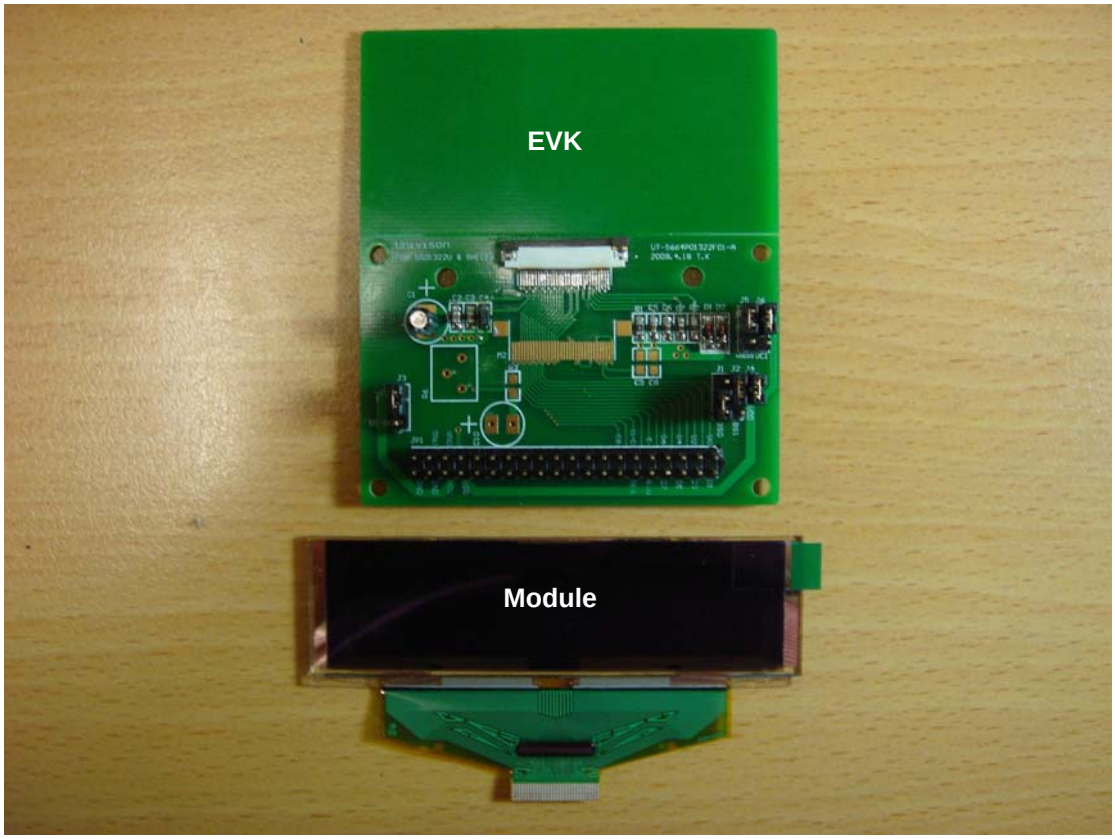


Figure 5 EVK PCB and OLED Module

UG-5664ASYDF0101 is (COF) type module, please refer to Figure 5, Figure 6.User can use leading wire to connect EVK with customer's system. The example shows as Figure 7.

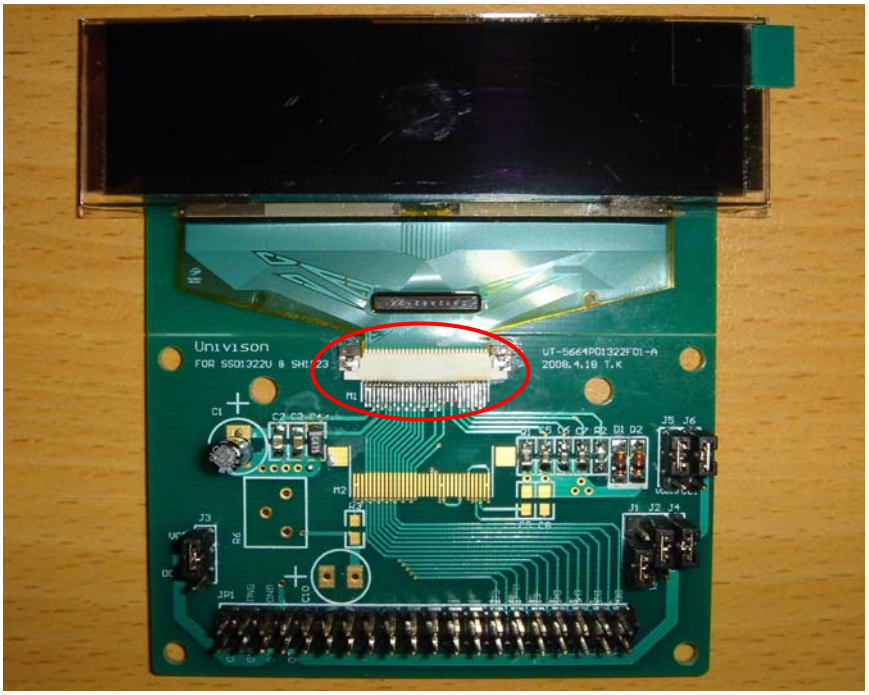


Figure 6 The combination of the module and EVK

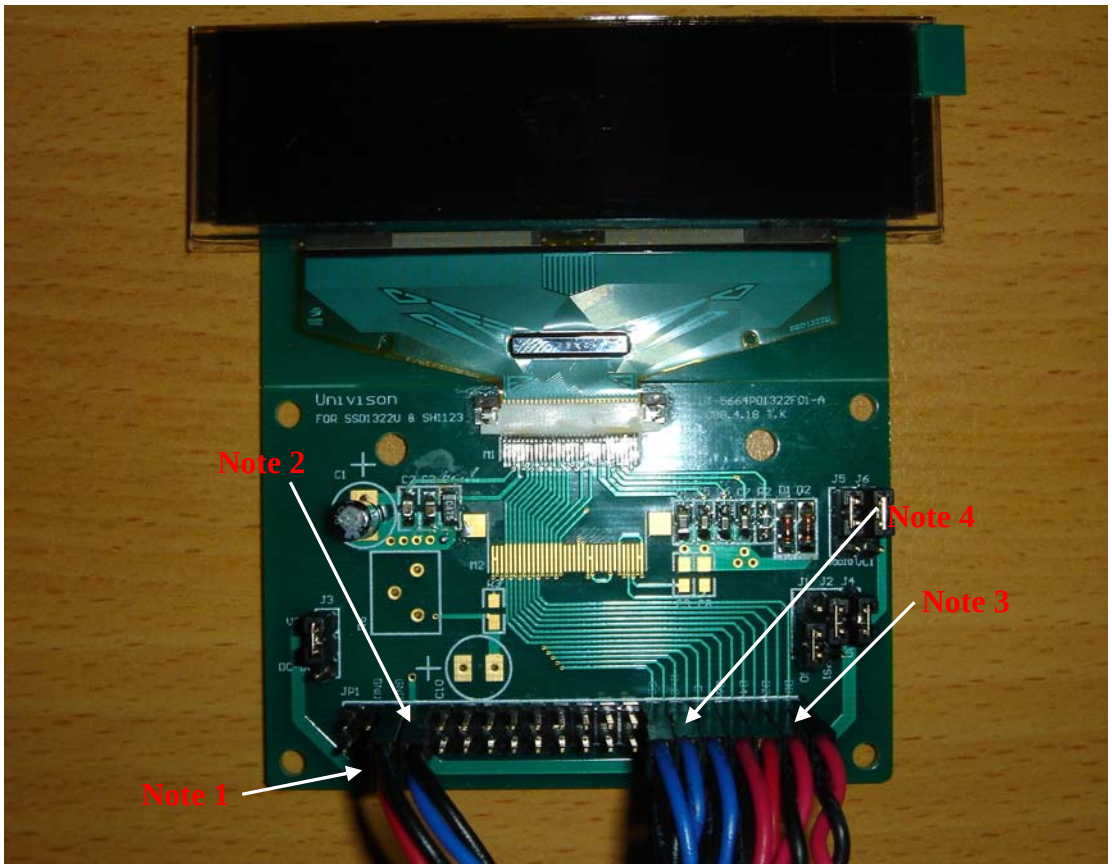


Figure 7 EVK with test platform

Note 1：It is OLED high voltage supply.

Note 2：It is logic voltage supply.

Note 3：Those are leading wire connect to control board. Those are data pin.(D0-D7)

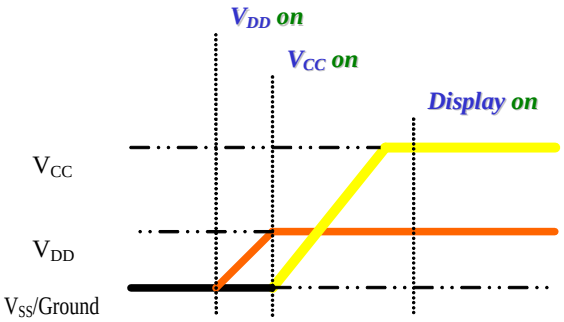
Note 4：Those are leading wire connect to control board. Those are control pin.
(E,R/W,D/C,RES,CS)

6.Power down and Power up Sequence

To protect OLED panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. Such that panel has enough time to charge up or discharge before/after operation.

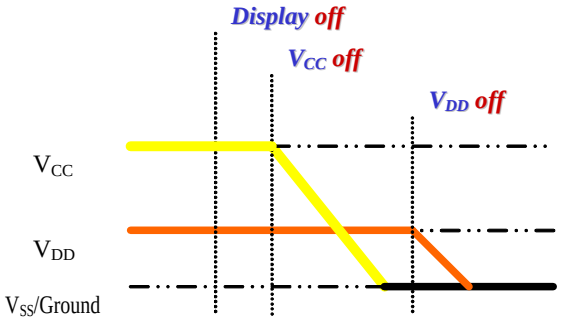
Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Driver IC Initial Setting
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
   (when V_{CC} is stable)
7. Send Display on command



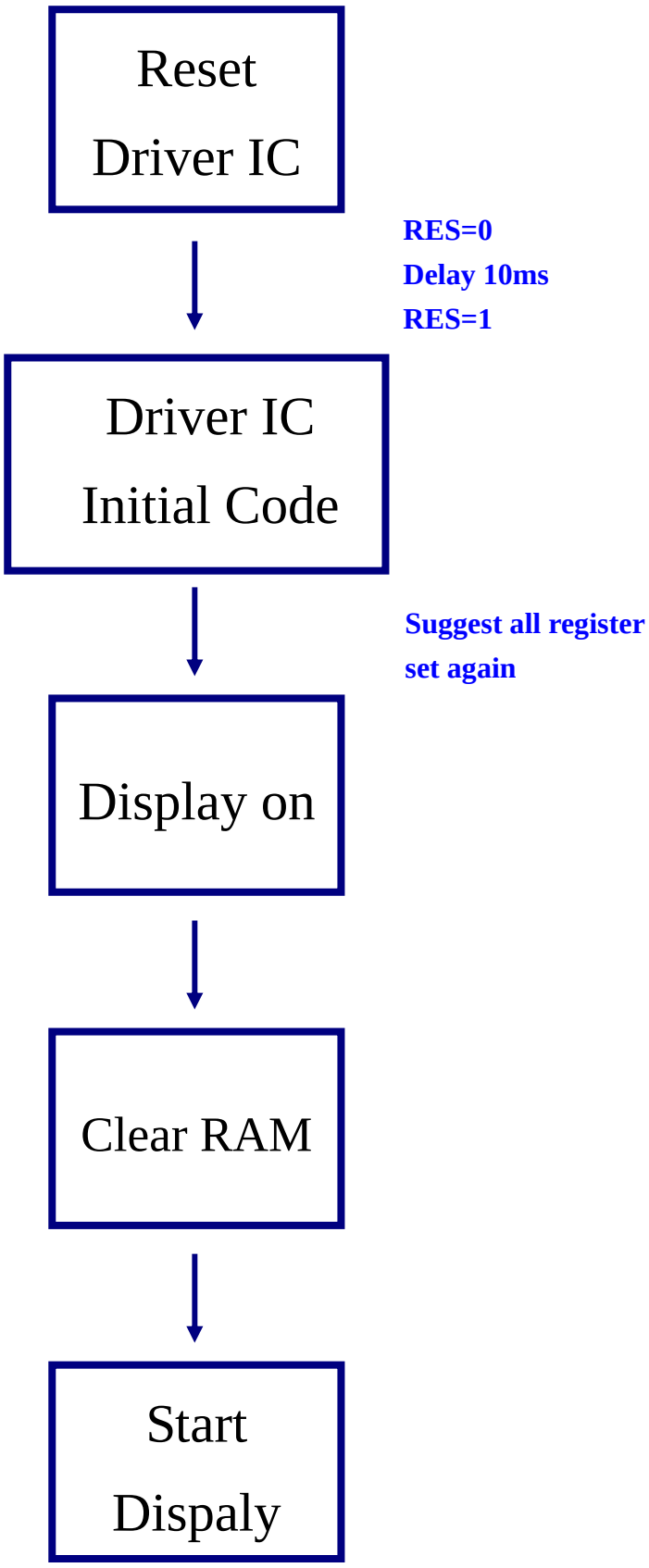
Power down Sequence:

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
   (when V_{CC} is reach 0 and
   panel is completely
   discharges)
4. Power down V_{DD}



7.How to use SSD1322 module

7.1 Initial Step Flow



7.2 RD recommend Initial Code for 80 Interface: