### **Features**

- Logic AND/NAND input
- 3V and 5V Input compatible
- Clocking speeds up to 20 MHz
- 20 ns Switching/delay time
- 2A Peak drive
- Isolated drains
- Low output impedance
- Low quiescent current
- Wide operating voltage— 4.5V-16V

### **Applications**

- CCD Drivers
- Short circuit protected switching
- Under-voltage shut-down circuits
- Switch-mode power supplies
- Motor controls
- Power MOSFET switching
- Switching capacitive loads
- Shoot-thru protection
- Latching drivers

### **Ordering Information**

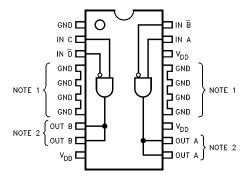
Part No.	Part No. Temp. Range		Outline #	
EL7243CM	−40°C to	20-Lead	MDP0027*	
	+85°C	Thermal SO	L	

### **General Description**

The EL7243C dual input, 2-channel driver achieves the same excellent switching performance of the EL7212 family while providing added flexibility. The power package makes this part extremely well suited for high frequency and heavy loads as in CCD applications. The 2-input logic and configuration is applicable to numerous power MOSFET drive circuits. As with other Elantec drivers, the EL7243C is excellent for driving large capacitive loads with minimal delay and switching times. "Shoot-thru" protection and latching circuits can be implemented by simply "cross-coupling" the 2-channels.

### **Connection Diagram**

### 20-Lead Thermal SOL Package EL7243C



7243-1

Note 1: Pins 4-7 and 14-17 are electrically connected. Note 2: Output pins must be tied together.

Manufactured under U.S. Patent Nos. 5,334,883, #5,341,047

## **EL7243C**

## Dual Input, High Speed, Dual Channel CCD Driver

### **Absolute Maximum Ratings**

16.5V Supply (V + to Gnd) 125°C Operating Junction Temperature

-0.3V to +0.3V above  $V^+$ Input Pins Power Dissipation

Combined Peak Output Current 20-pin "Batwing" SOIC 1500 mW

Storage Temperature Range  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ 

Ambient Operating Temperature  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ 

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore  $T_J = T_C = T_A$ .

Test Procedure

T 100% production tested and QA sample tested per QA test plan QCX0002.  $\mathbf{II}$ 

 $100\,\%$  production tested at  $T_{\rm A}=25^{\rm o}{\rm C}$  and QA sample tested at  $T_{\rm A}=25^{\rm o}{\rm C}$  ,

 $T_{\mbox{\footnotesize MAX}}$  and  $T_{\mbox{\footnotesize MIN}}$  per QA test plan QCX0002. III QA sample tested per QA test plan QCX0002.

IVParameter is guaranteed (but not tested) by Design and Characterization Data.

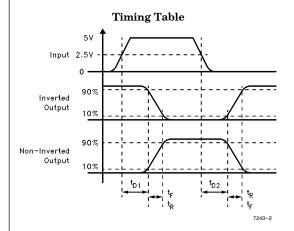
Parameter is typical value at  $T_A = 25^{\circ} C$  for information purposes only.

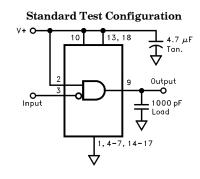
### DC Electrical Characteristics T<sub>A</sub> = 25°C, V<sub>DD</sub> = 15V unless otherwise specified

Parameter	Description	Test Conditions	Min	Тур	Max	Test Level	Units
Input							
$V_{IH}$	Logic "1" Input Voltage		2.4			I	v
$I_{IH}$	Logic "1" Input Current	@V <sub>DD</sub>		0.1	10	I	μΑ
$V_{IL}$	Logic "0" Input Voltage				0.8	I	v
$I_{\mathrm{IL}}$	Logic "0" Input Current	@0V		0.1	10	I	μΑ
V <sub>HVS</sub>	Input Hysteresis			0.3		v	v
Output							
R <sub>OH</sub>	Pull-Up Resistance	$I_{OUT} = -100 \text{ mA}$		3	6	I	Ω
R <sub>OL</sub>	Pull-Down Resistance	$I_{OUT} = +100 \text{ mA}$		4	6	I	Ω
$I_{PK}$	Peak Output Current	Source Sink		2 2		IV	A
$I_{DC}$	Continuous Output Current	Source/Sink	200			I	mA
Power Supply							
I <sub>S</sub>	Power Supply Current	Inputs High		1	2.5	I	mA
V <sub>S</sub>	Operating Voltage		4.5		16	I	V

# EL7243C Dual Input, High Speed, Dual Channel CCD Driver

AC Electrical Characteristics $\tau_A = 25^{\circ}$ C, $V = 15$ V unless otherwise specified							
Parameter	Description	Test Conditions	Min	Тур	Max	Test Level	Units
Switching Chara	cteristics						
t <sub>R</sub>	Rise Time	$egin{aligned} C_{ m L} &= 500 \  m pF \ C_{ m L} &= 1000 \  m pF \end{aligned}$			10 20	IV	ns
t <sub>F</sub>	Fall Time	$C_{L} = 500 \text{ pF}$ $C_{L} = 1000 \text{ pF}$			10 20	IV	ns
t <sub>D-ON</sub>	Turn-On Delay Time			20	25	IV	ns
t <sub>D-OFF</sub>	Turn-Off Delay Time			20	25	IV	ns





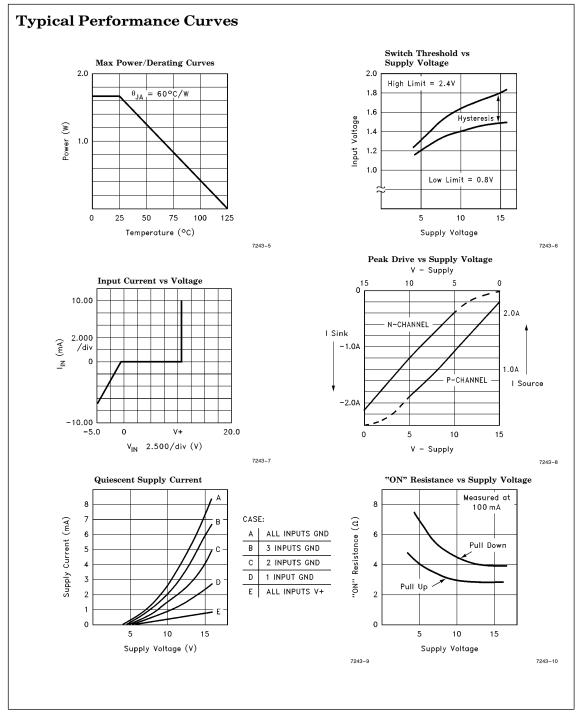
7243-3

Pins 19, 20 connected to  $V^{+}$ .

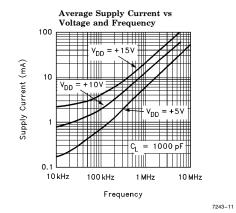
# Simplified Schematic Output Input Buffer I Inverting Buffer w/ Hysteresis Super Inverter Reference & Level Shifter Logic Gate

# EL7243C

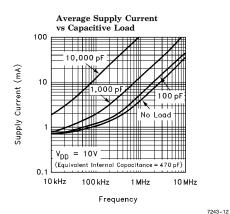
### Dual Input, High Speed, Dual Channel CCD Driver

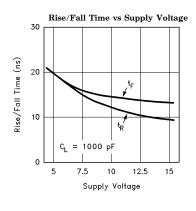


### Typical Performance Curves - Contd.



Rise/Fall Time vs Load 100 80 Rise/Fall Time (ns) 60 40 20 100 1,000 10,000 Load Capacitance (pF)

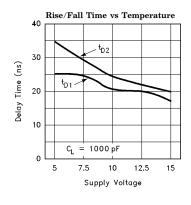


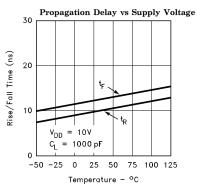


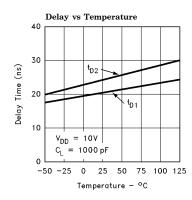
7243-14

# EL7243C Dual Input, High Speed, Dual Channel CCD Driver

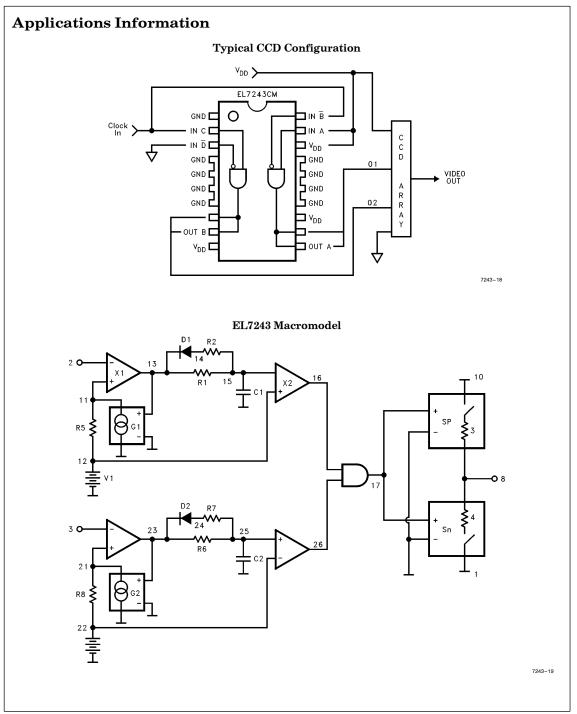
### Typical Performance Curves — Contd.







# EL7243CDual Input, High Speed, Dual Channel CCD Driver



## **EL7243C**

### Dual Input, High Speed, Dual Channel CCD Driver

### EL7243 Macromodel

```
* EL7243 Macromodel
* Revision A, January 1996
* Connections
                           Gnd
                                 {\bf Inp}\,+\,
                                       Inp-
                                              out
                                                     v_{cc}
.subckt M7243
                                                     10
V1 12 1 1.6
R1 13 15 1k
R2 14 15 5k
R5 11 12 100
C1 15 1 43.3pF
D1 14 13 dmod
X1 13 11 2 1 comp1
X2 16 12 15 1 comp1
V2 22 1 1.6
R6 23 25 1K
R7 24 25 5K
R8 21 22 100
C2 25 1 43.3pF
D2 24 23 dmod
X3 23 21 3 1 comp1
X4 26 25 22 1 comp1
X5 16 26 17 1 And-gate
sp 10 8 17 1 spmod
sn 8 1 17 1 snmod
g1 11 1 13 1 938u
g2 21 1 23 1 938u
.model dmod d
.model spmod vswitch ron = 3 \text{ roff} = 2 \text{meg von} = 1 \text{ voff} = 1.5
.model snmod vswitch ron = 4 roff = 2meg von = 3 voff = 2
.ends M7243
* AND Gate Subcircuit*
.subckt And-gate inp1 inp2 out-AS Vss-A
el out-A Vss-A table \{v(inp1)^*v(inp2)\} = (0, 3.2) (3.2, 0)
Rout-a out-a vss-a 10 meg
rinpa inp1 vss-a 10 meg
rinpb inp2 vss-a 10 meg
.ends and-gate
^{\ast} Comparator Subcircuit ^{\ast}
.subckt comp1 out inp inm vss
el out vss table \{(v(inp)-v(inm))^*5000\} = (0,0) (3.2, 3.2)
Rout out vss 10meg
Rinp inp vss 10meg
Rinm inm vss 10meg
```

.ends omp1

### General Disclaimer

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January 1996 Rev B