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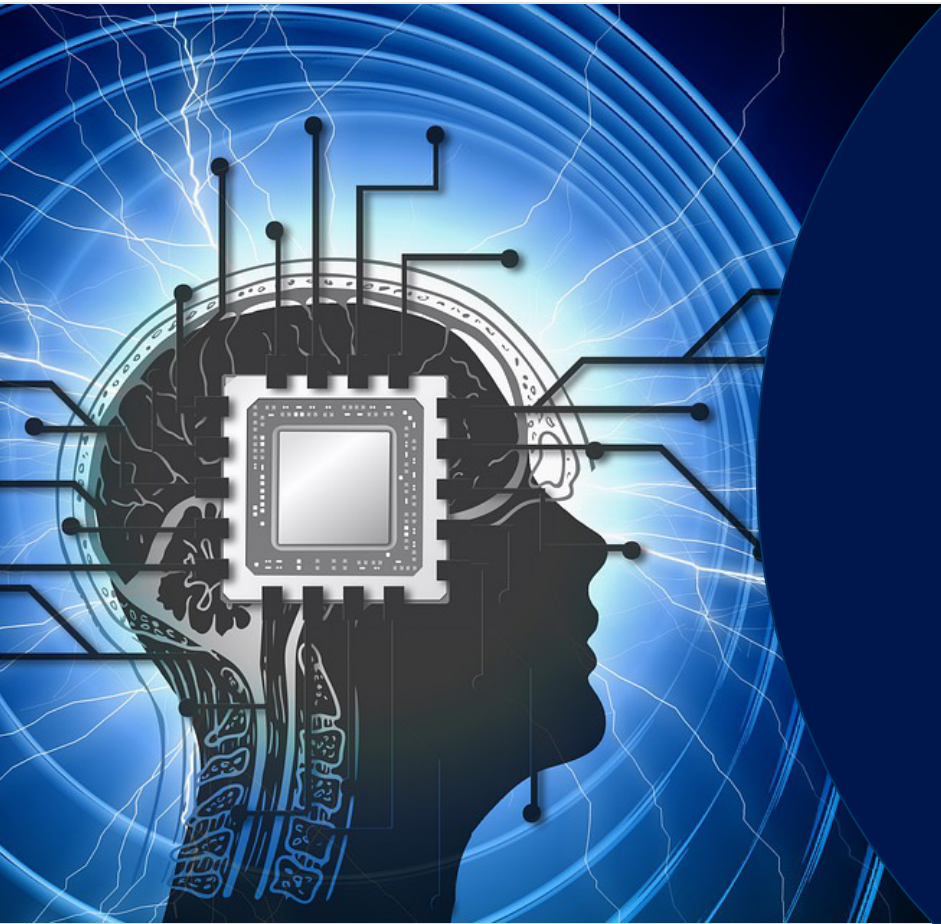
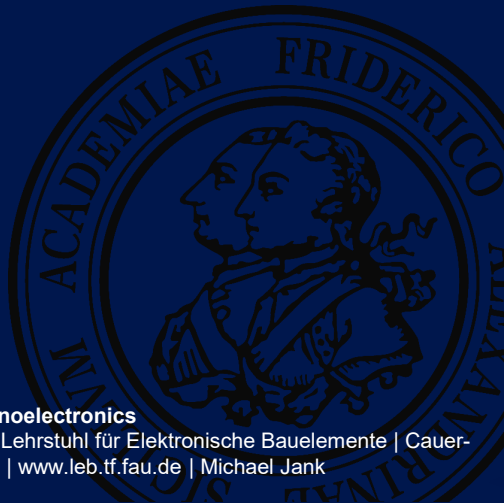


Halbleitertechnik IV- Nanoelectronics

Friedrich-Alexander-Universität Erlangen-Nürnberg | Lehrstuhl für Elektronische Bauelemente | Cauerstraße 6 | 91058 Erlangen | www.leb.tf.fau.de | Michael Jank

Scaling of MOSFETs



Halbleitertechnik IV - Nanoelectronics
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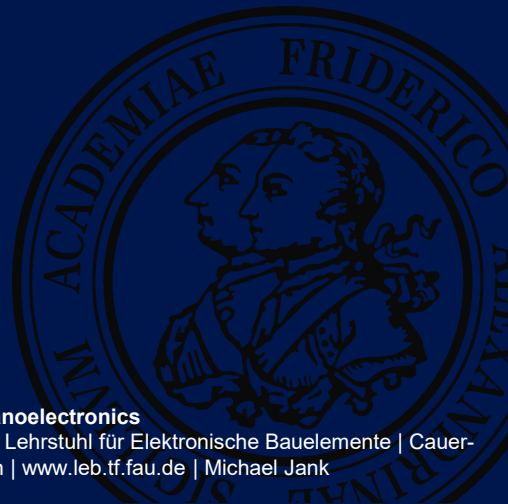
Objectives of the lecture

Mission and goals?



Scaling of MOSFETs

Objectives

- To know the different approaches for dimensional scaling in MOS technology and the reasons behind

- for the well defined schemes of constant-voltage and constant-field scaling you should be aware of the respective rules and

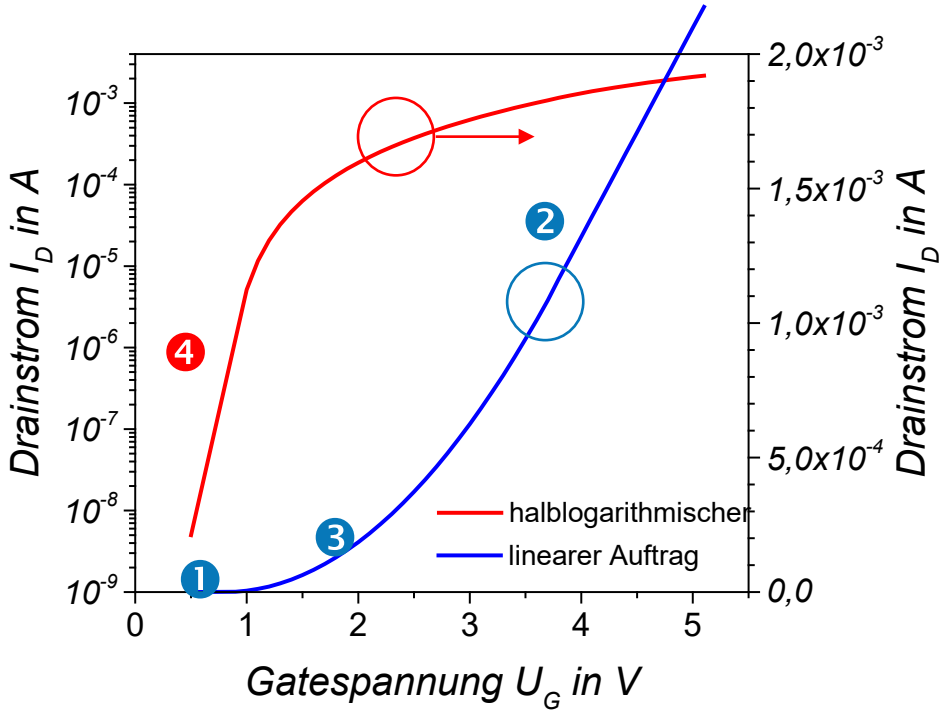
- the effects on the device behavior, especially the electrical fields and currents and critical device parameters

Nanoelectronics – Scaling of MOSFETs
Key parameters

- Most important circuit-related parameters of MOSFET
  - *threshold voltage* U_{Th}
  - *areal oxide capacity* C_{IS}
  - *(charge) carrier mobility* μ
  - *body effect coefficient* γ
  - *subthreshold swing S*
  - *transconductance* g_m *or* β
- Important technology criteria af MOSFETs
  - *channel length L*
  - *channel width W*
  - *substrate and well doping* $N_{A,D}$
  - *gate oxide thickness* d_{IS}
  - *junction depth of S/D areas* x_j
  - *(gate material: n-type polysilicon, p-type polysilicon, metal electrode)*

Nanoelectronics – Scaling of MOSFETs
Contents

- Transfer characteristics of a n-channel MOSFET (W=6 µm, L=3 µm, V_{TH}=0.8V, µ=750 cm²/Vs)



1. „OFF“
2. linear region
3. saturation region
4. subthreshold region

Nanoelectronics – Scaling of MOSFETs
Key parameters

- Metrics of MOS-Transistors
  - *Structure*
  - *Operation regions*
  - *Output and transfer characteristics*
  - *Dynamic behavior*

- Skaling rules
  - *Constant Voltage Scaling*
  - *Constant Field Scaling*
  - *Real / practical scaling*

Nanoelectronics – Scaling of MOSFETs
Key parameters

- Scaling of MOS devices I
  - *before: Scaling at constant voltage*
    - Advantages:
      - Compatibility of supply voltage (bipolar technology)
      - High switching speed

Nanoelectronics – Scaling of MOSFETs
Key parameters

- Scaling of MOS devices II: constant voltage
  - *typicall scaling with a constant α >1 (until approx. 0.8 µm linewidth); compatibility against bipolar technology (U_{DD} = 5 V)*

Parameter	scales to
Supply voltage U_{DD}	U_{DD}
Gate length L	L/α
Gate width W	W/α
Gate oxid thickness d_{IS}	d_{IS}/α
p-n junction depth x_j	x_j/α
Substrate doping $N_{A,D}$	$N_{A,D} \cdot \alpha$

$\alpha \approx 1{,}4$

$$E = \frac{U}{d}$$

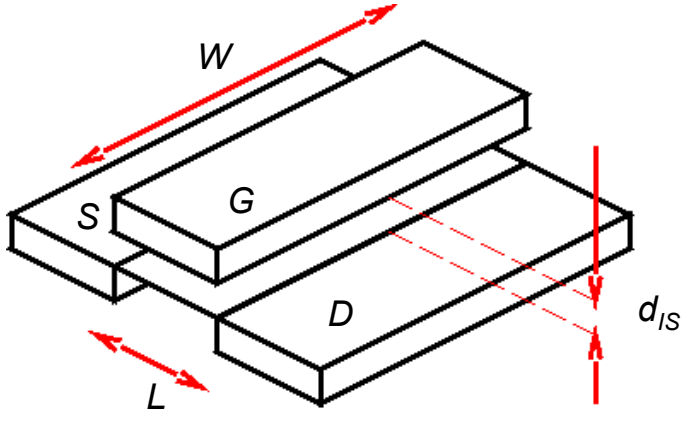
Field increases and leads to reliability problems: Scaling with constant field

Nanoelectronics – Scaling of MOSFETs
Key parameters

- Scaling of MOS devices I
  - *before: scaling at constant voltage*
    - Advantages:
      - Compatibility of supply voltage (bipolar technology)
      - High switching speed
    - Disadvantages:
      - increased field leads to problems (hot carriers)
      - strongly increasing power density >> high temperatures
  - *then (theoretically): scaling at constant field*
    - Advantage:
      - less power consumption
    - Disadvantages
      - no voltage compatibility

Nanoelectronics – Scaling of MOSFETs
Key parameters

- Scaling of MOS devices III: **const. field, theoretically**
- scaling by a factor α > 1
- primarily scaled parameters
  - Channel length $L \rightarrow L/\alpha$
  - Channel width $W \rightarrow W/\alpha$
  - Oxide thickness $d_{IS} \rightarrow d_{IS}/\alpha$
  - Doping conc. $N_{A,D} \rightarrow N_{A,D} \cdot \alpha$
  - **Supply Voltage $U \rightarrow U/\alpha$**



- effects of scaling on
  - Utilized area
  - Capacitances
  - Resistances
  - Power consumption
  - Threshold voltage U_{Th}
  - Drain current I_D
  - Gate delay t_{GD}
  - Transmission delay t_W

Nanoelectronics – Scaling of MOSFETs
Key parameters

- Scaling of MOS devices IV: constant voltage vs. constant field

Parameter	constant voltage	constant field
Supply Voltage V_{DD}	U_{DD}	$\boldsymbol{U_{DD} / \alpha}$
Gate Length L	L / α	L / α
Gate Width W	W / α	W / α
Oxide thickness d_{IS}	d_{IS} / α	d_{IS} / α
S/D junction depth x_j	x_j / α	x_j / α
Doping concentration $N_{A,D}$ (substrate)	$N_{A,D} \cdot \alpha$	$N_{A,D} \cdot \alpha$

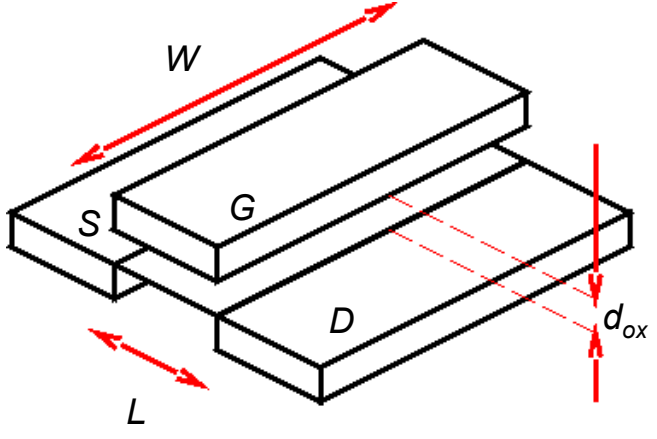
$$E = \frac{U}{d} = const.$$

Nanoelectronics – Scaling of MOSFETs
Key parameters

- Scaling of MOS devices V: areal scaling
  - *area*

$$A = L \cdot W$$

$$L \rightarrow \frac{L}{\alpha}, \qquad W \rightarrow \frac{W}{\alpha}$$



  - *after scaling*

$$A \rightarrow \frac{A}{\alpha^2}$$

- *Example: Transition from 90 nm node (technology) to 65 nm node*
  α = 1,4 → Area /2 → ***very good***

Nanoelectronics – Scaling of MOSFETs
Key parameters

- Scaling of MOS devices VI: capacity
  - *per area*

$$C_{IS} = \frac{\varepsilon_0 \varepsilon_{IS}}{d_{IS}} \qquad d_{IS} \rightarrow \frac{d_{IS}}{\alpha}$$

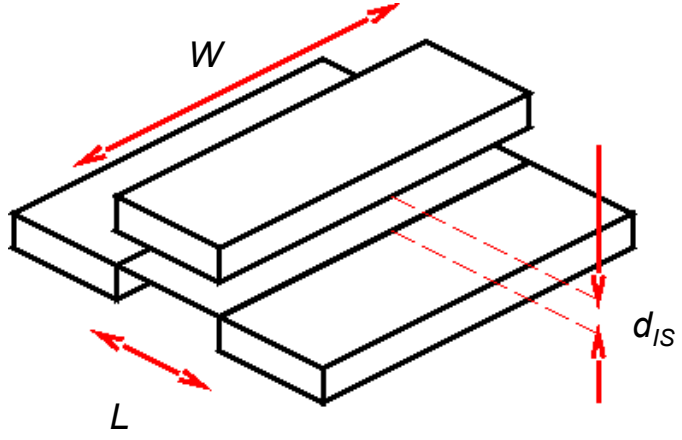
  - *areal capacity after scaling*

$$C_{IS} \rightarrow C_{IS} \cdot \alpha$$

    increases due to scaling
  - *Total capacity (absolute value)*

$$C = C_{IS} \cdot A \rightarrow \frac{C}{\alpha}$$

  - *Capacity gets smaller/larger? → good/bad?*



Nanoelectronics – Scaling of MOSFETs
Key parameters

- Scaling of MOS devices VII: treshold voltage

$$U_{Th} = U_{FB} + 2\phi_B - \frac{Q_{HL}}{C_{IS}} = \cancel{\phi_{MHL}}^{\approx 0} + 2\phi_B - \frac{Q_{IS} + Q_{HL}}{C_{IS}}$$

$$Q_{IS} = \int_0^{d_{IS}} \rho_{IS}\, x\, dx = \frac{1}{2} d_{IS}\rho$$

$$Q_{IS} \rightarrow \frac{Q_{IS}}{\alpha}$$

$$C_{IS} \rightarrow C_{IS} \cdot \alpha$$

$$\frac{Q_{IS}}{C_{IS}} \rightarrow \frac{1}{\alpha^2}\frac{Q_{IS}}{C_{IS}}$$

$$Q_{HL} = \pm\sqrt{2\varepsilon_{HL} q N_{A,D} |2\phi_B|}$$

$$N_{A,D} \rightarrow N_{A,D} \cdot \alpha, \quad |\phi_B| = \frac{kT}{q} \ln\left(\frac{N_{A,D}}{n_i}\right) \rightarrow \ln\alpha + \phi_B$$

$$N_{A,D}|2\phi_B| \overset{\text{ungefähr}}{\rightarrow} N_{A,D}|2\phi_B|$$

$$\frac{Q_{HL}}{C_{IS}} \rightarrow \frac{1}{\alpha}\frac{Q_{HL}}{C_{IS}}$$

- Scaled threshold voltage:

$$U_{Th} \rightarrow \frac{U_{Th}}{\alpha}$$

Nanoelectronics – Scaling of MOSFETs
Key parameters

- Scaling of MOS devices VIII: drain current (saturation)

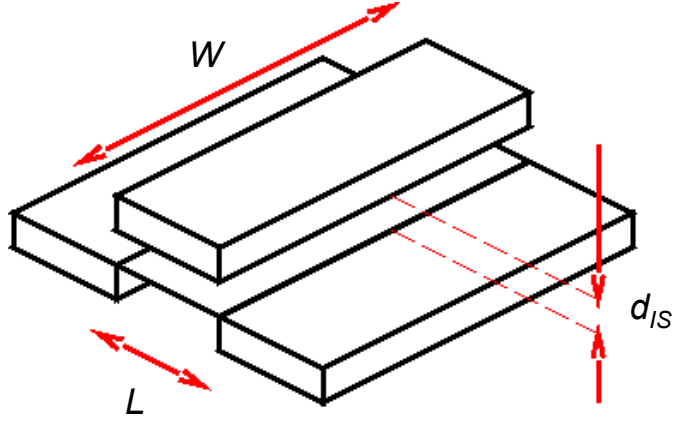
$$I_D = \frac{\mu C_{IS}}{2}\frac{W}{L}\left(U_G - U_{Th}\right)^2$$

$$U_G \rightarrow \frac{U_G}{\alpha},\quad U_{Th} = \frac{U_{Th}}{\alpha}$$

$$L \rightarrow \frac{L}{\alpha},\quad W = \frac{W}{\alpha},\quad C_{IS} = C_{IS}\cdot\alpha$$

Scaled saturation current

$$I_D \rightarrow \frac{I_D}{\alpha}$$



- Saturation current gets smaller! → but: really bad?

Nanoelectronics – Scaling of MOSFETs
Key parameters

- Scaling of MOS devices IX: gate delay

$$\tau_G = \frac{Q}{I_D} = \frac{CU_{DD}}{I_D}$$

$$C \rightarrow \boxed{\frac{C}{\alpha},} \quad I_D \rightarrow \boxed{\frac{I_D}{\alpha}} \qquad U_{DD} \rightarrow \boxed{\frac{U_{DD}}{\alpha}}$$

Scaled delay time

$$\boxed{\tau_{GD} \rightarrow \frac{\tau_{GD}}{\alpha}}$$

- Transistor gets faster! → good!

Nanoelectronics – Scaling of MOSFETs
Key parameters

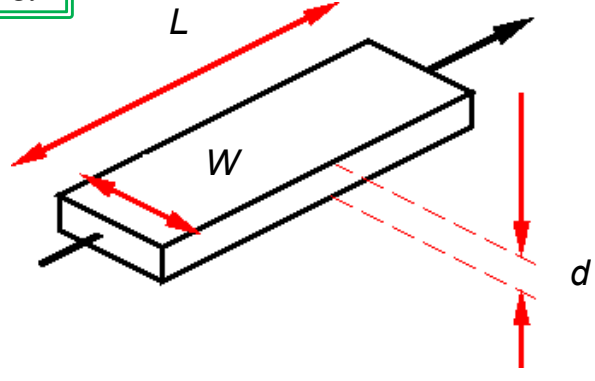
- Scaling of MOS devices X: resistivity of wiring

$$R = \rho \frac{L}{Wd}$$

$$L \rightarrow \frac{L}{\alpha} \qquad W \rightarrow \frac{W}{\alpha} \qquad d \rightarrow \frac{d}{\alpha}$$

scaled line resistivity

$$R \rightarrow R \cdot \alpha$$

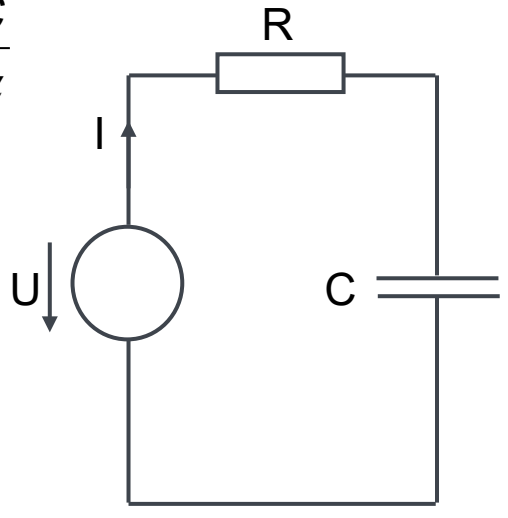


- Resistivity increases ! → bad!

Nanoelectronics – Scaling of MOSFETs
Key parameters

- Scaling of MOS devices XI: line delay

$$\tau_{wire} = RC \qquad R \rightarrow R \cdot \alpha \qquad C \rightarrow \frac{C}{\alpha}$$



scaled line delay

$$\tau_{wire} = const.$$

- delay time is constant: o.k.

Nanoelectronics – Scaling of MOSFETs

Key parameters

- Scaling of MOS devices XII: static power dissipation

$$P = UI \qquad U \rightarrow \frac{U}{\alpha} \qquad I \rightarrow \frac{I}{\alpha}$$

scaled power losses

$$P \rightarrow \frac{P}{\alpha^2}$$

- losses are strongly reduced: very good!

Nanoelectronics – Scaling of MOSFETs

Key parameters

- Scaling of MOS devices XIII: dynamic power dissipation capacitive discharging:

$$P = \frac{1}{2} C U^2 f \qquad U \rightarrow \frac{U}{\alpha},\ C \rightarrow \frac{C}{\alpha}$$

  scaled dynamic power loss (at fixed frequency)

$$P \rightarrow \frac{P}{\alpha^3}$$

- including an increasing frequency

$$f \rightarrow f \cdot \alpha \quad ? \qquad P \rightarrow \frac{P}{\alpha^2}$$

- also very good!

Nanoelectronics – Scaling of MOSFETs
Key parameters

- Summary of constant field scaling

Parameter	changes to
Area A	A / α^2
Capacities C	
Resistivities R	
Threshold Voltage U_{th}	U_{Th} / α
Drain current I_D	
Gate delay τ_G	
Line delay τ_{wire}	const.
Power losses P	$1 / \alpha^3$ to $1 / \alpha^2$

Nanoelectronics – Scaling of MOSFETs

But: is this really representing the reality?

- Historically: scaling @ fixed voltage
  - *Compatibility of supply voltages*
  - *high switching speeds*
  - *problems due to high electric fields (hot carriers)*
  - *strong increase in power density → high chip temperatures, low reliability*
- now (theoretically): scaling @ constant field
  - *low power consumption*
  - *no voltage compatibility*
- now (practically/additionally):

Trade offs with respect to device physics, voltage compatibility

Nanoelectronics – Scaling of MOSFETs
Real scaling

- Constant voltage, constant field, and real scaling (scaling by factors of α >1, β >1)

Parameter	constant voltage	constant field	α and β scaling
Supply Voltage V_{DD}	U_{DD}	$\boldsymbol{U_{DD} / \alpha}$	$\boldsymbol{U_{DD} / \beta}$
Gate Length L	L / α	L / α	L / α
Gate Width W	W / α	W / α	W / α
Oxide thickness d_{IS}	d_{IS} / α	d_{IS} / α	$\boldsymbol{d_{IS} / \beta}$
S/D junction depth x_j	x_j / α	x_j / α	x_j / α
Doping concentration $N_{A,D}$ (substrate)	$N \cdot \alpha$	$N \cdot \alpha$	$N \cdot \alpha$

Due to problems with gate oxide breakdown only constant field scaling below 800 nm node

Nanoelectronics – Scaling of MOSFETs
Real scaling

- Constant voltage, constant field, and real scaling (scaling by factors of α >1, β >1) influence on device and circuit parameters

Parameter	constant voltage	constant field	α and β scaling
Gate electric field	α	**1**	**1**
Depletion width	$1 / \alpha$	$1 / \alpha$	$1 / \alpha$
Gate area	$1 / \alpha^2$	$1 / \alpha^2$	$1 / \alpha^2$
Gate capacity	$1 / \alpha$		
Drain current	α		
Gate delay	$1 / \alpha^2$		
Current density	α^3	**α**	**α**
Power consumption	α	**$1 / \alpha^2 \ldots 1 / \alpha^3$**	**$1/(\alpha\beta) \ldots 1/(^2ß\alpha)$**
Power density	α^3	**1**	**1**

Due to problems with gate oxide breakdown only α and β scaling below 500 nm node

Nanoelectronics – Scaling of MOSFETs
Real scaling

- Technology nodes according to ITRS

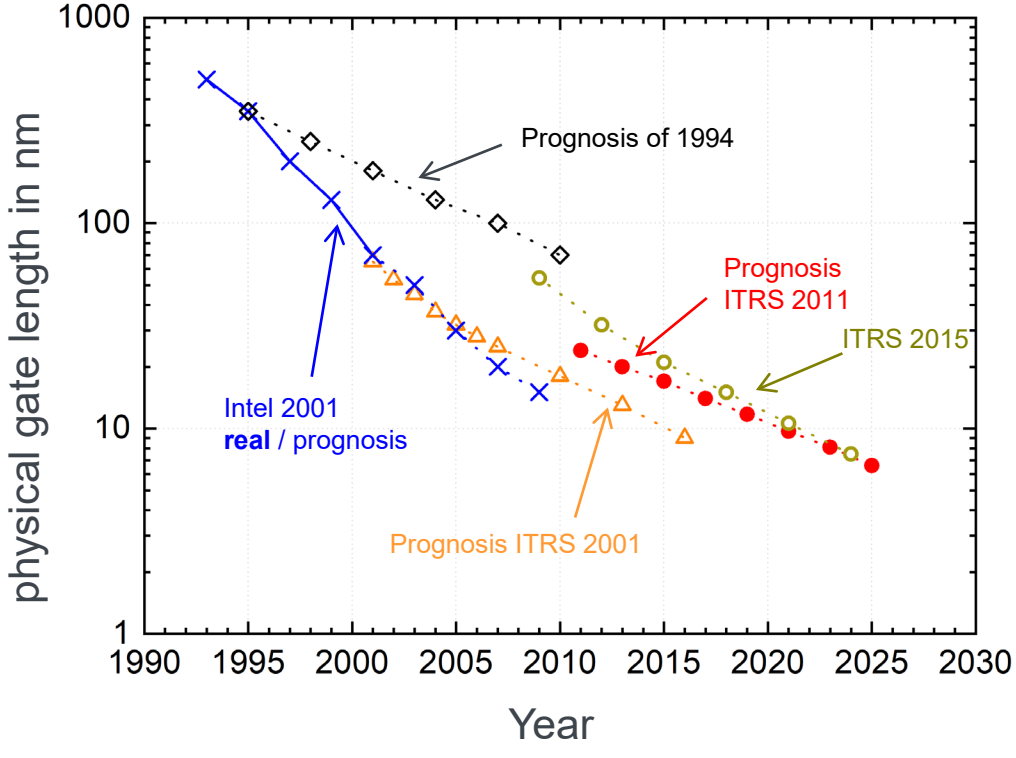
Year of production	2009	2012	2015	2018	2021	2024
Technology node	54 nm	32 nm	21 nm	15 nm	10,6 nm	7,5 nm
Equivalent oxide thickness (nm)	1,0 [1)]	0,85 [2)]	0,8 [3)]	0,73 [4)]	0,65 [4)]	0,6 [4)]
Supply voltage U_{DD} (V)	0,95	0,85	0,75	0,7	0,6	0,6
DRAM memory generation (Gb)	2	4	8	16	32	64
DRAM cell size (nm^2)	16 000	5 100	2 600	1 300	640	320
CPU (10^6 Transistors / Chip)	773	1 546	3 092	6 184	12 368	24 736
CPU clock frequency (GHz, on chip)	5,454	6,329	8,522	10,652	13,315	16,640

(International Technology Roadmap for Semiconductors, 2015/last edition)

[1)] Bulk Si, poly gate
[2)] Bulk Si, metal gate
[3)] FDSOI, metal gate
[4)] Multiple metal gate

Nanoelectronics – Scaling of MOSFETs
Real scaling

- Example: physical gate length (ITRS)



Thanks for your attention!