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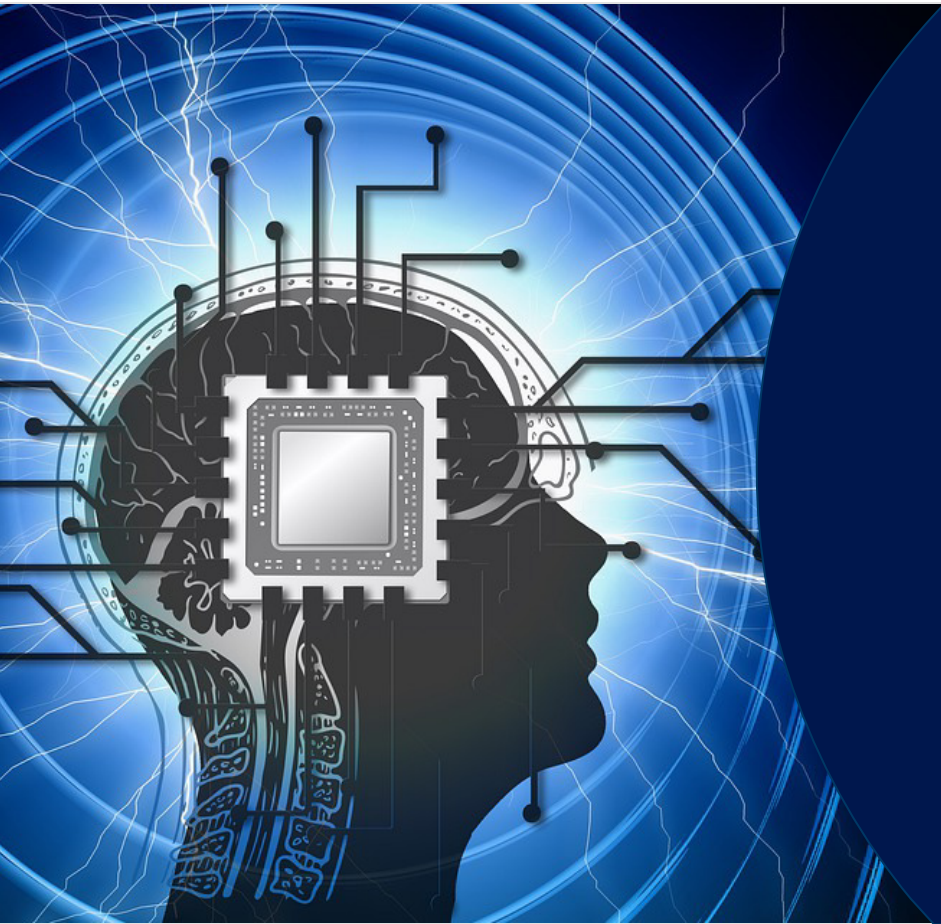


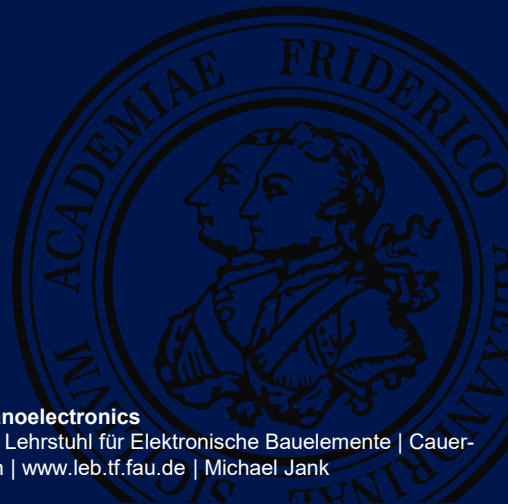
Halbleitertechnik IV- Nanoelectronics

Friedrich-Alexander-Universität Erlangen-Nürnberg | Lehrstuhl für Elektronische Bauelemente | Cauerstraße 6 | 91058 Erlangen | www.leb.tf.fau.de | Michael Jank

Tunneling

Objectives of the lecture

Mission and goals?



Tunneling

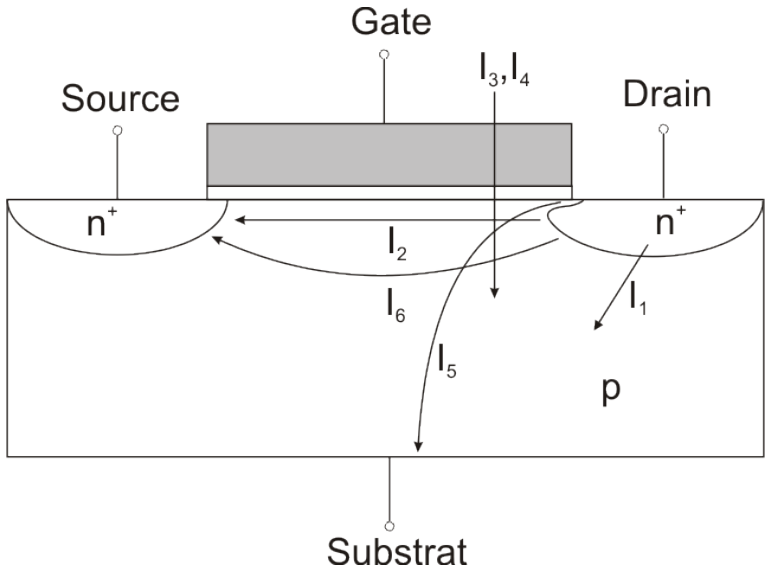
Objectives

You should understand

- the physical basics about generation of tunnel currents.
- tunneling mechanisms in MOSFETs, particularly at semiconductor-insulator-interfaces, their description and distinction.
- the background about replacement of SiO_2 in sub-100nm technology nodes.

Tunneling
Leakage Currents

- Overview of leakage and short channel effects



K. Roy et al., Proceedings of the IEEE 91, 305 (2003), technical current orientation

- I_1: blocking current p-n diode
- I_2: subthreshold current MOSFET
- I_3: gate leakage current
- I_4: injection of hot electrons
- I_5: Gate Induced Drain Leakage (GIDL)
- I_6: punch through

Assignment to

- geometry or architecture
- tunneling
- degradation

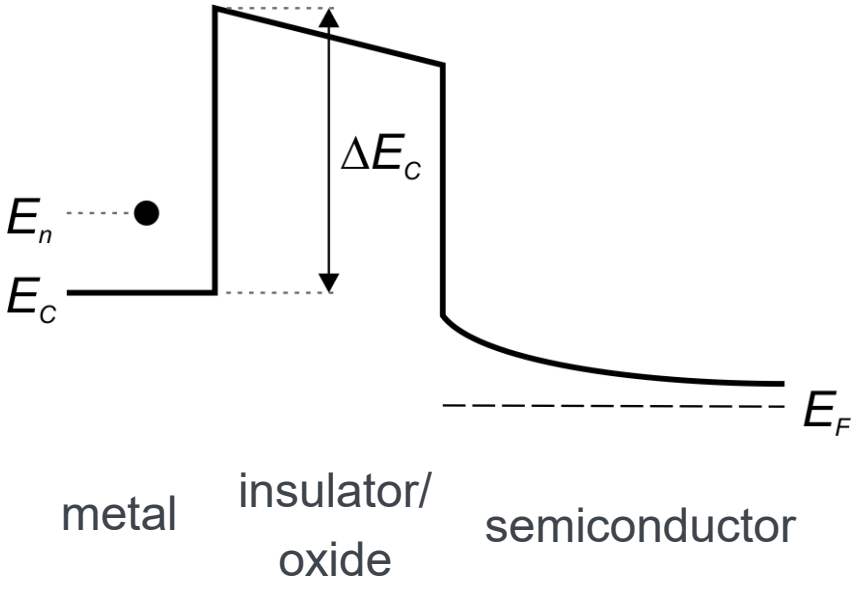
Tunneling
Outline

- Tunneling
  - *physical effects*
  - *band-to-band tunneling and gate-induced drain leakage (GIDL)*
  - *tunneling effects in insulators*
- Compensation of tunneling in scaling
  - *gate insulators with high dielectric constant*
  - *effective oxide thickness*
  - *integration aspects*

Tunneling

Physical effects

- Tunneling through a barrier
  - *According to classical mechanics, a barrier higher than the energy of the charge carrier energy cannot be overcome*
  - *Only possible: excite the particles (increase in kinetic particle energy by increasing temperature or accelerating) in order to provide sufficient energy.*
  - *The associated charge carrier transport process is called **thermionic emission** across a barrier*



Tunneling
Physical effects

- Quantum mechanical description of particles
  - *Quantum mechanically, electrons can be described as a matter wave with the 1-dimensional wave function*

$$\Psi(x,t) = \int_{k_0-\Delta k}^{k_0+\Delta k} \Psi_0 \exp\left(jk_x x - j\omega t\right) dk$$

  → probability of the particles staying at location x at time t

  - *The location-dependent exponential term with the x-component of the wave vector* ***k***

$$k_x = \frac{2\pi}{h} p_x = \frac{p_x}{\hbar}$$

  and the angular frequency ω describe a plane wave, the integral is the superposition of several plane waves

Tunneling
Physical effects

- SCHRÖDINGER's equation (stationary)
  - *the potential curve (physical system description) is not variable over time, i.e.*

$$\Psi(\vec{r},t) = \Psi(\vec{r}) \cdot \phi(t)$$

  - *thus, the SCHRÖDINGER equation can be transformed into*

$$\Psi(\vec{r})\left(j\hbar \frac{\partial}{\partial t}\phi(t) \right) = \phi(t)\left[\left(-\frac{\hbar^2}{2m_0}\nabla^2 + V(\vec{r}) \right)\Psi(\vec{r}) \right]$$

  - *assuming exponential solutions to the differential functions, the bracketed expressions on both sides can be transformed like*

$$j\hbar \frac{\partial}{\partial t}\phi(t) = h(\vec{r})\phi(t) \qquad \left(-\frac{\hbar^2}{2m_a}\nabla^2 + V(\vec{r}) \right)\Psi(\vec{r}) = g(t)\Psi(\vec{r})$$

Tunneling
Physical effects

- SCHRÖDINGER's equation (stationary)
  - *yielding*

$$\Psi(\vec{r})h(\vec{r})\phi(t) = \phi(t)g(t)\Psi(\vec{r}) \Rightarrow h(\vec{r}) = g(t)$$

  - *i.e. h and g must be constants!*
  - *dimension-wise this refers to an energy, the total energy E_0 of the electron*

$$\phi(t) = \phi_a \exp\left(-j\frac{E_0}{\hbar}t\right)$$

$$\Psi(\vec{r},t) = \Psi(\vec{r})\exp\left(-j\frac{E_0}{\hbar}t\right)$$

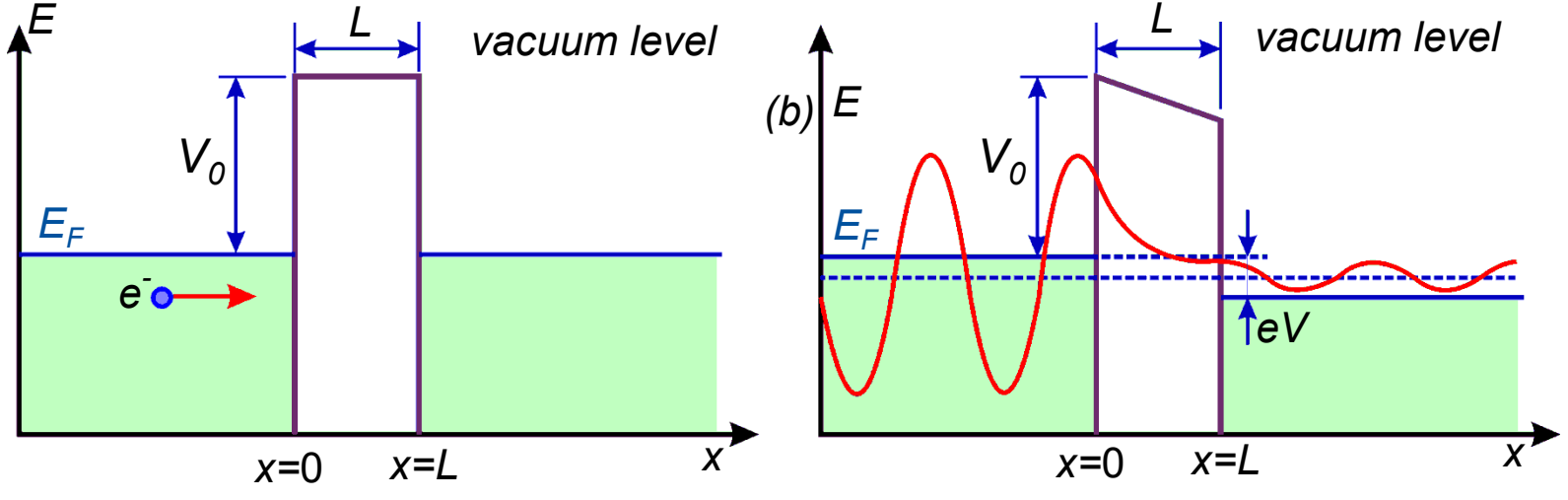
$$\left[-\frac{\hbar^2}{2m_a}\nabla^2 + V(\vec{r})\right]\Psi(\vec{r}) = E_0\Psi(\vec{r})$$

Tunneling

Physical effects

- Differences between quantum mechanical tunneling and classical mechanics
  - *the transmission probability is depending on width/thickness of the tunneling barrier and its height with respect to energy*

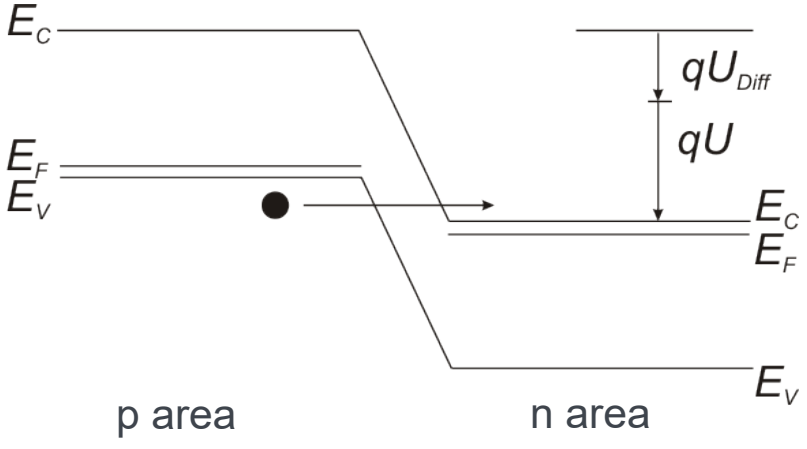
$$T \approx \exp(-2\alpha d) = \exp\left(-2\sqrt{2m(V_0 - E_0)\frac{d^2}{\hbar^2}}\right)$$



Tunneling

Band-to-band tunneling and gate induced leakage (GIDL)

- Blocking currents in a p-n junction (MOSFET on/off)
  - *drift and diffusion of minority carriers* $N_{A,D} \uparrow \rightarrow I_{rev} \downarrow$
  - *generation-/recombination current* ($N_{A,D} \uparrow \rightarrow I_{rev} \uparrow$)
  - *band-to-band tunneling* $N_{A,D} \uparrow \rightarrow I_{rev} \uparrow\uparrow$

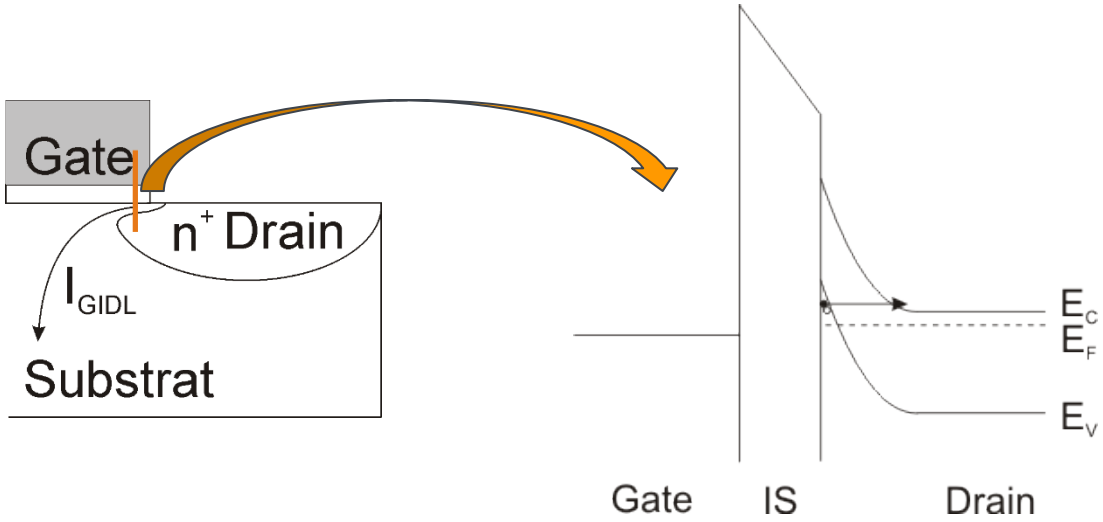


- *appears, when both n as well as p side of the junction are doped excessively (i.e. short SCR) or*
- *when e.g. a strongly accumulated p area contacts a highly doped n area.*

Tunneling

Band-to-band tunneling and gate induced leakage (GIDL)

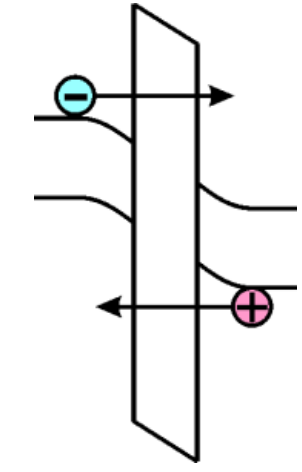
- Gate induced drain leakage (GIDL)
  - *deep depletion of the drain area in the overlap area of gate and drain, with the transistor switched off (hard, i.e., for n type: at very negative gate-to-source /gate-to-drain voltage)*
  - *Generation of electron-hole pairs by tunneling of electrons from the valence band into the conduction band, holes are accelerated to the substrate*

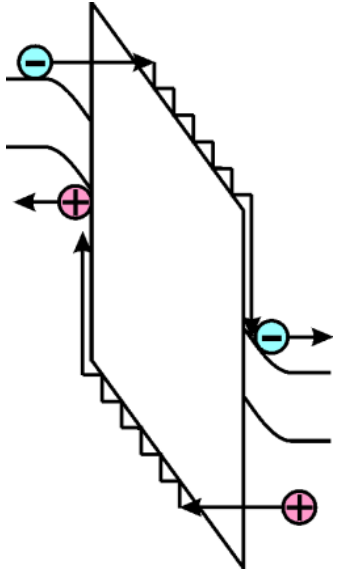


Tunneling

Tunneling in MOS-Insulators

- Direct tunneling
  - *depending on barrier height and insulator thickness*
- FOWLER-NORDHEIM tunneling
  - *barrier width is reduced by applying an electric field and resulting band bending.*
  - *charge carriers are injected into conduction or valence band of the insulator, where carrier transport is possible as in a semiconductor.*





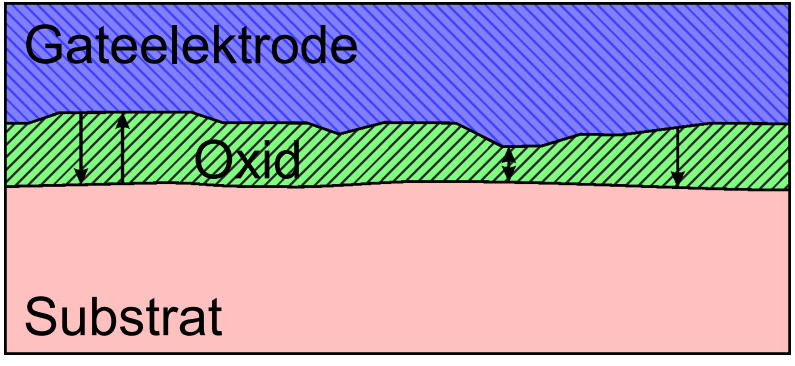
$$T \approx \exp\left(-2\frac{\sqrt{2m}}{\hbar^2}\int_0^d (V_0 - qE_{IS}x)dx \right)$$

$$J_{FN} = CE_{IS}^2 \exp\left(\frac{4}{3}\frac{\sqrt{2m}}{q\hbar^2}\phi_h^{3/2} \Big/ E_{IS} \right)$$

Tunneling

Tunneling in MOS-Insulators

- Implications of gate leakage (MOSFET on/off)
- Increase in leakage currents over time
  - *breaking of bonds, capture of charges*
  - *possibly leading to change of the leakage current mechanism*
- Defects and inhomogeneities of oxide thickness
  - *root cause: rough substrate surface and inhomogeneous processes*
  - *increased probability of breakthrough*
- $d_{IS} \downarrow \rightarrow I_G \uparrow$



Tunneling
Outline

- Tunneling
  - *physical effects*
  - *band-to-band tunneling and gate-induced drain leakage (GIDL)*
  - *tunneling effects in insulators*
- Compensation of tunneling in scaling
  - *gate insulators with high dielectric constant*
  - *effective oxide thickness*
  - *integration aspects*

Tunneling

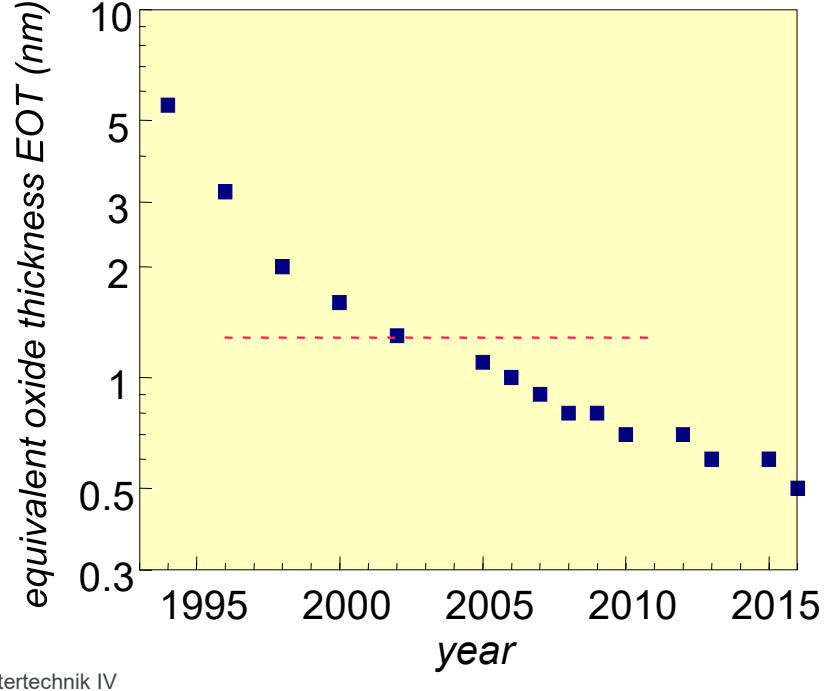
Gate insulators with high dielectric constant

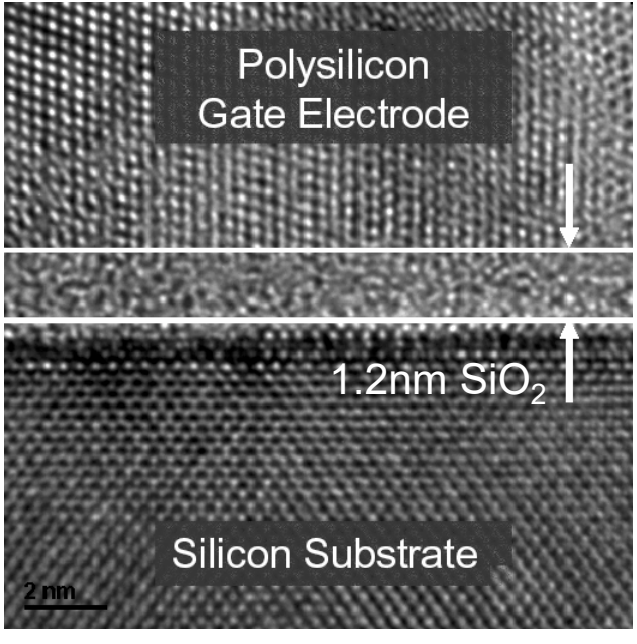
- Problems to be solved
  - *oxide thickness becomes thinner and thinner due to scaling rules*
    - high tunnel currents even at lowest (e.g. 1 V) operating voltage
  - *for structure sizes < 65 nm, high-k dielectrics are required to replace silicon oxide*
    - thicker layers can be used, which have lower tunnel currents and a higher breakdown voltage
    - the gate capacitance remains large enough to store enough charges for the transistor to be switched on
  - *metal gate electrodes*
    - lower sheet resistance → higher switching speed (see previous section)

Tunneling

Gate insulators with high dielectric constant

- Oxide thickness
  - *from 2002 on, gate oxide thickness theoretically was below 1.0 – 1.2 nm in thickness*
  - *this corresponds to only 4-5 atomic layers*

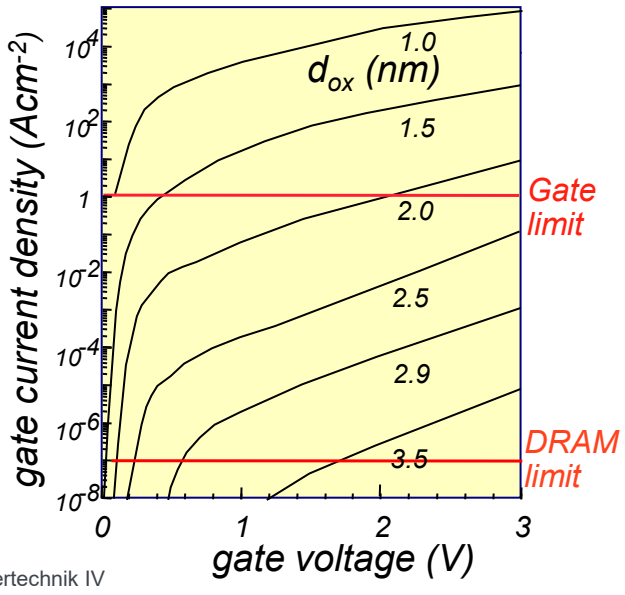


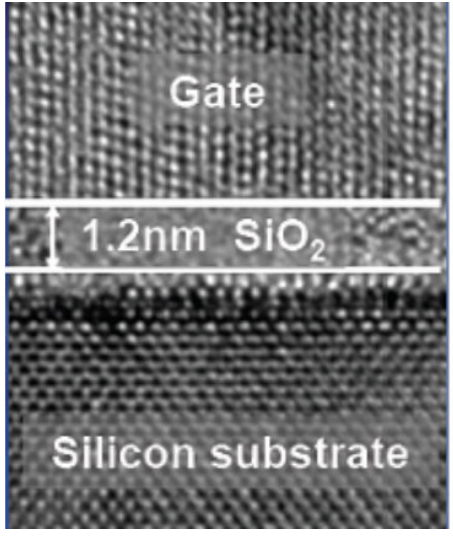


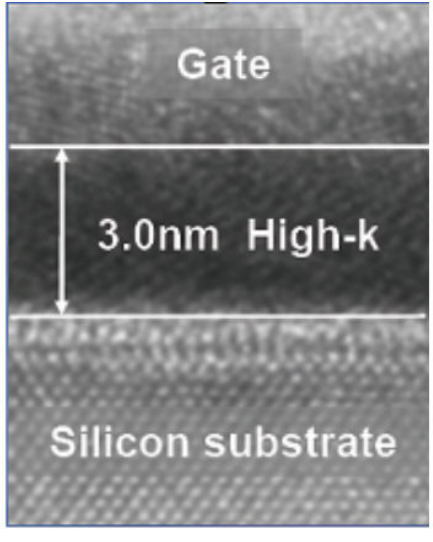
Tunneling

Gate insulators with high dielectric constant

- Why high-k dielectrics
  - *SiO_2 layers <1,6 nm show high leakage currents due to direct tunneling and will not insulate properly*
    - areal oxide capacitance ($C = \varepsilon_0\varepsilon_r / d_{INS}$) should be kept for high I_{ON} or transconductance β
    - replacement of SiO_2 by thick layer of an insulator having high ε.
  - *comparison of materials using "equivalent oxide thickness" 'EOT'*



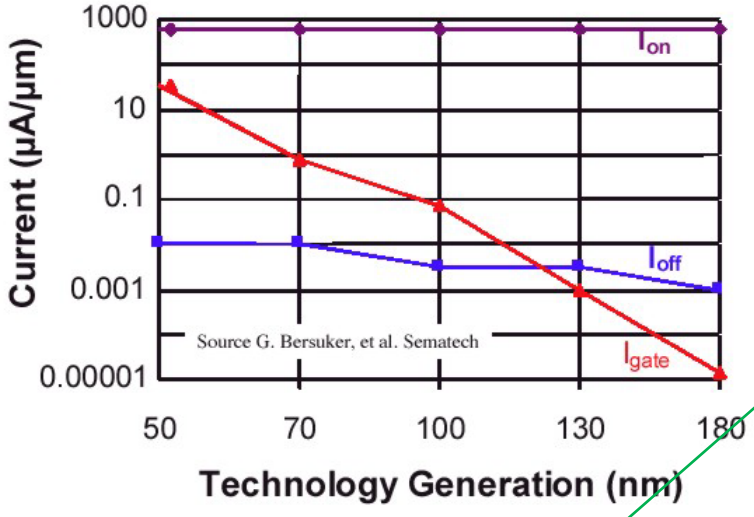




Tunneling

Equivalent Oxide Thickness

- Scaling of thin gate oxides



what high-k thickness can I afford to deposit?

- Solution: high-k dielectrics

$$C = \frac{\varepsilon_0 \varepsilon_r}{d_{INS}} \quad \Rightarrow \quad d_{IS} = \frac{\varepsilon_{IS}}{\varepsilon_{OX}} \cdot d_{OX,eff}$$

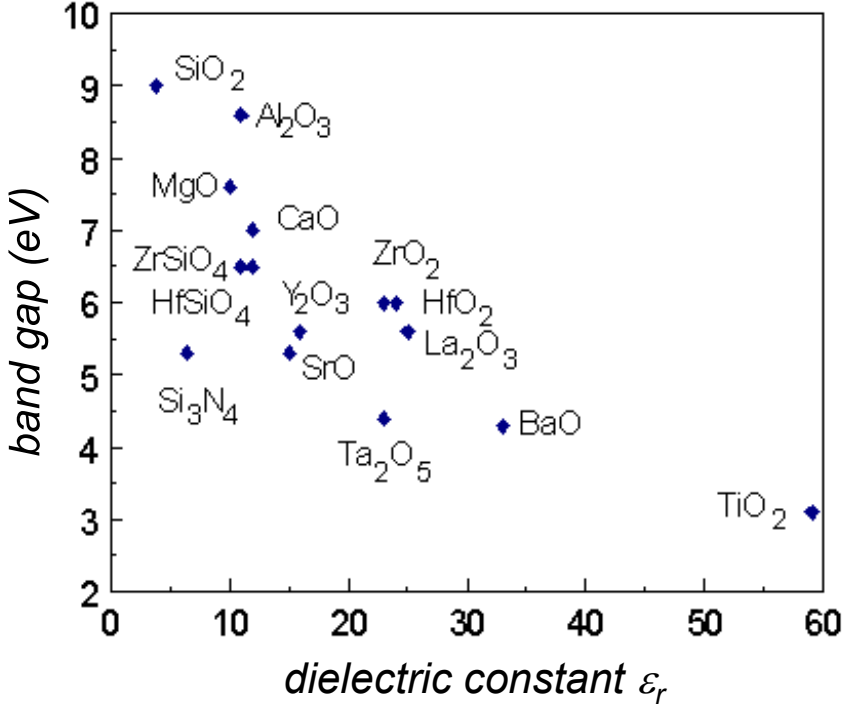
target: EOT

- Preservation of control/drive capability @ thicker insulator, i.e. reduced tunnel currents

Tunneling

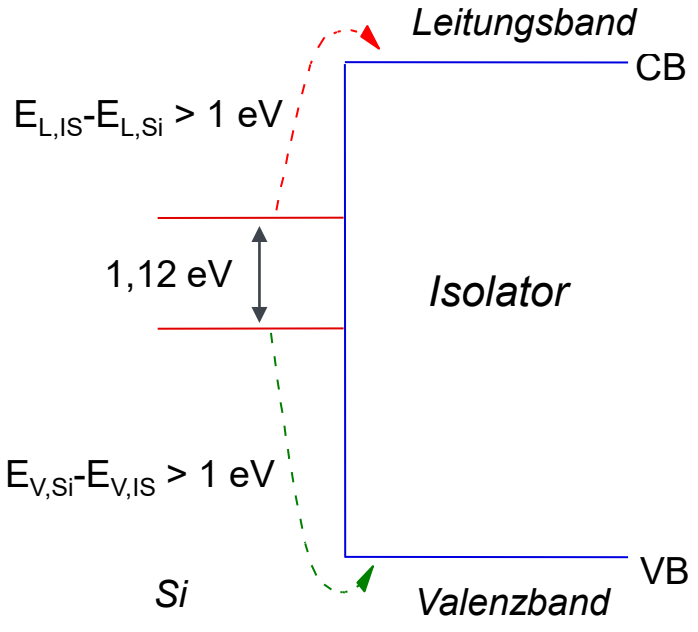
Integration Issues

- Requirements for new dielectrics
  - *sufficiently high ε_r (=k-value)*
- Chemical stability
  - *inertness against Si*
  - *prefer oxides with high formation heat (HfO_2, Zr-, Y-, La-, Al-oxides)*
  - *use of silicates instead of oxides (e.g. $HfSiO_4$,$ZrSiO_4$)*
  - *thermal stability (up to 1000°C)*
- Amorphous HfSiOx:N?
- Large barrier height (band offset)
- Low-defect interfaces (interface trap density D_{it})

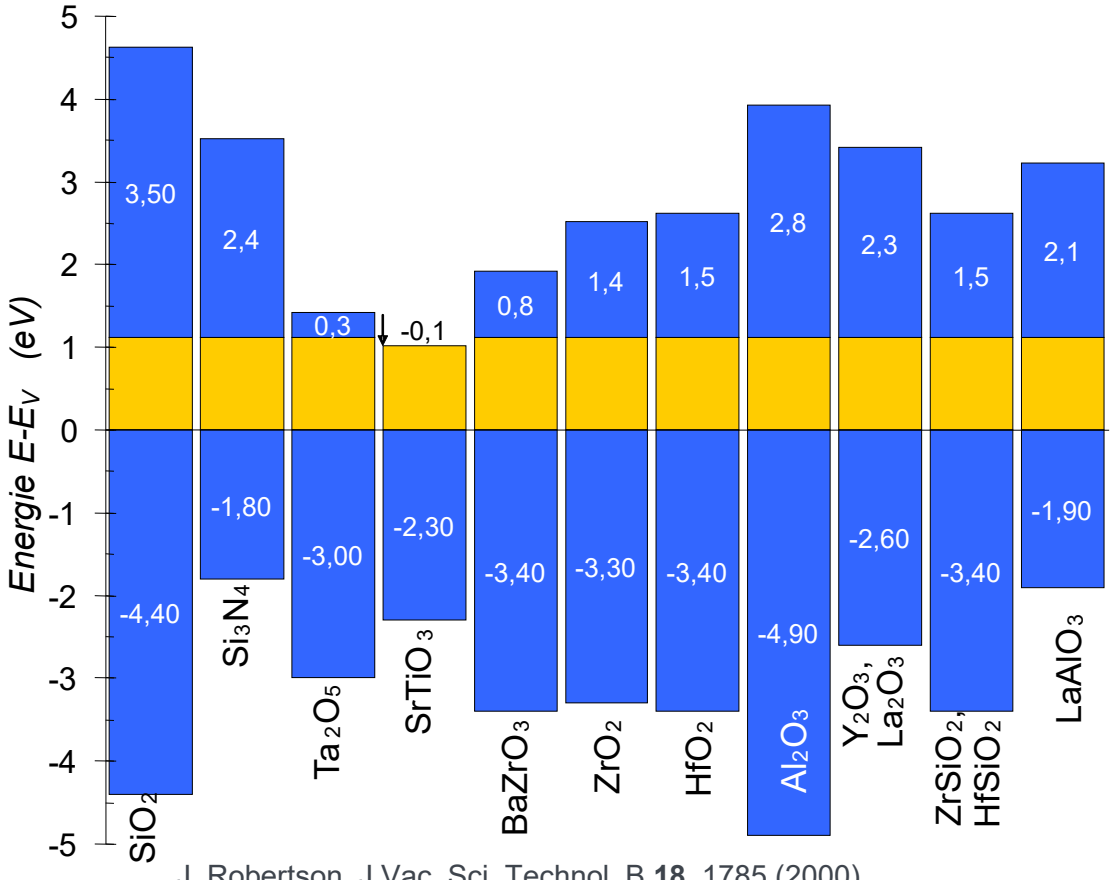


Tunneling
Integration Issues

- Requirements for new dielectrics
  - *Large barrier height (band offset)*



Barrier height should exceed 1 eV
both for e^- and h^+



J. Robertson, J Vac. Sci. Technol. B **18,** 1785 (2000)

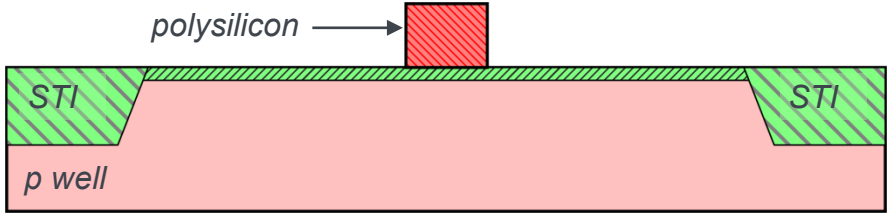
Tunneling
Integration Issues

- Processing of high-k materials and corresponding metal gate electrodes
  - *derived from traditional “Poly-Gate“ process (see introduction video on CMOS processing)*
    1. deposition of the gate dielectric and annealing
    2. metal deposition
    3. photolithography (metal gate)
    4. metal etching (generally dry etching)
    5. ion implantation (source/drain areas)
    6. annealing (RTA, Rapid Thermal Annealing)
  - *problems*
    - metal resistance against ion implantation
    - metal stability during annealing (typ. > 900 °C)
  - *dielectric and metal deposition after S/D formation would be ideal*
    - but how about alignment?

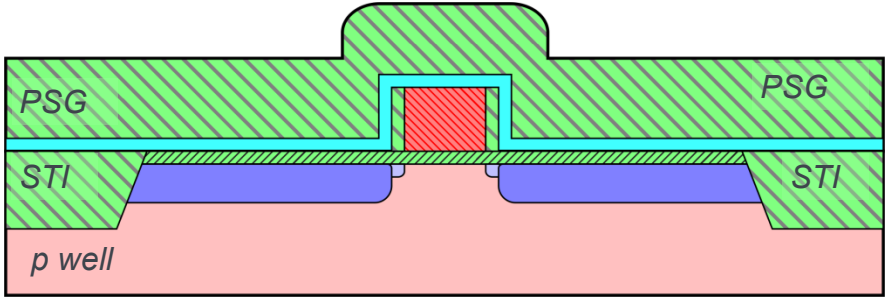
Tunneling

Gate insulators with high dielectric constant

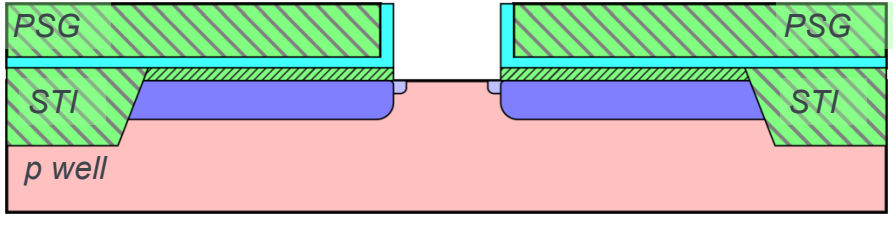
- Process flow for metal gate by ”Dummy Gate” or ”Replacement Gate” process



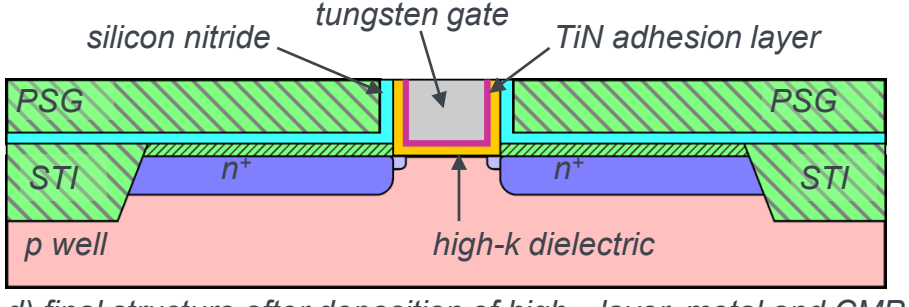
a) initial preparation of polysilicon dummy



b) after LDD implantation, spacer definition, CVD nitride, S/D implantation and CVD PSG deposition



c) structure after CMP and etching of nitride, oxide, polysilicon and oxide



d) final structure after deposition of high-ε layer, metal and CMP

Tunneling
Integration Issues

- Summary: metal and high-ε gate process
  - *for < 100 nm MOSFETs*
  - *feasible dielectrics:*
    - Tantal pentoxide Ta_2O_5: ε_r ~ 25
    - Titanium dioxide TiO_2: ε_r of up to 80
    - Hafnia HfO_2: ε_r ~ 30-40
    - Zirkonium silicate $ZrSiO_4$: ε_r ~ 10-15
    - Hafnium silicate $HfSiO_4$: ε_r ~ 10-15
  - *highly complex process*
  - *only feasible for sub-100 nm MOSFETS*
  - *from 65 nm onwards solely HfO_2 is used*

Tunneling
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Thanks for your attention!