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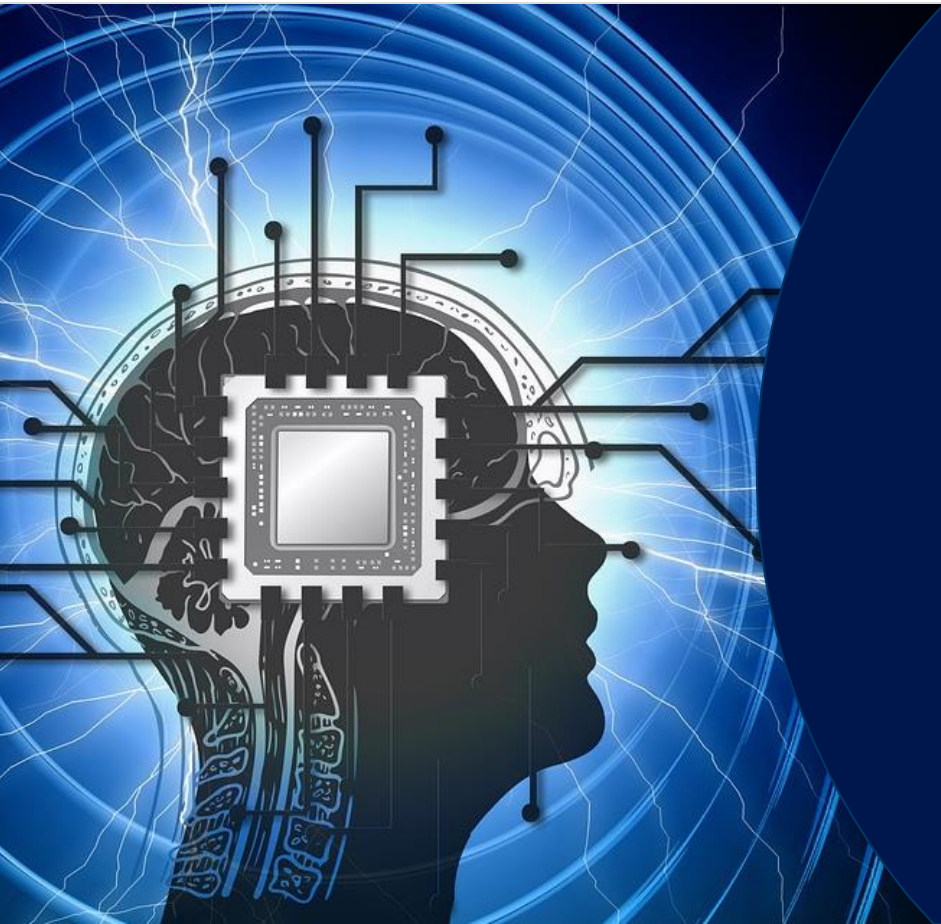

Halbleitertechnik IV- Nanoelectronics

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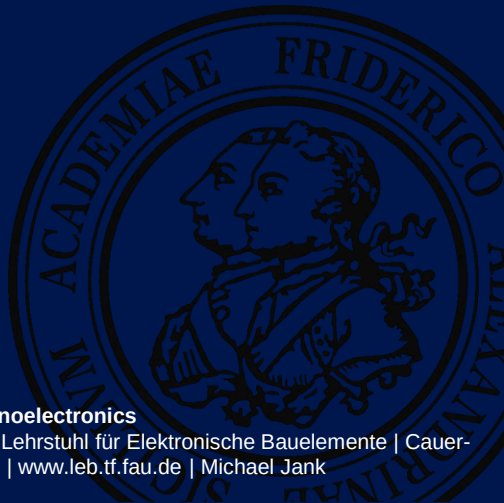
p-n Junctions and MOS Devices



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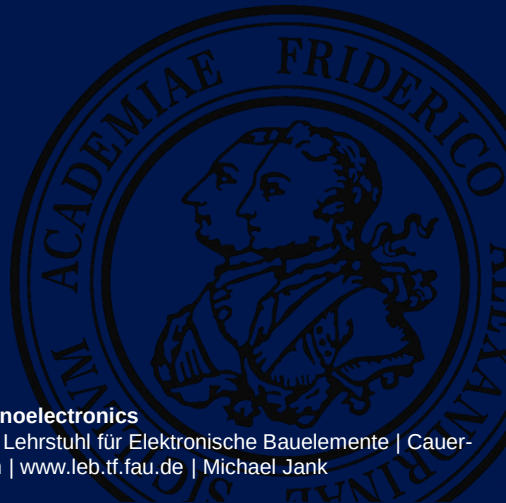
Objectives of the lecture

Mission and goals?



p-n Junctions and MOS Devices

Objectives

- With the knowledge of band-structure models and related carrier concentrations we can define and analyze very basic device structures:

- By the example of p-n junctions you should be able to describe semiconductor interfaces with respect to free and fixed charges, resulting electrical fields and potentials and to further discuss the behavior of diodes under external bias

- The operation modes of the metal-oxide-semiconductor structure are crucial prerequesites to the operation of MOS-type switches such as MOSFETs. It is important to know how they can be controlled via the gate and how characteristic parameters (e.g. threshold voltage) are determined

- The chapter ends with a comprehensive introduction to fabrication of CMOS circuits

Nanoelectronics – p-n Junctions and MOS Devices
Contents

- p-n Junctions
  - *Band-structure models and contact between p and n type semiconductors*
  - *Charge, field and potential distributions*
  - *Diode operation*
  - *Width of space-charge region*
- The MOS Structure and MOS Field-Effect Transistors
  - *Operation modes of the MOS diode*
  - *Threshold voltage of MOSFETs*
  - *Operation ranges of MOSFETs*
  - *Modelling of MOSFETs*
  - *Parasitic elements of MOSFETs*
- Processing of Integrated Circuits

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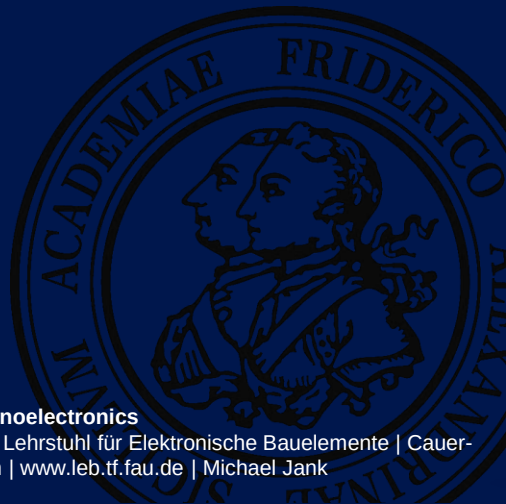
p-n Junctions

Simplified solid-state physics for the description of electron devices



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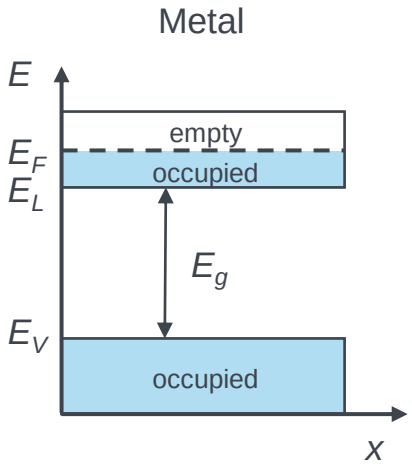
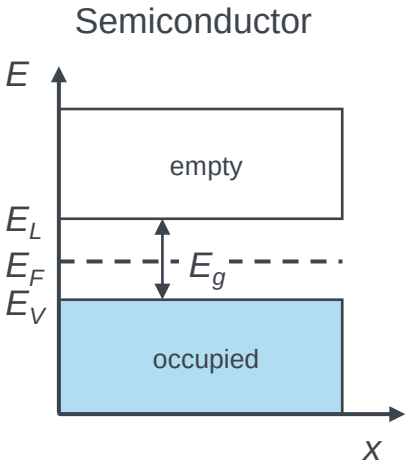
p-n Junctions
Band structures

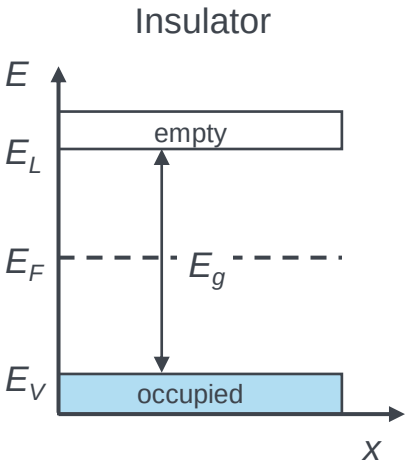
- Metal, Semiconductor, Insulator



Conduction Band (CB) is partly filled with electrons. FERMI level lies within CB



CB is empty, Valence Band (VB) is filled with electrons, narrow (approx. 0.5 eV) to wide (approx. 4 eV) band gap

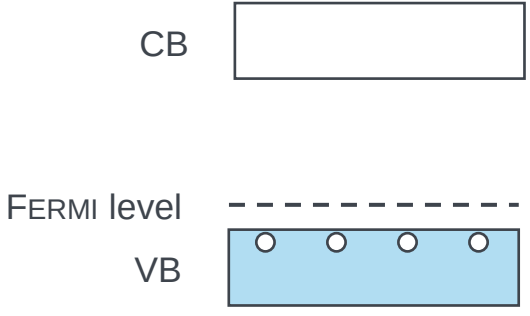


CB is empty, VB is completely filled with electrons, extremely wide band gap (> 4-5 eV)

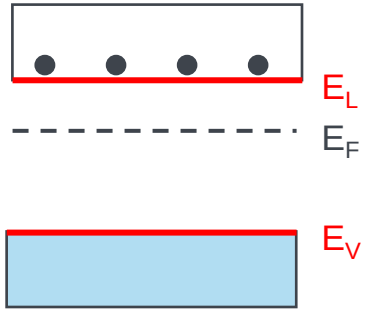
p-n Junctions

Doping of Semiconductors

- The energy of the FERMI level is a measure for the local concentration of (free) carriers



A missing electrone in the VB is more likely than in an intrinsic semiconductor:
p-type semiconductor

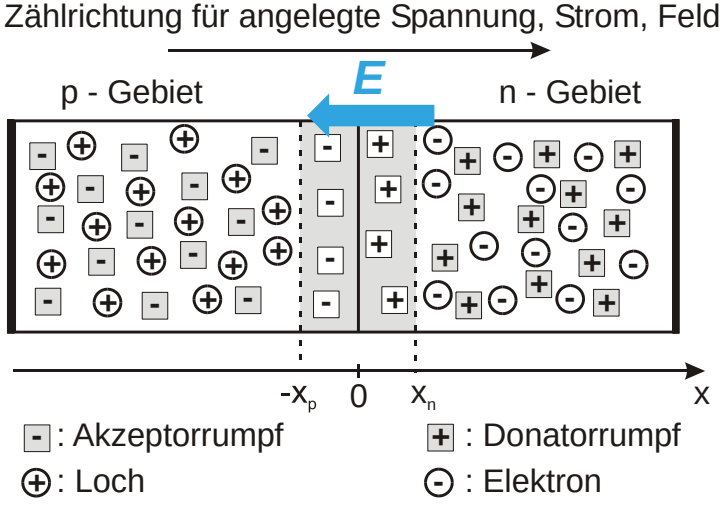


n-type semiconductor

p-n Junctions

Bringing p- and n-type semiconductors into contact

- p-n junction: Generation of space charge regions and electric fields
  - *Free (charge) carriers diffuse due to concentration gradients and recombine partly with complementary charges*
  - *The depletion of free carriers leaves behind ionized atoms, i.e. fixed local charges. The "space charge" is the source to formation of an electric field* ***E***

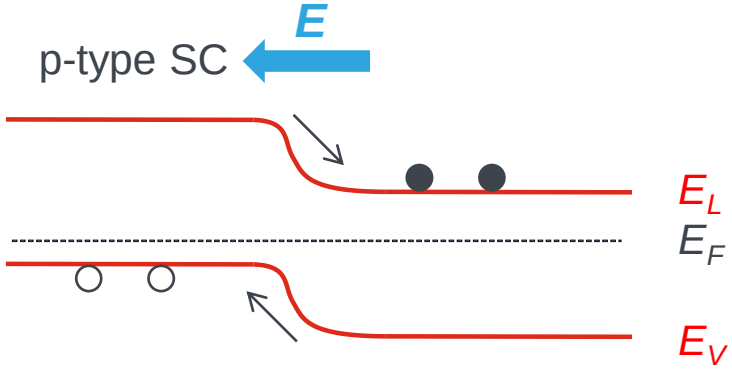


p-n Junctions

p-n junction in the band-structure model

- In thermodynamic equilibrium the FERMI level is constant
  - *CB and VB have to compensate for the change in flavor of the semiconductor*
  - *This leads to the formation of a barrier*

Barrier pushes electrons back,
“confines them to the n region“



Field(barrier) repels holes,
„will stay in p region“

p-n Junctions

Space charge, Fields and Potentials I

– POISSON equation

$$\frac{d\boldsymbol{E}}{dx} = -\frac{d^2\phi}{dx^2} = \frac{\rho(x)}{\varepsilon_{HL}\varepsilon_0}$$

where:

$\boldsymbol{E}$	: electric field
ϕ	: potential
ρ	: space charge density
ε_0	: permittivity of vacuum
ε_{HL}	: dielectric constant (k-value) of material

– Space charge density

$$\rho(x) = q\left[N_D^+(x) - N_A^-(x) + p(x) - n(x)\right]$$

where:

$N_D^+(x)$	: concentration of ionized donor atoms
$N_A^-(x)$	: concentration of ionized acceptor atoms
$n(x)$	: concentration of free electrons
$p(x)$	: concentration of free holes

p-n Junctions

Space charge, Fields and Potentials II

– The electric field may be derived from the first MAXWELL equation (1D):

$$\frac{dE}{dx} = \frac{\rho(x)}{\varepsilon_{HL}\varepsilon_0}$$

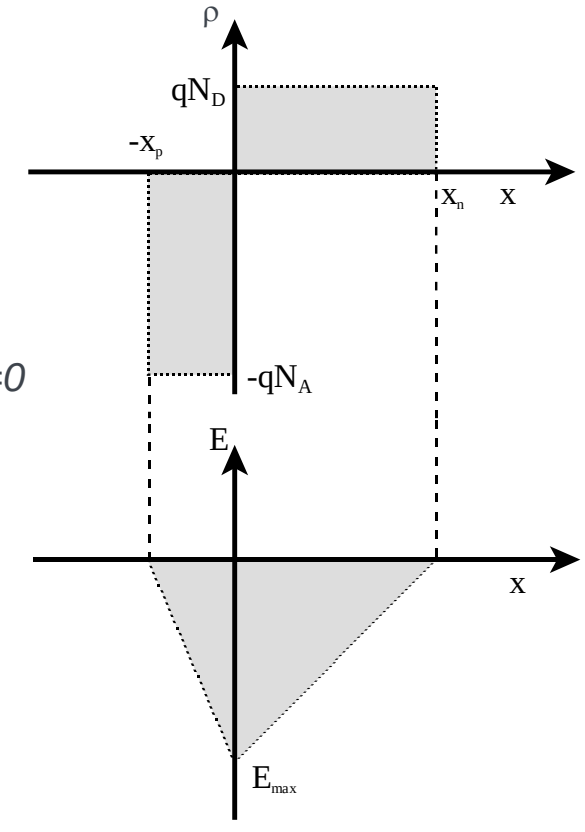
with boundary conditions: $E(-x_p)=0$ and $E(x_n)=0$

– Results:

$$-x_p \le x < 0: \; E(x) = -\frac{q \cdot N_A}{\varepsilon_{HL}\varepsilon_0}(x + x_p)$$

$$0 \le x \le x_n: \; E(x) = \frac{q \cdot N_D}{\varepsilon_{HL}\varepsilon_0} \cdot (x - x_n)$$

$$x \le -x_p \wedge x \ge x_n \quad E(x) = 0$$



p-n Junctions

Space charge, Fields and Potentials III

The potential distribution can be calculated by integration of the field (POISSON equation)

$$\boldsymbol{E} = -grad\,\phi \overset{1D}{=} \frac{d\phi}{dx}$$

with boundary condition $\phi(x \to -\infty) = \phi(-x_p) = 0$ and $\phi(x \to \infty) = \phi(x_n) = U_{Diff}$

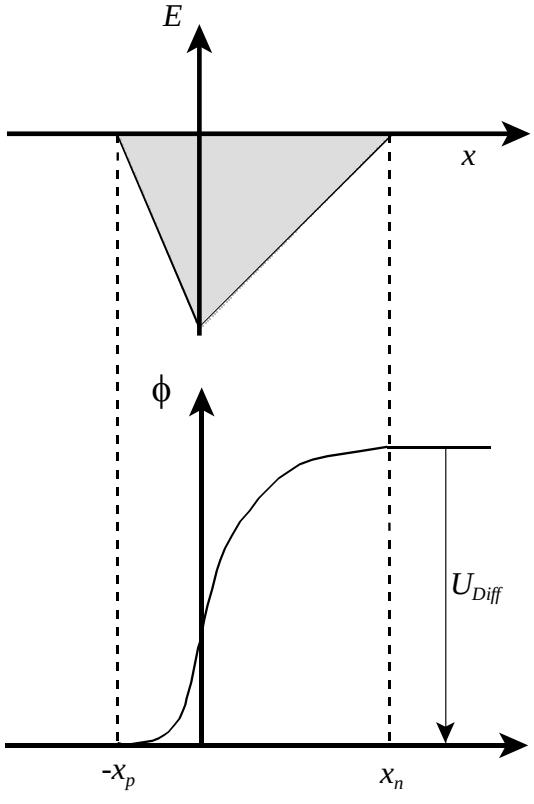
$$-x_p \le x < 0: \quad \phi(x) = \frac{q \cdot N_A}{\varepsilon_{HL}\varepsilon_0} \cdot \frac{(x + x_p)^2}{2}$$

$$0 \le x \le x_n: \quad \phi(x) = U_{Diff} - \frac{q \cdot N_D}{\varepsilon_{HL}\varepsilon_0} \cdot \frac{(x - x_n)^2}{2}$$

$$x \le -x_p: \quad \phi(x) = 0$$

$$x \ge x_n: \quad \phi(x) = U_{Diff}$$

$$U_{Diff} = \frac{k \cdot T}{q} ln\left(\frac{N_A N_D}{n_i^2}\right)$$



p-n Junctions

Space charge, Fields and Potentials IV

The function of the band edges is given by

$$E = -q\phi$$

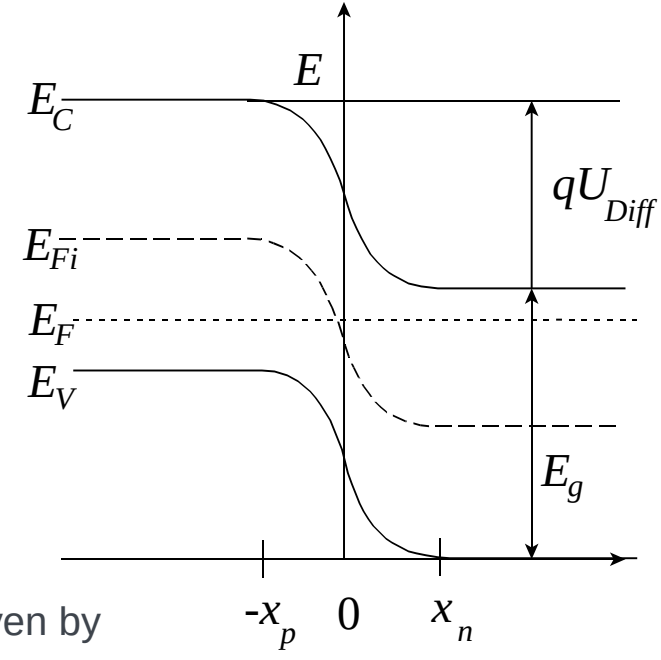
and follows directly from the potential distribution

- e.g. for the conduction band E_C in the range of $-x_p \leq x \leq 0$:

$$E_C(x) = E_C(-\infty) - \frac{q^2 N_A}{\varepsilon_{HL}\varepsilon_0} \cdot \frac{(x + x_p)^2}{2}$$

and for $0 \leq x \leq x_n$:

$$E_C(x) = E_C(-\infty) - qU_{Diff} + \frac{q^2 N_D}{\varepsilon_{HL}\varepsilon_0} \cdot \frac{(x - x_n)^2}{2}$$



- The function of the valence band E_V is given by

$E_C - E_V = E_g$ where E_g: band gap

p-n Junctions

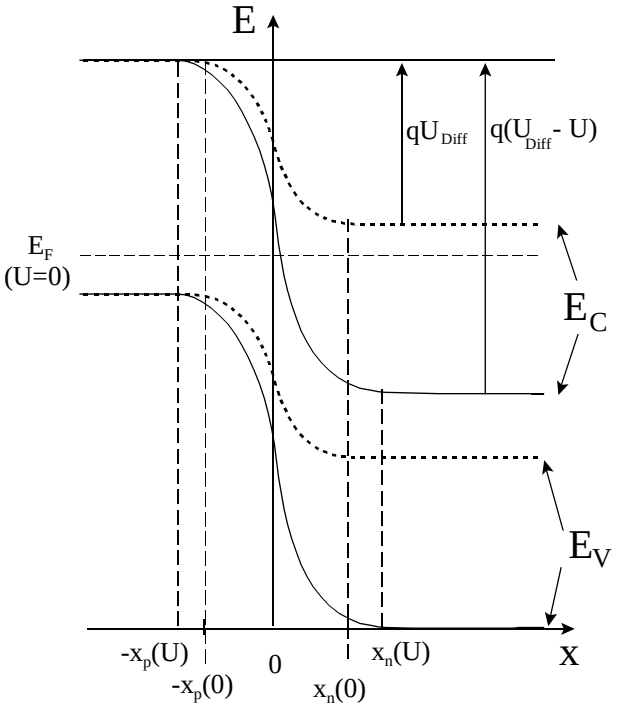
p-n junction in diode operation I

- What happens, if a voltage is applied to the p-n junction
  - *If the external voltage has the same sign as the diffusion voltage V_{diff}, the diffusion barrier is enlarged (band edges are bent stronger, field is increased)*

    ⇨ *Blocking mode*

  - *If diffusion voltage is compensated, the barrier is lowered or even diminishes*

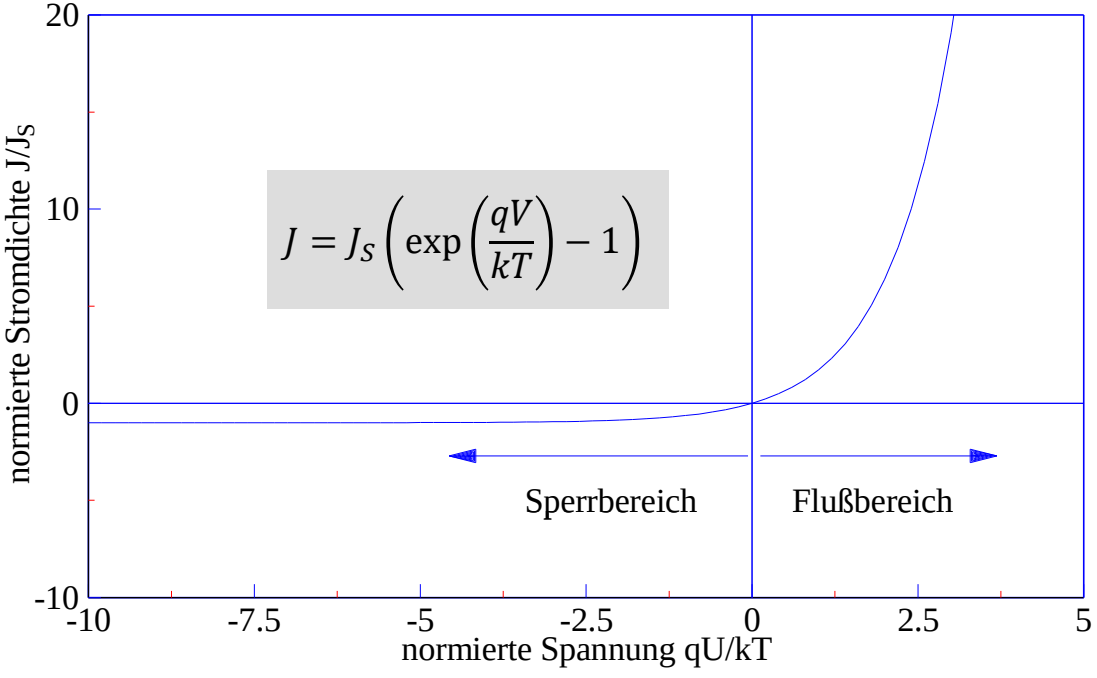
    ⇨ *Forward mode*



p-n Junctions

p-n junction in diode operation II

- i-v characteristics of p-n diode



J_S: saturation current density

p-n Junctions

p-n junction in diode operation III – width of space charge region

- taking into account charge neutrality

$$x_p N_A = x_n N_D$$

  and the equation for the diffusion voltage from slide 13, the width of the space charge region w_{RL} can be calculated

- without external bias it yields

$$w_{RL} = x_n + x_p = \sqrt{\frac{2\varepsilon_0 \varepsilon_{HL} U_{Diff}}{q} \cdot \left(\frac{1}{N_A} + \frac{1}{N_D} \right)}$$

- with an external bias U it is slightly modified into

$$w_{RL} = \sqrt{\frac{2\varepsilon_0 \varepsilon_{HL} (U_{Diff} - U)}{q} \cdot \left(\frac{1}{N_A} + \frac{1}{N_D} \right)}$$

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The MOS Structure and MOS Field-Effect Transistors

What are the basic principles for transistor operation, operating modes, specialities of the device architecture

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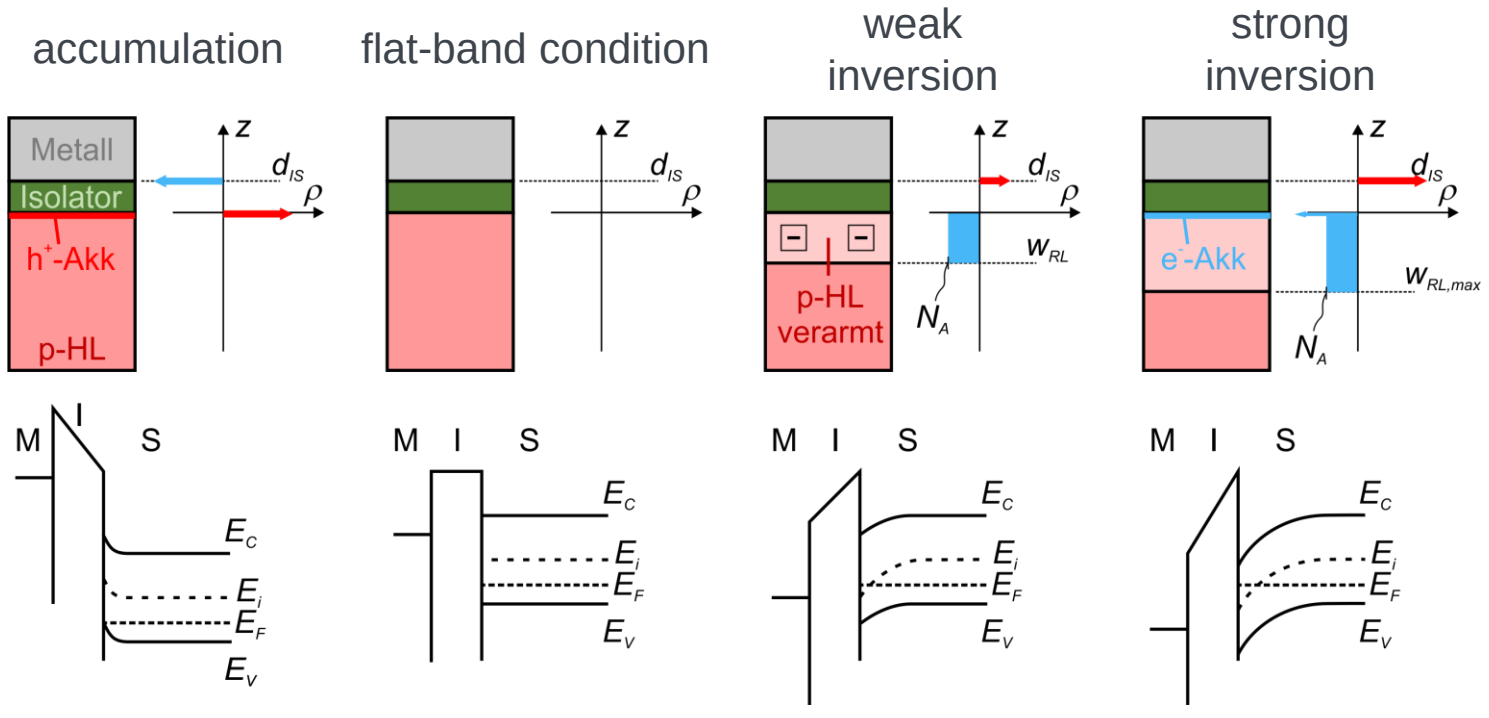
The MOS Structure and Field-Effect Transistors

Operating modes of a MOS structure (MOS diode)

- MOS = Metal-Oxide-Semiconductor, in general also MIS / Metal-Insulator-Semiconductor



M: metal, I: insulator, S: semiconductor, ρ: charge density

The MOS Structure and Field-Effect Transistors

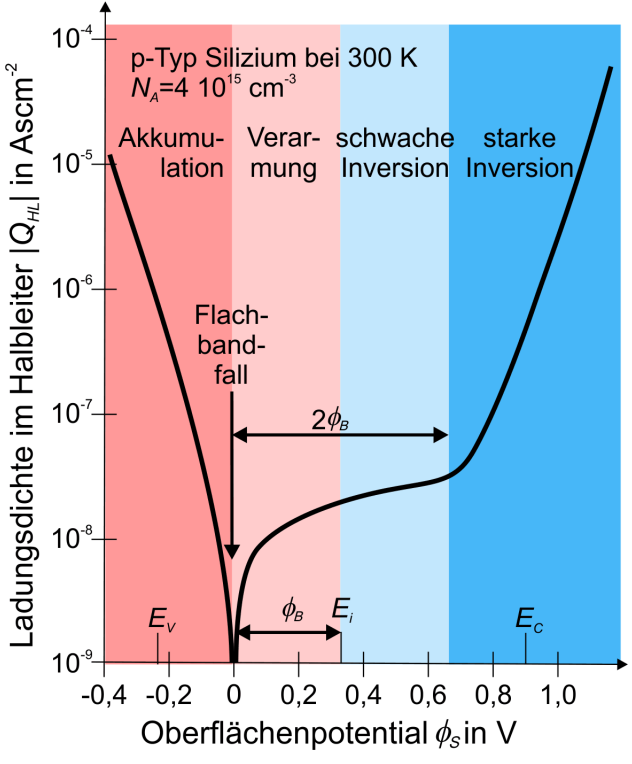
Charge density @ interface (transistor channel)

- Areal carrier density (in the semiconductor) depends on the interface potential ϕ_S
  - *exponential increase of the carrier density at the semiconductor surface in accumulation and strong inversion*
  - *strong inversion from maximum extension of SCR*

$$w_{RL,\max} = \sqrt{\frac{4\varepsilon_0\varepsilon_{HL}|\phi_B|}{qN_A}} \quad \text{where} \quad \phi_B = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)$$

  - extremly high density of free carriers after entering into strong inversion
  - strong band bending ϕ_B effects minority carrier density at the interface exceeding majority carrier density in the volume

⇨ *Appearence of a conduction channel*



The MOS Structure and Field-Effect Transistors

Threshold voltage of a MOSFET

- The threshold voltage is evaluated at $\phi_S = 2\phi_B$:

$$U_{Th} = U_{FB} - \frac{Q_{HL}}{C_{IS}} + 2\phi_B \qquad \text{mit} \qquad U_{FB} = \varphi_M - \left(\chi_{Si} + \frac{E_g}{2q} + \varphi_B \right) - \frac{Q_{IS}}{C_{IS}}$$

$$Q_{HL} = \pm\sqrt{4\varepsilon_0 \varepsilon_{HL} q N |\phi_B|}$$

+: n-type ($N = N_D$)
-: p-type ($N = N_A$)

$$\text{p - HL}: \phi_B = \frac{kT}{q} ln \frac{N_A}{n_i} \qquad \text{n - HL}: \phi_B = \frac{kT}{q} ln \frac{n_i}{N_D}$$

$$C_{IS} = \frac{\varepsilon_{IS}\, \varepsilon_0}{x_{IS}}$$

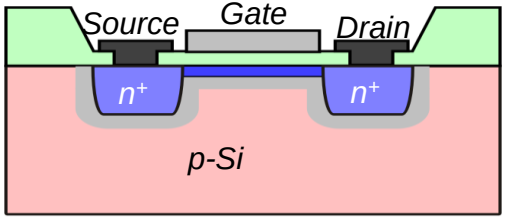
$$Q_{IS} = Q_{V,eff} + Q_A$$

U_{FB}:	flat-band voltage
ϕ_M:	gate work function
χ_{Si}:	electron affinity of silicon
E_g:	band gap of silicon
q:	unity charge
x_{IS}:	insulator thickness
$Q_{V,eff}$:	eff. insulator volume charge
Q_A:	interface charge of insulator

The MOS Structure and Field-Effect Transistors

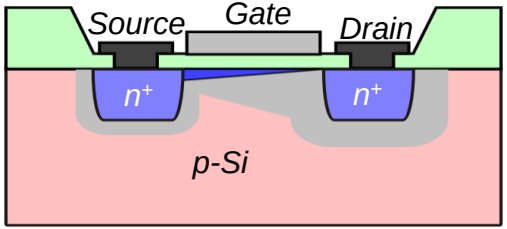
Operating modes MOSFET

- For n-channel MOSFET
  - *Linear region*



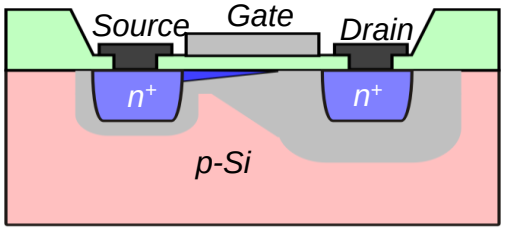
$$0 < U_D << U_G - U_{Th}$$

  - *Triode region*



$$0 < U_D < U_G - U_{Th}$$

  - *Saturation region*



$$U_D > U_G - U_{Th}$$

The MOS Structure and Field-Effect Transistors

Modeling of MOSFETs

- Transistor equations (n-channel) for long and wide channels
  - *OFF state ($U_G - U_{Th} < 0$)*

$$I_D = 0 \qquad (1)$$

  - Linear and triode region ($0 < U_D < U_G - U_{Th}$)

$$I_D = \beta\left((U_G - U_{Th})\,U_D - \frac{U_D^{\,2}}{2}\right) \qquad (2)$$

  - Saturation region ($U_D > U_G - U_{Th}$)

$$I_D = \frac{\beta}{2}(U_G - U_{Th})^2 \qquad (3)$$

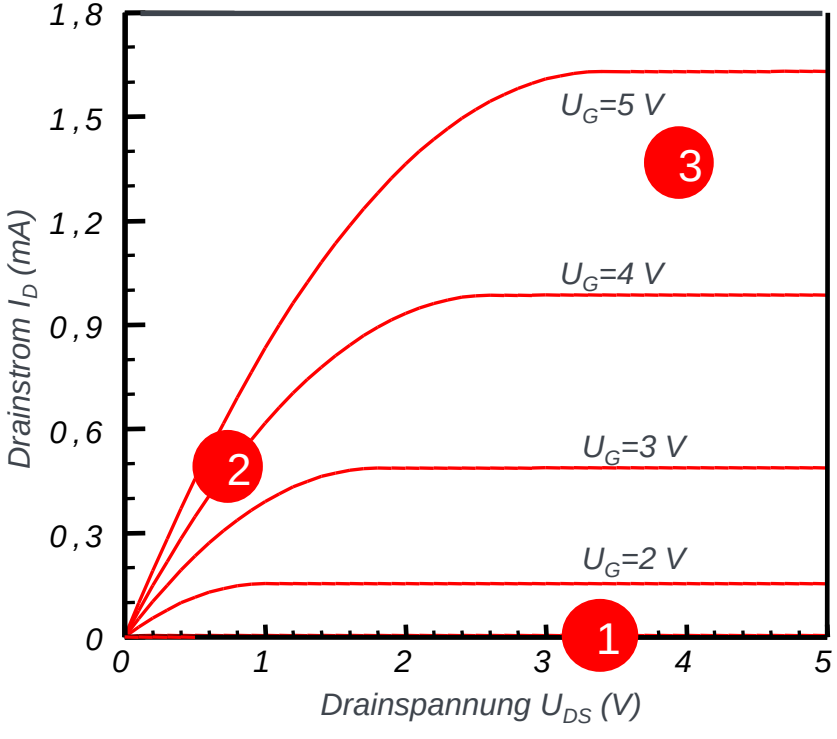
$$\beta = \mu\, C_{IS}\, \frac{W}{L}$$

The MOS Structure and Field-Effect Transistors

MOSFET characteristics

- Output characteristics

  (W=6 µm, L=3 µm, U_{Th}=0,8V, d_{IS}=20nm, μ_0=750cm²/Vs)



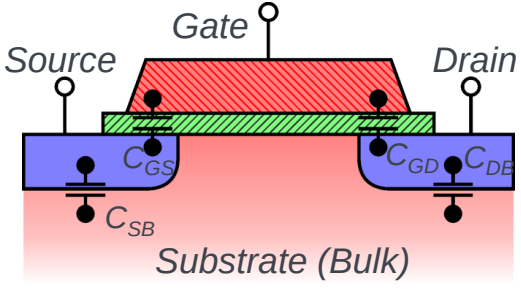
– Transconductance (saturation region):

$$g_m = \left.\frac{\partial I_D}{\partial U_G}\right|_{U_D=\text{const}} \overset{\text{z.B.}}{=} \beta\left(U_G - U_{Th}\right)$$

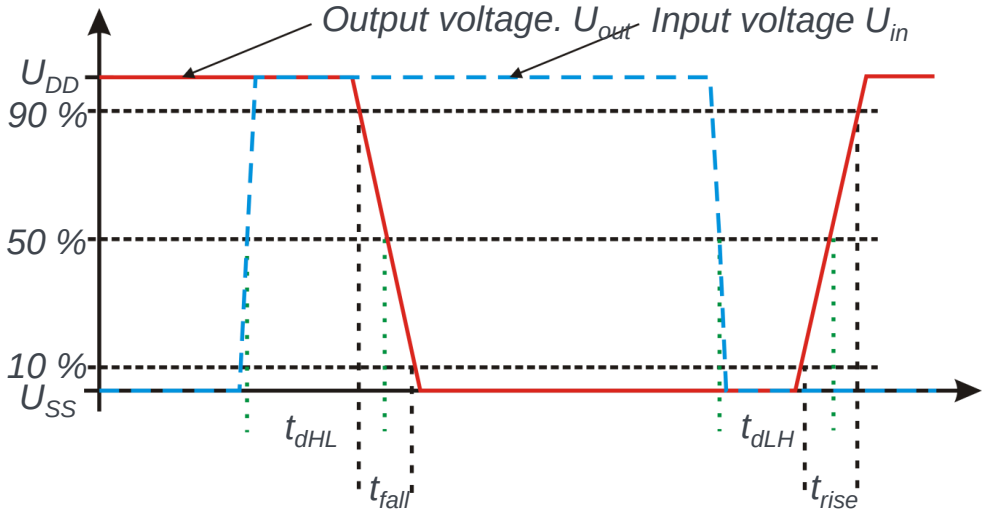
The MOS Structure and Field-Effect Transistors

Parasitic elements in MOSFETs

- Delay time in CMOS circuits
  - *Due to: re-charging of FET capacities and capacities of wiring*



$$t_d = C_{ges} \cdot \frac{\Delta U}{I} \approx \frac{2\,C_{ges}}{\mu\,C_{IS}U_{DD}} \cdot \frac{L}{W}$$



- *Counter-measure: reduce C_{ges}*

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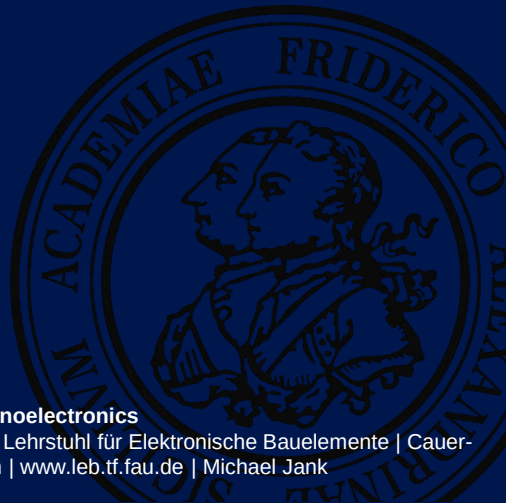
Processing of Integrated Circuits

e.g. n-channel transistor in a CMOS flow



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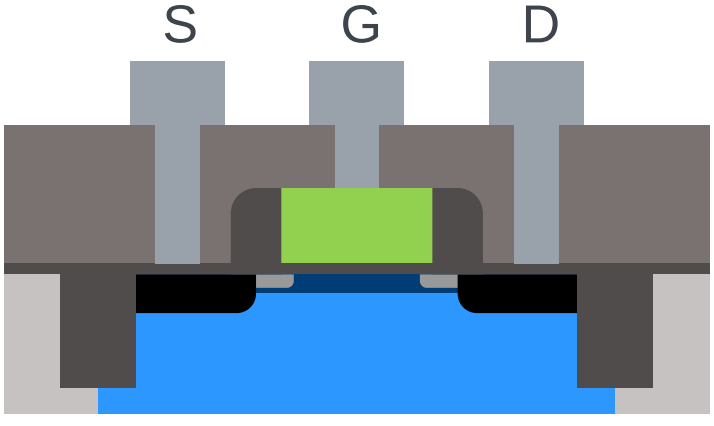
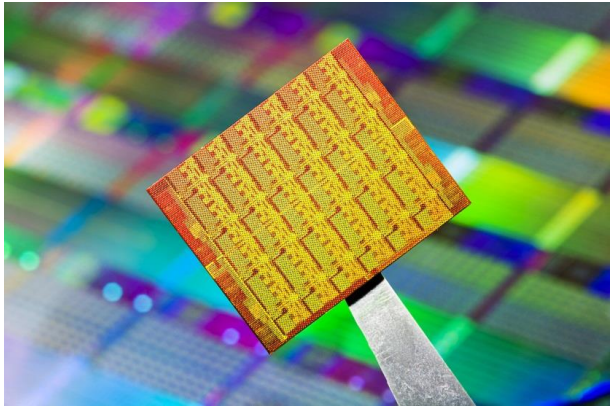
Processing of Integrated Circuits

CMOS process integration

- Processing of metal-oxide-silicon field-effect transistor (MOSFET)





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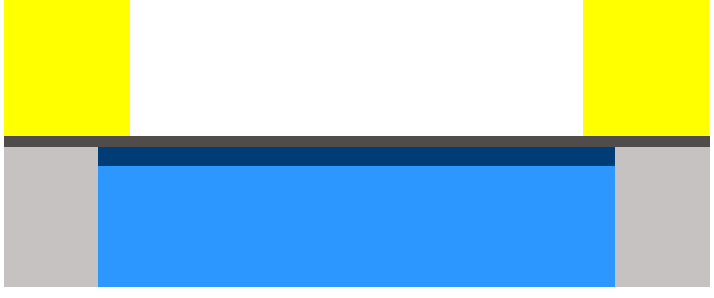
Processing of Integrated Circuits

CMOS process integration

- Processing of metal-oxide-silicon field-effect transistor (MOSFET)



1. n doped substrate
2. sacrificial oxide
3. p well lithography [1]
4. p well implantation
5. n channel implantation
6. resist removal
7. *n well Lithography [2]*
8. *n well implantation*
9. *p channel implantation*
10. *resist removal*
11. implant anneal
12. removal of sacrificial oxide

…

Processing of Integrated Circuits

CMOS process integration

- Processing of metal-oxide-silicon field-effect transistor (MOSFET)

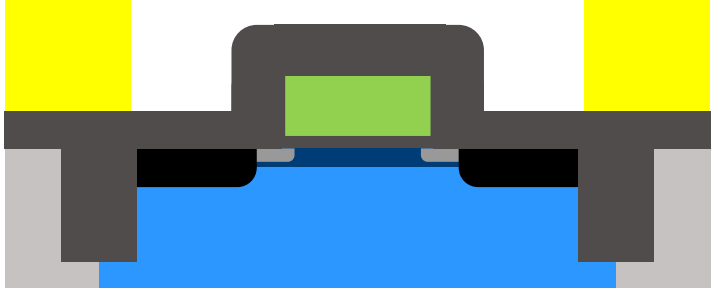
13. sacrificial oxide
14. lithography insulation [3]
15. RIE shallow trench
16. resist removal
17. oxidation
18. CVD oxide (trench fill)
19. CMP
20. back etch
21. gate oxidation
22. polysilicon deposition
23. polysilicon lithography [4]
24. RIE poly gate
25. resist removal

…

Processing of Integrated Circuits

CMOS process integration

- Processing of metal-oxide-silicon field-effect transistor (MOSFET)

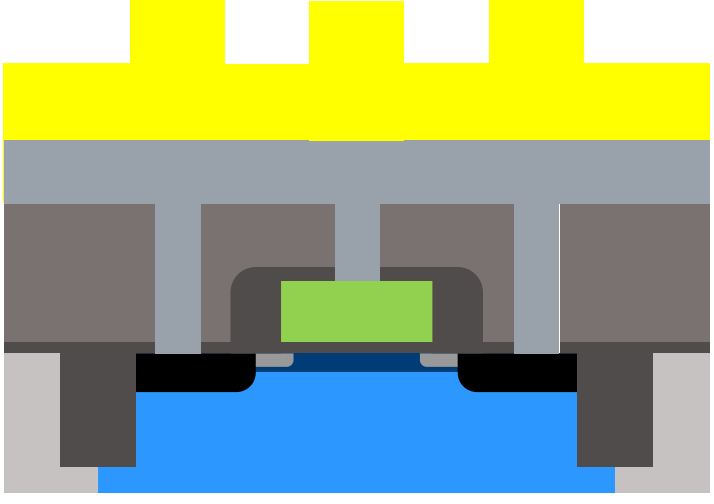


26. Oxidation polysilicon
27. lithography n channel / LDD [5]
28. ion implantation LDD
29. resist removal
30. *lithography p channel / LDD [6]*
31. *ion implantation LDD*
32. *resist removal*
33. CVD TEOS oxide
34. back etch
35. substrate oxidation
36. lithography n channel [7]
37. n contact implant
38. resist removal
39. *lithography p channel [8]*
40. *p contact implantation*
41. *resist removal*

Procesisng of Integrated Circuits

CMOS process integration

- Processing of metal-oxide-silicon field-effect transistor (MOSFET)



42. etching sacrificial oxide
43. liner oxidation
44. CVD TEOS/BPSG oxide
45. anneal / reflow
46. CMP
47. lithography via [9]
48. RIE/wet etch via
49. resist removal
50. clean, metal conditioning
43. barrier metallization
44. aluminum deposition
45. CMP
46. lithography metal [10]
47. RIE Metall
48. resist removal

…

Nanoelectronics – p-n Junctions and MOS Devices
Contents

- p-n Junctions
  - *Band-structure models and contact between p and n type semiconductors*
  - *Charge, field and potential distributions*
  - *Diode operation*
  - *Width of space-charge region*
- The MOS Structure and MOS Field-Effect Transistors
  - *Operation modes of the MOS diode*
  - *Threshold voltage of MOSFETs*
  - *Operation ranges of MOSFETs*
  - *Modelling of MOSFETs*
  - *Parasitic elements of MOSFETs*
- Processing of Integrated Circuits

Thanks for your attention!