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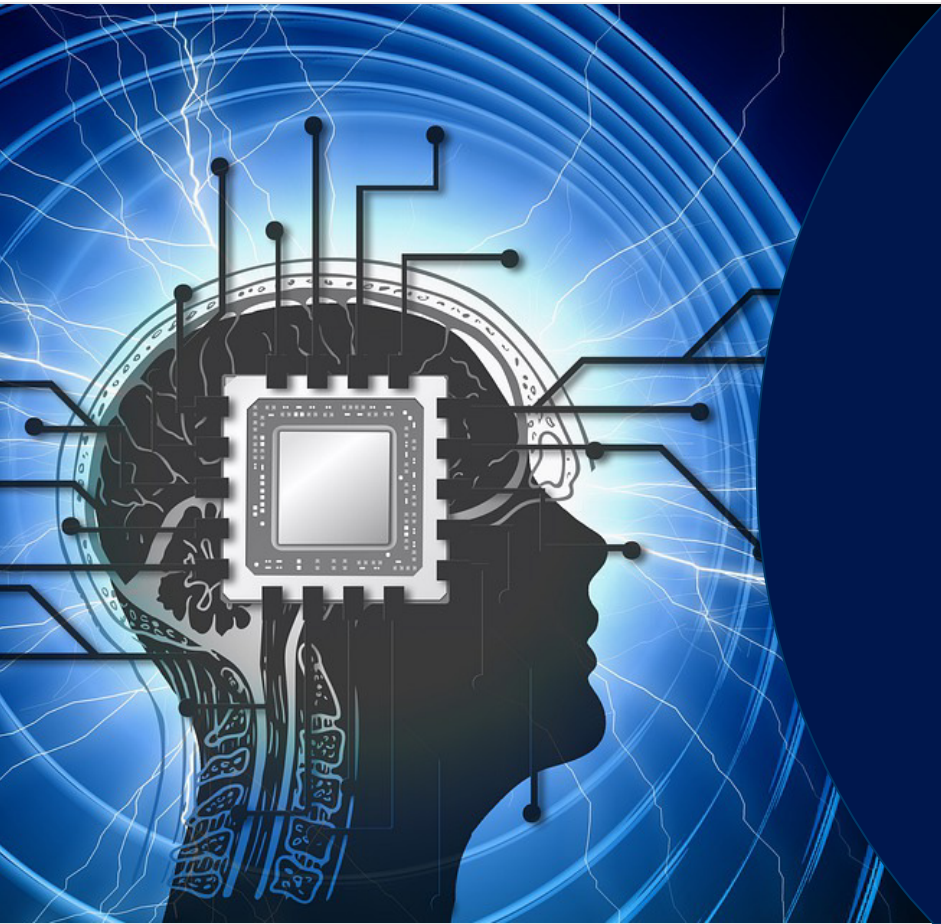


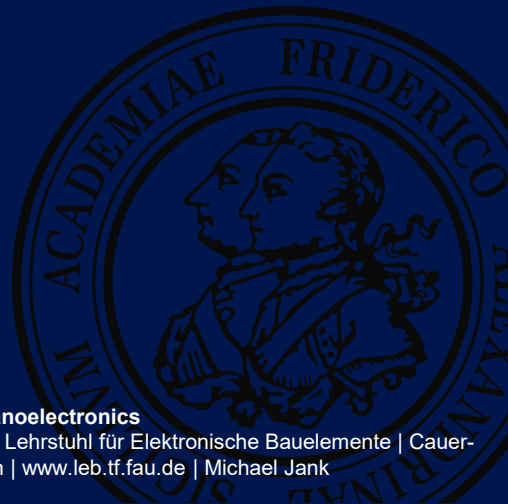
Halbleitertechnik IV- Nanoelectronics

Friedrich-Alexander-Universität Erlangen-Nürnberg | Lehrstuhl für Elektronische Bauelemente | Cauerstraße 6 | 91058 Erlangen | www.leb.tf.fau.de | Michael Jank

Short-channel effects

Objectives of the lecture

Mission and goals?



Short Channel Effects

Objectives

- You should take away the effects of aggressive scaling of devices according to the scaling paradigms on both the electrical parameters of devices as well as secondary aspects like reliability
- In particular, the issue of leakage currents as well as different mechanisms behind,
- geometrical effects from short and narrow channels and
- degradation by strongly accelerated carriers

will be discussed

Short Channel Effects

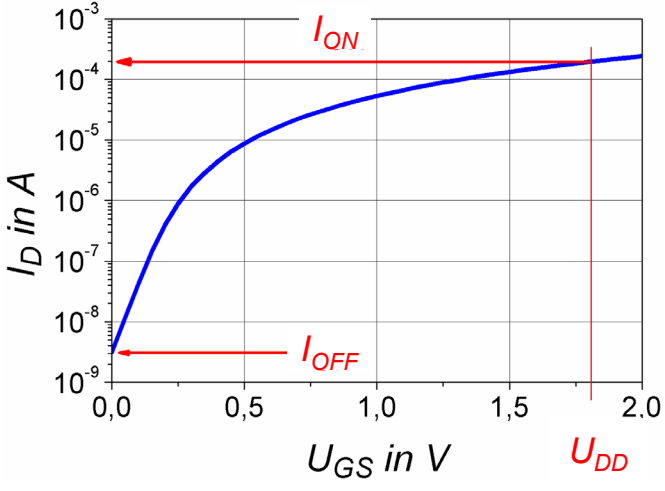
Outline

- Leakage currents in MOS transistors
- Geometrical and layout effects in scaling
  - *p-n junctions*
  - *subthreshold current*
  - *Drain-Induced Barrier Lowering (DIBL) and Punch Through*
  - *charge sharing model*
  - *narrow channel effect*
- Degradation by hot carriers
  - *hot holes from avalanche multiplication*
  - *channel hot electrons*

Short Channel Effects

Leakage Currents

- Scaling of MOS devices may be accompanied by unwanted effects
- Reduction of the ratio of ON-level of saturation current when MOSFET is fully conducting to OFF-Level current in subthreshold regime (I_{ON}/I_{OFF} ratio)
- Other leakage currents
- Short channel effects
- Reliability aspects
- Wiring issues

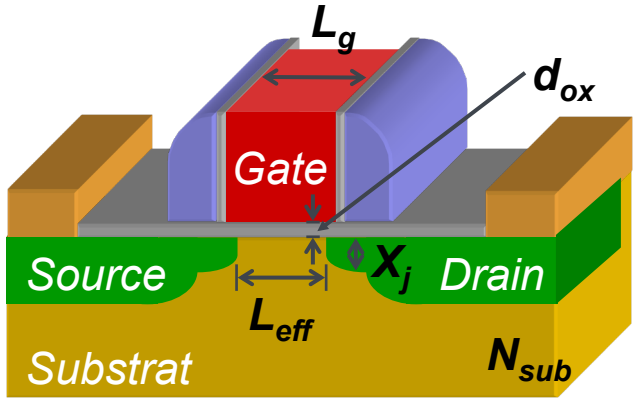


Transfer characteristics

Short Channel Effects

Leakage Currents

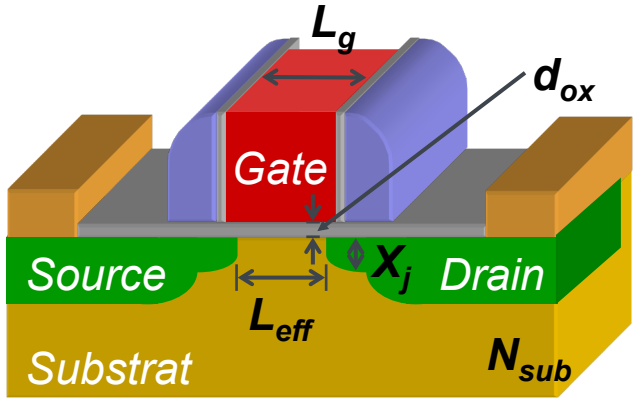
- Leeakage currents are the most critical issue in scaling
- Desired:
  - *maximum ON current ($I_{ON} = I_{Dsat}$)*
  - *minimum OFF current*
- Impact of scaling rules on (leakage) currents
- Increased substrate doping concentration
  - *lower mobility ($I_{ON}\downarrow$),*
  - *higher p-n capacitance: typicallly only observed during switching, not directly related to ON or OFF currents. However, higher currents are needed for (re-)charging of p-n junctions, when capacitance is higher ($I_{ON}\downarrow$).*
  - *band-to-band tunnel currents at p-n junctions ($I_{OFF}\uparrow$)*
  - *higher defect densities lead to charge carrier generation in blocked p-n junctions ($I_{OFF}\uparrow$)*



Short Channel Effects

Leakage Currents

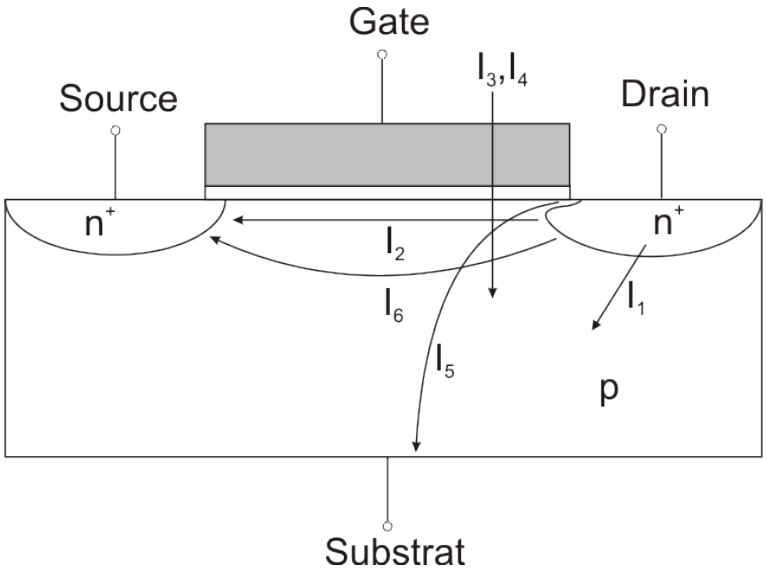
- Leakage currents are the most critical issue in scaling
- Desired:
  - *maximum ON current ($I_{ON} = I_{Dsat}$)*
  - *minimum OFF current*
- Impact of scaling rules on (leakage) currents
- Reduced thickness of gate dielectrics
  - *Tunneling leads to an increase in gate leakage ($I_{OFF}\uparrow$)*
- (Ultra-)shallow p-n junctions at Source and Drain
  - *increased series resistance (laterally) R_{SD} ($I_{ON}\downarrow$)*
- Problems are partly addressed by relaxed constant field scaling
  - *e.g. weaker scaling of gate insulator thickness by $\beta < \alpha$*
  - *however, for meeting all demands of scaling, especially in sub-100 nm technologies, new materials/architectures are mandatory*



Short Channel Effects

Leakage Currents

- Overview of leakage and short channel effects



K. Roy et al., Proceedings of the IEEE 91, 305 (2003), technical current orientation

- I_1: blocking current p-n diode
- I_2: subthreshold current MOSFET
- I_3: gate leakage current
- I_4: injection of hot electrons
- I_5: Gate Induced Drain Leakage (GIDL)
- I_6: punch through

Assignment to

- geometry or architecture
- tunneling
- degradation

Short Channel Effects

Outline

- Leakage currents in MOS transistors
- Geometrical and layout effects in scaling
  - *p-n junctions*
  - *subthreshold current*
  - *Drain-Induced Barrier Lowering (DIBL) and Punch Through*
  - *charge sharing model*
  - *narrow channel effect*
- Degradation by hot carriers
  - *hot holes from avalanche multiplication*
  - *channel hot electrons*

Short Channel Effects

Geometrical and layout effects in scaling

- Blocking currents in p-n junctions
- Drift / diffusion of minority carriers
  - *reverse saturation current is related to doping concentration*
  - $$j_S = q n_i^2 \left(\frac{D_n}{L_n N_A} + \frac{D_p}{L_p N_D} \right)$$

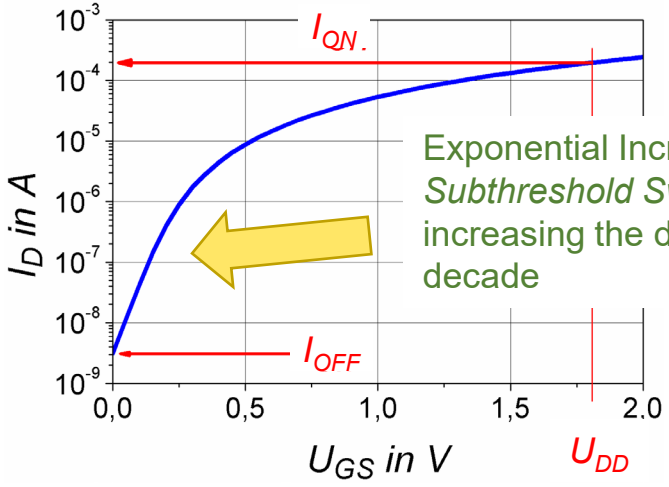
    then: $N_{A,D}\uparrow \rightarrow I_{rev}\downarrow$
  - *consider also decreasing minority carrier lifetimes or diffusion lengths with increasing doping concentrationdue to increased defect concentration > effect may be neglected against doping concentration effect*
- Generation and recombination current
  - *increasing defect concentration leads to an increase in leakage current:* $N_{A,D}\uparrow \rightarrow I_{GEN,REK}\uparrow$
- Band-to-band tunneling $N_{A,D} \uparrow \rightarrow I_{rev}\uparrow$
  - *see chapter on tunneling*

Short Channel Effects

Geometrical and layout effects in scaling

- Subthreshold current / subthreshold swing S

$$S = \ln 10 \cdot \frac{kT}{q}\left(1+\frac{C_{HL}}{C_{OX}}\right) = 2{,}3 \cdot \frac{kT}{q}\left(1+\frac{C_{HL}}{C_{OX}}\right)$$



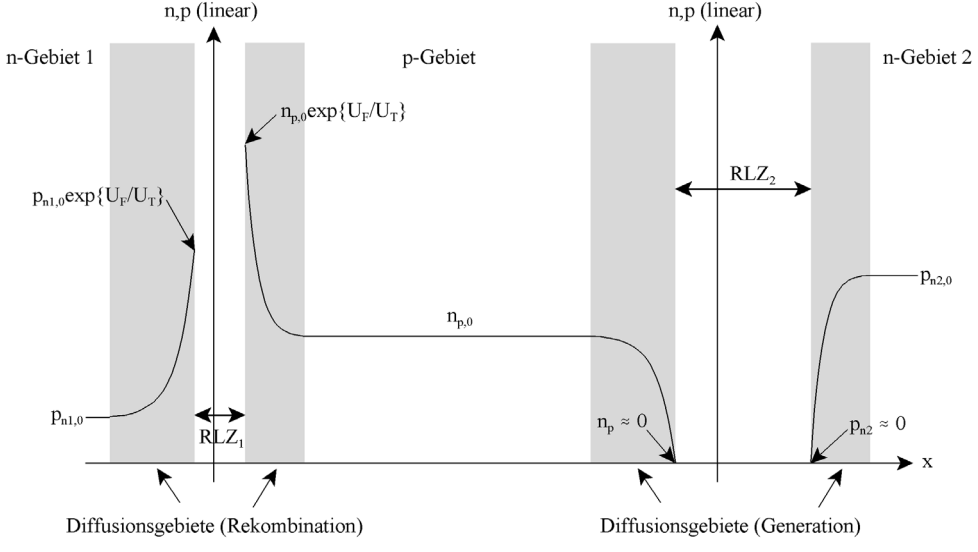
Transfer characteristics

Exponential Increase of drain current at $U_{GS} < U_{TH.}$
Subthreshold Swing described the voltage needed for increasing the draun current by a factor of 10, i.e. a decade

Short Channel Effects

Geometrical and layout effects in scaling

- Subthreshold current / subthreshold swing S: modeling
- *Consider channel area (Source-Substrate-Drain) as a bipolar junction transistor*
  - *distribution of base minority carriers by charge triangle (e.g. Halbleiterbauelemente, Nano IV)*



Short Channel Effects

Geometrical and layout effects in scaling

- Subthreshold current / subthreshold swing S: modeling
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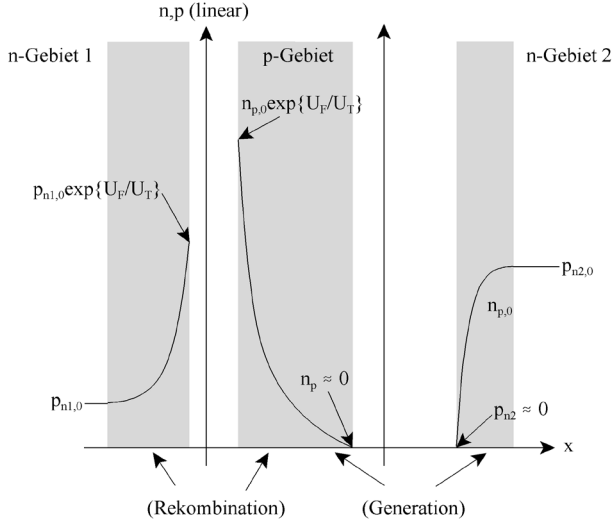
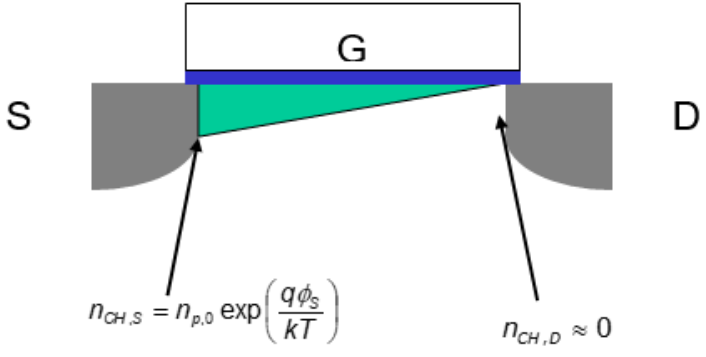




Short Channel Effects

Geometrical and layout effects in scaling

- Subthreshold current / subthreshold swing S: modeling
- *The diffusion current in subthreshold can be calculated as*

$$I_D = AqD_n \frac{dn}{dx} = AkT\mu \frac{n_{CH,S} - 0}{L} = A \frac{kT\mu n_i^2}{LN_A} \exp\left(\frac{q\phi_S}{kT}\right)$$

  - *the crossection A is the width W of the transistor times depth d_{HL} of minority carrier distribution*

$$d_{HL} = \frac{kT}{qE_S} = \frac{kT\sqrt{\varepsilon_0 \varepsilon_{HL}}}{q\sqrt{2qN_A\phi_S}}$$

decay length of surface potential, reduction by *kT/q*

Short Channel Effects

Geometrical and layout effects in scaling

- Subthreshold current / subthreshold swing S: modeling
- *According to the definition of subthreshold swing S*

$$S = \left(\frac{d \log I_D}{dU_{GS}} \right)^{-1} = \ln 10 \cdot \left(\frac{d \ln I_D}{dU_{GS}} \right)^{-1}$$

  - *the drain current from diffusion triangle*

$$\ln I_D = \ln\left(A \frac{kT \mu n_i^2}{L N_A} \right) + \frac{q \phi_S}{kT}$$

  - *is differentiated to yield*

$$\frac{d \ln I_D}{dU_{GS}} = \frac{d}{dU_{GS}} \ln\left(A \frac{kT \mu n_i^2}{L N_A} \right) + \frac{d}{dU_{GS}} \frac{q \phi_S}{kT} \approx 0 + \frac{q}{kT} \cdot \frac{d \phi_S}{dU_{GS}}$$

Short Channel Effects

Geometrical and layout effects in scaling

- Subthreshold current / subthreshold swing S: modeling
- *the modification of surface potential is given by charge vs. voltage considerations*

$$\frac{dQ_{HL}}{dU_{GS}} = C_{ges}$$

- *and accordingly*
-

$$Q_{HL} = \sqrt{2\varepsilon_0 \varepsilon_{HL} q N_A \phi_S}$$

$$\frac{dQ_{HL}}{d\phi_S} = \sqrt{2\varepsilon_0 \varepsilon_{HL} q N_A} \cdot \frac{1}{2} \phi_S^{-\frac{1}{2}} = \sqrt{\frac{\varepsilon_0 \varepsilon_{HL} q N_A}{2\phi_S}} = C_{HL}$$

is derived after differentiation for ϕ_S

- *Please also be aware that in this case the charging/decharging of the semiconductor is exclusively guided by extension or reduction of the SCR (subthreshold!)*

Short Channel Effects

Geometrical and layout effects in scaling

Subthreshold current / subthreshold swing S: modeling

- *altogether, the derivative of ϕ_S against U_{GS} is given by*

$$\frac{d\phi_S}{dU_{GS}} = \frac{dQ_{HL}}{dU_{GS}} \cdot \frac{d\phi_S}{dQ_{HL}} = \frac{C_{ges}}{C_{HL}} = \frac{C_{OX}}{C_{OX} + C_{HL}} = \left(1 + \frac{C_{HL}}{C_{OX}}\right)^{-1}$$

- *and the subthreshold swing can accordingly be calculated as*

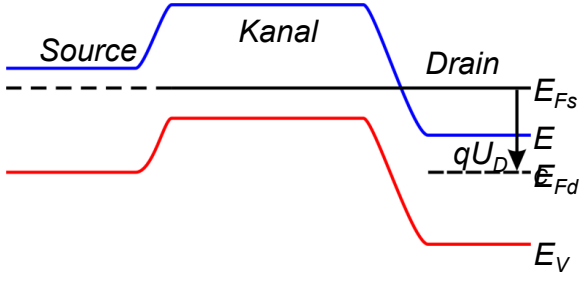
$$S = \ln 10 \cdot \frac{kT}{q}\left(1 + \frac{C_{HL}}{C_{OX}}\right) = 2{,}3 \cdot \frac{kT}{q}\left(1 + \frac{C_{HL}}{C_{OX}}\right)$$

Short Channel Effects

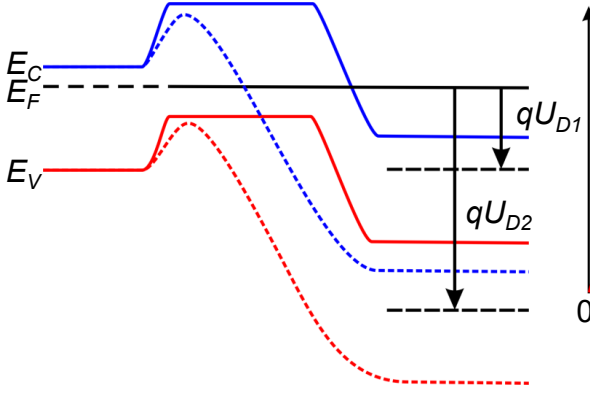
Geometrical and layout effects in scaling

Punch-through effect (MOSFET *OFF*)

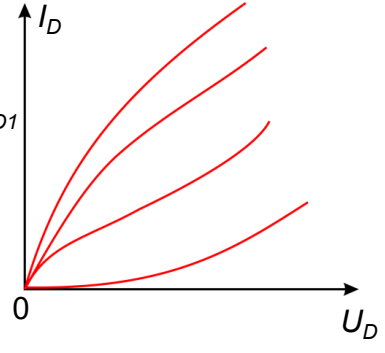
- *Drain SCR extends over the entire channel towards Source SCR*
  - potential barrier at Source is reduced
  - drain current is strongly increased
- *Main factors*
  - drain-source and gate-bulk-voltages
  - *Doping concentration*



Band diagramm before Punch Through



Band diagram in Punch Through



Modification of output curve by Punch Through

Short Channel Effects

Geometrical and layout effects in scaling

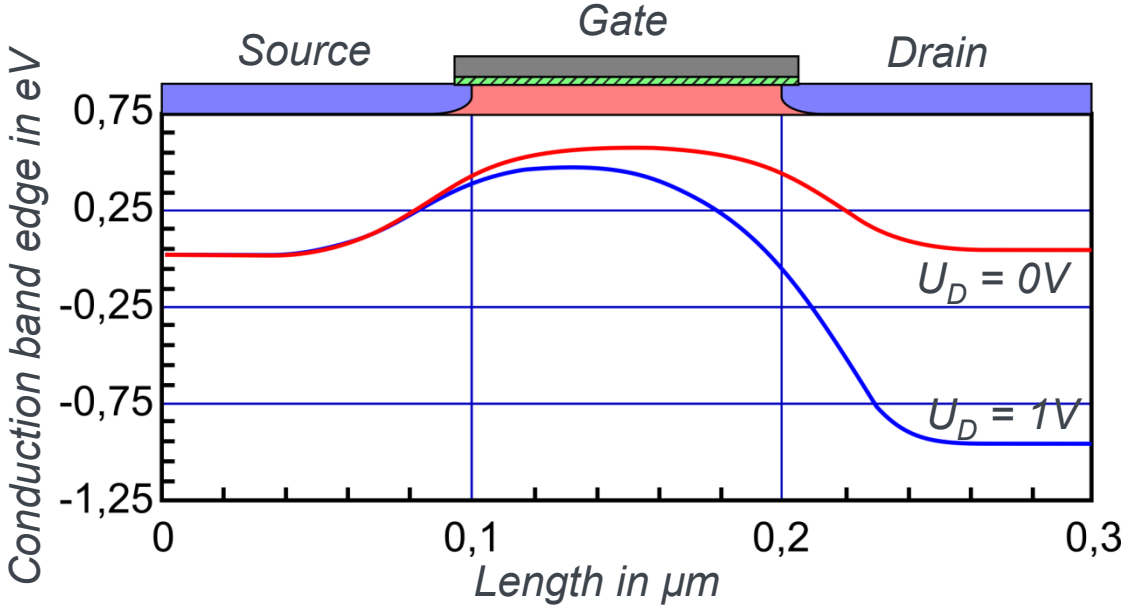
Drain-induced barrier lowering DIBL for short channels

- *Extension of SCRs is dependent on drain-to-source voltage*
- *for $U_{DS} > 0$ the drain-to-bulk SCR reaches source and reduces the barroer height at the source-substrate junction*
- *reduced threshold voltage can be observed*

DIBL factor σ:

$$\Delta U_{Th} = -\sigma U_D$$

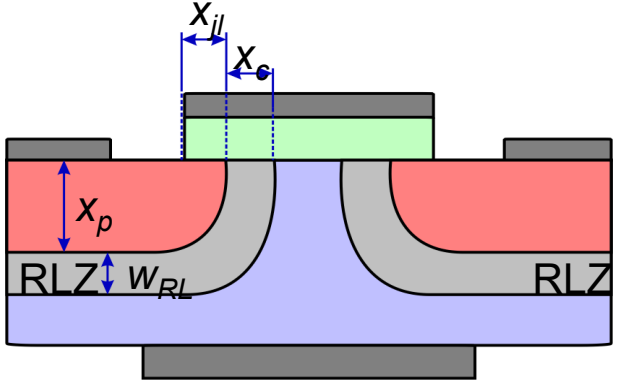
$$\sigma \sim \frac{(d_{IS} / nm)}{(L / \mu m)^3}$$



Short Channel Effects

Geometrical and layout effects in scaling

- Charge sharing in short channel transistors
  - *p-n junctions of source and drain reduce the absolut channel charge*
    - less charge on the gate is needed for turning on the MOSFET
    - *reduction of U_{TH} (roll-off) for short channels*
  - *charge-separation factor F_S*



$$F_s = 1 - \frac{x_c + x_{jL}}{L}\sqrt{1 - \left(\frac{x_p}{x_p + w_{RL}}\right)^2} - \frac{x_{jL}}{L}$$

x_c, x_{jL}: process dependent

$$w_{RL} = \sqrt{\frac{2\varepsilon_0\varepsilon_{Si}}{N_{Sub}} \cdot (U_B + U_{diff})}$$

U_B: Bulk-Source voltage

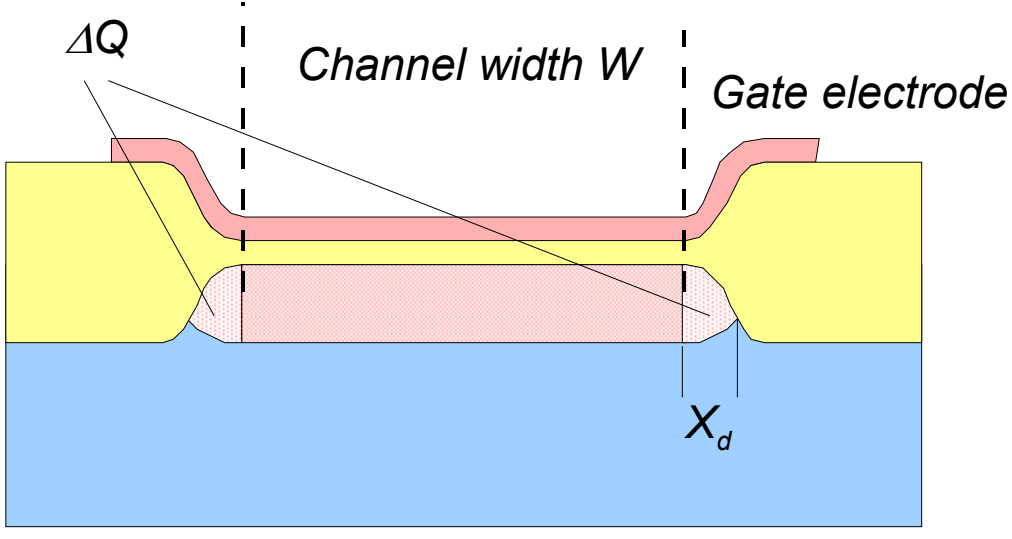
- *Impact on threshold voltage*

$$U_{Th} = U_{FB} + 2\phi_B + \gamma F_s\sqrt{2\phi_B - U_B}$$

Short Channel Effects

Geometrical and layout effects in scaling

- Narrow-channel effect



Increasing U_{TH}

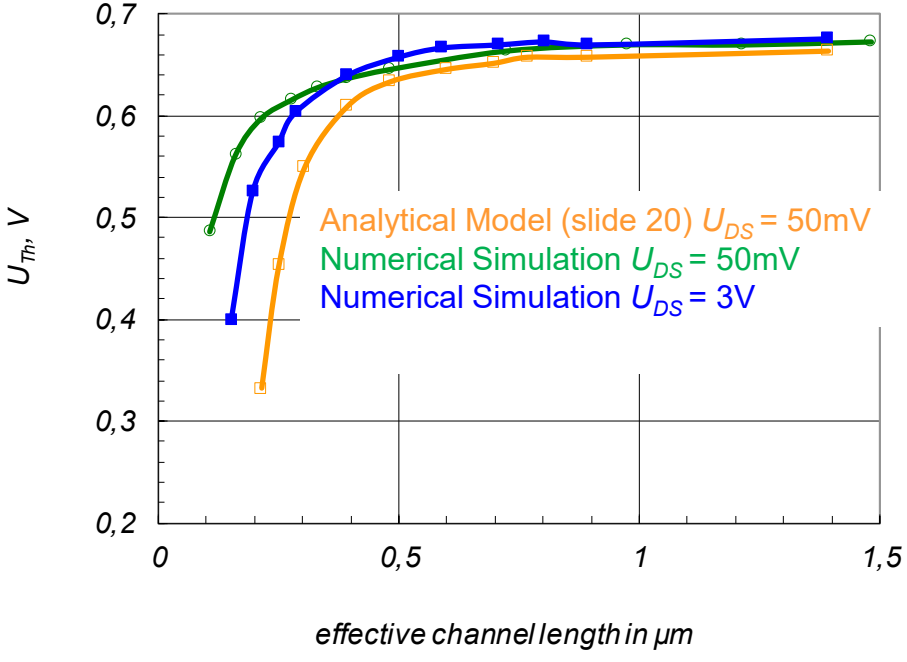
$$\Delta U_{Th} = \frac{\delta \pi \varepsilon_{Si}}{4 C_{IS} W} \cdot \left(2\phi_B - U_B\right)$$

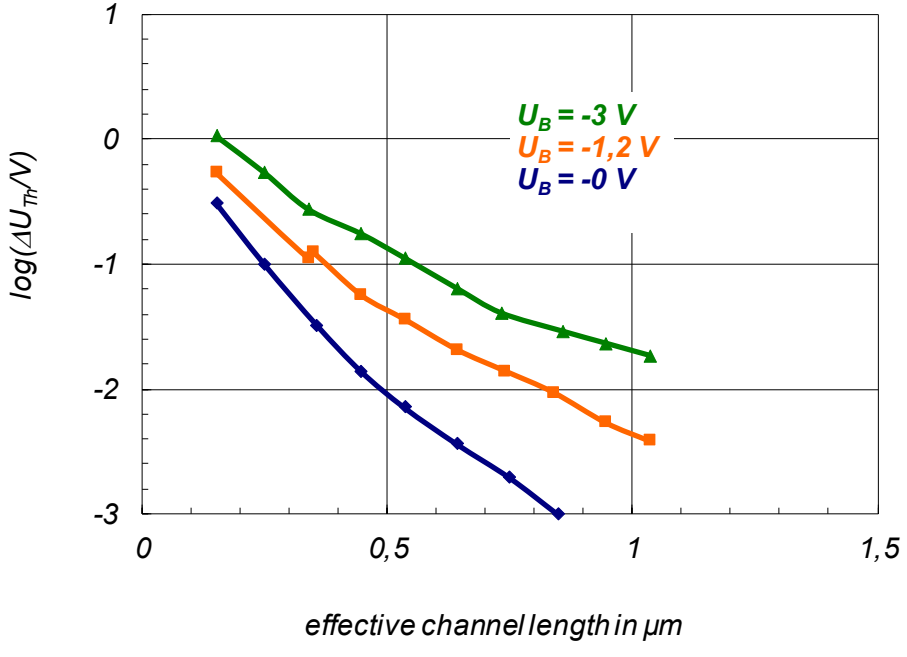
δ: process dependent parameter

Short Channel Effects

Geometrical and layout effects in scaling

- Reduction of U_{TH} by charge sharing and DIBL





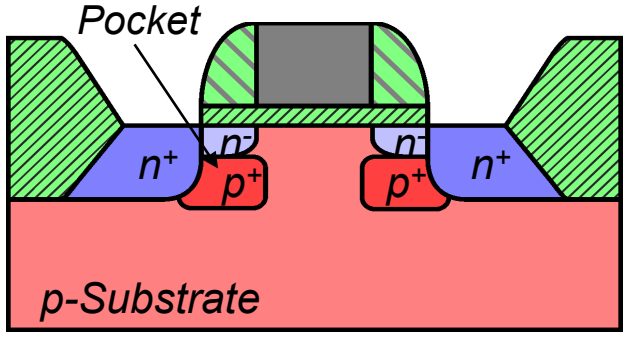
- Both effects decrease threshold voltage

Short Channel Effects

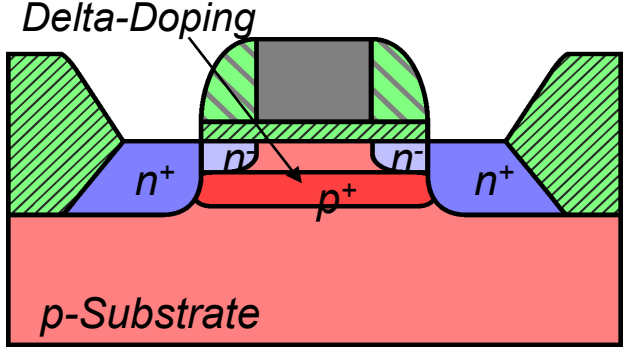
Geometrical and layout effects in scaling

- Measures for reduction of roll-off and Punch Through
  - *local increase of substrate doping below the channel for less SCR widths*

HALO- / Pocket-Implantation



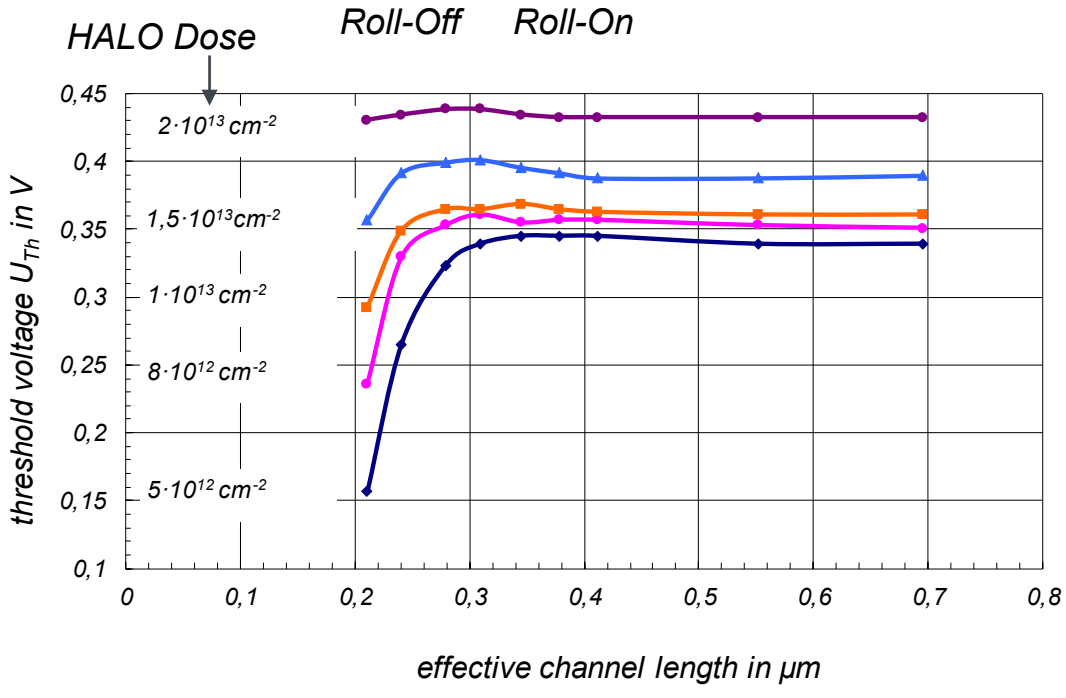
Delta-Doping (Punch-Through)



Short Channel Effects

Geometrical and layout effects in scaling

- Measures for reduction of roll-off and Punch Through



After Wann et al., IEEE Trans. Electron Dev. 43, 1742 (1996)

Short Channel Effects

Geometrical and layout effects in scaling

- Steady reduction of feature sizes results in a change of transistor parameters by short-channel effects
  - *technological challenges*

long channel MOSFET	short channel MOSFET	root causes
U_{Th} independent of L and W	U_{Th} **reduces** mit L, **increases** with lower W	charge separation, DIBL, narrow channel
U_{Th} independent of U_{DD}	U_{Th} reduces with increasing U_{DD}	DIBL
Subthreshold current increases linearly with decreasing L	Subthreshold current increases strongly with decreasing L	charge separation
Saturation drain current is independent of U_{DD}	Saturation drain current increases with U_{DD}	DIBL

- Simple solution to challenges by modified manufacturing of MOSFETs

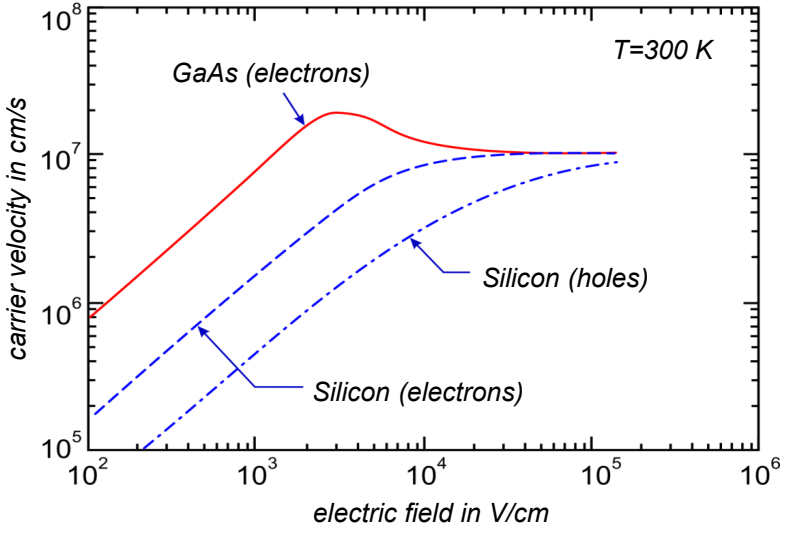
Short Channel Effects

Outline

- Leakage currents in MOS transistors
- Geometrical and layout effects in scaling
  - *p-n junctions*
  - *subthreshold current*
  - *Drain-Induced Barrier Lowering (DIBL) and Punch Through*
  - *charge sharing model*
  - *narrow channel effect*
- Degradation by hot carriers
  - *hot holes from avalanche multiplication*
  - *channel hot electrons*

Short Channel Effects
Degradation

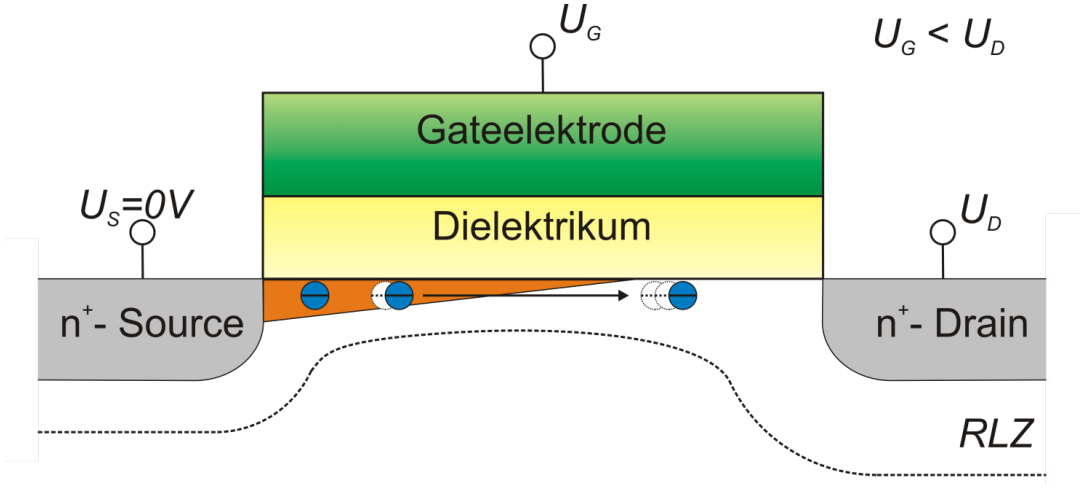
- Hot carriers
  - *first-ever severe short channel effect*
  - *critical gate legths*
    - n-channel: $L < 0.8$ µm
    - p-channel: $L < 0.5$ µm
  - *high electric field strengths at the drain-side end of the channel when in saturation mode*
    - highly accelerated electrons and holes can surmount the potential barrier between substrate and insulator



Short Channel Effects

Degradation

- Injection of hot holes into the insulator (n-type MOSFET)
  - *Drain Avalanche Hot Carrier Injection (DAHC)*
  - *observed when $U_{DS} > U_{GS}$*

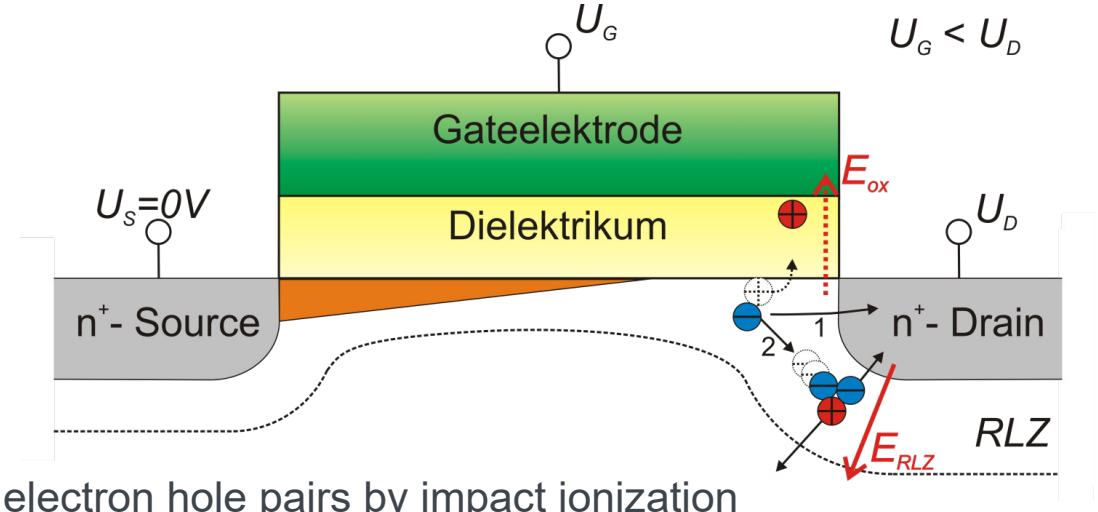


- Acceleration of electrons in lateral electric field
  - *high kinetic energy (=hot electrons)*

Short Channel Effects

Degradation

- Injection of hot holes into the insulator (n-type MOSFET)
  - *regarding curents, an even stronger acceleration appears through avalanche effect*

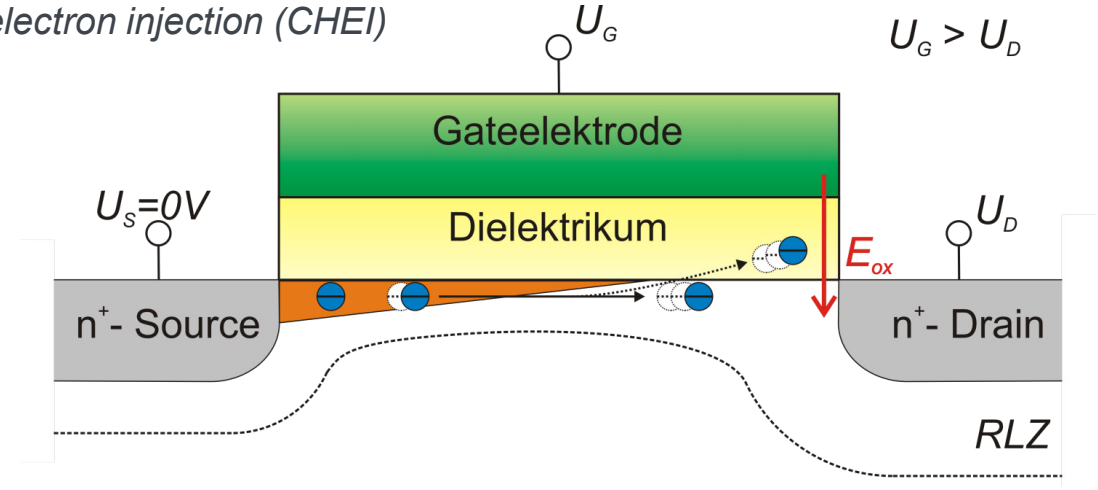


- Generation of electron hole pairs by impact ionization
  - *drift of hot electrons into drain area (lateral field) → I_D↑*
  - *drift of hot holes in the SCR field towards the substrate → $I_{D(S)}$, I_B↑*
  - *increased drain and substrate currents mainly generate thermal losses*

Short Channel Effects

Degradation

- Injection of hot channel electrons (n-type MOSFET)
  - *in case of UGS > UDS (more linear / triode region)*
  - *Channel hot electron injection (CHEI)*

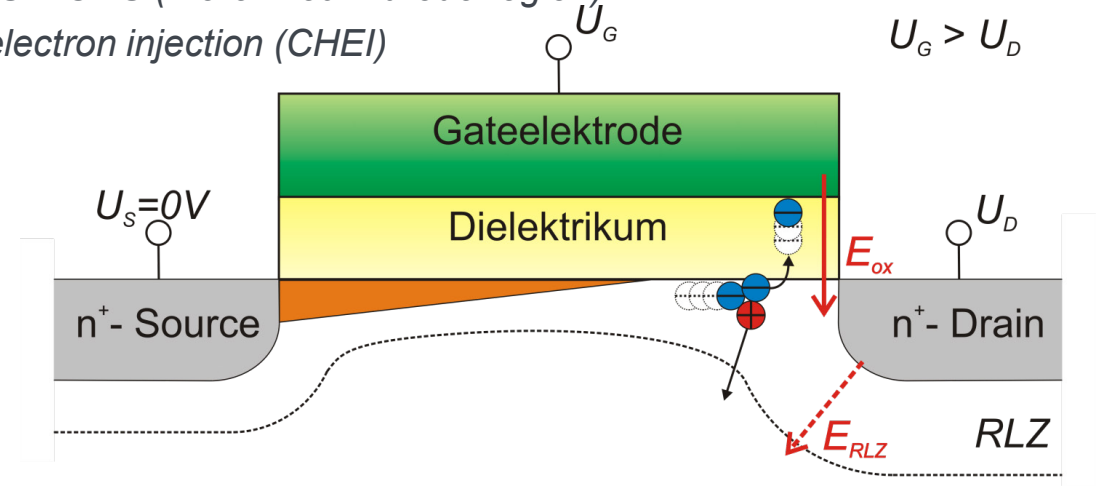


1. Acceleration of electrons in lateral electric field
   - *high kinetic energy (→ hot electrons)*
   - *direct injection into dielectric by scattering with lattice atoms*

Short Channel Effects

Degradation

- Injection of hot channel electrons (n-type MOSFET)
  - *in case of UGS > UDS (more linear / triode region)*
  - *Channel hot electron injection (CHEI)*

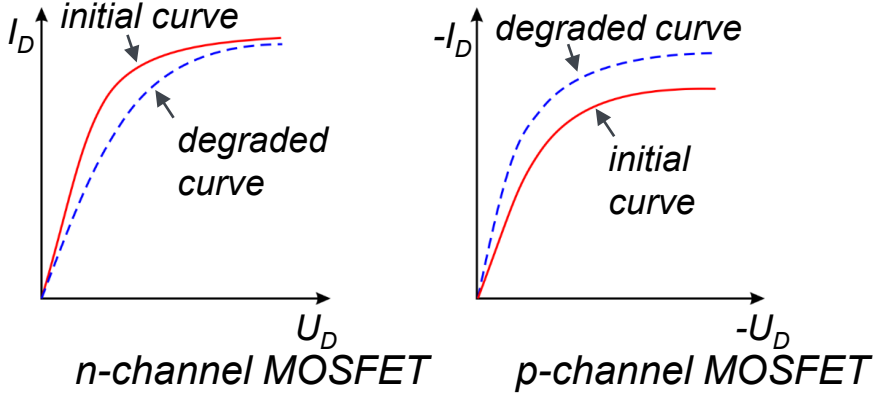


2. Generation of electron-hole-pairs by impact ionization
   - *deflection of electrons in the vicinity of drain contact by vertical field*
   - *semiconductor-dielectric barrier is surmounted by high kinetic energy*

Short Channel Effects

Degradation

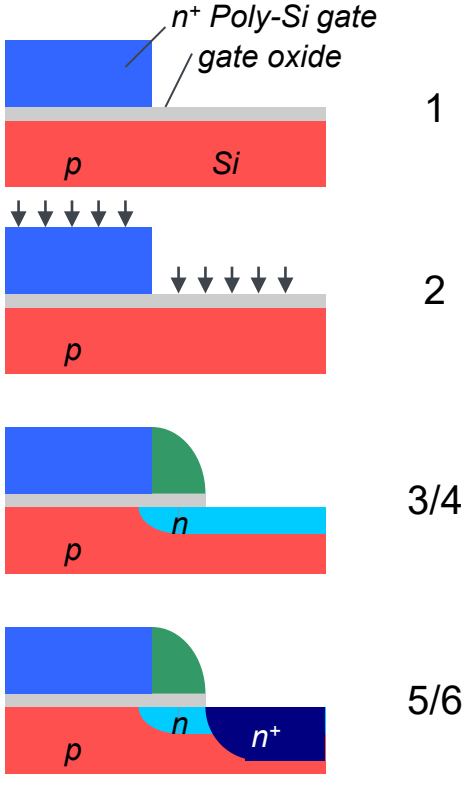
- While the strong drain-to-substrate current during DAHC in observed only temporarily, the low number of hot carriers injected into the dielectric cause a permanent alteration of device characteristics
  - *n-channel transistor: reduced electron mobiity in channel (interface degradation)*
  - *p-channel transistor: modification of threshold voltage in the vicinity of the drain, effective shortening of the channel (length)*
  - *degradation of MOSFET characteristics*



Short Channel Effects

Degradation

- Counter measure: Lightly-Doped Drain (LDD-) structures
  - *reduction of lateral field strength at drain and source*
  - *but: additional resistivity in the channel*
- Preparation
  1. *polysilicon gate patterning*
  2. *LDD implantation, Phosphorus (approx. $4 \cdot 10^{13} cm^{-2}$)*
  3. *spacer formation (LPCVD and anisotropic etching)*
  4. *thermal oxidation*
  5. *S/D implantation, Arsenic (approx. $5 \cdot 10^{15} cm^{-2}$)*
  6. *activation/diffusion*



Short Channel Effects

Outline

- Leakage currents in MOS transistors
- Geometrical and layout effects in scaling
  - *p-n junctions*
  - *subthreshold current*
  - *Drain-Induced Barrier Lowering (DIBL) and Punch Through*
  - *charge sharing model*
  - *narrow channel effect*
- Degradation by hot carriers
  - *hot holes from avalanche multiplication*
  - *channel hot electrons*

Thanks for your attention!