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Cross Domain Clock Synchronization Based on Data Packet Relay in 5G-TSN Integrated Network

1st Zichao Chai
National University of Defense Technology
Changsha, China
chaizc21@163.com

2nd Wei Liu
National University of Defense Technology
Changsha, China
wliu_nudt@hotmail.com

3rd Mao Li
National University of Defense Technology
Changsha, China
lm950819@163.com

4th Jing Lei
National University of Defense Technology
Changsha, China
leijing@nudt.edu.cn

***Abstract*—The 5G-TSN integrated network can effectively support time-critical industrial applications and realize real-time communication between all industrial equipment. However, the 5G-TSN integrated network involves different clock domains and the end-to-end cross domain clock synchronization problem needs to be solved. Based on detailed analysis of the synchronization process between 5G and TSN networks, this paper proposes a cross domain clock synchronization method based on data packet relay. The proposed method regards 5G network as logical TSN bridge which is only responsible for the forwarding of timestamped data packets. The clock domain compensation technology is introduced to estimate the residence time of 5G timing messages. The simulation results demonstrate that synchronization accuracy is significantly improved and complexity is reduced.**

***Keywords*—5G, Time Sensitive Network, Clock synchronization, Data packet relay**

I. Introduction

The Time Sensitive Network (TSN) based on Ethernet architecture can realize real-time communication and high precision clock synchronization between industrial devices in the local area network [1]. Due to data transmission characteristics of ultra-low latency, ultra-low jitter and extremely low packet loss rate, TSN network has been widely used in many industrial fields including audio and video sharing, automatic control and smart grid. Considering that 5G network supports mission-critical communications with ultra reliability and low latency, the integration of 5G and TSN network can achieve cross domain connection and reliable coordination of devices among multiple TSN networks. The end-to-end cross domain clock synchronization is the basis for integration of 5G and TSN networks.

The TSN protocols extend media access control (MAC) layer standard of traditional Ethernet to ensure high precision clock synchronization, precise traffic scheduling and intelligent network management mechanisms. [2] introduces TSN protocols in detail from four aspects of data flow synchronization, management, control and security. The key principle of TSN is to assign priorities to different data flows and to ensure the successful transmission of high priority flows through traffic scheduling and frame preemption (IEEE 802.1Q [3]) under the condition of clock synchronization. The IEEE 802.1AS standard is developed based on the IEEE 1588v2 protocol and is mainly used to solve the clock synchronization problem of TSN network [4]. IEEE 802.1AS is a clock synchronization protocol based on distributed master-slave structure. First, the master slave relationship is established according to the Best Clock Master Algorithm (BCMA). Then the master clock node directly embeds timing information in data frame based on MAC layer hardware to form a synchronization message and forwards it to the slave clock node through TSN bridge.

The 5G network also has clock synchronization function. On the base station side, besides satellite timing, the clock synchronization between 5G base stations is achieved through the bearer network and the IEEE 1588v2 protocol in scenarios of poor satellite signal (factories, subways, underground garages, urban high-rise buildings); On the terminal side, the 5G standard defines broadcast System Information Block 9 (SIB 9) signaling and implements clock synchronization between terminals through the base station broadcast. In addition, to improve synchronization accuracy and avoid errors caused by access and retransmission delays, [5] suggests using the underlying frame to transmit time information. [6] compares the synchronization overhead, resolution and duration of 5G different periodic physical layer signals, such as System Information Block (SIB) and Master Information Block (MIB), and proposes a 5G clock synchronization based on physical layer signals, which significantly improves synchronization accuracy and reduces synchronization overhead.

For the 5G-TSN integrated network, [7] proposes to treat 5G system as TSN bridge and design an adaptive module to process TSN protocol and information. The advantage of above proposal is that the parameters and processes of 5G system will not be exposed to TSN network. The 5G Release 16 protocol has incorporated the above proposal into specification and introduces new entities at the two edges

Corresponding author: Wei Liu (E-mail: wliu_nudt@nudt.edu.cn)

of 5G system to provide TSN conversion functions, namely NW-TT at UPF layer and DS-TT at terminal side [8]. [9] analyzes the different hybrid topology schemes composed of 5G and TSN network which has different characteristics and use cases. Based on this, [10] proposes a clock synchronization technology that combines one-way message mechanism and IEEE 802.1AS for 5G-TSN integrated networks which significantly reduces synchronization overhead. For NW-TT and DS-TT, [11] analyzes the clock synchronization process of downlink and proposes a design scheme that can support the cooperative work of multiple clock domains. However, there are differences in the synchronization process and timing messages between the 5G clock domain and the TSN clock domain. It is still a difficult problem to achieve low complexity and high precision cross domain clock synchronization in the 5G-TSN integrated network.

In this paper, a cross domain clock synchronization based on data packet relay in 5G-TSN integrated network is proposed, which can jointly estimate end-to-end clock frequency skew and phase offset. To this end, the contributions of this paper can be summarized as follows:

(1) As an independent clock domain, the 5G network is only responsible for the forwarding of timestamp messages and avoids the complexity of timestamp conversion.

(2) The residence time of 5G timing messages is estimated based on the clock domain compensation technology, which significantly improves synchronization accuracy and robustness.

(3) The entire 5G network is used as logical TSN bridge to ensure the compatibility of 5G and TSN networks.

II. Clock Synchronization Model of 5G-TSN Integrated Network

Based on the system architecture of 5G-TSN integrated network, this paper designs the clock synchronization model of 5G-TSN integrated network as shown in Fig. 1. The 5G-TSN integrated network is divided into the 5G clock domain and the TSN clock domain. The master clock (MC) of TSN clock domain is modeled as

$$C_{MC}(t) = t, \tag{1}$$

where t is real time. The clock model of TSN devices is

$$C_i(t) = \alpha_i t + \beta_i, i = 0, 1, 2...N. \tag{2}$$

where α_i and β_i are clock frequency skew and phase offset of TSN device, respectively.

As a complete clock domain, the 5G system must achieve end-to-end clock synchronization. The 5G base station can share a unified time reference with the external master clock, such as satellite time service or Coordinated Universal Time. The 5G core network realizes clock synchronization with base station through bearer network based on the IEEE 1588v2 protocol. The UE can maintain synchronization with base station based on timing message exchange technology. So the clock model of 5G clock domain can be modeled as

$$C_{5G}(t) = \alpha_{5G} t + \beta_{5G}, \tag{3}$$

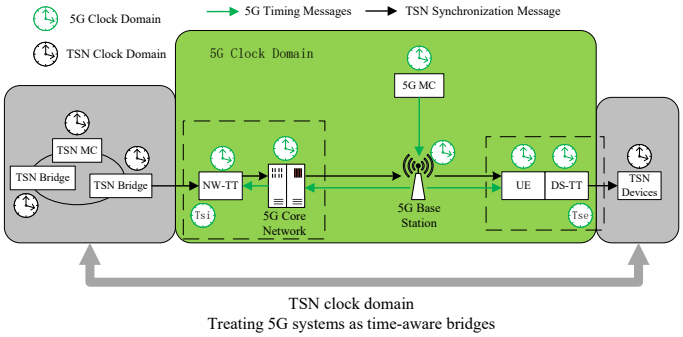

Fig. 1. Clock synchronization model of 5G-TSN integrated network

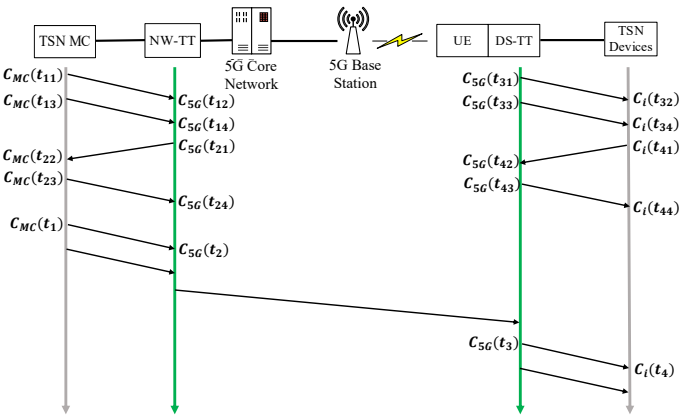

Fig. 2. The end-to-end clock synchronization process of 5G-TSN integrated network

where α_{5G} and β_{5G} are clock frequency skew and phase offset of TSN device, respectively.

This paper regards 5G system as a transparent clock and uses Protocol Data Unit (PDU) session to forward TSN timing messages to complete clock synchronization between TSN device and TSN MC. To improve synchronization accuracy while ensuring the applicability to 5G system, this paper adopts a method based on packet relay and delay compensation. The 5G system directly relays timing message of TSN GM node to TSN device without converting timestamp according to local clock. In addition, the residence time of timing messages needs to be calculated and converted to TSN clock domain by 5G system. To deal with this issue, NW-TT and DS-TT need to receive time information (accumulated delay, clock frequency skew, link delay, etc.) in the TSN timing message, and record timestamp (Tsi, Tse) of timing message on ingress and egress ports of 5G system.

III. Synchronization Protocol

According to the clock synchronization model of 5G-TSN integrated network, a cross domain clock synchronization based on data packet relay is proposed. Considering that the TSN MC and TSN devices are only separated by a 5G logical bridge, the clock synchronization process is shown in Fig. 2.

A. clock frequency skew and link delay estimation algorithm

The clock frequency skew and link delay between TSN MC and NW-TT, DS-TT and TSN devices are calculated. Considering that synchronization process between TSN MC and NW-TT, DS-TT and TSN devices is similar, we take TSN GM and NW-TT as an example.

First, the TSN MC sends two synchronization messages to NW-TT and records two sending timestamps $C_{MC}(t_{11})$, $C_{MC}(t_{13})$. The NW-TT records two receiving timestamps $C_{5G}(t_{12})$, $C_{5G}(t_{14})$. The NW-TT combines (3) and (1) to get as follows:

$$\begin{cases} C_{MC}(t_{11}) = t_{11} \\ C_{5G}(t_{12}) = \alpha_{5G} t_{12} + \beta_{5G} \\ C_{MC}(t_{13}) = t_{13} \\ C_{5G}(t_{14}) = \alpha_{5G} t_{14} + \beta_{5G} \end{cases} \tag{4}$$

Assuming that the link delay d_1 between TSN MC and NW-TT remains unchanged in a short period of time, the following formula is obtained.

$$\begin{cases} C_{MC}(t_{12}) = C_{MC}(t_{11}) + d_1 \\ C_{MC}(t_{14}) = C_{MC}(t_{13}) + d_1 \end{cases} \tag{5}$$

By combining (4) and (5), the estimated value of relative clock frequency skew between TSN GM and NW-TT can be expressed as

$$\hat{\alpha}_{5G} = \frac{C_{5G}(t_{14}) - C_{5G}(t_{12})}{C_{MC}(t_{13}) - C_{MC}(t_{11})} \tag{6}$$

Then, TSN MC and NW-TT perform two-way message exchange process and NW-TT calculates link delay d_1. The relationship of four timestamps $C_{5G}(t_{21})$, $C_{MC}(t_{22})$, $C_{MC}(t_{23})$ and $C_{5G}(t_{24})$ as follows:

$$\begin{cases} C_{5G}(t_{21}) = \alpha_{5G} t_{21} + \beta_{5G} \\ C_{MC}(t_{22}) = t_{22} \\ C_{MC}(t_{23}) = t_{23} \\ C_{5G}(t_{24}) = \alpha_{5G} t_{24} + \beta_{5G} \end{cases} \tag{7}$$

Because the mathematical relationship between local time of TSN GM $C_{MC}(t_{21})$, $C_{MC}(t_{22})$, $C_{MC}(t_{23})$, $C_{MC}(t_{24})$ and link delay d_1 is

$$\begin{cases} C_{MC}(t_{22}) = C_{MC}(t_{21}) + d_1 \\ C_{MC}(t_{23}) = C_{MC}(t_{24}) - d_1 \end{cases} \tag{8}$$

Substituting (7) and (8) to (9), the estimated value of link delay between TSN GM and NW-TT can be written as

$$\hat{d}_1 = \frac{\frac{1}{\hat{\alpha}_{5G}}[C_{5G}(t_{24}) - C_{5G}(t_{21})] - [C_{5G}(t_{23}) - C_{5G}(t_{22})]}{2} \tag{9}$$

Similarly, the relative clock frequency skew $\frac{\alpha_i}{\alpha_{5G}}$ and link delay d_2 between DS-TT and TSN devices can also be calculated according to the above process.

$$\frac{\hat{\alpha}_i}{\alpha_{5G}} = \frac{C_i(t_{34}) - C_i(t_{32})}{C_{5G}(t_{33}) - C_{5G}(t_{31})} \tag{10}$$

$$\hat{d}_2 = \frac{\frac{\hat{\alpha}_{5G}}{\alpha_i}[C_i(t_{44}) - C_i(t_{41})] - [C_{5G}(t_{43}) - C_{5G}(t_{42})]}{2} \tag{11}$$

B. cross domain clock synchronization algorithm

The TSN MC transmits timing messages to TSN devices through 5G logical bridge to complete clock synchronization between TSN MC and TSN devices. The 5G system as a transparent clock is only responsible for forwarding timing messages. First, TSN MC sends a synchronization message to NW-TT and records the sending timestamp $C_{MC}(t_1)$. When receiving the synchronization message, NW-TT records receiving timestamp $C_{5G}(t_2)$. Then, TSN MC sends a follow-up message to inform NW-TT of timestamp $C_{MC}(t_1)$. Next, NW-TT composes timestamp $C_{MC}(t_1)$, $C_{5G}(t_2)$ and the time information (relative clock frequency skew $\hat{\alpha}_{5G}$ and link delay $\hat{d}_1$) obtained in the first step into a 5G timing message and sends it to DS-TT.

Similarly, after receiving 5G timing message, DS-TT sends synchronization message to TSN device and records sending timestamp $C_{5G}(t_3)$. When TSN device receives the synchronization message, it records receiving timestamp $C_i(t_4)$. Finally, DS-TT sends timestamp $C_{5G}(t_3)$ and 5G timing message ($C_{MC}(t_1)$, $C_{5G}(t_2)$, $\hat{\alpha}_{5G}$ and $\hat{d}_1$) to the TSN device as follow-up message.

After completing above synchronization process, the TSN device can calculate clock frequency skew and phase offset relative to TSN MC based on the acquired time information. The clock frequency skew between TSN device and TSN MC is

$$\hat{\alpha}_i = \frac{\hat{\alpha}_i}{\alpha_{5G}} \cdot \hat{\alpha}_{5G} \tag{12}$$

where $\frac{\hat{\alpha}_i}{\alpha_{5G}}$ is estimated value of relative frequency skew between TSN device and 5G clock domain. The $\hat{\alpha}_{5G}$ is estimated value of relative frequency skew between 5G clock domain and TSN MC.

By analyzing above synchronization process, the relationship between TSN MC local time $C_{MC}(t_1)$, $C_{MC}(t_4)$ and total link delay, residence time can be represented as

$$C_{MC}(t_4) - C_{MC}(t_1) = D + d \tag{13}$$

where d is total link delay between TSN device and TSN MC. The formula is as follows:

$$d = \hat{d}_1 + \frac{\hat{d}_2}{\hat{\alpha}_{5G}} \tag{14}$$

The D is residence time of 5G timing messages. Taking into account the difference between 5G clock domain and TSN clock domain, clock domain compensation technology is used to convert the time to TSN clock domain. The formula is as follows:

$$D = \frac{C_{5G}(t_3) - C_{5G}(t_2)}{\hat{\alpha}_{5G}} \tag{15}$$

Furthermore, the relationship of timestamp $C_{MC}(t_1)$ and $C_i(t_4)$ can be written as

$$\begin{cases} C_{MC}(t_1) = t_1 \\ C_i(t_4) = \alpha_i t_4 + \beta_i \end{cases} \tag{16}$$

Combining (13) and (16), clock phase offset between TSN device and TSN MC can be obtained as

$$\hat{\beta}_i = C_i(t_4) - \hat{\alpha}_i[D + d + C_{MC}(t_1)] \tag{17}$$

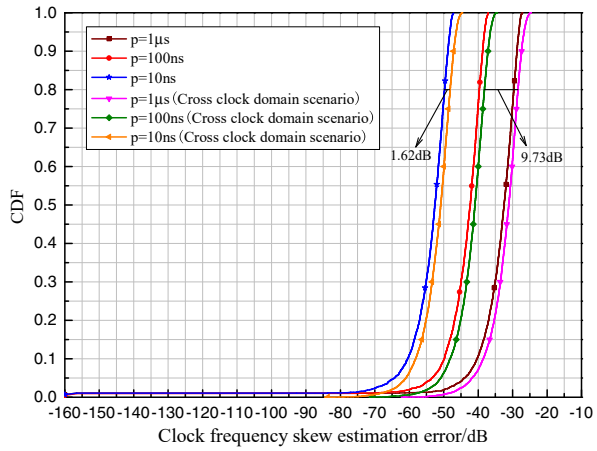

Fig. 3. The cumulative distribution function (CDF) of clock frequency skew estimation errors in single clock domain scenarios and cross clock domain scenarios

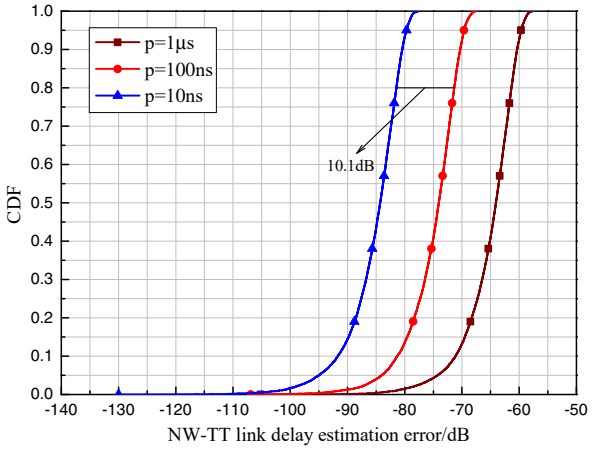

Fig. 4. The CDF of link delay estimation error between TSN GM and NW-TT

According to the above analysis and calculation, the estimated value of clock frequency skew and phase offset between TSN device and TSN MC can be expressed as

$$\begin{cases} \hat{\alpha}_i = \frac{\hat{\alpha}_i}{\alpha_{5G}} \hat{\alpha}_{5G} \\ \hat{\beta}_i = C_i(t_4) - \hat{\alpha}_i[D + d + C_{MC}(t_1)] \end{cases} \tag{18}$$

IV. Simulation Results

In this section, numerical results are presented to verify performance of the proposed method. The experimental scenario is that TSN MC connects 1000 TSN devices with different clock frequency skew and phase offset through 5G network, in which clock frequency skew is $\alpha_i \in (0.99, 1.01)$ and clock phase offset is $\beta_i \in (-10, 10)ms$. The simulation experiment measures $M = 10000$ times for each device to ensure accuracy.

To verify the effectiveness of clock frequency skew estimation algorithm based on packet relay in single clock domain scenarios and cross clock domain scenarios, the cumulative distribution function (CDF) of clock frequency skew estimation errors between TSN GM and NW-TT, between TSN GM and TSN devices under different timestamp accuracy ($p = 1\mu s, p = 100ns, p = 10ns$) is shown in Fig. 3. In the two scenarios, the clock frequency skew estimation error and timestamp accuracy are negatively correlated. The timestamp accuracy is increased by 10 times, the clock frequency skew estimation error is decreased by about 10dB. For example, when the timestamp accuracy is increased from $p = 1\mu s$ to $p = 100ns$, the clock frequency skew estimation error in a single clock domain scenario is reduced by 9.73dB. When the timestamp accuracy is $p = 10ns$, the clock frequency skew estimation error of two scenes is the lowest and can be kept below -48dB.

Moreover, it can be found that when the timestamp accuracy is $p = 10ns$, the frequency skew estimation error of cross 5G-TSN clock domain scenario is only 1.62dB larger than single clock domain scenario. Compared with single clock domain scenario, the proposed algorithm has a small performance loss in cross 5G-TSN clock domain scenario.

To verify the performance of link delay estimation algorithm in the single hop scenario, the CDF of link delay estimation error between TSN GM and NW-TT under different timestamp accuracy is compared, as shown in Fig. 4. It can be found that the link estimation error is negatively correlated with timestamp accuracy. Every ten times the timestamp accuracy increases, the link estimation error decreases by about 10dB. For example, when the timestamp accuracy is increased from $p = 100ns$ to $p = 10ns$, the link delay estimation error is reduced by 10.1dB. Furthermore, when the timestamp accuracy is $p = 10ns$, the link estimation error is the smallest and can be maintained below -80dB.

Fig. 5 shows the CDF of end-to-end clock phase offset estimation error between TSN GM and TSN devices under different timestamp accuracy in a cross 5G-TSN clock domain scenario. Moreover, this simulation experiment compared the performance difference of clock phase offset estimation algorithm based on packet relay with and without clock domain compensation. It can be seen that when there is clock domain compensation, the end-to-end clock phase offset estimation error is negatively correlated with timestamp accuracy. The timestamp accuracy is increased by 10 times, the clock phase offset estimation error is reduced by about 10dB. For example, when the timestamp accuracy is increased from $p = 100ns$ to $p = 10ns$, the clock phase offset estimation error is reduced by 9.75dB. When the timestamp accuracy is $p = 10ns$, the phase offset estimation error is less than -65dB which can achieve microsecond synchronization accuracy. When there is no clock domain compensation, the clock phase offset estimation error is independent of timestamp accuracy. The reason is that the residence time of timing message in the 5G system is not converted to TSN clock domain. The estimation error is greater than the error caused by timestamp and becomes main factor affecting estimation accuracy. Furthermore, when the timestamp accuracy is $p = 100ns$, the phase offset estimation error with clock domain compensation is 27.59dB lower than that without clock domain compensation. It can be found that

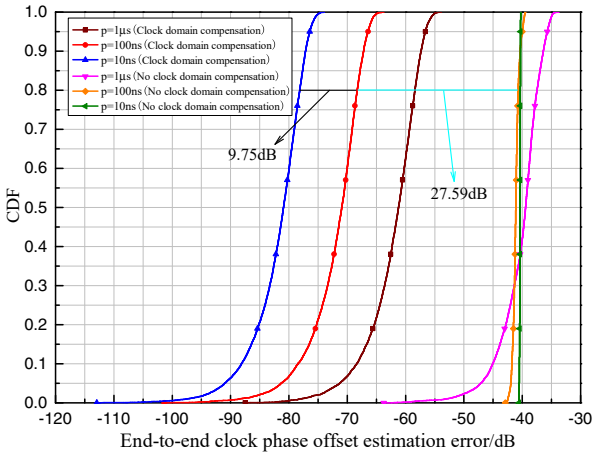

Fig. 5. The CDF of end-to-end clock phase offset estimation error with and without clock domain compensation

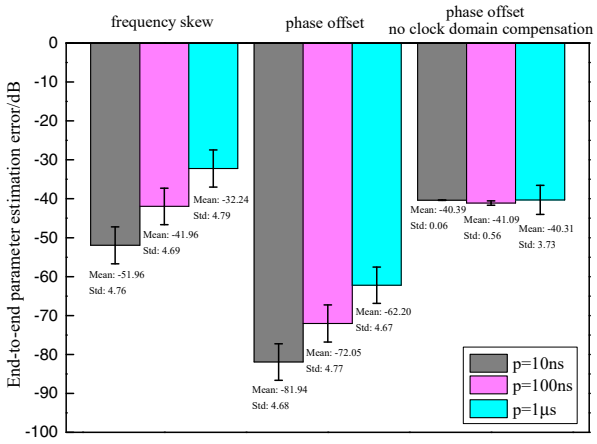

Fig. 6. The parameter estimation error of cross domain clock synchronization algorithm based on packet relay

the performance of clock phase offset estimation algorithm based on packet relay with clock domain compensation has been significantly improved.

Fig. 6 shows the parameter estimation error of cross domain clock synchronization algorithm based on packet relay under different timestamp accuracy, including clock frequency skew, clock phase offset with/without clock domain compensation. For clock frequency skew and clock phase offset with clock domain compensation, the higher timestamp accuracy, the smaller mean value of estimation error. But the standard deviation is not significantly affected. In addition, when there is clock domain compensation, the mean value of clock phase offset estimation error is about 30dB lower than the clock frequency skew estimation error. The reasons is that the performance of clock frequency skew estimation algorithm is more sensitive to timestamp error and link delay change. The clock phase offset estimation algorithm is more robust to timestamp errors, and can compensate for link delays and residence time. The estimation error does not fluctuate greatly with the number of node hops. For clock phase offset without clock domain compensation, since it is mainly affected by residence time, the mean value of estimation error is not much different under the three timestamp accuracy. At the same time, the difference between 5G clock domain and TSN clock domain is stable, so the standard deviation of clock phase offset without clock domain compensation is smaller.

V. Conclusion

For the 5G-TSN integrated network, a cross domain clock synchronization method based on packet relay is proposed which can realize the joint estimation of end-to-end clock frequency skew and phase offset while being compatible with 5G and TSN networks. This method realizes timing information exchange across clock domains based on packet relay and avoids the complexity of timestamp conversion. At the same time, the idea of clock domain compensation is introduced to estimate residence time of 5G timing messages which significantly improves clock synchronization performance. The simulation results show that the proposed method can achieve microsecond level synchronization accuracy in cross clock domain scenarios. Moreover, the proposed method has good robustness whose performance is independent of clock domain differences and node hop counts.

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