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Abstract—

Index Terms—Clock synchronization, Time sensitive networking, Precision time protocol (PTP), AS6802

I. Introduction

Many modern control strategies are time-triggered, and control systems are mostly distributed, so precise synchronization and time-deterministic communication are required. Time Sensitive Networking (TSN) is currently the most promising time deterministic communication method in industrial Ethernet applications. In the future, TSN will replace or extend most current industrial fieldbuses with its unified communication paradigm. Since wired-only networks cannot scale with a large number of nodes in a large automation project, hybrid solutions with wired backbone networks and multiple smaller wireless islands are considered(fig1). In these hybrid architectures, the wireless part should meet the same same requirement. Due to the low-latency and high-precision characteristics of the 5G network, it is the most likely communication protocol to become the wireless TSN carrier in the future. At present, for the problem of 5G and TSN integration, the solution given by 3GPP protocol and various communication manufacturers is 5G bridge. The role of a bridge is assigned to the 5G network through CNC, and the protocol converter at the wired and wireless interface records the time stamp to calculate the residence time inside the 5G network, so that the TSN wired devices at both ends of the 5G network can meet the synchronization requirements. However,This solution cannot meet the synchronization requirements of future wireless TSN devices. Therefore, this study targets heterogeneous TSN networks, it is necessary to solve the problem of accumulated errors within the wireless network. As the number of hops increases, the wireless cumulative error has a more obvious impact on synchronization. As shown in Figure 1, when the network scale is large, the synchronization accuracy will be affected to a subtle level, and the synchronization accuracy will no longer meet the TSN synchronization requirements. . Therefore, I propose a wireless cumulative error solution for 5G networks, which controls the internal end-to-end delay of 5G through carrier spacing, and performs cumulative error compensation at the wireless TSN node, so that the internal synchronization accuracy of wireless TSN can meet the requirements.

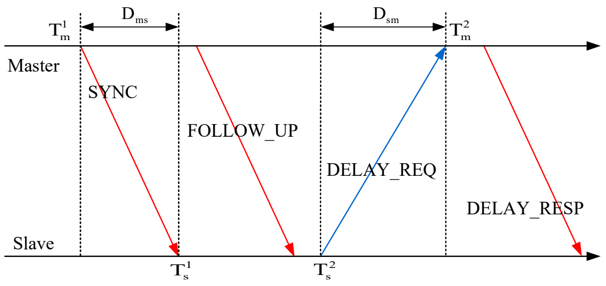

Fig. 1. Heterogeneous network clock synchronization architecture.

II. Clock Model

Due to the complexity of the industrial site, the crystal oscillator of the device clock will be greatly affected, and the initial clock state and rate of change of the clock will deviate, causing errors between clocks.Specifically, the clock of one node can be expressed by

$$C_i(t) = \alpha_i(t)t + \beta_i \tag{1}$$

Where α_i and β are the time-varying clock skew and constant clock offset to the reference clock. Ideally, α=1 and β=0. The change of the slope comes from the drift of the internal crystal oscillator of the clock, and the difference in the initial state comes from the error during network initialization. The crystal frequency of the clock is affected by the specific industrial environment, such as temperature, voltage, aging degree, etc. In the synchronization process, in addition to the accuracy of the clock, the delay between nodes is also an important factor affecting the synchronization accuracy.The delay can be expressed by

$$Delay = D_d + D_r \tag{1}$$

Where D_d is the deterministic delay, which is mostly composed of transmission delay and can be eliminated by measurement, D_r is the random delay, which is mostly composed of propagation delay jitter and cumulative error. According to the reference[], propagation delay jitter can be measured periodically to reduce its effect on synchronization accuracy, however, accumulated errors may have a large impact on synchronization accuracy in large-scale networks.

A. Clock Synchronization Mechanism Design

Clock synchronization schemes are mainly divided into two-way communication and broadcast schemes. The broadcast scheme uses the broadcast method to distribute the reference clock to all wireless nodes, which is usually used when the transmission delay is unstable and varies greatly. The 5G network itself has the characteristics of low latency and high stability, and in practical applications, the wireless network is mainly used for ”last mile connection”, and the distance to the same access point (AP) is usually much less than 100m, so the maximum propagation delay should be Less than 400ns, in view of this situation, for the sake of synchronization accuracy, the synchronization scheme is divided into two steps to execute:

- Determine the master-slave level of the wireless clock by broadcasting
- Pairwise two-way communication synchronization for nodes between adjacent levels

The wireless root node embeds the count k=0 into the synchronization message to broadcast and sends, and the received node sets the count k to k+1 as the local level and sends the broadcast synchronization message containing k+1 to the next level. And so on until all nodes have determined their level. The situation assumed in the research is a tree topology, and the binary tree is used for traversal. There is only broadcast communication between a single node and the left and right adjacent nodes, which is distributed layer by layer, as shown in the figure2:

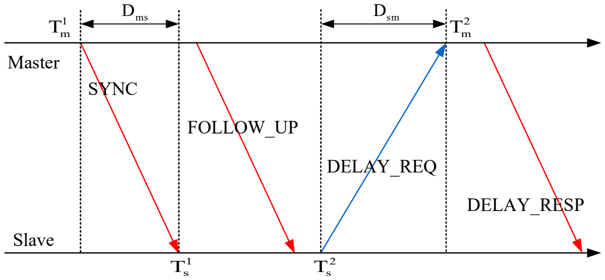

Fig. 2. Wireless network clock synchronization topology, k represents the number of hops in the network, respectively.

After the hierarchy level is established, synchronization is performed by a pairwise synchronization scheme, with each interval being one time slot. The slave clock will receive several reference timestamps G from the master clock through the middle, and record the local time L. The algorithm for the synchronization process is as follows After several groups of time stamps are exchanged, the estimated values of frequency difference and clock deviation are obtained by linear regression, and the local clock is corrected by the following formula:

$$L' = L(1 + \frac{\widehat{\sigma}}{f_0}) - \widehat{o} + [\frac{G_0 - L_0}{T_s lot}] \tag{2}$$

It can be seen from the above formula that the influence caused by the accumulated error depends on the size of the time slot in the synchronization process, and the time slot determines the synchronization accuracy. The upper limit of accuracy, when the number of nodes increases, the synchronization delay increases, and the impact of the time slot length on the cumulative error is more obvious.

$$t = (\alpha + \sigma)t + \beta + \delta$$

Algorithm 1 clock synchronization process in a clock level initialization period

```
Input: Time stamp sent by $k_{i-1}$ level clock, $T_G^n, n = 1, 2 \ldots$; Local time stamp of $k$ level clock, $T_L^n, n = 1, 2 \ldots$, clock synchronization period $P_{sync}$, time slot $\tau$;
Output: corrected local clock, $L'$;
while $time \in P_{sync}$ do
    while $time = n\tau, n = 1, 2 \ldots$ do
        if $State$ = initialization then
            $k_{i-1}$ level clock exchanges information with $k$ level clock, and $k$ level clock gets $T_G^n, n = 1, 2 \ldots$;
            if receives $T_G^n, n = 1, 2 \ldots$ then
                record local time $T_L^n, n = 1, 2 \ldots$,
            end if
            the estimated values of frequency difference $\widehat{f}$ and clock deviation $\widehat{o}$ are obtained by linear regression;
            the $k_{i-1}$ level clock adjust its local time with $L' = L(1 + \frac{\widehat{\sigma}}{f_0}) - \widehat{o} + [\frac{G_0 - L_0}{T_s lot}]$;
        end ifSTATE=;
        if receives $corr$ then
            SM adjusts local time;
        end if
        if $time + P_t > P_f$ and receives $f_{FM}$ then
            SM adjusts local frequency;
        end if
    end while
end while
```

$$t_(wired) = (\alpha_1 + \sigma_1)t + \beta_1 + \delta_1$$

$$t_(wireless) = (\alpha_2 + \sigma_2)t + \beta_2 + \delta_2$$

$$t_1 = (\alpha_1 + \sigma_1)t + \beta_1 + \delta_1$$

$$t = \frac{t_1 - \beta_1 - \delta_1}{\alpha_1 + \sigma_1}$$

$$t_2 = (\frac{t_1 - \beta_1 - \delta_1}{\alpha_1 + \sigma_1} + delay)(\alpha_2 + \sigma_2) + \beta_2 + \delta_2$$

$$t = \frac{t_3 - \beta_2 - \delta_2}{\alpha_2 + \sigma_2}$$

$$t_4 = (\frac{t_3 - \beta_2 - \delta_2}{\alpha_2 + \sigma_2} + delay)(\alpha_1 + \sigma_1) + \beta_1 + \delta_1$$

$$m = \frac{\alpha_2 + \sigma_2}{\alpha_1 + \sigma_1}$$

$$2delay = t_2 - t_1 + t_4 - t_3$$

$$2delay = m(t_2 - t_1 + t_4 - t_3) - (m - 1/m)(\beta_1 + \delta_1) + (m - 1/m)(\beta_2 + \delta_2)$$

$$2delay = m(t_2 - t_1 + t_4 - t_3) - (m - 1/m)(\beta_2 + \delta_2)$$

$$2delay = m(t_2 - t_1 + t_4 - t_3) - (m - 1/m)(\beta_2 + \delta_2)$$

$$m = \frac{\alpha_2 + \sigma_2}{\alpha_1 + \sigma_2}$$

B. Wireless end-to-end latency optimization

Since the research object is the wireless TSN network with 5G as the carrier, the 5G network frame structure is shown in the following figure: In 5G, the length of the radio frame and subframe is the same, the radio frame is 10ms, and the subframe length is 1ms The number of ofdm symbols contained in a time slot in 5G is 14, and the number of time slots contained in each subframe is different under different carrier intervals ssb (clock synchronization message) fixedly occupies 4 ofdm symbols, so the duration and period of ssb under different subcarrier intervals are different, The 5G subcarrier spacing is adjustable, and the 5G protocol has a recommended set of subcarrier spacing parameters for different application scenarios. Due to the assignable characteristics of the subcarrier spacing of the 5G network, the number of subcarriers can be reduced by increasing the subcarrier spacing, and the symbol length of the ofdm can be reduced, thereby reducing the delay and reducing the accumulated error. In the case of a certain transmission environment, the coherence bandwidth is the same, the larger the subcarrier spacing (ie subcarrier bandwidth), the smaller the number of subcarriers, and the larger the bandwidth of each subcarrier, resulting in the possibility of frequency selective attenuation. higher (occurs when the signal bandwidth is greater than the coherence bandwidth). Therefore, in the simulation, it is necessary to meet the delay requirement first and then use the equalizer to compensate to ensure the synchronization accuracy.

Algorithm 2 CM clock synchronization process in a P_f period

```
Input: Time information sent by GM, $T_{GM}$; Time information sent by SM, $T'_{SM}$; Local time information of CM $T_{CM}$; Frequency sent by FM, $f_{FM}$; Preset threshold, $\zeta$;
Output: Time correction value $corr$; GM status, $GS$;
while $time \in P_f$ do
    while receives $T'_{SM}$ do
        CM calculates $corr$ and adjusts local time;
        CM sends $corr$ to FM, SM and SC;
        if $time + P_t > P_f$ then
            if receives $f_{FM}$ then
                CM adjusts local frequency;
            end if
            $GS = abnormal$;
            if receives $T_{GM}$ and $|T_{GM} - T_{CM}| \leq \zeta$ then
                $GS = normal$;
            end if
        end if
    end while
end while
```

Algorithm 3 FM clock synchronization process in a P_f period

```
Input: Time information sent by GM, $T'_{GM}$; Time correction value sent by CM, $corr$; GM status, $GS$;
Output: Local frequency information of FM, $f_{FM}$;
while $time \in P_f$ do
    repeat
        if $GS$ = normal then
            if receives $T'_{GM}$ then
                FM calculates frequency offset and adjusts local frequency;
            end if
            if receives $corr$ then
                FM adjusts local time;
            end if
        end if
    until $time + P_t > P_f$
    FM generates $f_{FM}$ and injects it into the network;
end while
```

III. Performance Evaluation

In this section, we investigate the effectiveness of our proposed hierarchical clock synchronization mechanism. A network structure was built in OMNET++ to verify the performance, as shown in Fig. 5. We first remodeled the clock in OMNET++ according to the mathematical model of the clock (1) and (2) established in section II. The frequency of GM is set to 1MHz. Set the parameters of all other nodes to $\Delta_0 = 20$ppm, $F_i = 1$MHz, $\delta = 20$ppm, and $\phi_i \sim \mathcal{N}(0, 0.1^2)$. We choose the SC node as the comparison node and set the bandwidth of all links to 100M. The propagation delay of all links is set to 25ns. Then the proposed mechanism is compared with the gPTP in terms of synchronization accuracy and speed.

A. Synchronization Accuracy

Fig. 6 shows the tendency of the synchronization errors over time when using the synchronization mechanism we proposed and gPTP with $P_t = 2$s. From Fig. 6, one can see that the synchronization errors of gPTP produce large fluctuations due to the influence of frequency offset, and errors of our proposed mechanism change steadily. Under our proposed mechanism, the errors are lower than those under gPTP. The results imply the effectiveness of our mechanism. The frequency offset can cause cumulative time errors, resulting in poor performance. Our proposed mechanism synchronizes the frequency and eliminates errors caused by frequency offset.

Fig. 7 shows the synchronization errors that our proposed mechanism and gPTP can achieve with different P_t. The box plot in the figure is the synchronization errors obtained with the increase of simulation time in each period. The line in the figure and the small graph are the medians of the synchronization errors obtained with different P_t. We can see that with the same P_t, the errors of the proposed mechanism is smaller than that of gPTP, which means our proposed mechanism can maintain high synchronization accuracy. As the P_t decreases, this difference also decreases. This is because as P_t decreases, the errors caused by the frequency offset gradually decrease, and the gPTP errors also become smaller. Furthermore, from the box plot in the figure, we can see that the errors of the proposed mechanism are limited to a specific range, and the fluctuation is smaller, which is better than gPTP.

B. Synchronization Speed

Fig. 8 shows the synchronization speed of the two mechanisms with different P_t. We define the synchronization speed as the time when the relative error between the current synchronization accuracy and the median synchronization accuracy is 20%. It can be observed from the figure that the time required for our proposed mechanism is shorter than gPTP, which means that the synchronization speed of our proposed mechanism is faster and synchronization efficiency is higher than gPTP. The synchronization speed of gPTP is slow because it requires multiple cycles of synchronization to eliminate the errors gradually. Moreover, the frequency offset will continue to bring errors, resulting in a long time to achieve the required synchronization accuracy. Our method relies on the SM to provide a reference clock to eliminate errors at the beginning of synchronization quickly. After frequency synchronization, the errors become smaller, so that the synchronization accuracy is always kept in a low range.

C. Performance Analysis

The synchronization mechanism proposed in this work adopts a hierarchical structure. Since all SMs are synchronized with GM, the calculation of the underlying network can eliminate random errors. Moreover, due to the combination of distributed synchronization, which avoids the situation that tree-based synchronization errors will accumulate as the network scale increases, the synchronization process can be increased compared to gPTP with the same synchronization period. It can achieve the required synchronization accuracy faster, resulting in higher synchronization efficiency, which can also be seen from Fig. 8.

IV. Conclusions

This paper has studied the clock synchronization for TSN. A hierarchical clock synchronization mechanism was proposed. Considering the synchronization time slot difference and the time-frequency coupling relationship, the offset of time and frequency are cooperatively regulated. Through the performance analysis and verification, the effectiveness and performance improvement of the proposed hierarchical synchronization mechanism was demonstrated. In the future, we will do further research on synchronization reliability.

Acknowledgment

This work was supported by National Key Research and Development Program of China (2018YFB1702100).

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