PV200 Semestral project

Tomas Jaros

February 1, 2023

1 Introduction

In this semestral project the task was to use hardware description languages, such as Verilog or VHDL and implement a MD5 cracker of some sorts. My solution tried to implement two versions. One mostly in software programmed in C and running on softcore CPU communicating with MD5 core through several registers available in the custom functions unit of the CPU. Second one is supposed to be running purely without any software.

2 Equations

Here is an inline equation: $F = ma$. Below is a block equation which we can label as Eq. (1).

$$a^2 + b^2 = c^2 \tag{1}$$

3 Figures and tables

Fig. 1 is an example figure.

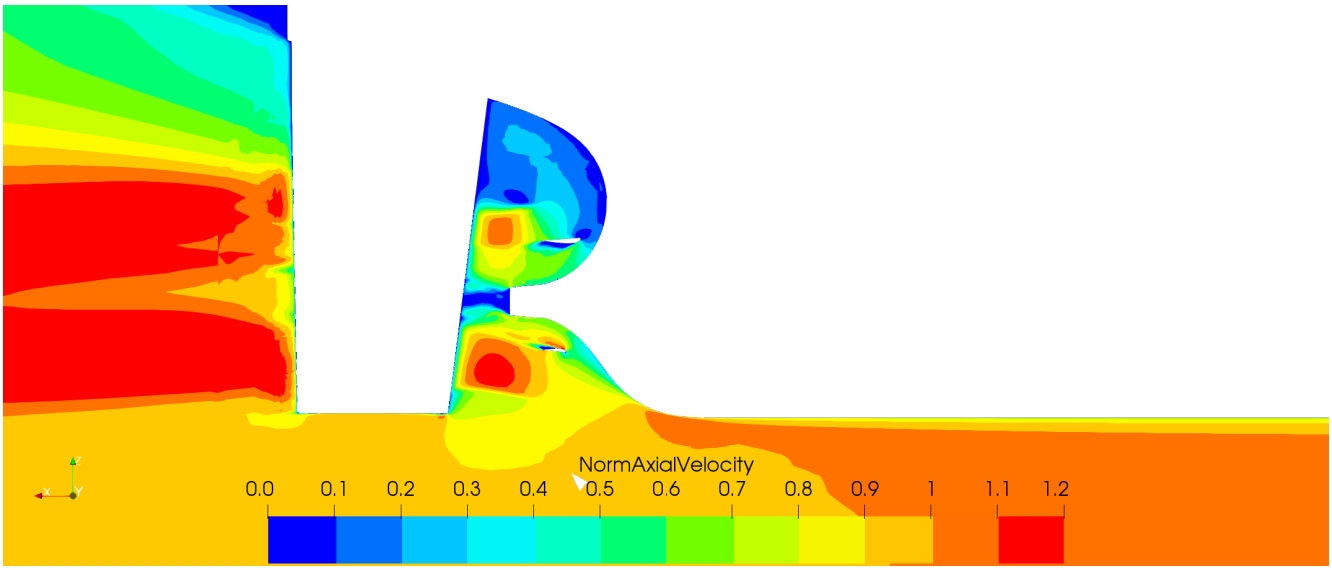

Figure 1: An example image.

Table 1 is an example table.

4 Code

Below is some C++ code.

```
tmp<fvVectorMatrix> tUEqn
(
    fvm::div(phi, U)
```

Table 1: An example table.

Heading 1	Heading 2	Heading 3
1	2	3
4	5	6
7	8	9

```
    + MRF.DDt(U)
    + turbulence->divDevReff(U)
    ==
    fvOptions(U)
);
```

References