ECE337 Lab 6 evaluation sheet

Student Name: _____

MG Account: _____

		TA Initials	Date	Score
(14)	**Preparation Phase (submit Lab6Prep)**			
(3)	Completed Pseudo-code for timer	_____	_____	_____
(3)	Controller State Transition Diagram	_____	_____	_____
(1)	Completed RTL diagram for the Controller block	_____	_____	_____
(2)	Completed RTL diagram for the Decode block	_____	_____	_____
(2)	Completed functional block diagram for the timer block built using flex_counter module from lab 3	_____	_____	_____
(2)	Completed schematic diagram for the scl_edge block	_____	_____	_____
(1)	Completed schematic diagram for the sda_sel block	_____	_____	_____
(14)	**Phase 1 Block Coding and Testing (submit Lab6Phase1)**			
(2)	Functional scl_edge.sv			_____
(1)	Functional sda_sel.sv			_____
(2)	Functional tx_fifo.sv			_____
(2)	Functional decode.sv			_____
(2)	Complete test bench for scl_edge.sv			_____
(1)	Complete test bench for sda_sel.sv			_____
(2)	Complete test bench for decode.sv			_____
(2)	Complete test bench for tx_fifo.sv			_____
(72)	**Phase 2 I2C Tx-only Slave Design Implementation**			
(72)	Mapped Version Score (submit Lab6Phase2) *Reminder: Only the most recent mapped submission score will count*			_____