ECE337 Lab 3 evaluation sheet

Student Name: _____

MG Account: _____

		TA Initials	Date	Score
(1)	**Lab3 folder and provided files in SVN**	_____	_____	_____
(5)	**16-bit Adder Hierarchical Design & Verification**			
(1)	Simple source simulation of the 16-bit adder	_____	_____	_____
(1)	Add Internal Assertions to 1-bit Full Adder Design	_____	_____	_____
(1)	Add Internal Assertions to 16-bit Adder Design	_____	_____	_____
(2)	Mapped generate structural 16-bit Adder Automated Grading Results (submit Lab3A)			_____
(6)	**Using Parameters to create Flexible/Scalable Designs**			
(1)	Simulate Flexible StP SR design with provided test bench	_____	_____	_____
(2)	Mapped Flexible StP SR Automated Grading Results (submit Lab3FS)			_____
(1)	Simulate Flexible PtS SR design with provided test bench	_____	_____	_____
(2)	Mapped Flexible PtS SR Automated Grading Results (submit Lab3FP)			_____
(1)	**Current version of files in SVN**	_____	_____	_____
(9)	**Code Coverage Verification of Current Designs**			
(1)	Demonstrate Code coverage (<u>does not have to be 100%</u>)	_____	_____	_____
(4)	Coverage based Source 16-bit Adder Test Bench Automated Grading Results (submit Lab3CC)			_____
(4)	Coverage based Mapped 16-bit Adder Test Bench Automated Grading Results (submit Lab3CC)			_____
(10)	**Designing a Flexible Counter with Controlled Rollover**			_____
(4)	4-bit Counter RTL Diagram (submit Lab3FC)			_____
(6)	Mapped Counter Automated Grading Results (submit Lab3FC)			_____