ECE337 Lab 2 evaluation sheet

Student Name: _____

MG Account: _____

		TA Initials	Date	Score
(1)	**Lab2 folder and provided files in SVN**	_____	_____	_____
(7)	**Sensor Error Detector Coding and Testing**			
(1)	Simulation of structural style with test bench	_____	_____	_____
(2)	Mapped STRUCTURAL style automated grading results			_____
(2)	Mapped DATAFLOW style automated grading results			_____
(2)	Mapped BEHAVIORAL style automated grading results			_____
(7)	**Design Schematics and Synthesis Optimization**			
(1)	Generated a schematic for the DATAFLOW style	_____	_____	_____
(1)	Generated a schematic for the STRUCTURAL style	_____	_____	_____
(1)	Generated a schematic for the BEHAVIORAL style	_____	_____	_____
(1)	Generated a schematic for the BEHAVIORAL style from the second synthesis pass with the modified makefile	_____	_____	_____
(1)	For the circuit resulting from the first synthesis pass of BEHAVIORAL style Verilog with the modified makefile, what are the: Critical Path Delay _____ Area _____ Power consumption _____	_____	_____	_____
(1)	For the circuit resulting from the second synthesis pass of BEHAVIORAL style Verilog with the modified makefile, what are the: Critical Path Delay _____ Area _____ Power consumption _____	_____	_____	_____
(1)	Which code style is easiest to modify if the number of bits in the input data was altered? Why?	_____	_____	_____

TURN OVER

(1)	**Current version of Sensor Detector files in SVN**	_____ _____	_____
(16)	**Building Block Coding and Testing**		
(2)	Mapped 1-bit Adder Automated Grading Results		_____
(6)	Mapped 4-bit Serial-to-Parallel Shift Register Automated Grading Results		_____
(6)	Mapped 4-bit Parallel-to-Serial Shift Register Automated Grading Results		_____
(2)	Mapped Synchronizer Automated Grading Results		_____