ECE337 Lab 1 Evaluation Sheet

Student Name: _____

MG Account: _____

		TA Initials	Date	Score
(3)	**Subversion SmartSVN Setup**			
(3)	Setup the repository and add Lab1 directory correctly	_____	_____	_____
(17)	**Compiling and Verifying a Comparator**			
(5)	The comparator.v code compiles without errors	_____	_____	_____
(1)	In the ModelSim Verilog Editor what color are:	_____	_____	_____
	RESERVED Verilog words? _____			
	COMMENTS in Verilog code? _____			
(1)	The Signal and Wave Windows are set up correctly	_____	_____	_____
(4)	TEST A: Wave forms are showing proper errors and Results are shown in HEXADECIMAL	_____	_____	_____
(2)	Error free run through Leda	_____	_____	_____
(4)	TEST B: Wave forms are correct and Results are shown in DECIMAL	_____	_____	_____
(5)	**Synthesis of Comparator**			
(1)	How many options/variables are available for the 'mapped/%' rule?	_____	_____	_____
(1)	Comparator synthesis command:	_____	_____	_____
(1)	ERROR-FREE synthesis of Comparator	_____	_____	_____
(2)	CORRECT simulation of synthesized Comparator	_____	_____	_____

TURN OVER

Score

(7) Digital Design Refresher: Sensor Error Detector

(3) Truth Table for Sensor Error Detector _____

(4) K-maps and SUM OF PRODUCTs equation for Sensor Error Detector _____

(8) Digital Design Refresher: "1101" Detector

(2) Moore state transition diagram for the detector _____

(2) Mealy state transition diagram for the detector _____

(2) RTL Diagram for Moore model _____

(2) RTL Diagram for Mealy model _____

(5) Digital Design Refresher: Hardware Building Blocks

(2) RTL Diagram for MSB Serial-to-Parallel Shift-Register _____

(2) RTL Diagram for MSB Parallel-to-Serial Shift-Register _____

(1) RTL Diagram for Synchronizer _____