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# ZPU Reference Handbook



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## Introduction

The Zylin ZPU is the worlds smallest 32 bit CPU with GCC tool chain. The ZPU is a small CPU in two ways: it takes up very little resources and the architecture itself is small. The latter can be important when learning about CPU architectures and implementing variations of the ZPU where aspects of CPU design is examined. In academia students can learn VHDL, CPU architecture in general and complete exercises in the course of a year. The current ZPU instruction set and architecture has not changed for the last couple of years and can be considered quite stable. This shall be presented in detail the following chapters.

Part of this work is based on previous work done by Álvaro Lopes - [alvieboy@alvie.com](mailto:alvieboy@alvie.com) (see legal notice) on the ZPUino – a derivative work of the original ZPU core by Øyvind Harboe - [oyvind.harboe@zylin.com](mailto:oyvind.harboe@zylin.com). The original ZPUino can be found on the internet on the following website: <http://www.alvie.com/zpuino>. Furthermore, the original ZPU and the “ZPU Project” can also be found on the internet on the following website: <https://github.com/zylin/zpu>.

# Instruction Set Summary

## Stack Operation Definitions

TOS = Top Of Stack = SP  
 mem[SP] = valid data = stackA

PUSH:

SP = SP - 1;  
 mem[SP] = data;

POP:

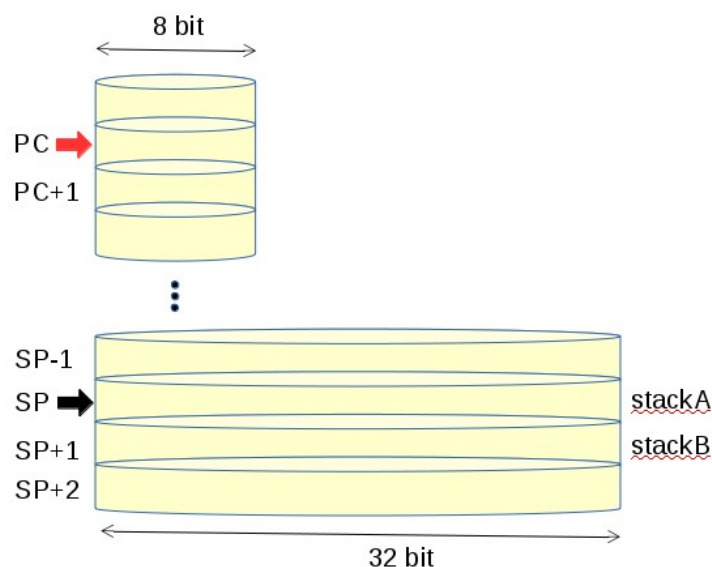
data = mem[SP];  
 SP = SP + 1;

## Memory Operations

PC : Accesses memory in 8 bit cells

SP : Accesses memory in 32 bit cells

NOTE: although PC points to 8 bit cells, the ZPU state machine always fetches 32 bit words and internally breaks down the words into bytes. The Stack Pointer, however, is a pointer to 32 bit cells which are aligned on 4-byte boundary, i.e. SP results in a memory fetch to address 4\*SP and.



NOTE: the CPU implementation in VHDL is such that the TOS

(stackA) and mem[SP+1] (stackB), i.e. both instruction operands, are normally not immediately written back to memory in order to save CPU cycles. Care should be taken while reading the code to exactly understand when (due to state transitions) the stackA and/or stackB need to be written back to memory. See also instruction description below for a better understanding.

This means that stackA and stackB internal variables are actually cached versions of the corresponding memory positions. When SP changes, the stackA and stackB have to be updated accordingly and so does the memory positions corresponding to stackA (SP) and/or stackB (SP+1) before SP is updated.

## Core instructions summary

<i>Mnemonic</i>	<i>Opcode</i>	<i>Description</i>
BREAKPOINT	0000 0000	Sets 'break' line to logic '1'
IM x	1xxx xxxx	
STORESP x	010 $\bar{x}$ xxxx	
LOADSP x	011 $\bar{x}$ xxxx	
ADDSP x	0001 xxxx	
EMULATE x	001x xxxx	
POPPC	0000 0100	
LOAD	0000 1000	
STORE	0000 1100	
PUSHSP	0000 0010	
POPSP	0000 1101	
ADD	0000 0101	
AND	0000 0110	
OR	0000 0111	
NOT	0000 1001	
FLIP	0000 1010	
NOP	0000 1011	

## Optional instructions (emulated)

<i>Mnemonic</i>	<i>Opcode</i>	<i>Decimal</i>	<i>Description</i>
?	0010 0000	32	
N/A	0010 0001	33	
LOADH	0010 0010	34	
STOREH	0010 0011	35	
LESSTHAN	0010 0100	36	
LESSTHANOREQUAL	0010 0101	37	
ULESSTHAN	0010 0110	38	
ULESSTHANOREQUAL	0010 0111	39	
SWAP	0010 1000	40	
MULT	0010 1001	41	
LSHIFTRIGHT	0010 1010	42	
ASHIFLEFT	0010 1011	43	
ASHIFTRIGHT	0010 1100	44	
CALL	0010 1101	45	
EQ	0010 1110	46	
NEQ	0010 1111	47	
NEG	0011 0000	48	
SUB	0011 0001	49	
XOR	0011 0010	50	
LOADB	0011 0011	51	
STOREB	0011 0100	52	
DIV	0011 0101	53	
MOD	0011 0110	54	
EQBRANCH	0011 0111	55	
NEQBRANCH	0011 1000	56	
POPPCREL	0011 1001	57	
CONFIG	0011 1010	58	
PUSHPC ( <i>a</i> )	0011 1011	59	
SYSCALL ( <i>a</i> )	0011 1100	60	
PUSHSPADD	0011 1101	61	
HALFMULT	0011 1110	62	
CALLPCREL	0011 1111	63	

## Instruction Mapping

➤	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	BRK	NA4	PUSHSP	NA3	POPPC	ADD	AND	OR	LOAD	NOT	FLIP	NOP	STORE	POPSP	NA2	NA
0001	ADDTOP	SHIFT	ADDSP	ADDSP	ADDSP	ADDSP	ADDSP	ADDSP	ADDSP	ADDSP	ADDSP	ADDSP	ADDSP	ADDSP	ADDSP	ADDSP
0010	?	N/A	EMU	EMU	EMU	EMU	EMU	EMU	EMU	EMU	EMU	EMU	EMU	EMU	EMU	EMU
0011	EMU	EMU	EMU	EMU	EMU	EMU	EMU	EMU	EMU	EMU	EMU	EMU	EMU	EMU	EMU	EMU
0100	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP
0101	POP	POPDOWN	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP
0110	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP
0111	DUP	DUPSTACKB	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP
1000	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM
1001	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM
1010	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM
1011	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM
1100	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM
1101	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM
1110	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM
1111	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM

## Implemented Instructions

↗	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	BRK	NA4	PUSHSP	NA3	POPPC	ADD	AND	OR	LOAD	NOT	FLIP	NOP	STORE	POPSP	NA2	NA
0001	ADDSP	ADDSP	ADDSP	ADDSP	ADDSP	ADDSP	ADDSP	ADDSP	ADDSP	ADDSP	ADDSP	ADDSP	ADDSP	ADDSP	ADDSP	ADDSP
0010	?	N/A	EMU	EMU	EMU	EMU	EMU	EMU	EMU	EMU	EMU	EMU	EMU	EMU	EMU	EMU
0011	EMU	EMU	EMU	EMU	EMU	EMU	EMU	EMU	EMU	EMU	EMU	EMU	EMU	EMU	EMU	EMU
0100	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP
0101	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP	STORESP
0110	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP
0111	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP	LOADSP
1000	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM
1001	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM
1010	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM
1011	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM
1100	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM
1101	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM
1110	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM
1111	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM



## Instructions Specification

OPCODE	<b>IM x</b>																
MACHINE CODE	<b>1xxxxxxxx</b>																
IMPLEMENTED	<b>YES</b>																
EMULATED	<b>NO</b>																
SP ACTION	<b>single PUSH</b>																
DESCRIPTION	Pushes immediate value into TOS																
PSEUDOCODE	<pre> if (idim='0') { // no previous IM     idim      = 1;     mem[sp+1] = stackB;     stackB    = stackA;     stackA    = {mem[sp][24:0], x[6:0]}; // sign extend     sp        = sp - 1; } else {      // previous IM     stackA    = { stackA[31:7], x[6:0] }; } </pre>																
EQUIVALENT CODE	<pre> if (!idim) {     push(x); } else {     idim = 1;     a     = pop();     push( a&lt;&lt;7 + x ); } </pre>																
INTERNAL LAYOUT	<p>PREVIOUS "IM" (idim='1'):</p> <table border="1"> <thead> <tr> <th>Before</th> <th>After</th> </tr> </thead> <tbody> <tr> <td>SP-1 → [ ]</td> <td>SP-1 → [ ]</td> </tr> <tr> <td>SP → [ ] ← A</td> <td>SP → [ ] ← A = {A[31:7], x}</td> </tr> <tr> <td>SP+1 → [ ] ← B</td> <td>SP+1 → [ ] → B</td> </tr> </tbody> </table> <p>ELSE (idim='0'):</p> <table border="1"> <thead> <tr> <th>Before</th> <th>After</th> </tr> </thead> <tbody> <tr> <td>SP-1 → [ ]</td> <td>SP → [ ] ← A = sign_ext(x)</td> </tr> <tr> <td>SP → [ ] ← A</td> <td>SP+1 → [ ] → B</td> </tr> <tr> <td>SP+1 → [ ] ← B</td> <td>SP+2 → [B]</td> </tr> </tbody> </table>	Before	After	SP-1 → [ ]	SP-1 → [ ]	SP → [ ] ← A	SP → [ ] ← A = {A[31:7], x}	SP+1 → [ ] ← B	SP+1 → [ ] → B	Before	After	SP-1 → [ ]	SP → [ ] ← A = sign_ext(x)	SP → [ ] ← A	SP+1 → [ ] → B	SP+1 → [ ] ← B	SP+2 → [B]
Before	After																
SP-1 → [ ]	SP-1 → [ ]																
SP → [ ] ← A	SP → [ ] ← A = {A[31:7], x}																
SP+1 → [ ] ← B	SP+1 → [ ] → B																
Before	After																
SP-1 → [ ]	SP → [ ] ← A = sign_ext(x)																
SP → [ ] ← A	SP+1 → [ ] → B																
SP+1 → [ ] ← B	SP+2 → [B]																

OPCODE	<b>EMULATE</b> <b>x</b>								
MACHINE CODE	<b>001</b> <b>xxxxxx</b>								
IMPLEMENTED	<b>YES</b>								
EMULATED	<b>NO</b>								
SP ACTION	<b>PUSH</b>								
DESCRIPTION	If the instruction is not implemented in hardware, this instruction will fired-up the microcode implementation of the function. 0<= x <= 31								
PSEUDOCODE	<pre> mem[sp+1] = stackB; // save cached stackB sp        = sp - 1; // make room for push stackB    = stackA; stackA    = pc + 1; // return address pc        = 32*x;   // microcode at address 32*x fetch(); </pre>								
EQUIVALENT CODE	<i>call(32*x);</i>								
INTERNAL LAYOUT	<table border="0"> <thead> <tr> <th>Before</th><th>After</th></tr> </thead> <tbody> <tr> <td>SP-1 → [ ]</td><td>SP → [ ] ← A = <b>return_address</b></td></tr> <tr> <td>SP → [ ] ← A</td><td>SP+1 → [ ] ← B</td></tr> <tr> <td>SP+1 → [ ] ← B</td><td>SP+2 → [B]</td></tr> </tbody> </table>	Before	After	SP-1 → [ ]	SP → [ ] ← A = <b>return_address</b>	SP → [ ] ← A	SP+1 → [ ] ← B	SP+1 → [ ] ← B	SP+2 → [B]
Before	After								
SP-1 → [ ]	SP → [ ] ← A = <b>return_address</b>								
SP → [ ] ← A	SP+1 → [ ] ← B								
SP+1 → [ ] ← B	SP+2 → [B]								

OPCODE	<b>STORESP x</b>												
MACHINE CODE	<b>010xxxxx</b>												
IMPLEMENTED	<b>YES</b>												
EMULATED	<b>NO</b>												
SP ACTION	<b>POP</b>												
DESCRIPTION	Pop TOS and store it at mem[SP+x]												
PSEUDOCODE	<pre> (storeSP) mem[sp+x] = stackA;  // NOTE: x is always unsigned stackA    = stackB; sp        = sp + 1; (storeSP2) stackB    = mem[sp+1]; </pre>												
EQUIVALENT CODE	<pre> mem[SP+x] = TOS; pop(); </pre>												
INTERNAL LAYOUT	<table border="1"> <thead> <tr> <th>Before</th><th>After</th></tr> </thead> <tbody> <tr> <td>SP → [ ] ← A</td><td>SP → [ ] ← A (= prev B)</td></tr> <tr> <td>SP+1 → [ ] ← B</td><td>SP+1 → [ ] → B (fetched )</td></tr> <tr> <td>SP+2 → [ ]</td><td></td></tr> <tr> <td>...</td><td></td></tr> <tr> <td>SP+x → [ ? ]</td><td>SP+x-1 → [A] (modified)</td></tr> </tbody> </table>	Before	After	SP → [ ] ← A	SP → [ ] ← A (= prev B)	SP+1 → [ ] ← B	SP+1 → [ ] → B (fetched )	SP+2 → [ ]		...		SP+x → [ ? ]	SP+x-1 → [A] (modified)
Before	After												
SP → [ ] ← A	SP → [ ] ← A (= prev B)												
SP+1 → [ ] ← B	SP+1 → [ ] → B (fetched )												
SP+2 → [ ]													
...													
SP+x → [ ? ]	SP+x-1 → [A] (modified)												

OPCODE	<b>LOADSP x</b>												
MACHINE CODE	<b>011xxxxx</b>												
IMPLEMENTED	<b>YES</b>												
EMULATED	<b>NO</b>												
SP ACTION	<b>PUSH</b>												
DESCRIPTION	Push value at mem[SP+x] into stack												
PSEUDOCODE	<pre> (LoadSP) mem[sp+1] = stackB;      // writeback cached stackB sp        = sp - 1;      // required for push (LoadSP2) read      = mem[SP+x+1]; // fetch mem[SP+x] (LoadSP3) stackB    = stackA;      // stackB is now = old stackA stackA    = read;        // stackA = mem[SP+x] </pre>												
EQUIVALENT CODE	<pre> a = mem[sp+x]; push(a); </pre>												
INTERNAL LAYOUT	<table border="1"> <thead> <tr> <th>Before</th> <th>After</th> </tr> </thead> <tbody> <tr> <td>SP-1 → [ ]</td> <td>SP → [ ] → A (= v )</td> </tr> <tr> <td>SP → [ ] ← A</td> <td>SP+1 → [ ] ← B (= prev A)</td> </tr> <tr> <td>SP+1 → [ ] ← B</td> <td>SP+2 → [ ]</td> </tr> <tr> <td>...</td> <td></td> </tr> <tr> <td>SP+x → [v]</td> <td>SP+x+1 → [v]</td> </tr> </tbody> </table>	Before	After	SP-1 → [ ]	SP → [ ] → A (= v )	SP → [ ] ← A	SP+1 → [ ] ← B (= prev A)	SP+1 → [ ] ← B	SP+2 → [ ]	...		SP+x → [v]	SP+x+1 → [v]
Before	After												
SP-1 → [ ]	SP → [ ] → A (= v )												
SP → [ ] ← A	SP+1 → [ ] ← B (= prev A)												
SP+1 → [ ] ← B	SP+2 → [ ]												
...													
SP+x → [v]	SP+x+1 → [v]												

OPCODE	<b>ADDSP x</b>
MACHINE CODE	<b>0001xxxx</b>
DESCRIPTION	<code>mem[sp] = mem[sp] + mem[sp+x&lt;&lt;2];</code>

OPCODE	<b>BREAKPOINT</b>
MACHINE CODE	<b>00000000</b>
DESCRIPTION	<code>call exception vector</code>

OPCODE	<b>SHIFTLTLEFT</b>
MACHINE CODE	<b>00000001</b>
DESCRIPTION	.

OPCODE	<b>PUSHSP</b>
MACHINE CODE	<b>00000010</b>
DESCRIPTION	<code>mem[sp-1] = sp; sp = sp - 1;</code>

OPCODE	<b>POPINT</b>
MACHINE CODE	<b>00000011</b>
DESCRIPTION	<code>pc = mem[sp]; sp = sp + 1; fetch() ; decode() ; clear_interrupt_flag();</code>

OPCODE	<b>POPPC</b>
MACHINE CODE	<b>00000100</b>
DESCRIPTION	<code>pc = mem[sp]; sp = sp + 1;</code>

OPCODE	<b>ADD</b>
MACHINE CODE	<b>00000101</b>
DESCRIPTION	<code>mem[sp+1] = mem[sp+1] + mem[sp]; sp = sp + 1;</code>

OPCODE	<b>AND</b>
MACHINE CODE	<b>00000110</b>
DESCRIPTION	<code>mem[sp+1] = mem[sp+1] &amp; mem[sp]; sp = sp + 1;</code>

OPCODE	<b>OR</b>
MACHINE CODE	<b>00000111</b>
DESCRIPTION	<code>mem[sp+1] = mem[sp+1]   mem[sp]; sp = sp + 1;</code>

OPCODE	<b>LOAD</b>
MACHINE CODE	<b>00001000</b>
DESCRIPTION	<code>mem[sp] = mem[ mem[sp] ];</code>

OPCODE	<b>NOT</b>
MACHINE CODE	<b>00001001</b>
DESCRIPTION	<code>mem[sp] = not mem[sp];</code>

OPCODE	<b>NOT</b>
MACHINE CODE	<b>00001001</b>
DESCRIPTION	<code>mem[sp] = not mem[sp];</code>

OPCODE	<b>FLIP</b>
MACHINE CODE	<b>00001010</b>
DESCRIPTION	<code>mem[sp] = flip( mem[sp] );</code>

OPCODE	<b>NOP</b>
MACHINE CODE	<b>00001011</b>
DESCRIPTION	<code>no operation</code>

OPCODE	<b>STORE</b>
MACHINE CODE	<b>00001100</b>
DESCRIPTION	<code>mem[mem[sp]] = mem[sp+1];</code> <code>sp = sp + 2;</code>

OPCODE	<b>POPSP</b>
MACHINE CODE	<b>00001101</b>
DESCRIPTION	<code>sp = mem[sp];</code>

OPCODE	<b>COMPARE / IPSUM</b>
MACHINE CODE	<b>00001110</b>
DESCRIPTION	<pre> c  = mem[sp]; s  = mem[sp+1]; sum = 0; while (c--&gt;0){     sum += halfword(mem[s],s);     s    += 2; }; sp      = sp+1; mem[sp] = sum; (overwrites mem[0] &amp; mem[4] words) </pre>

OPCODE	<b>SNCPY</b>
MACHINE CODE	<b>00001111</b>
DESCRIPTION	<pre> c = mem[sp]; d = mem[sp+1]; s = mem[sp+2]; while ( *(char*)s != 0 &amp;&amp; c&gt;0 ){     *((char*)d++) =* ((char*)s++));     c-- }; sp = sp+3; (overwrites mem[0] &amp; mem[4] words) </pre>

OPCODE	<b>SNCPY</b>
MACHINE CODE	<b>00100000</b>
DESCRIPTION	<pre> c = mem[sp]; d = mem[sp+1]; s = mem[sp+2]; while (c--&gt;0) {     mem[d++] = mem[s++]; } sp = sp+3; (overwrites mem[0] &amp; mem[4] words) </pre>

OPCODE	<b>WCPY</b>
MACHINE CODE	<b>00100001</b>
DESCRIPTION	<pre> v = mem[sp]; c = mem[sp+1]; d = mem[sp+2]; while (c--&gt;0) {     mem[d++] = v; } sp = sp+3; (overwrites mem[0] &amp; mem[4] words) </pre>

OPCODE	<b>LOADH</b>
MACHINE CODE	<b>00100010</b>
DESCRIPTION	<code>mem[sp] = halfword[ mem[sp] ];</code>

OPCODE	<b>STOREH</b>
MACHINE CODE	<b>00100011</b>
DESCRIPTION	<pre> halfword[mem[sp]] = (mem[sp+1] &amp; 0xFFFF); sp = sp + 2; </pre>

OPCODE	<b>LESSTHAN</b>
MACHINE CODE	<b>00100100</b>
DESCRIPTION	<pre> if ( (mem[sp]-mem[sp+1]) &lt; 0 ){     mem[sp+1] = 1 } else {     mem[sp+1] = 0; } sp = sp + 1; </pre>

OPCODE	<b>LESSTHANOEQUAL</b>
MACHINE CODE	<b>00100101</b>
DESCRIPTION	<pre> if ( (mem[sp]-mem[sp+1]) &lt;= 0 ){     mem[sp+1] = 1 } else {     mem[sp+1] = 0; } sp = sp + 1; </pre>



OPCODE	<b>ULESSTHAN</b>
MACHINE CODE	<b>00100101</b>
DESCRIPTION	<pre> if ( (unsigned(mem[sp])-unsigned(mem[sp+1])) &lt; 0 ){     mem[sp+1] = 1 } else {     mem[sp+1] = 0; } sp = sp + 1; </pre>

OPCODE	<b>ULESSTHANORQUAL</b>
MACHINE CODE	<b>00100110</b>
DESCRIPTION	<pre> if ( (unsigned(mem[sp])-unsigned(mem[sp+1])) &lt;= 0 ){     mem[sp+1] = 1 } else {     mem[sp+1] = 0; } sp = sp + 1; </pre>

OPCODE	<b>SWAP</b>
MACHINE CODE	<b>00101000</b>
DESCRIPTION	.

OPCODE	<b>MULT</b>
MACHINE CODE	<b>00101001</b>
DESCRIPTION	<pre> mem[sp+1] = mem[sp+1] * mem[sp]; sp        = sp + 1; </pre>

OPCODE	<b>LSHIFTRIGHT</b>
MACHINE CODE	<b>00101010</b>
DESCRIPTION	<pre> mem[sp+1] = mem[sp+1] &gt;&gt; (mem[sp] &amp; 0x1f); sp        = sp + 1; </pre>

OPCODE	<b>ASHIFLEFT</b>
MACHINE CODE	<b>00101011</b>
DESCRIPTION	<pre> mem[sp+1] = mem[sp+1] &lt;&lt; (mem[sp] &amp; 0x1f); sp        = sp + 1; </pre>

OPCODE	<b>ASHIFTRIGHT</b>
MACHINE CODE	<b>00101100</b>
DESCRIPTION	<code>mem[sp+1] = mem[sp+1] signed&gt;&gt; (mem[sp] &amp; 0x1f);</code> <code>sp = sp + 1;</code>

OPCODE	<b>CALL</b>								
MACHINE CODE	<b>00101101</b>								
IMPLEMENTED	<b>YES</b>								
EMULATED	<b>YES</b>								
SP ACTION	<b>POP + PUSH</b>								
DESCRIPTION	jumps to memory address TOP, while adjusting the stack with the return address pc+1								
PSEUDO CODE	<code>x = stackA[L-1:0]; // (POP) L: mem address lines</code> <code>stackA = pc + 1; // (PUSH) return address</code> <code>pc = x; // jump to x</code>								
EQUIVALENT CODE	<code>x = pop();</code> <code>call(x); // pushes PC+1 into stack</code>								
INTERNAL LAYOUT	<table border="1"> <thead> <tr> <th>Before</th> <th>After</th> </tr> </thead> <tbody> <tr> <td>SP-1 → [ ]</td> <td>SP-1 → [ ]</td> </tr> <tr> <td>SP → [ ] ← A</td> <td>SP → [ ] ← A (= pc+1)</td> </tr> <tr> <td>SP+1 → [ ] ← B</td> <td>SP+1 → [ ] ← B</td> </tr> </tbody> </table>	Before	After	SP-1 → [ ]	SP-1 → [ ]	SP → [ ] ← A	SP → [ ] ← A (= pc+1)	SP+1 → [ ] ← B	SP+1 → [ ] ← B
Before	After								
SP-1 → [ ]	SP-1 → [ ]								
SP → [ ] ← A	SP → [ ] ← A (= pc+1)								
SP+1 → [ ] ← B	SP+1 → [ ] ← B								

OPCODE	<b>EQ</b>
MACHINE CODE	<b>00101110</b>
DESCRIPTION	<code>if ( mem[sp] == mem[sp+1] ) {</code> <code>    a = 1;</code> <code>} else {</code> <code>    a = 0;</code> <code>}</code> <code>mem[sp+1] = a;</code> <code>sp = sp + 1</code>

OPCODE	<b>NEQ</b>
MACHINE CODE	<b>00101111</b>
DESCRIPTION	<pre> if ( mem[sp] != mem[sp+1] ) {     a = 1; } else {     a = 0; } mem[sp+1] = a; sp      = sp + 1 </pre>

OPCODE	<b>NEG</b>
MACHINE CODE	<b>00110000</b>
DESCRIPTION	<pre> mem[sp] = NOT(mem[sp]) + 1; </pre>

OPCODE	<b>SUB</b>
MACHINE CODE	<b>00110001</b>
DESCRIPTION	<pre> mem[sp+1] = mem[sp+1] - mem[sp]; sp      = sp+1; </pre>

OPCODE	<b>XOR</b>
MACHINE CODE	<b>00110010</b>
DESCRIPTION	<pre> mem[sp+1] = mem[sp+1] XOR mem[sp]; sp      = sp+1; </pre>

OPCODE	<b>LOADB</b>
MACHINE CODE	<b>00110011</b>
DESCRIPTION	<pre> mem[sp] = byte[ mem[sp] ]; </pre>

OPCODE	<b>STOREB</b>
MACHINE CODE	<b>00110100</b>
DESCRIPTION	<pre> byte[mem[sp]] = (mem[sp+1] &amp; 0xFF); sp      = sp + 2; </pre>

OPCODE	<b>DIV</b>
MACHINE CODE	<b>00110101</b>
DESCRIPTION	.

OPCODE	<b>MOD</b>
MACHINE CODE	<b>00110110</b>
DESCRIPTION	.

OPCODE	<b>EQBRANCH</b>
MACHINE CODE	<b>00110111</b>
DESCRIPTION	<pre> if ( mem[sp+1] == 0 ) {     pc = pc + mem[sp];     sp = sp + 2; } </pre>

OPCODE	<b>NEQBRANCH</b>
MACHINE CODE	<b>00111000</b>
DESCRIPTION	<pre> if ( mem[sp+1] != 0 ) {     pc = pc + mem[sp];     sp = sp + 2; } </pre>

OPCODE	<b>POPPCREL</b>
MACHINE CODE	<b>00111001</b>
DESCRIPTION	<pre> pc = pc + mem[sp]; sp = sp + 1; </pre>

OPCODE	<b>CONFIG</b>
MACHINE CODE	<b>00111010</b>
DESCRIPTION	.

OPCODE	<b>PUSHPC</b>
MACHINE CODE	<b>00111011</b>
DESCRIPTION	<pre> sp      = sp - 1; mem[sp] = pc; </pre>

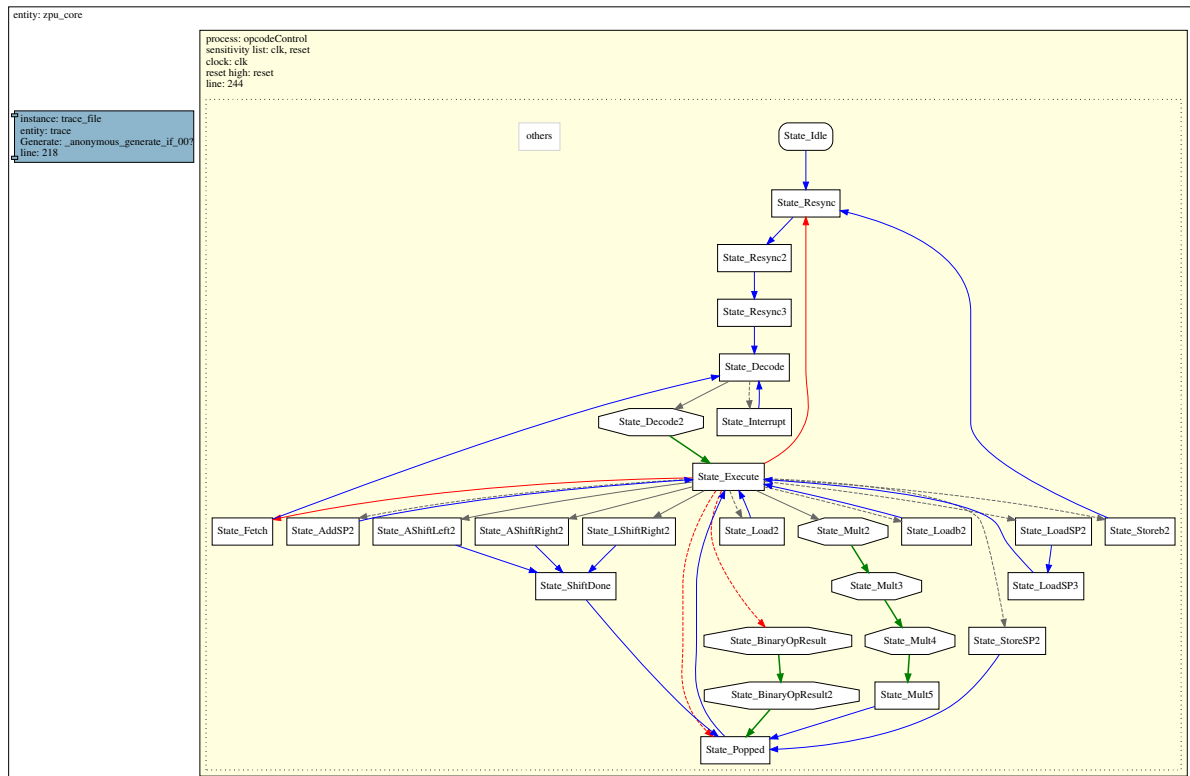
OPCODE	<b>SYSCALL</b>
MACHINE CODE	<b>00111100</b>
DESCRIPTION	.

OPCODE	<b>PUSHSPADD</b>
MACHINE CODE	<b>00111101</b>
DESCRIPTION	<code>mem[sp] = sp + (mem[sp] &lt;&lt; 2)</code>

OPCODE	<b>HALFMULT</b>
MACHINE CODE	<b>00111110</b>
DESCRIPTION	<code>mem[sp+1] = 16bits(mem[sp]) * 16bits(mem[sp+1]);</code> <code>sp = sp + 1;</code>

OPCODE	<b>CALLPCREL</b>										
MACHINE CODE	<b>00111110</b>										
IMPLEMENTED	<b>YES</b>										
EMULATED	<b>YES</b>										
SP ACTION	<b>POP + PUSH</b>										
DESCRIPTION	jumps to memory address PC + TOP, while adjusting the stack with the return address pc+1										
PSEUDOCODE	<code>x = stackA[L-1:0]; // (POP) L: mem address lines</code> <code>stackA = pc + 1; // (PUSH) return address</code> <code>pc = pc + x; // jump to pc+x</code>										
EQUIVALENT CODE	<code>x = pop();</code> <code>call(pc+x); // pushes PC+1 into stack</code>										
INTERNAL LAYOUT	<table> <tr> <th>Before</th><th>After</th></tr> <tr> <td>-----+-----</td><td></td></tr> <tr> <td>SP-1 → [ ]</td><td>SP-1 → [ ]</td></tr> <tr> <td>SP → [ ] ← A</td><td>SP → [ ] ← A (= pc+1)</td></tr> <tr> <td>SP+1 → [ ] ← B</td><td>SP+1 → [ ] ← B</td></tr> </table>	Before	After	-----+-----		SP-1 → [ ]	SP-1 → [ ]	SP → [ ] ← A	SP → [ ] ← A (= pc+1)	SP+1 → [ ] ← B	SP+1 → [ ] ← B
Before	After										
-----+-----											
SP-1 → [ ]	SP-1 → [ ]										
SP → [ ] ← A	SP → [ ] ← A (= pc+1)										
SP+1 → [ ] ← B	SP+1 → [ ] ← B										

# State Machine Transition Diagram



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