CS/ECE 5710/6710 Digital VLSI Design
Final Report
Due Wednesday, December 16

Goal: To document your group's project, and your group's standard cell library

Overview

Your final report (one per group) should contain three parts:

The first part is a conference-style paper of no more than 10 pages that describes your project. The target audience for this paper is someone who is knowledgeable about VLSI, but would like to know the details behind your project. That means that you don't have to explain how CMOS gates work, but you should describe what your project is, what it's useful for, why it's interesting, and what your approach was to building the project.

The body of the paper should document the work you did on your project. What does the project do specifically? What is the target application? What are the interesting circuit parts of your project? How did you do those interesting parts? What special features did your project include? Why? What is the overall block diagram of your project? How would you interface to your chip? How would you operate your chip? What other external pieces would you need to build a system around your chip? What is the testing (simulation) environment? How did you test the project? What were the results?

Evaluation of the results of your project is an important part of the paper. Include figures and tables as they make sense. Finally, include a conclusions section where you recap the main features of your project, and give some opinions on what you did well and what you could have done better. Include references at the end if they are appropriate.

The paper should be no more than 10 pages and formatted in "camera ready" double-column form. There's a LaTeX format file on the Canvas page that the IEEE uses for its camera-ready document production, but I'm guessing that there aren't that many LaTeX users out there any more. It's still one of the main standards for academic document production, but you can use whatever you're comfortable with. I'll also include a MS Word example format from an IEEE journal. You can use this template if you prefer Word. Whatever text formatter you use, you should use double-column text with text either 10pt or 11pt. Look at any IEEE journal or conference to see how these papers should be formatted. Include a title and author list, then an abstract, an introduction, a paper body with technical details, a conclusion, and references if appropriate.

The second part of the final documentation is a set of detailed design documents that cover the actual circuits and layouts. Please spend some time to make sure that it's well organized! I'd like to see the complete overview of your project, a block diagram of the major pieces, and a plot of the floorplan showing those major pieces. Also include the pinout and diagram that shows how your project would fit into a system. Then include circuits (schematics) and layouts for all the major pieces of your design that you did by hand. Also include any Verilog code you wrote and synthesized. You don't need to include test results for the sub-pieces, but you should include overall test results from running the complete project in simulation. Please include a table of contents or a readme file that describes what I'm looking at and where it is in the document. Make sure to include the name of your top-level project cell, and a directory path to your Lib6710_xx directory, and to your project directory.

The third part is documentation of your standard cell library. I'd like details of each cell that ended up in your library: schematic, layout, behavioral (Verilog) model, timing data, and user's guide (if it's more complex than a gate). Include enough documentation so that someone not in your group could conceivably use your standard cells in their own designs. Commercial cell library documentation has a page or more for each cell showing the schematic, the layout, a short description of the function (this can be as short as one line of Boolean equation), and a table showing some of the performance information. This is essentially an abbreviated version of the information that's in a .lib file – a few combinations of delays for differnet input slopes and output loads, for example You don't have to be all that careful about this part because it's also contained in your .lib file. For simple combinational gates your documentaiton can be just a page or two of schematic, Verilog behavioral, and layout information, along with a Boolean expression for function. For a cell like a DFF, the behavioral view will have details of the behavior, but it would be good to have just a sentence or two about the overall behavior (e.g. "Rising edge triggered, master slave flip flop with asynchronous active-low clear")

In addition to the document about your library, please handin your .lef, .lib, and .v fiiles instead of printing them out. Use handin using the "Report" assignment for all documents you handin (part1 paper, part2 documentation, part3 library documentation, and Lib6710_xx.lef, .lib, and .v files.

In addition to the materials handed in using handin and the Report assignmnent, please let me know what the directory path is to your Lib6710_xx directory, and to your main project directory. Make sure that your Cadence data is readable by your group (I can become a member of any group in the class to see your data). Part of your "part 2 documentation" should include the top-level project cell name so that I can go lok at that if I need to.