T.E.S.S. Cell Data Sheet

ECE 6710 – Digital VLSI Design

Group 09

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AOI21

Cell Description:
This is a standard 3 input AND OR INVERT (AOI) cell. This cells functionality is described by the following Boolean equation:

$$Y = \neg((A \wedge B) \vee C)$$

Truth Table:

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Behavioral Verilog:

```
//Verilog HDL for "Lib6710_06", "AOI21X1" "behavioral"
module AOI21X1( Y, A, B, C );
  input A;
  input C;
  output Y;
  input B;
  assign Y = ~((A&B) | C);
  specify
  (A => Y) = (1.0, 1.0);
  (B => Y) = (1.0, 1.0);
  (C => Y) = (1.0, 1.0);
  endspecify
endmodule
```

Cell Size:

Drive Strength	Height (µM)	Width (µM)
AOI21X1	27.0	9.6

Performance:

Propagation Delay (Rising Outputs):

Drive Strength	Min. (nS)	Max. (nS)
AOI21X1	0.249604	3.820011

Output Rise Time:

Drive Strength	Min. (nS)	Max. (nS)
AOI21X1	0.207889	3.203555

Propagation Delay (Falling Outputs):

Drive Strength	Min. (nS)	Max. (nS)
AOI21X1	0.367765	5.978167

Output Fall Time:

Drive Strength	Min. (nS)	Max. (nS)
AOI21X1	0.287229	4.7676

Logic Symbol:

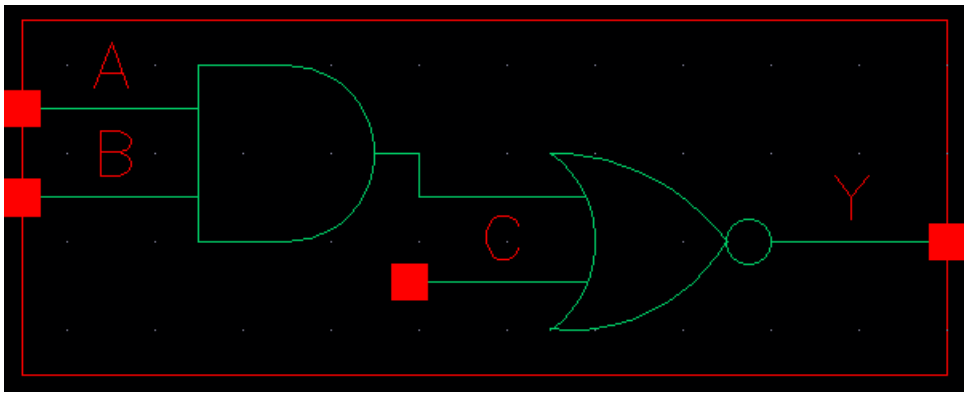

Figure 1: Symbol View for the AOI21 cell.

CMOS Schematic:

The following figure displays the CMOS schematics for the AOI21 cell

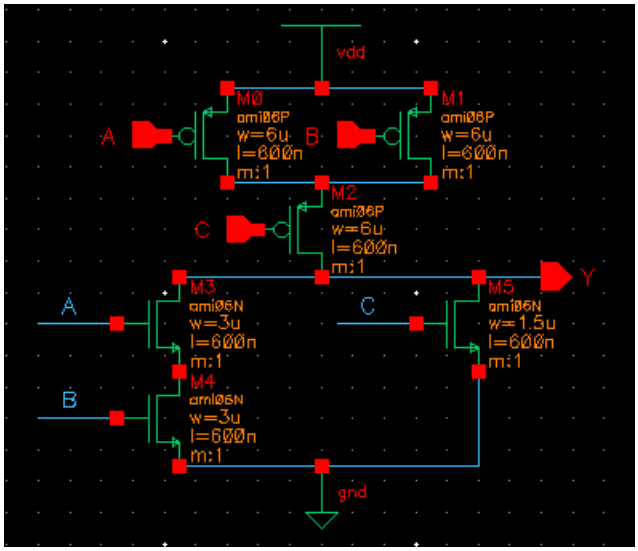

Figure 2: CMOS Schematic for the AOI21X1 cell.

CMOS Layout:

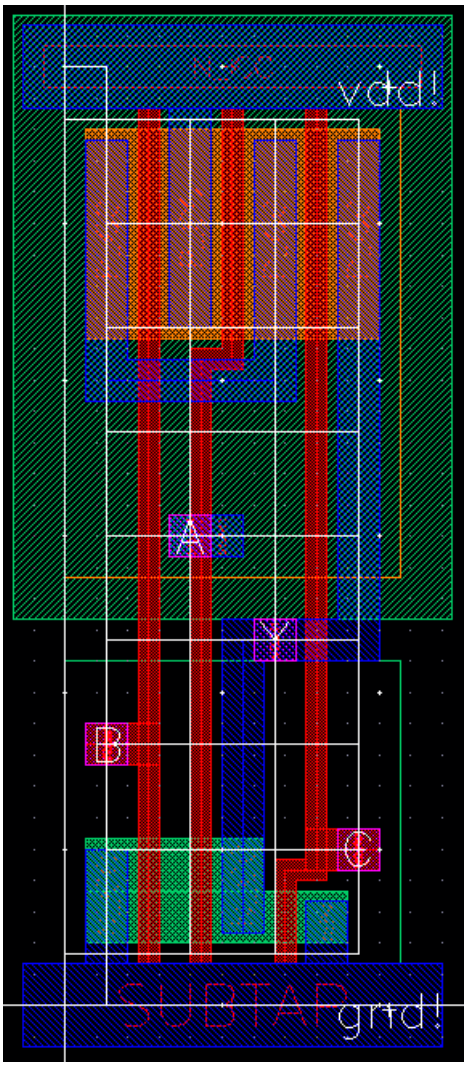

Figure 3: CMOS layout for the AOI21X1 cell.

AOI22

Cell Description:
This is a standard 4 input AND OR INVERT (AOI) cell. This cells functionality is described by the following Boolean equation:

$$Y = \neg((A \wedge B) \vee (C \wedge D))$$

Truth Table:

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Behavioral Verilog:

```
//Verilog HDL for "Lib6710_06", "AOI22x1" "behavioral"
module AOI22X1( Y, A, B, C, D );
 input A;
 input B;
 output Y;
 input C;
 input D;
 assign Y = ~((A&B) | (C&D));
 specify
 (A => Y) = (1.0, 1.0);
 (B => Y) = (1.0, 1.0);
 (C => Y) = (1.0, 1.0);
 (D => Y) = (1.0, 1.0);
 endspecify
endmodule
```

Cell Size:

Drive Strength	Height (µM)	Width (µM)
AOI22X1	27.0	12.0

Performance:

Propagation Delay (Rising Outputs):

Drive Strength	Min. (nS)	Max. (nS)
AOI22X1	0.257172	3.554636

Output Rise Time:

Drive Strength	Min. (nS)	Max. (nS)
AOI22X1	0.21.544	2.844555

Propagation Delay (Falling Outputs):

Drive Strength	Min. (nS)	Max. (nS)
AOI22X1	0.280125	3.91496

Output Fall Time:

Drive Strength	Min. (nS)	Max. (nS)
AOI22X1	0.209476	3.092532

Logic Symbol:

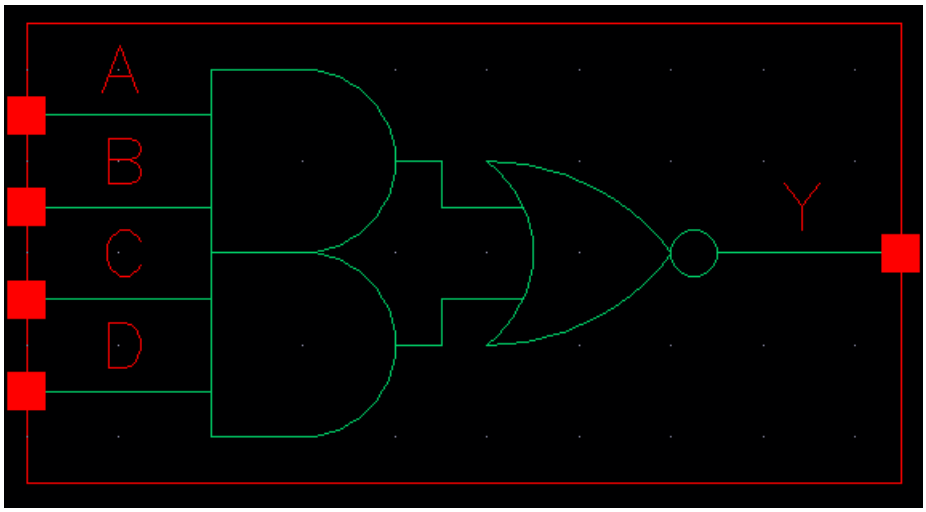

Figure 4: Symbol View for the AOI22 cell.

CMOS Schematic:

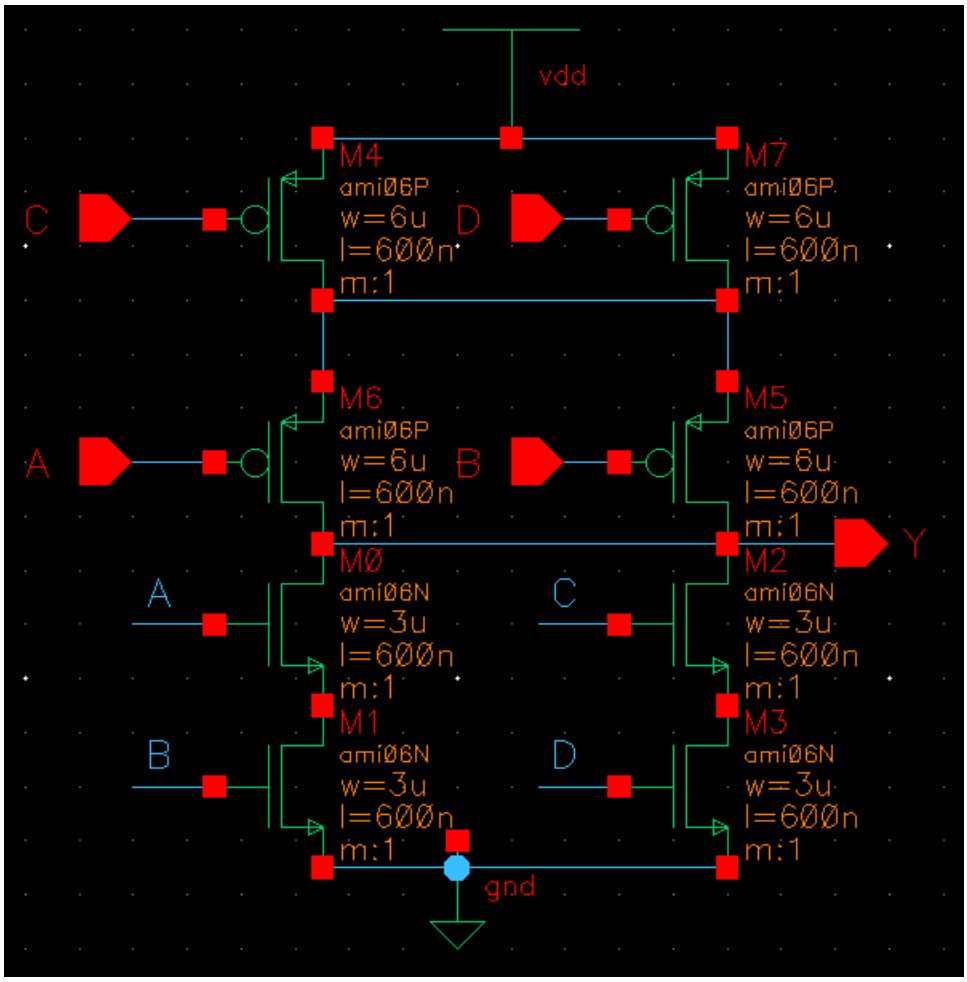

Figure 5: CMOS Schematic for the AOI22X1 cell.

CMOS Layout:

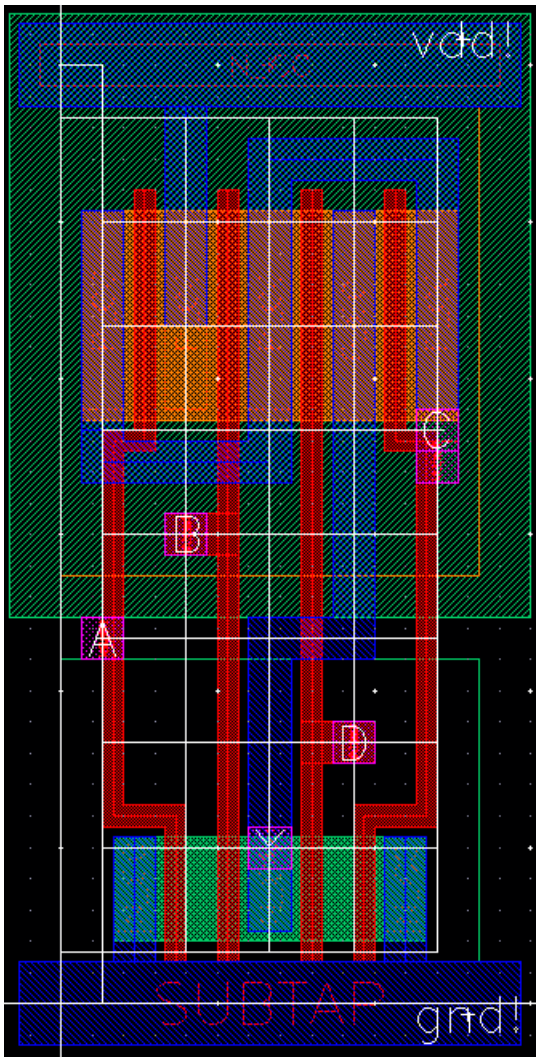

Figure 6: CMOS layout for the AOI22X1 cell.

BUF

Cell Description:

This is a standard buffer cell with the following Boolean equation.

$$Y = A$$

Each buffer is constructed by two inverters in series. To compensate for rise and fall times the input inverter is scaled appropriately by required drive strength of the output. In this cell library the both the BUFX2 and BUFX4 are driven by an inverter with a drive strength of 1, and the BUFX8 is driven by an invert with a drive strength of 2.

Truth Table:

A	Y
0	0
1	1

Behavioral Verilog:

The behavioral Verilog for the inverter is independent of its drive strength. Replace the N in the module name with the respective drive strength (i.e. 1, 2, and 4).

```
//Verilog HDL for "Lib6710_06", "BUFX2" "behavioral"
module BUFX2 ( Y, A );
 input A;
 output Y;
  buf _i0(Y,A);
   specify
    (A => Y) = (1.0, 1.0);
  endspecify
endmodule
```

Cell Size:

Drive Strength	Height (µM)	Width (µM)
BUFX2	27.0	7.2
BUFX4	27.0	7.2
BUFX8	27.0	9.6

Performance:

Propagation Delay (Rising Outputs):

Drive Strength	Min. (nS)	Max. (nS)
BUFX2	0.460967	4.271176
BUFX4	0.550102	4.247614
BUFX8	0.453907	4.082325

Output Rise Time:

Drive Strength	Min. (nS)	Max. (nS)
BUFX2	0.200962	3.287624
BUFX4	0.214433	3.139659
BUFX8	0.185384	3.129319

Propagation Delay (Falling Outputs):

Drive Strength	Min. (nS)	Max. (nS)
BUFX2	0.428696	4.678109
BUFX4	0.468653	4.338193
BUFX8	0.433059	4.346652

Output Fall Time:

Drive Strength	Min. (nS)	Max. (nS)
BUFX2	0.204083	3.555283
BUFX4	0.195164	3.149672
BUFX8	0.184735	3.146479

Logic Symbol:

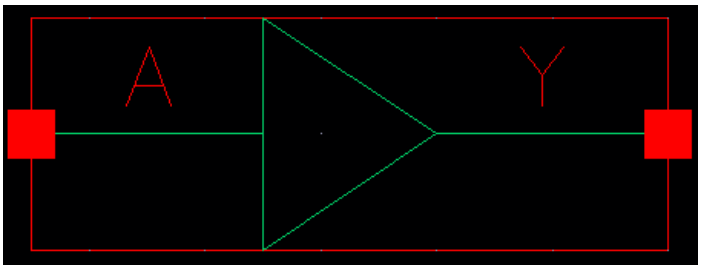

Figure 7: Symbol View for the buffer cell.

CMOS Schematic:

The following figures display the CMOS schematics for the BUF cells.

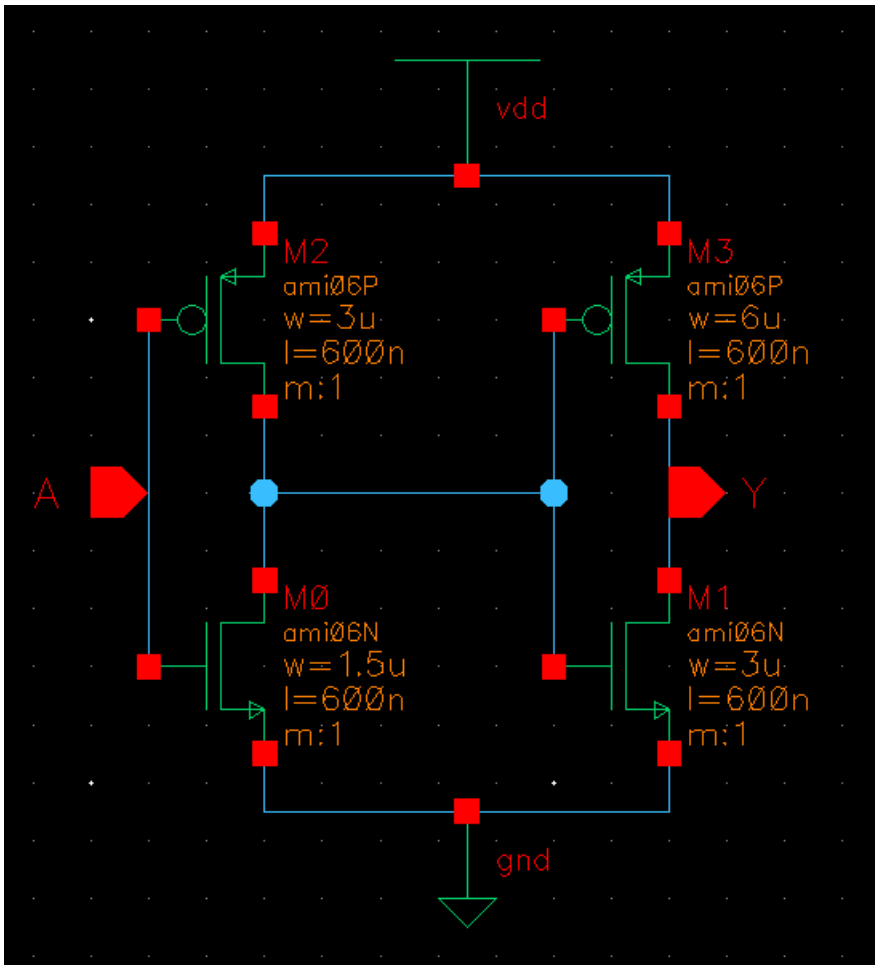

Figure 8: CMOS Schematic for the BUFX2 cell.

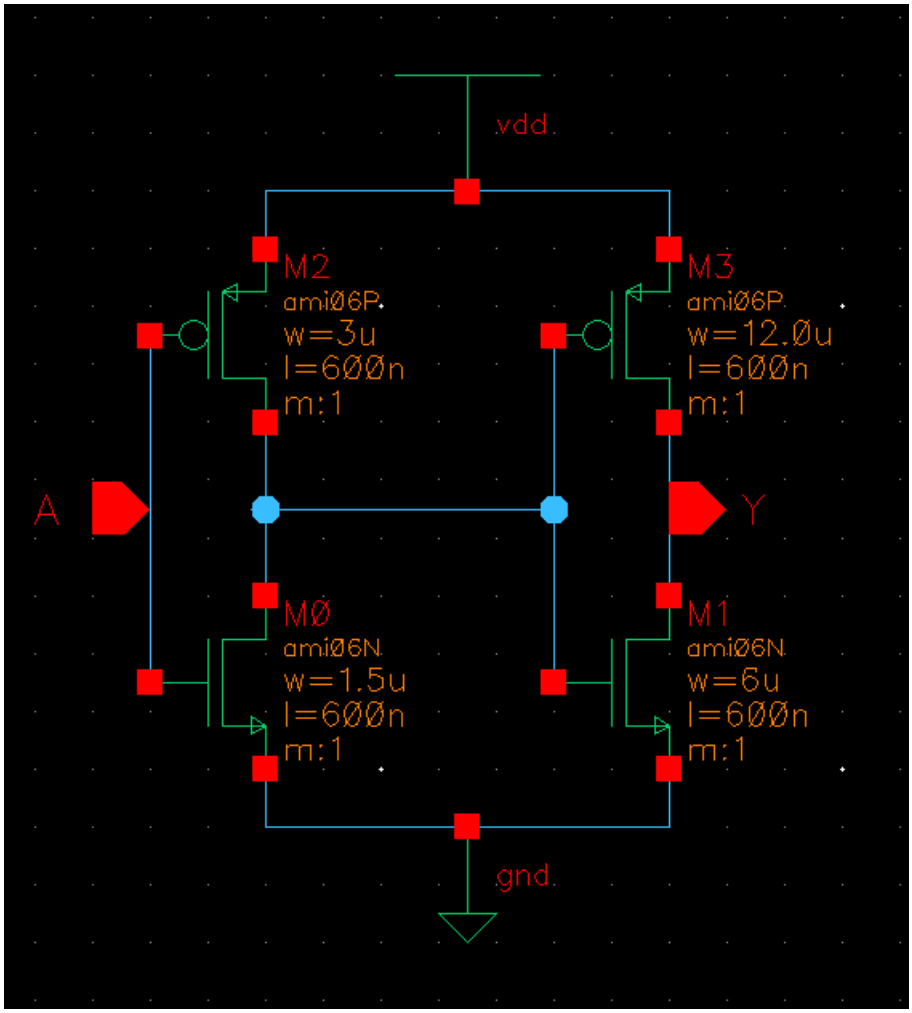

Figure 9: CMOS Schematic for the BUFX2 cell.

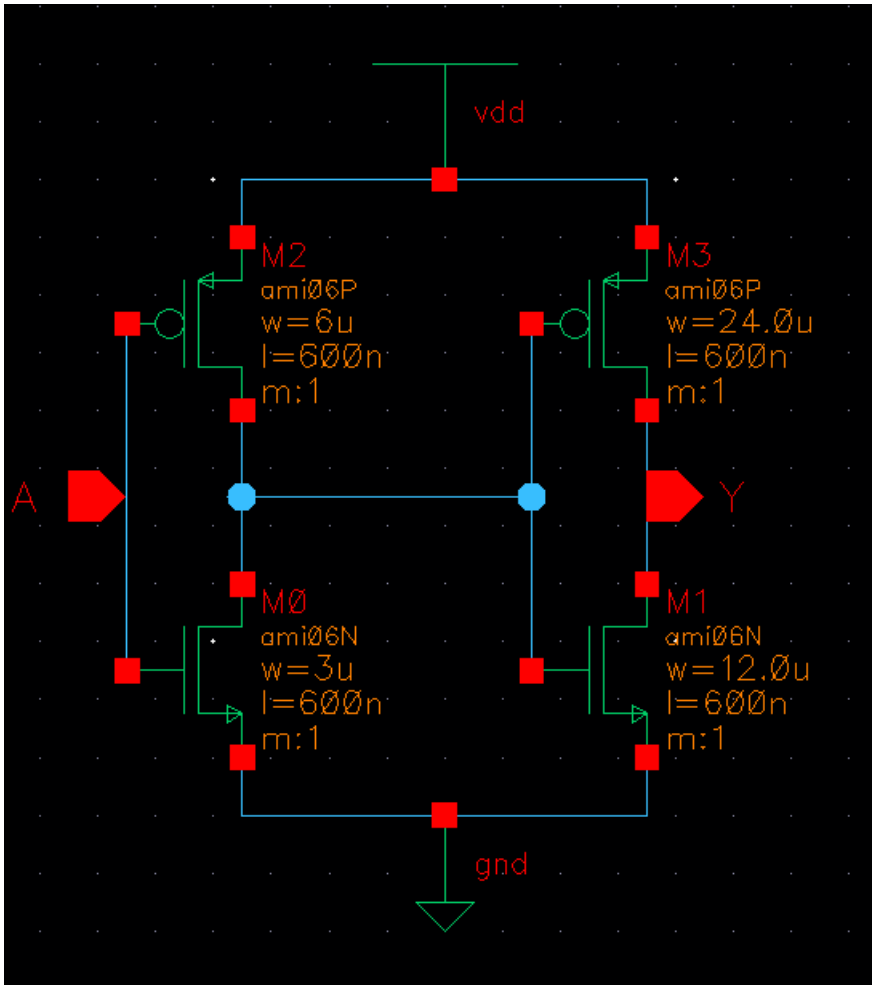

Figure 10: CMOS Schematic for the BUFX8 cell.

CMOS Layout:

The following figures display the CMOS layouts for the BUF cells.

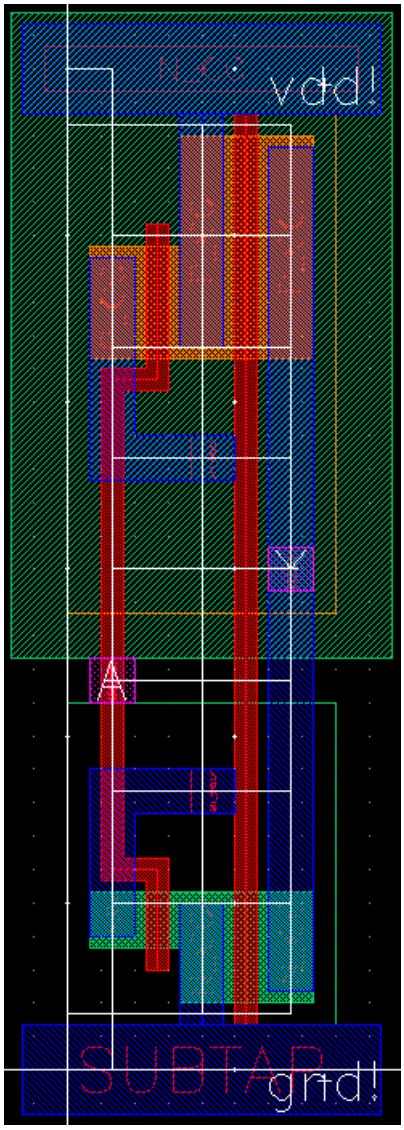

Figure 11: CMOS layout for the BUFX2 cell.

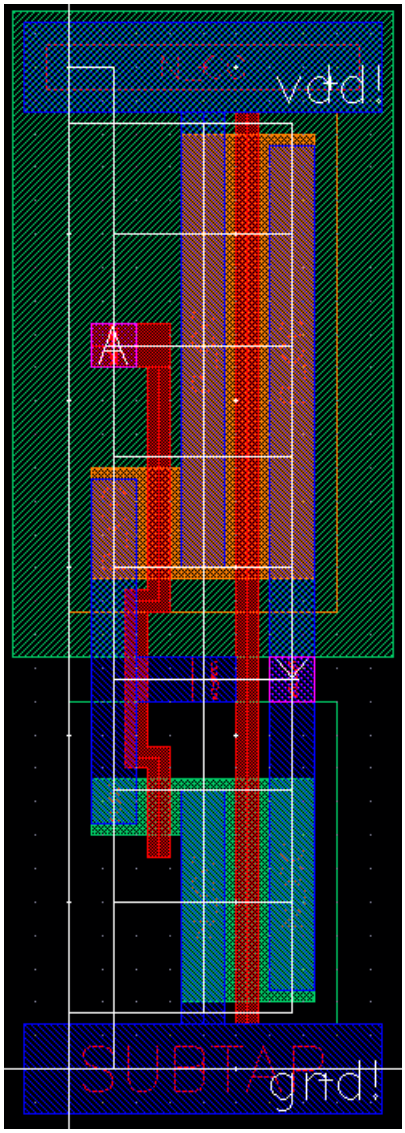

Figure 12: CMOS layout for the BUFX4 cell.

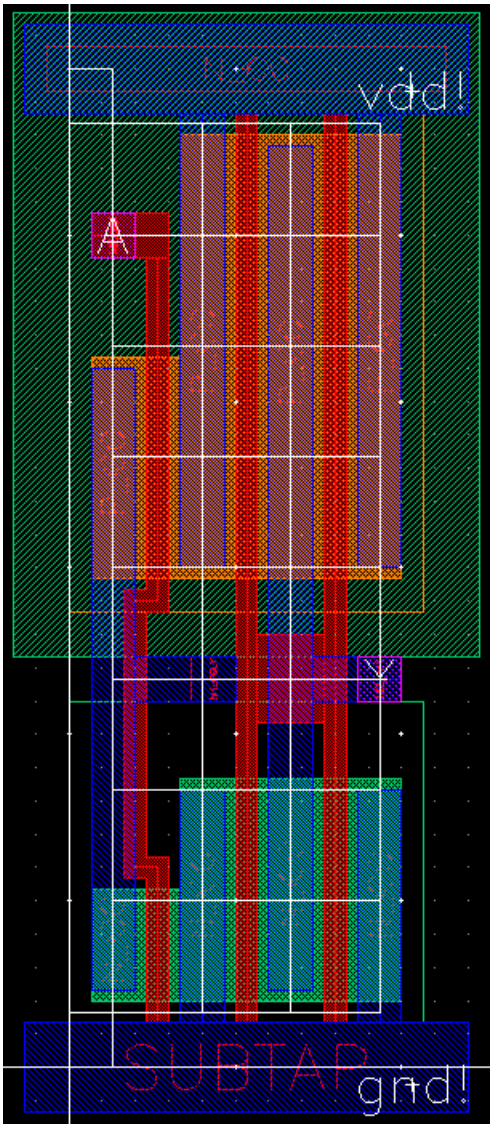

Figure 13: CMOS layout for the BUFX8 cell.

DFF

Cell Description:

This is a standard single-bit, positive-edge triggered flip-flop with an asynchronous, active low clear signal. The input signal to this cell is sampled on the rising edge of the clock signal, and both the sampled signal and its compliment are provided at the output of the cell.

Truth Table:

CLK	D	CLRBAR	Q	$\neg Q$
0	0	0	0	1
0	0	1	Q	$\neg Q$
0	1	0	0	1
0	1	1	Q	$\neg Q$
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

Behavioral Verilog:

```
//Verilog HDL for "Lib6710_06", "DFF" "behavioral"
module DFF ( Q, QB, CLRB, CLK, D );
 input CLRB;
 input CLK;
 input D;
 output reg Q;
 output QB;
 assign QB = ~Q;
 always@(posedge CLK or negedge CLRB)
 begin
        if(~CLRB)
                Q <= 1'b0;
        else
                Q <= D;
 end
 specify
        (D => Q) = (1.0, 1.0);
        (D => QB) = (1.0, 1.0);
        (CLK => Q) = (1.0, 1.0);
        (CLK => QB) = (1.0, 1.0);
        (CLRB => Q) = (1.0, 1.0);
        (CLRB => QB) = (1.0, 1.0);
 endspecify
```

endmodule

Cell Size:

Drive Strength	Height (µM)	Width (µM)
DFFX1	27.0	48

Performance:

Propagation Delay (Rising Outputs):

Drive Strength	Min. (nS)	Max. (nS)
DFFX1	0.675642	6.273002

Output Rise Time:

Drive Strength	Min. (nS)	Max. (nS)
DFFX1	0.211785	3.679774

Propagation Delay (Falling Outputs):

Drive Strength	Min. (nS)	Max. (nS)
DFFX1	1.704999	7.24334

Output Fall Time:

Drive Strength	Min. (nS)	Max. (nS)
DFFX1	0.260326	4.774839

Setup Time:

Drive Strength	Min. (nS)	Max. (nS)
DFFNEGCLKX1	0.09375	0.35625

Hold Time:

Drive Strength	Min. (nS)	Max. (nS)
DFFNEGCLKX1	0.09375	0.3375

Logic Symbol:

Figure 14: Symbol View for the DFF cell.

CMOS Schematic:

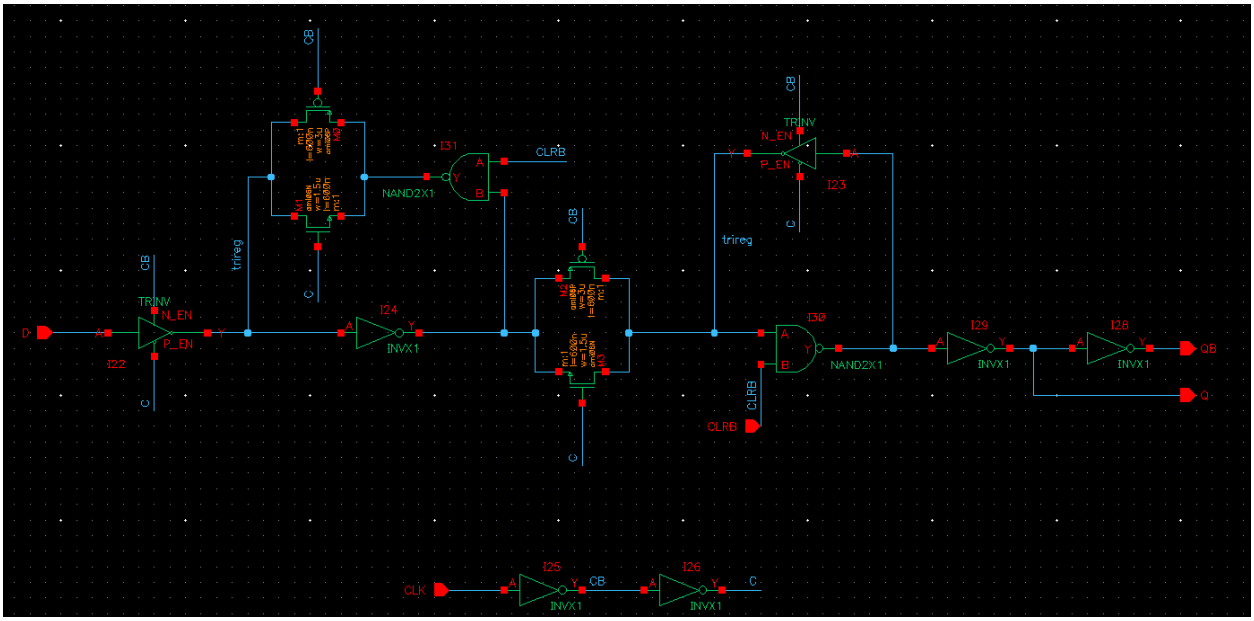

Figure 15: CMOS schematic for the DFFX1 Cell

CMOS Layout:

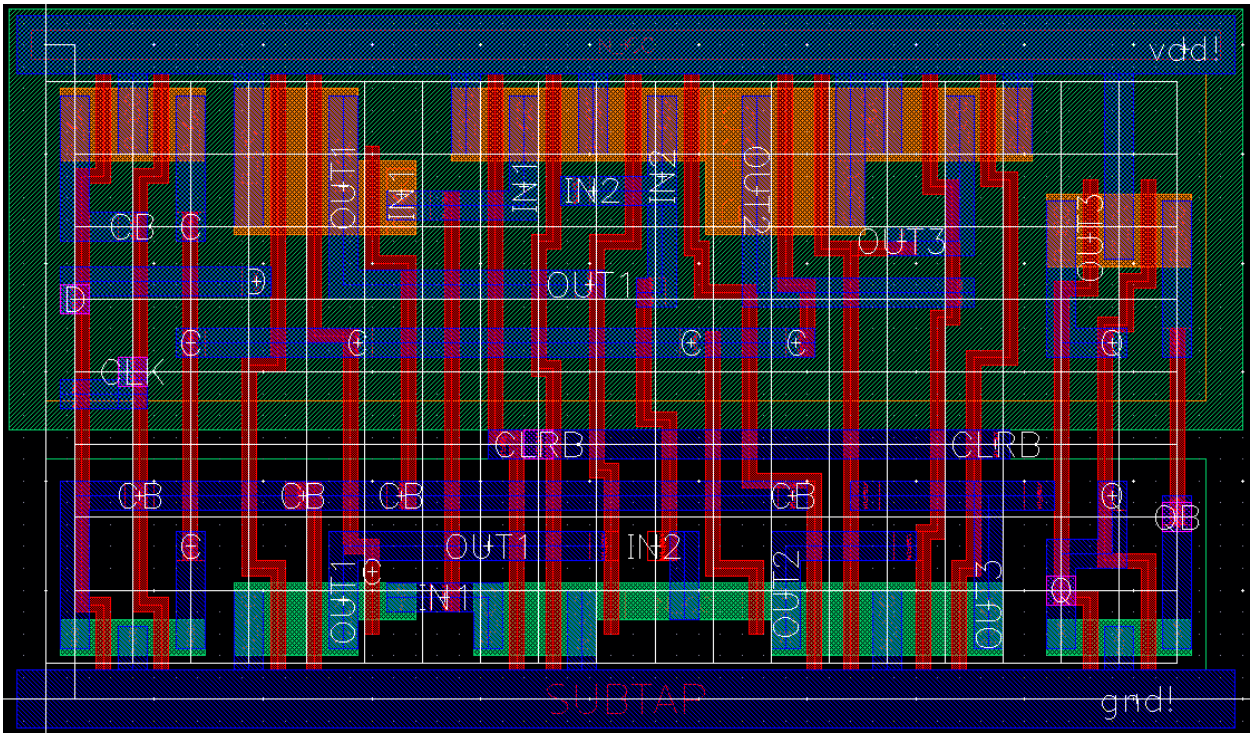

Figure 16: CMOS layout for the DFFX1 cell.

DFFNEGCLK

Cell Description:

This is a standard single-bit, negative-edge triggered flip-flop with an asynchronous, active low clear signal. The input signal to this cell is sampled on the falling edge of the clock signal, and both the sampled signal and its compliment are provided at the output of the cell.

Truth Table:

CLK	D	CLRBAR	Q	$\neg Q$
0	0	0	0	1
0	0	1	0	1
0	1	0	1	0
0	1	1	Q	$\neg Q$
1	0	0	0	1
1	0	1	Q	$\neg Q$
1	1	0	0	1
1	1	1	Q	$\neg Q$

Behavioral Verilog:

```
//Verilog HDL for "Lib6710_06", "DFFNEGCLK" "behavioral"
module DFFNEGCLK( Q, QB, CLRB, CLK, D );
 input CLRB;
 input CLK;
 input D;
 output reg Q;
 output QB;
 assign QB = ~Q;
 always@(negedge CLK or negedge CLRB)
 begin
        if(~CLRB)
                Q <= 1'b0;
        else
                Q <= D;
 end
 specify
        (D => Q) = (1.0, 1.0);
        (D => QB) = (1.0, 1.0);
        (CLK => Q) = (1.0, 1.0);
        (CLK => QB) = (1.0, 1.0);
        (CLRB => Q) = (1.0, 1.0);
        (CLRB => QB) = (1.0, 1.0);
 endspecify
```

endmodule

Cell Size:

Drive Strength	Height (µM)	Width (µM)
DFFNEGCLKX1	27.0	48

Performance:

Propagation Delay (Rising Outputs):

Drive Strength	Min. (nS)	Max. (nS)
DFFNEGCLKX1	0.675636	5.683413

Output Rise Time:

Drive Strength	Min. (nS)	Max. (nS)
DFFNEGCLKX1	0.211913	3.679757

Propagation Delay (Falling Outputs):

Drive Strength	Min. (nS)	Max. (nS)
DFFNEGCLKX1	0.691711	7.06816

Output Fall Time:

Drive Strength	Min. (nS)	Max. (nS)
DFFNEGCLKX1	0.260502	4.776157

Setup Time:

Drive Strength	Min. (nS)	Max. (nS)
DFFNEGCLKX1	0.01875	0.4125

Hold Time:

Drive Strength	Min. (nS)	Max. (nS)
DFFNEGCLKX1	0.01875	0.50625

Logic Symbol:

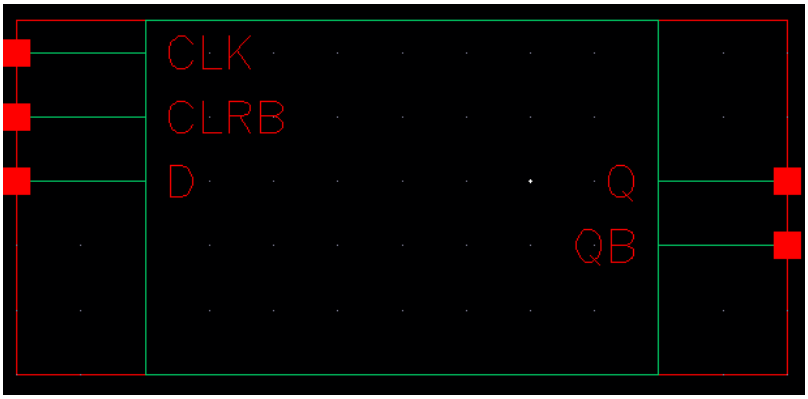

Figure 17: Symbol View for the DFFNEGCLK cell.

CMOS Schematic:

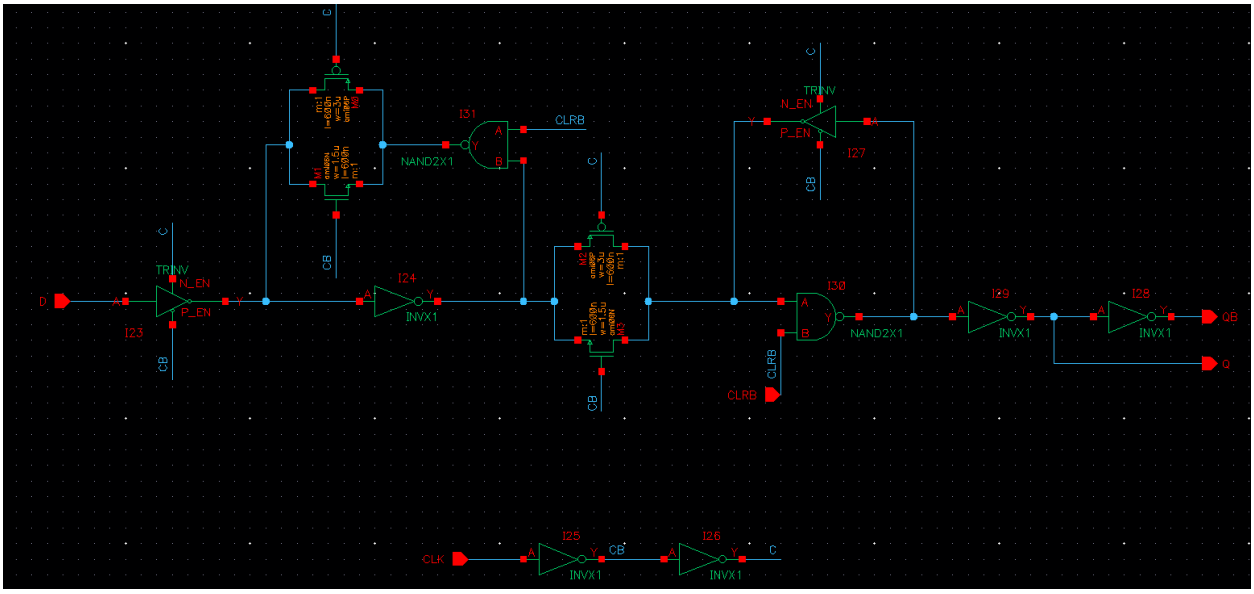

Figure 18: CMOS schematic for the DFFNEGCLKX1 Cell

CMOS Layout:

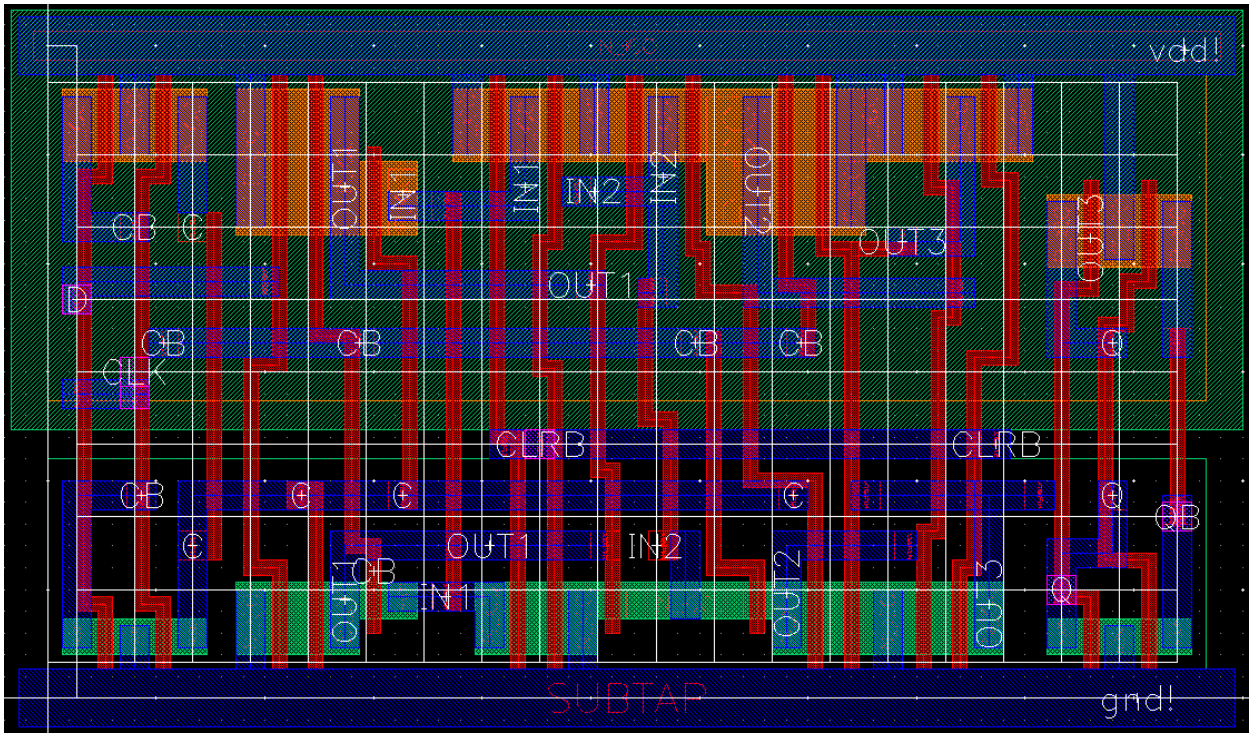

Figure 19: CMOS layout for the DFFNEGCLKX1 cell.

DFFQ

Cell Description:

This is a standard single-bit, positive-edge triggered flip-flop with an asynchronous, active low clear signal. The input signal to this cell is sampled on the rising edge of the clock signal, only the sampled signal is available at the output of the cell.

Truth Table:

CLK	D	CLRBAR	Q
0	0	0	0
0	0	1	Q
0	1	0	0
0	1	1	Q
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Behavioral Verilog:

```
//Verilog HDL for "Lib6710_06", "DFF" "behavioral"
module DFFQ( Q, CLRB, CLK, D );
 input CLRB;
 input CLK;
 input D;
 output reg Q;
 always@(posedge CLK or negedge CLRB)
 begin
        if(~CLRB)
                Q <= 1'b0;
        else
                Q <= D;
 end
 specify
        (D => Q) = (1.0, 1.0);
        (CLK => Q) = (1.0, 1.0);
        (CLRB => Q) = (1.0, 1.0);
 endspecify
endmodule
```

Cell Size:

Drive Strength	Height (µM)	Width (µM)
DFFQX1	27.0	45.6

Performance:

Propagation Delay (Rising Outputs):

Drive Strength	Min.	Max.
DFFQX1	1.149946	5.339675

Output Rise Time:

Drive Strength	Min.	Max.
DFFQX1	0.231738	3.619157

Propagation Delay (Falling Outputs):

Drive Strength	Min.	Max.
DFFQX1	0.599594	7.151095

Output Fall Time:

Drive Strength	Min.	Max.
DFFQX1	0.278052	4.701212

Setup Time:

Drive Strength	Min. (nS)	Max. (nS)
DFFNEGCLKX1	0.09375	0.35625

Hold Time:

Drive Strength	Min. (nS)	Max. (nS)
DFFNEGCLKX1	0.09375	0.3375

Logic Symbol:

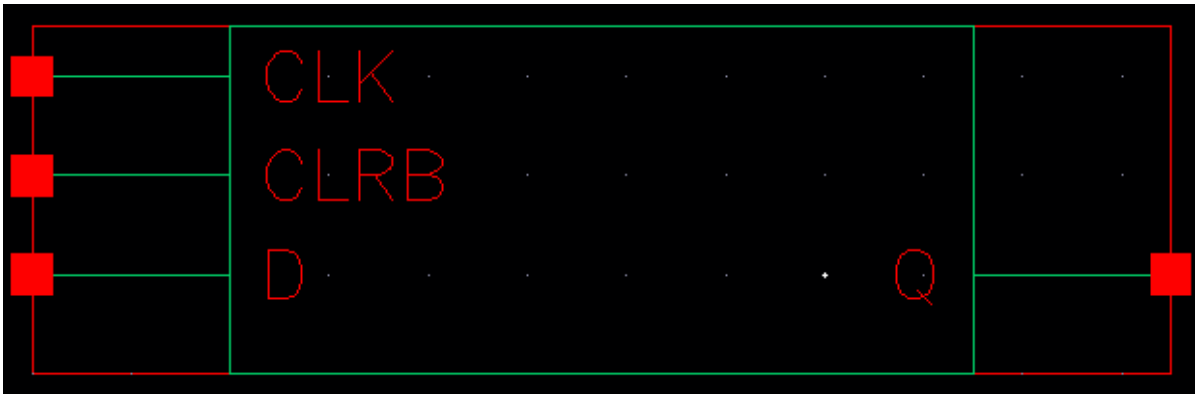

Figure 20: Symbol View for the DFFQ cell.

CMOS Schematic:

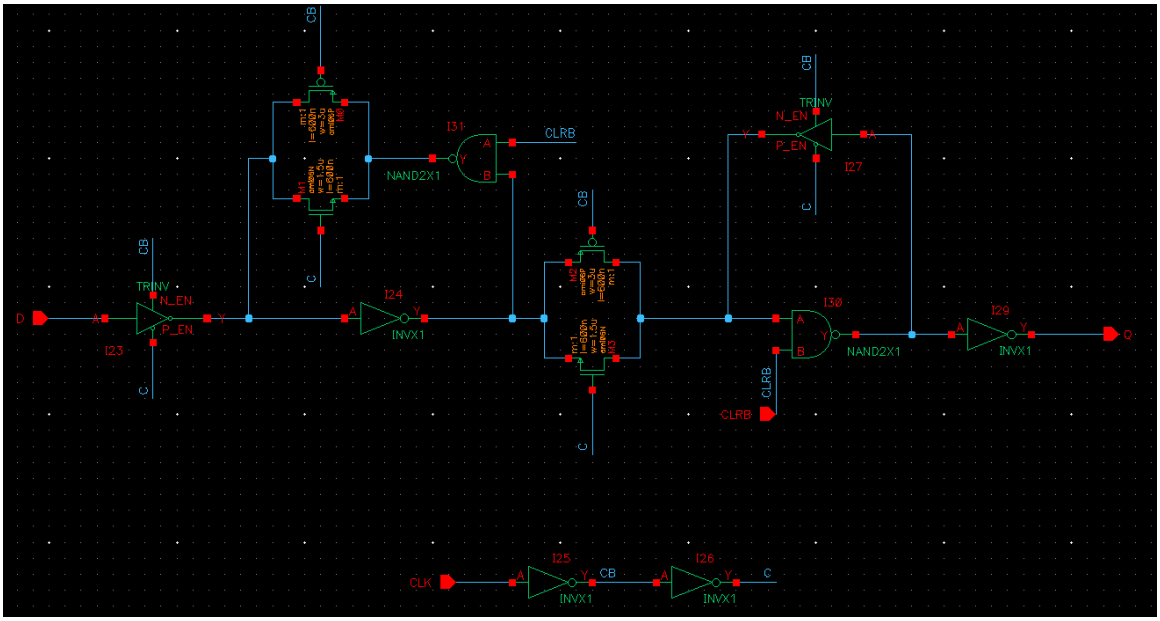

Figure 21: CMOS schematic for the DFFQX1 Cell

CMOS Layout:

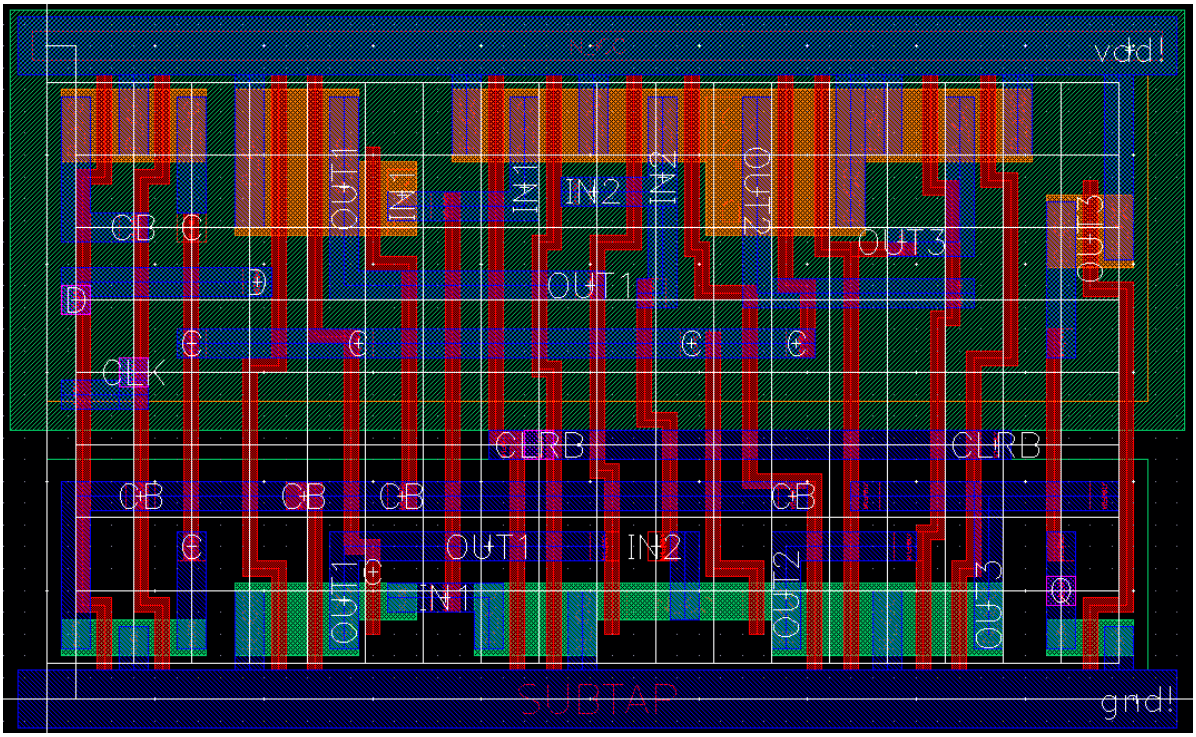

Figure 22: CMOS layout for the DFFQX1 cell.

DFFQB

Cell Description:

This is a standard single-bit, positive-edge triggered flip-flop with an asynchronous, active low clear signal. The input signal to this cell is sampled on the rising edge of the clock signal, only the compliment of the sampled signal is available at the output of the cell.

Truth Table:

CLK	D	CLRBAR	$\neg Q$
0	0	0	0
0	0	1	$\neg Q$
0	1	0	0
0	1	1	$\neg Q$
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

Behavioral Verilog:

```
//Verilog HDL for "Lib6710_06", "DFF" "behavioral"
module DFFQB( QB, CLRB, CLK, D );
 input CLRB;
 input CLK;
 input D;
 output reg QB;
 always@(posedge CLK or negedge CLRB)
 begin
        if(~CLRB) //Active low clear
                QB <= 1'b1;
        else
                QB <= ~D;
 end
 specify
        (D => QB) = (1.0, 1.0);
        (CLK => QB) = (1.0, 1.0);
        (CLRB => QB) = (1.0, 1.0);
 endspecify
endmodule
```

Cell Size:

Drive Strength	Height (µM)	Width (µM)
DFFQBX1	27.0	48

Performance:

Propagation Delay (Rising Outputs):

Drive Strength	Min.	Max.
DFFQX1	0.675642	5.858591

Output Rise Time:

Drive Strength	Min.	Max.
DFFQX1	0.211785	3.62198

Propagation Delay (Falling Outputs):

Drive Strength	Min.	Max.
DFFQX1	1.351753	6.912037

Output Fall Time:

Drive Strength	Min.	Max.
DFFQX1	0.260326	4.699816

Setup Time:

Drive Strength	Min. (nS)	Max. (nS)
DFFNEGCLKX1	0.09375	0.35625

Hold Time:

Drive Strength	Min. (nS)	Max. (nS)
DFFNEGCLKX1	0.09375	0.3375

Logic Symbol:

Figure 23: Symbol View for the DFFQB cell.

CMOS Schematic:

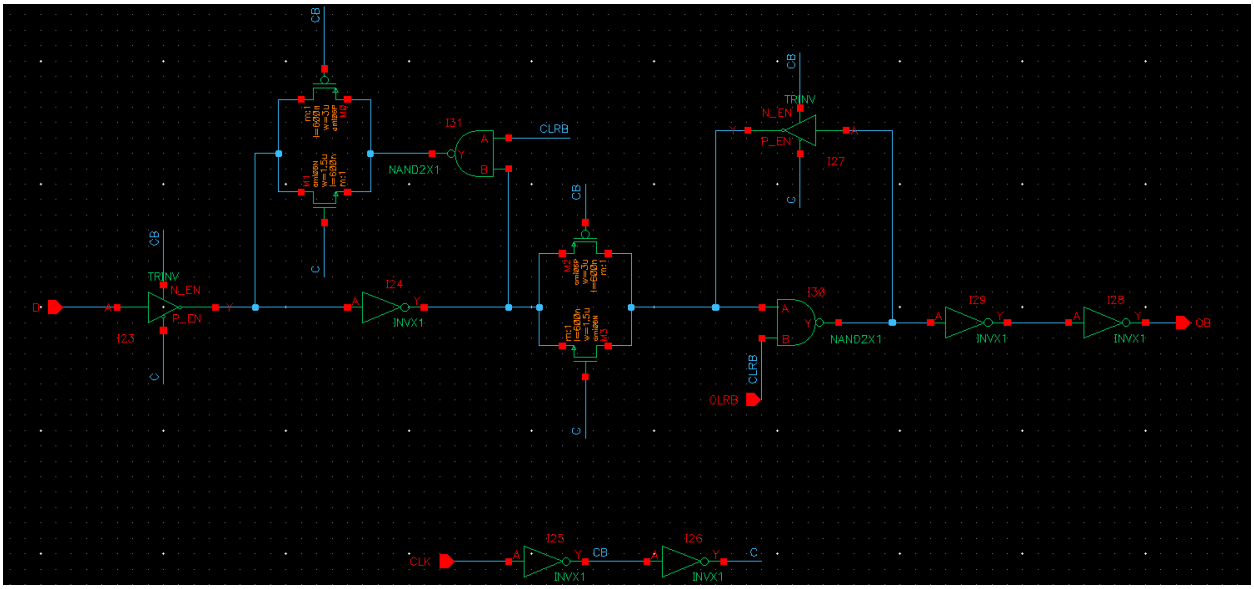

Figure 24: CMOS schematic for the DFFQBX1 Cell

CMOS Layout:

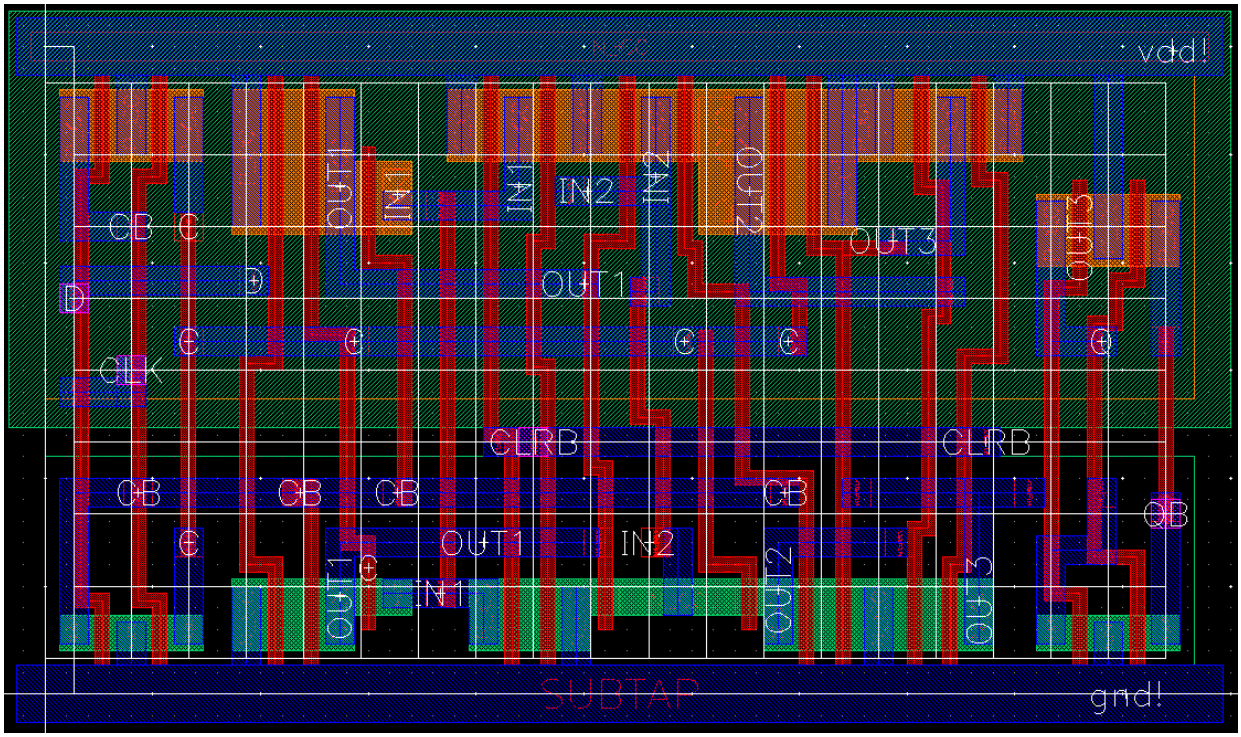

Figure 25: CMOS layout for the DFFQBX1 cell.

FA

Cell Description:

This is a standard full adder (FA) cell. This cell has 3 inputs A, B, and Cin, along with two outputs Sum and Cout. The function of this cell adds the two operands (A, and B) together along with the Cin which is the carry-in value from the previous stage of the adder. Once added together, the cell produces a Sum value, and a Cout (carry out) value if necessary.

Truth Table:

Cin	A	B	Sum	$Cout$
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Behavioral Verilog:

Cell Size:

Drive Strength	Height (µM)	Width (µM)
FAX1	27.0	40.8
FAX2	27.0	40.8

Performance:

Propagation Delay (Rising Outputs):

Drive Strength	Min. (nS)	Max. (nS)
FAX1	0.545184	4.956384
FAX2	0.547069	4.692737

Output Rise Time:

Drive Strength	Min. (nS)	Max. (nS)
FAX1	0.236312	3.636292
FAX2	0.217119	5.140482

Propagation Delay (Falling Outputs):

Drive Strength	Min. (nS)	Max. (nS)
FAX1	0.661016	6.331661
FAX2	0.590398	5.12905

Output Fall Time:

Drive Strength	Min. (nS)	Max. (nS)
FAX1	0.293497	4.717055
FAX2	0.231074	3.558365

Logic Symbol:

The following figure displays the symbol for the full adder. The symbol is the same for both available drive strengths.

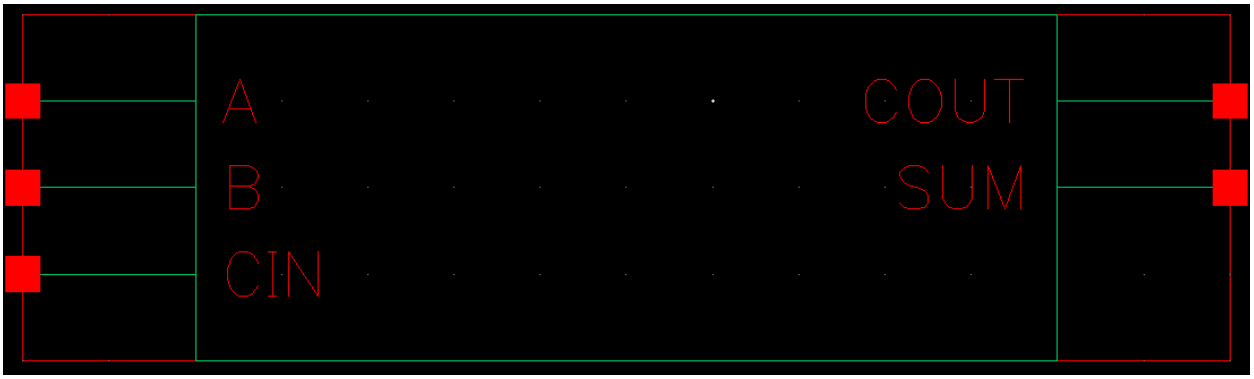

Figure 26: Symbol View for the FA cell.

CMOS Schematic:

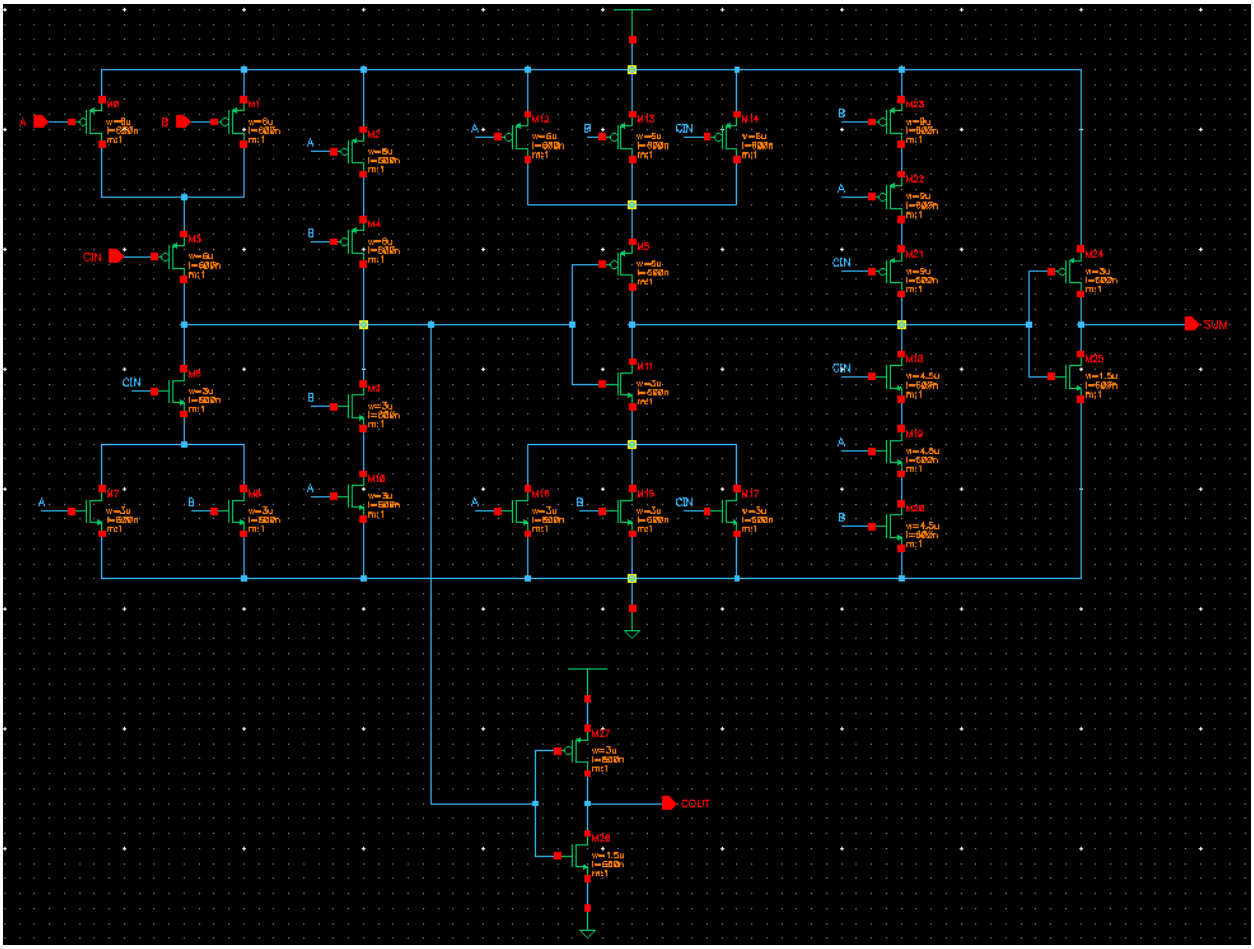

Figure 27: CMOS schematic view for the FAX1 cell.

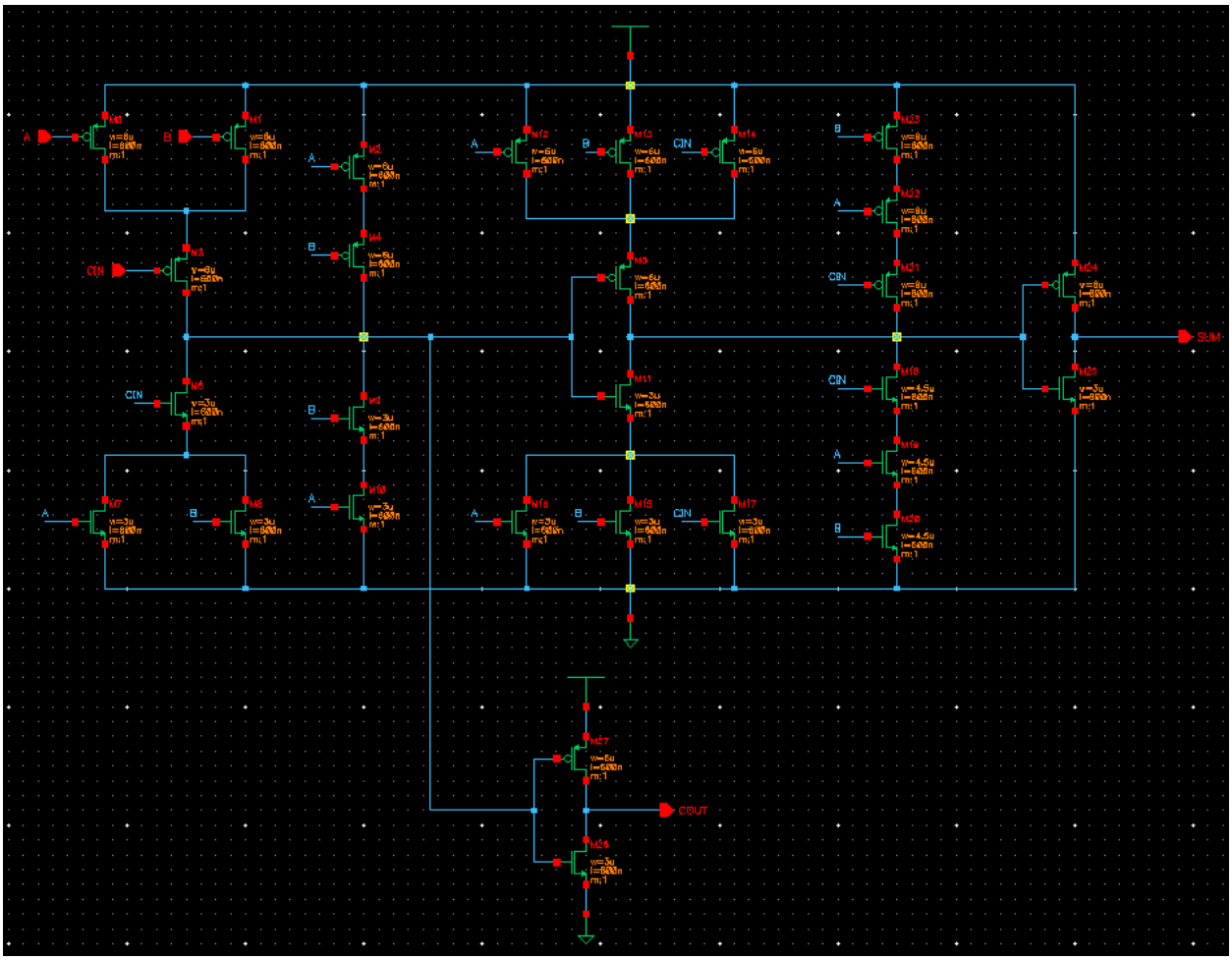

Figure 28: CMOS schematic view for the FAX2 cell.

CMOS Layout:

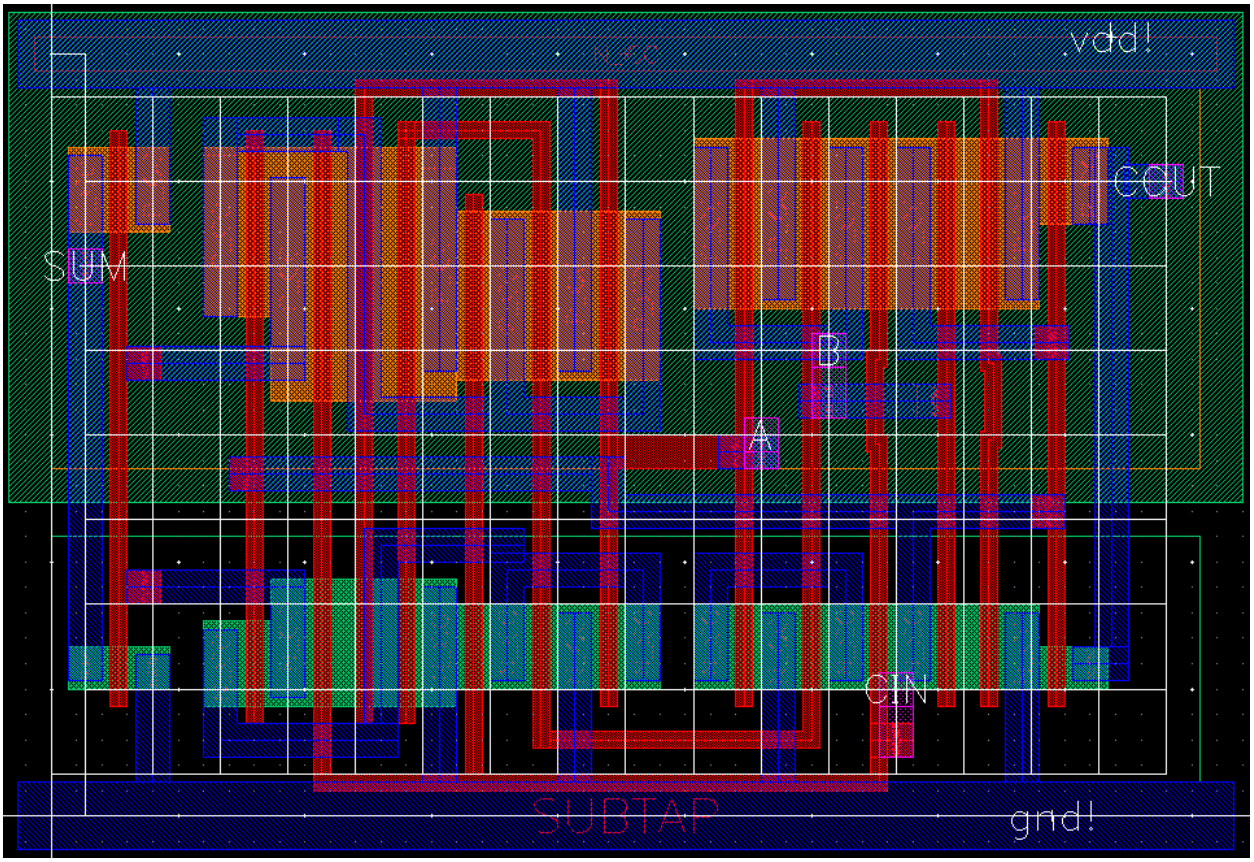

Figure 29: CMOS layout view for the FAX1 cell.

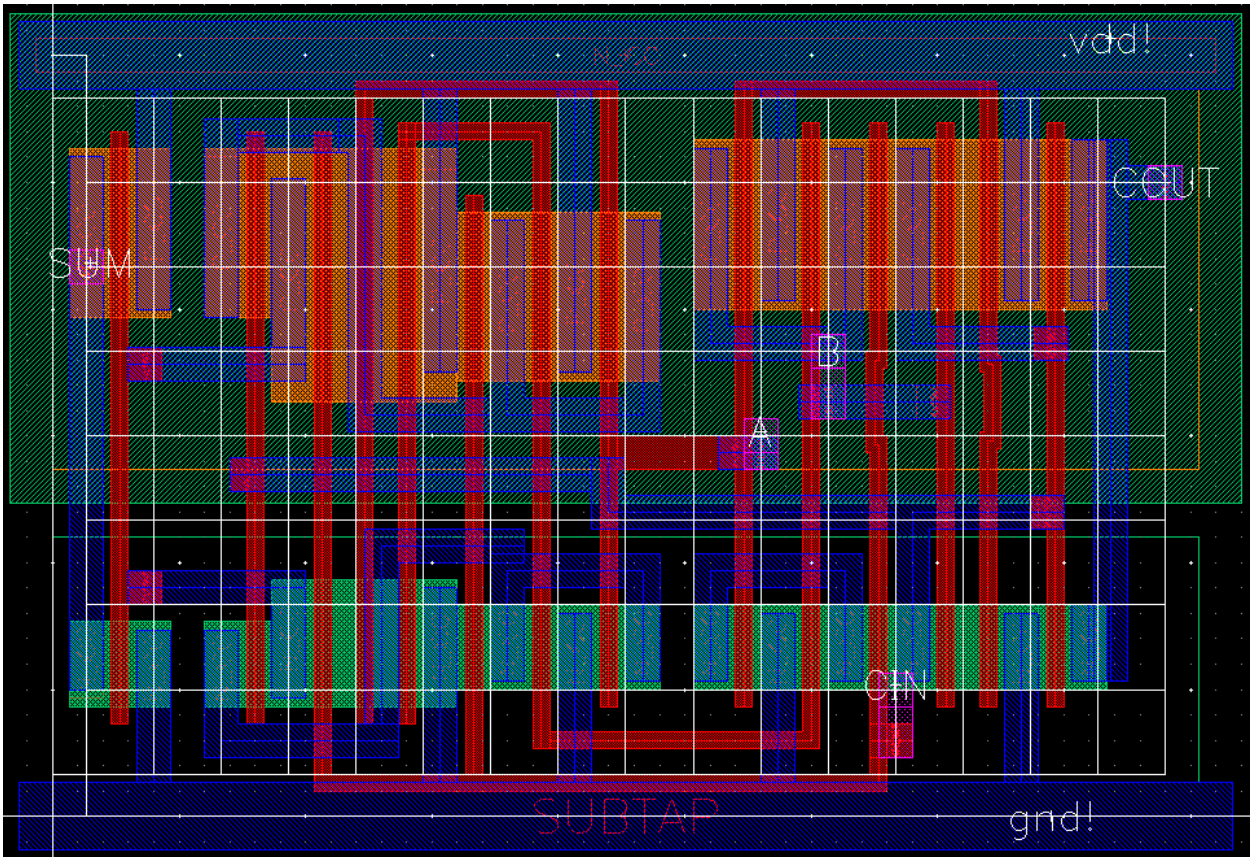

Figure 30: CMOS layout view for the FAX2 cell.

FIL

Cell Description:

This is a standard FILLler (FILLL) cell. The purpose of this cell is to allow the place and router to fill spaces between cells with a blank cell. This is used to ensure that the nwell regions implanted in the substrate are continuous for each row of cells.

Cell Size:

Drive Strength	Height (µM)	Width (µM)
FILL1	27.0	2.4
FILL2	27.0	4.8
FILL3	27.0	7.2
FILL4	27.0	9.6
FILL8	27.0	19.2

CMOS Layout:

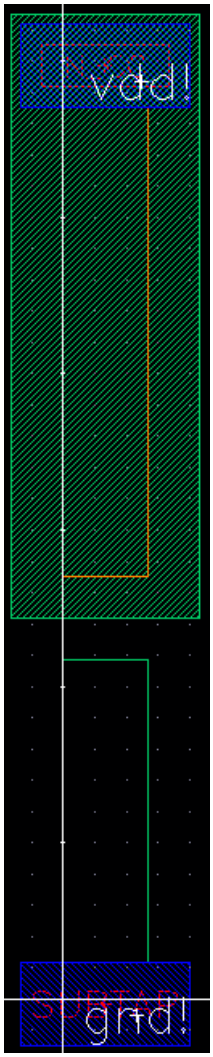

Figure 31: CMOS layout view for the FILL1 cell.

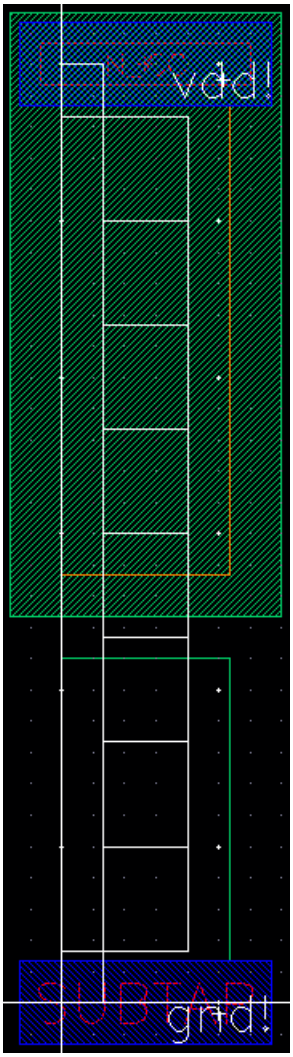

Figure 32: CMOS layout view for the FILL2 cell.

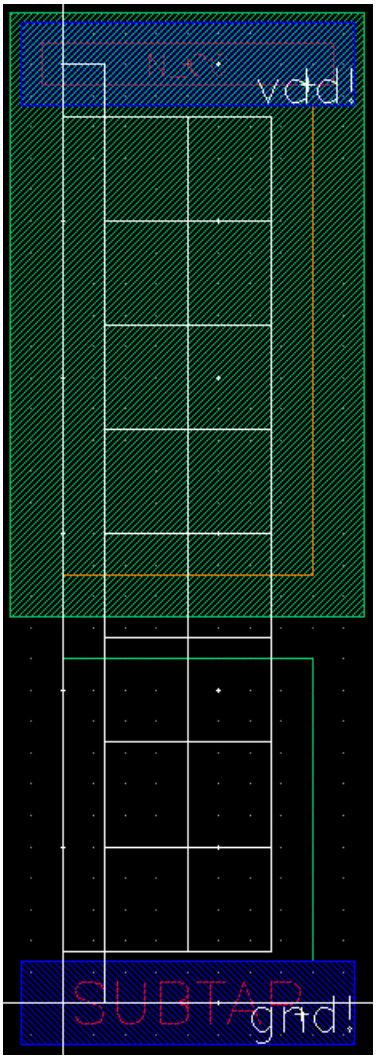

Figure 33: CMOS layout view for the FILL3 cell.

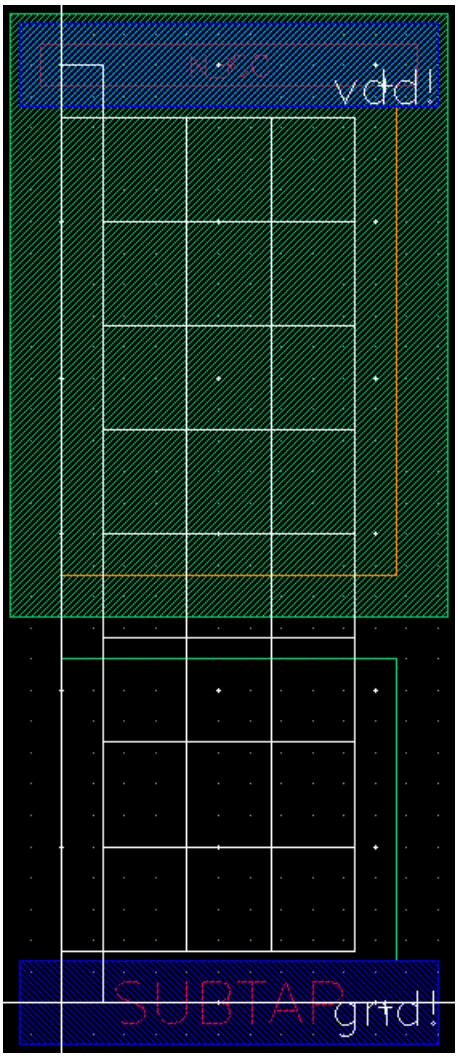

Figure 34: CMOS layout view for the FILL4 cell.

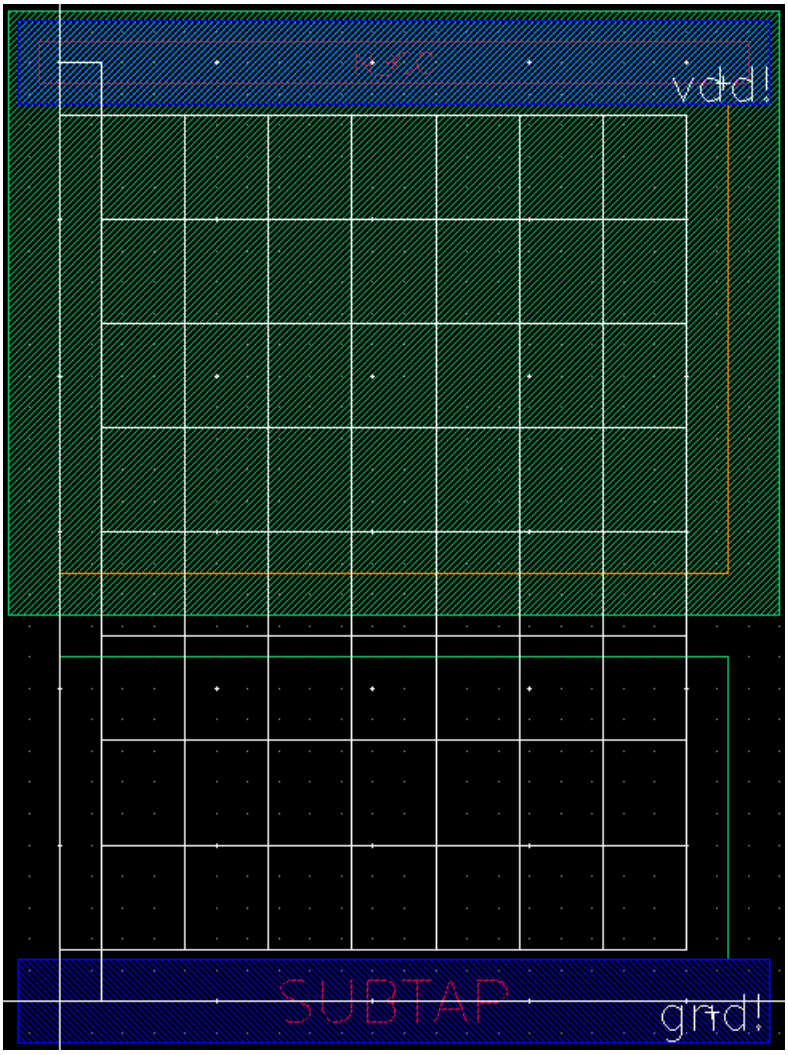

Figure 35: CMOS layout view for the FILL8 cell.

INV

Cell Description:
This is a standard inverter cell with the following Boolean equation.

$$Y = \neg A$$

Truth Table:

A	Y
0	1
1	0

Behavioral Verilog:
The behavioral Verilog for the inverter is independent of its drive strength. Replace the N in the module name with the respective drive strength (i.e. 1, 2, 4, and 8).

```
//Verilog HDL for "Lib6710_06", "INVXN" "behavioral"
module INVXN ( Y, A );
  output Y;
   input  A;
   not _i0(Y, A);
   specify
     (A => Y) = (1.0, 1.0);
   endspecify
endmodule
```

Cell Size:

Drive Strength	Height (µM)	Width (µM)
INVX1	27.0	4.8
INVX2	27.0	4.8
INVX4	27.0	4.8
INVX8	27.0	7.2

Performance:

Propagation Delay (Rising Outputs):

Drive Strength	Min. (nS)	Max. (nS)
INVX1	0.261011	4.441372
INVX2	0.225636	4.087162
INVX4	0.20974	3.927988
INVX8	0.19849	3.917132

Output Rise Time:

Drive Strength	Min. (nS)	Max. (nS)
INVX1	0.208141	3.634253
INVX2	0.173378	3.283945
INVX4	0.157781	3.127143
INVX8	0.14623	3.115807

Propagation Delay (Falling Outputs):

Drive Strength	Min. (nS)	Max. (nS)
INVX1	0.353699	5.887184
INVX2	0.257917	4.566921
INVX4	0.223438	4.095382
INVX8	0.210379	4.073315

Output Fall Time:

Drive Strength	Min. (nS)	Max. (nS)
INVX1	0.267747	4.725145
INVX2	0.185996	3.561277
INVX4	0.156828	3.151193
INVX8	0.145615	3.129725

Logic Symbol

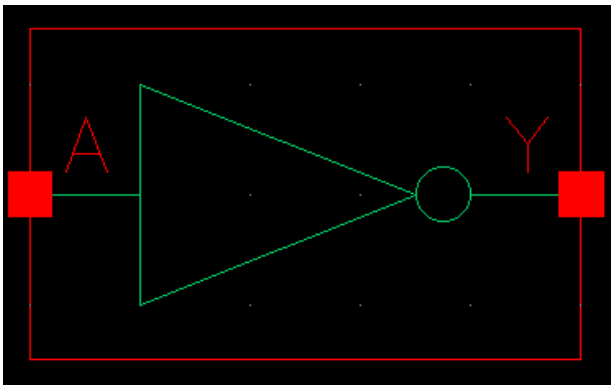

Figure 36: Symbol View for the inverter cell.

CMOS Schematic

The following figure displays the CMOS schematic for the invert cell with a 1 times drive strength

(INVX1), all drive strengths have the same schematic with transistor widths that scale by the drive strength factor (i.e. the width of the PMOS in the INVX2 is 6.0µM and the NMOS width is 3.0µM) .

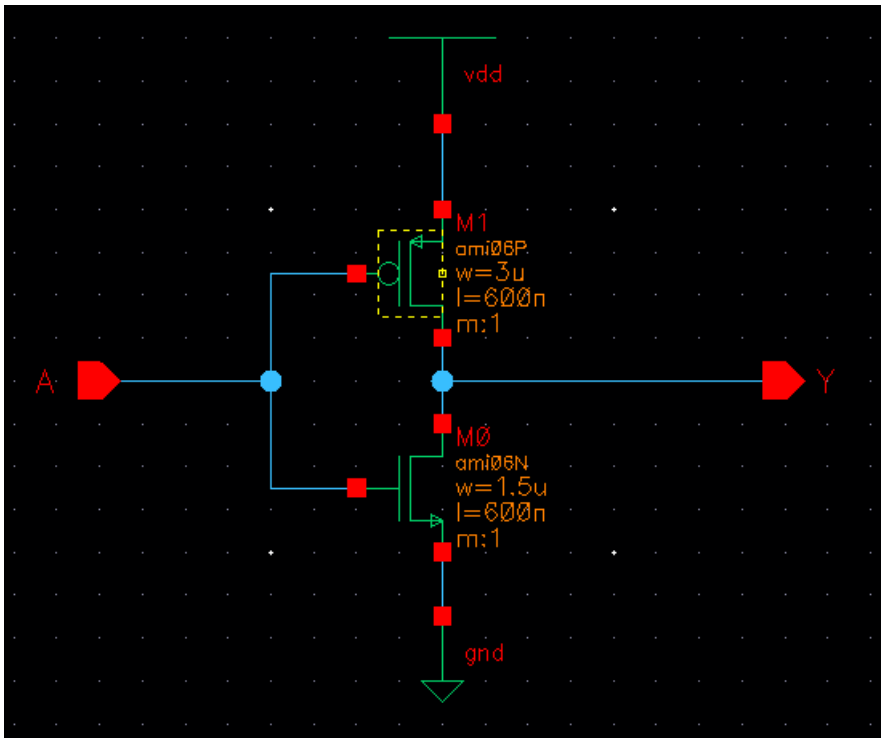

Figure 37: CMOS Schematic for the INVX1 cell.

CMOS Layout:

The following figures display the CMOS layouts for the INV cells.

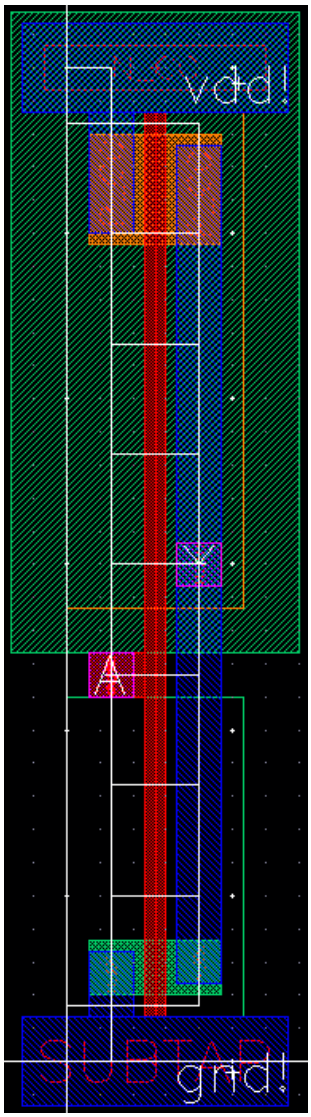

Figure 38: CMOS layout for the INVX1 cell.

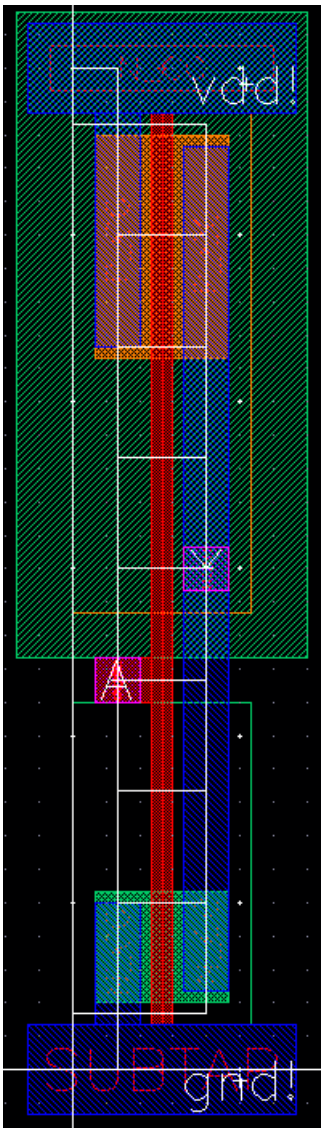

Figure 39: CMOS layout for the INVX2 cell.

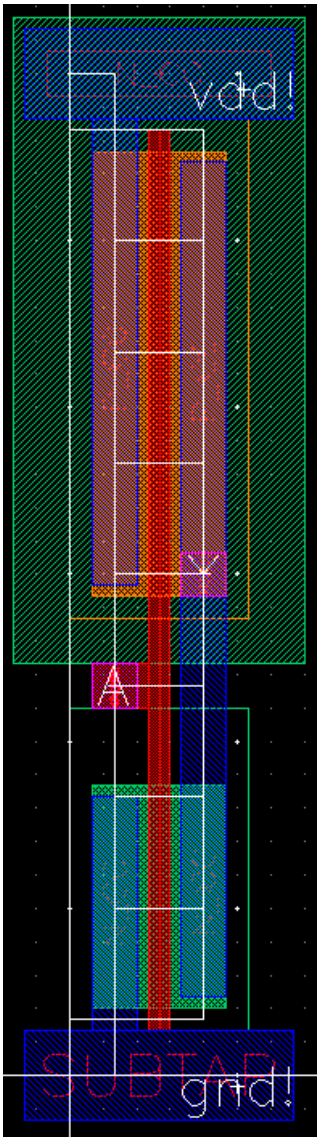

Figure 40: CMOS layout for the INVX4 cell.

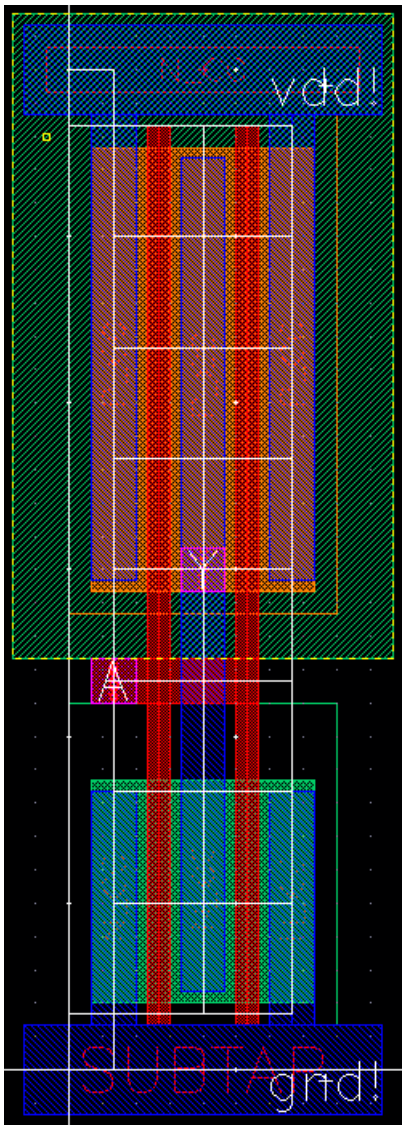

Figure 41:CMOS layout for the INVX8 cell.

MUXINV

Cell Description:
This is a standard 2 input multiplexor with an inverted output cell described by the following Boolean equation.

$$\boldsymbol{Y} = (\neg \boldsymbol{A} \wedge \neg \boldsymbol{S}) \vee (\neg \boldsymbol{B} \wedge \boldsymbol{S})$$

Truth Table:

S	A	B	Y
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Behavioral Verilog:

```
//Verilog HDL for "Lib6710_06", "MUXINV2x1" "behavioral"
module MUXINV2X1( Y, A, B, S );
 input A;
 input S;
 output Y;
 input B;
 assign Y = ~((~S&A) | (S&B));
 specify
 (A => Y) = (1.0, 1.0);
 (B => Y) = (1.0, 1.0);
 (S => Y) = (1.0, 1.0);
 endspecify
endmodule
```

Cell Size:

Drive Strength	Height (µM)	Width (µM)
MUXINV2X1	27.0	14.4

Performance:

Propagation Delay (Rising Outputs):

Drive Strength	Min. (nS)	Max. (nS)
MUXINV2X1	0.331604	4.139029

Output Rise Time:

Drive Strength	Min. (nS)	Max. (nS)
MUXINV2X1	0.262615	3.2300027

Propagation Delay (Falling Outputs):

Drive Strength	Min. (nS)	Max. (nS)
MUXINV2X1	0.33067	3.905376

Output Fall Time:

Drive Strength	Min. (nS)	Max. (nS)
MUXINV2X1	0.248249	3.015543

Logic Symbol:

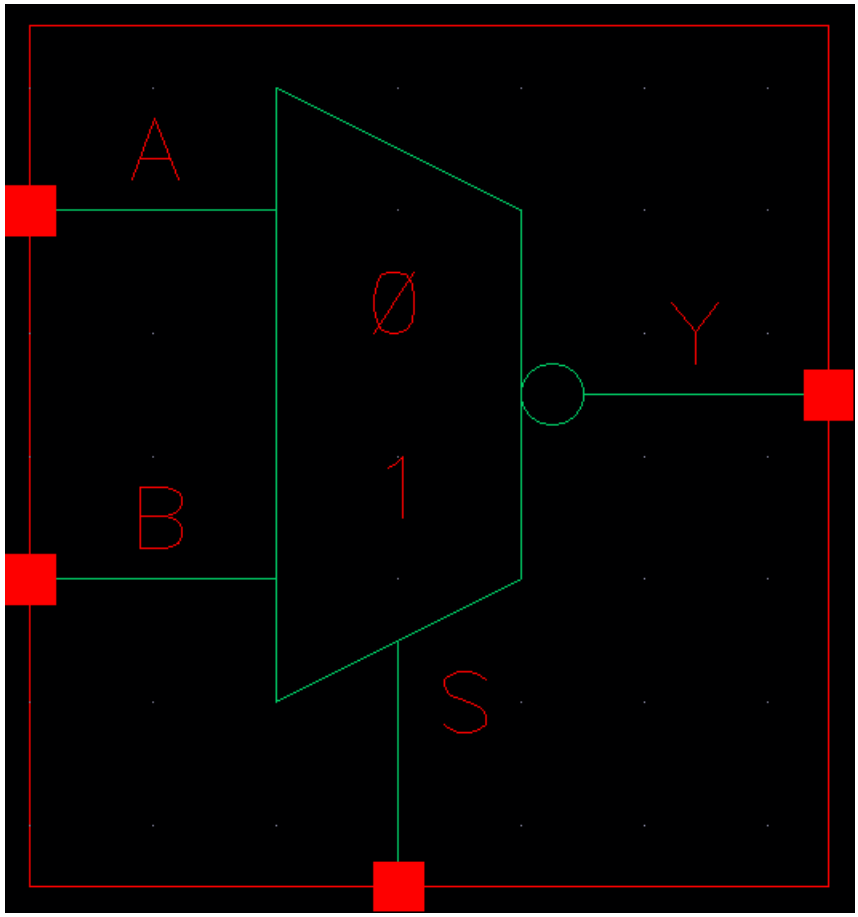

Figure 42: Symbol View for the MUXINV cell.

CMOS Schematic:

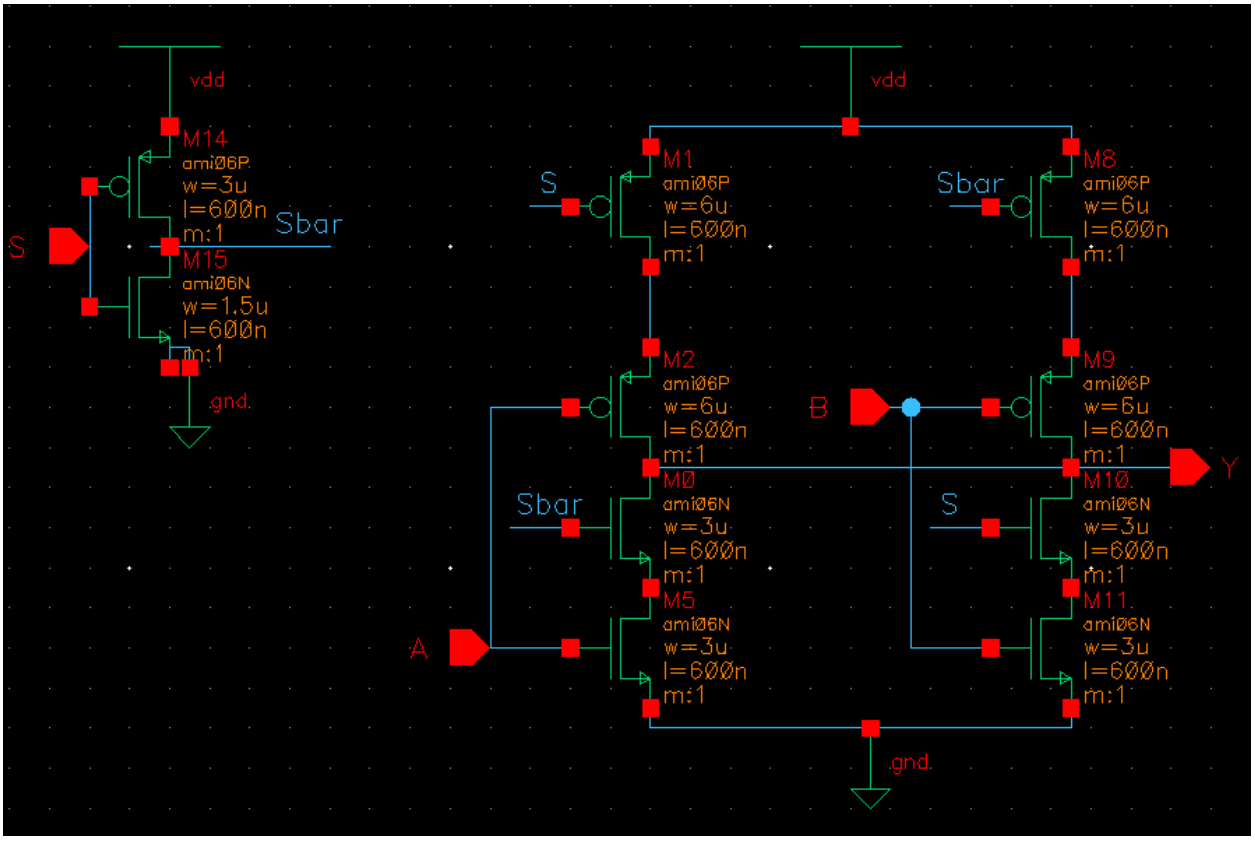

Figure 43: CMOS Schematic for the MUXINV2X1 cell.

CMOS Layout:

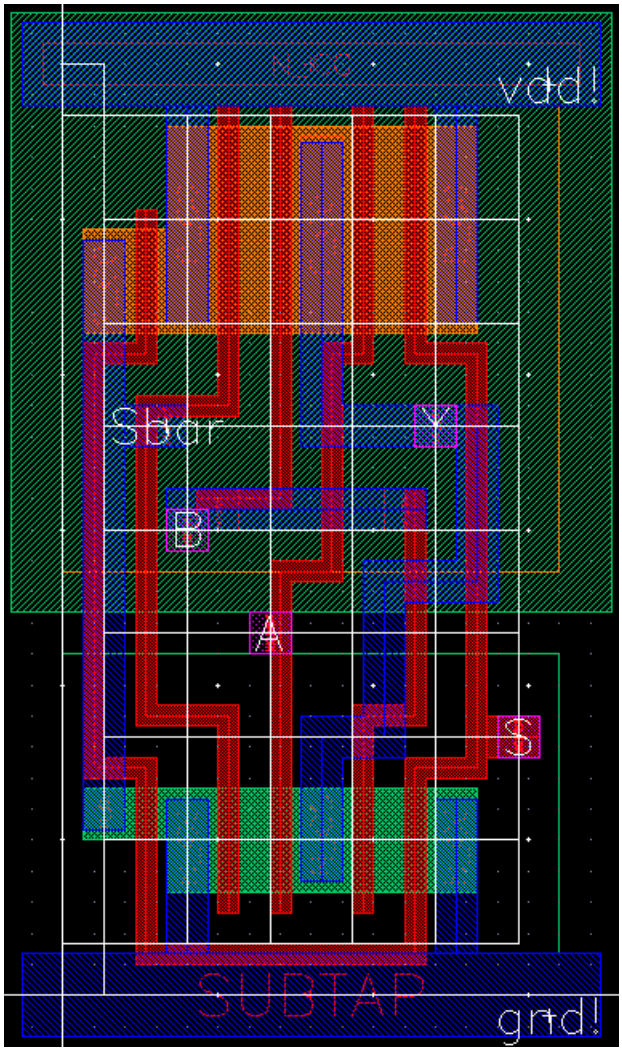

Figure 44: CMOS layout for the MUXINV2X1 cell.

NAND

Cell Description:
This is a standard NAND cell with the following Boolean equation.

$$Y = \neg(A \wedge B)$$

Truth Table:

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Behavioral Verilog:
The behavioral Verilog for the NAND is independent of its drive strength. Replace the N in the module name with the respective drive strength (i.e. 1, 2).

```
//Verilog HDL for "Lib6710_06", "NAND2X1" "behavioral"
module NAND2X1 ( Y, A, B );
  output Y;
  input  A;
  input  B;
  nand _i0(Y, A, B);
  specify
    (A => Y) = (1.0, 1.0);
    (B => Y) = (1.0, 1.0);
  endspecify
endmodule
```

Cell Size:

Drive Strength	Height (µM)	Width (µM)
NAND2X1	27.0	7.2
NAND2X2	27.0	7.2

Performance:

Propagation Delay (Rising Outputs):

Drive Strength	Min. (nS)	Max. (nS)
NAND2X1	0.287135	4.512479
NAND2X2	0.24711	4.144368

Output Rise Time:

Drive Strength	Min. (nS)	Max. (nS)
NAND2X1	0.221013	3.676704
NAND2X2	0.18531	3.321374

Propagation Delay (Falling Outputs):

Drive Strength	Min. (nS)	Max. (nS)
NAND2X1	0.239633	3.695076
NAND2X2	0.200718	3.297926

Output Fall Time:

Drive Strength	Min. (nS)	Max. (nS)
NAND2X1	0.182966	2.933345
NAND2X2	0.148219	2.57788

Logic Symbol:

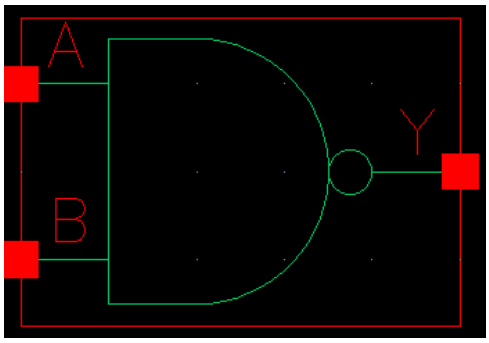

Figure 45: Symbol View for the NAND cell.

CMOS Schematic:

The following figure displays the CMOS schematic for the NAND cell with a 1 times drive strength (NAND2X1), all drive strengths have the same schematic with transistor widths that scale by the drive strength factor (i.e. the width of the PMOS in the NAND2X2 is 6.0µM and the NMOS width is 6.0µM) .

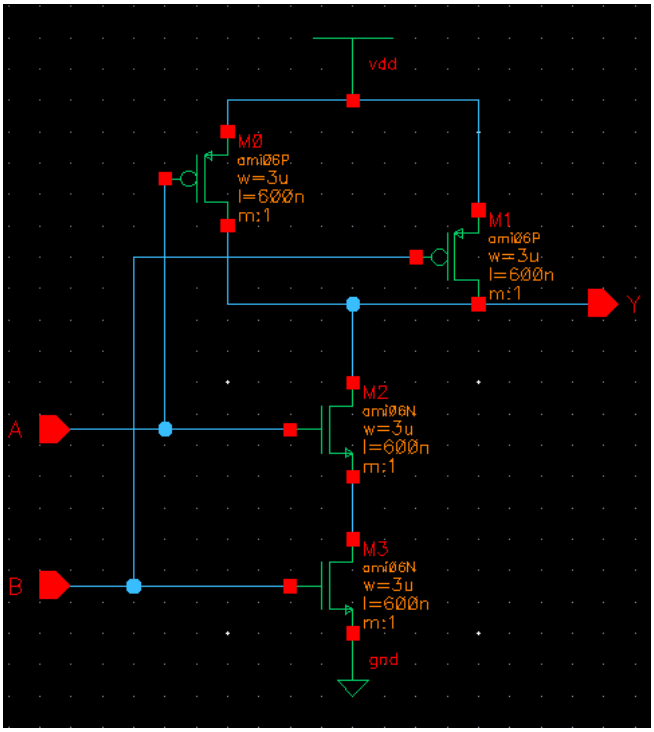

Figure 46: CMOS Schematic for the NAND2X1 cell.

CMOS Layout:

The following figures display the CMOS layouts for the NAND cells.

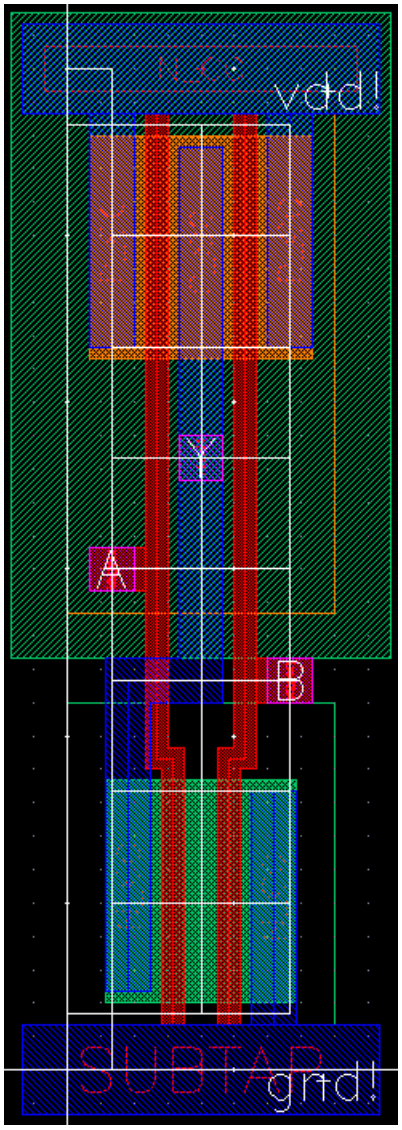

Figure 47: CMOS layout for the NAND2X1 cell.

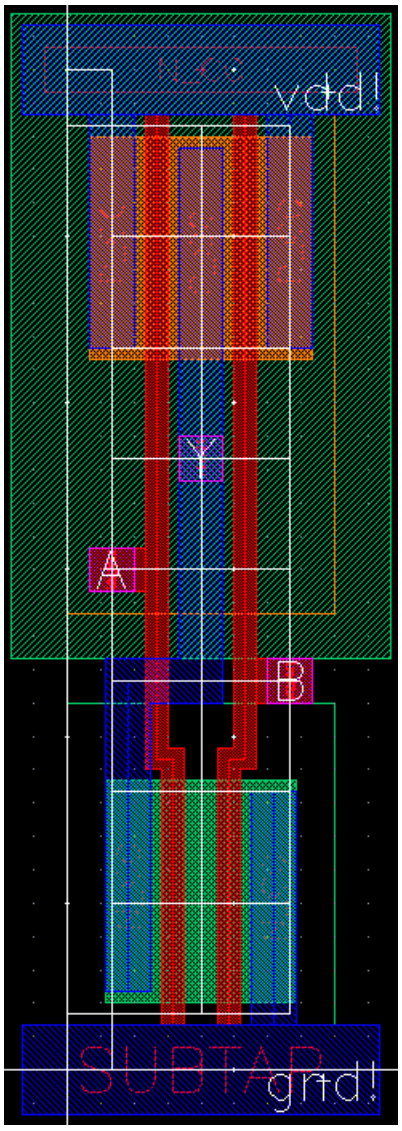

Figure 48: CMOS layout for the NAND2X2 cell.

NOR

Cell Description:

This is a standard NOR cell with the following Boolean equation.

$$Y = \neg(A \vee B)$$

Truth Table:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Behavioral Verilog:

The behavioral Verilog for the NOR is independent of its drive strength. Replace the N in the module name with the respective drive strength (i.e. 1, 2).

```
//Verilog HDL for "Lib6710_06", "NOR2X2" "behavioral"
module NOR2X2 ( Y, A, B );
 input A;
 output Y;
 input B;
 nor _i0(Y, A, B);
 specify
        (A => Y) = (1.0, 1.0);
        (B => Y) = (1.0, 1.0);
 endspecify
endmodule
```

Cell Size:

Drive Strength	Height (µM)	Width (µM)
NOR2X1	27.0	7.2
NOR2X1	27.0	7.2

Performance:

Propagation Delay (Rising Outputs):

Drive Strength	Min.	Max.
NOR2X1	0.264909	3.863364
NOR2X2	0.250601	3.703823

Output Rise Time:

Drive Strength	Min.	Max.
NOR2X1	0.214311	3.165392
NOR2X2	0.187695	3.003025

Propagation Delay (Falling Outputs):

Drive Strength	Min.	Max.
NOR2X1	0.428223	6.032361
NOR2X2	0.304294	4.673979

Output Fall Time:

Drive Strength	Min.	Max.
NOR2X1	0.294217	4.824453
NOR2X2	0.265084	3.63339

Logic Symbol:

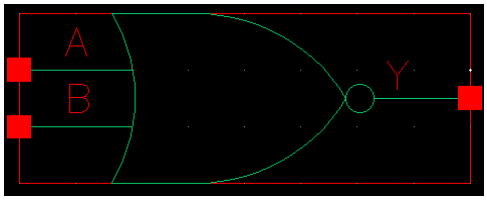

Figure 49: Symbol View for the NOR cell.

CMOS Schematic:

The following figures display the CMOS schematics for the NOR cells.

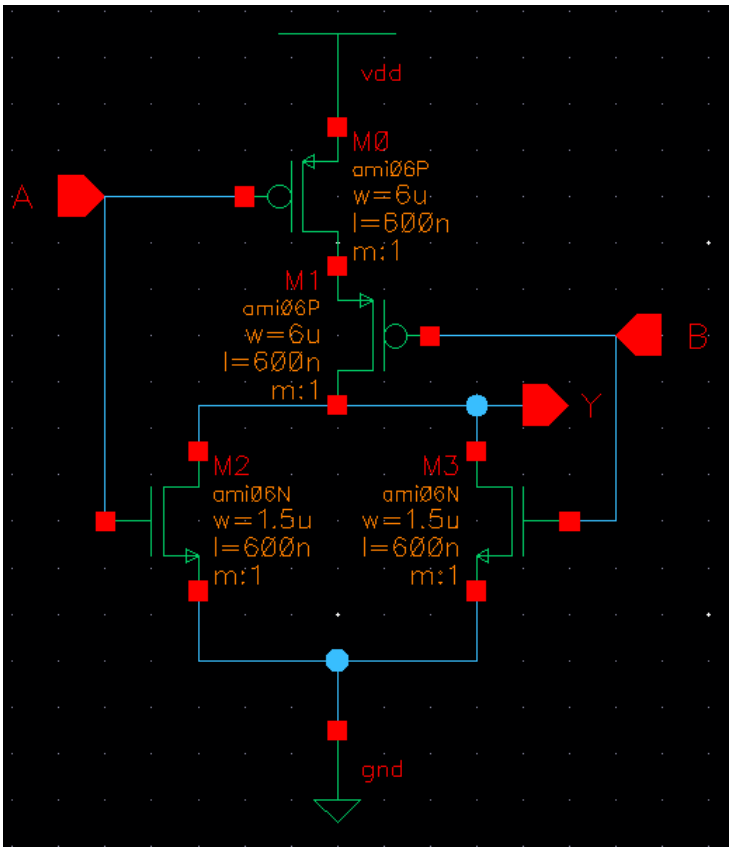

Figure 50: CMOS Schematic for the NOR2X1 cell.

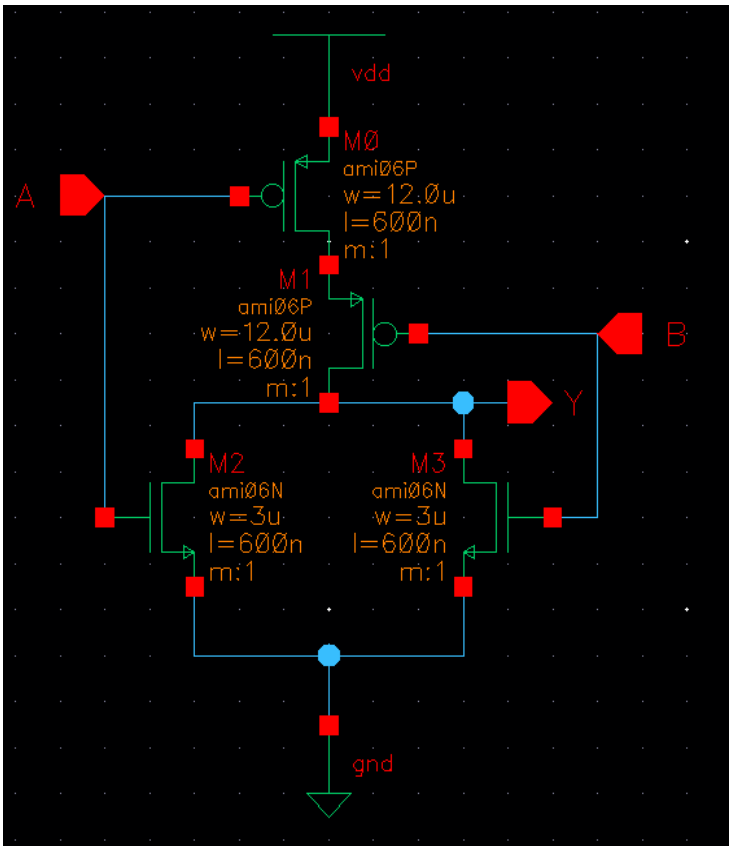

Figure 51: CMOS Schematic for the NOR2X2 cell.

CMOS Layout:

The following figures display the CMOS layouts for the NOR cells.

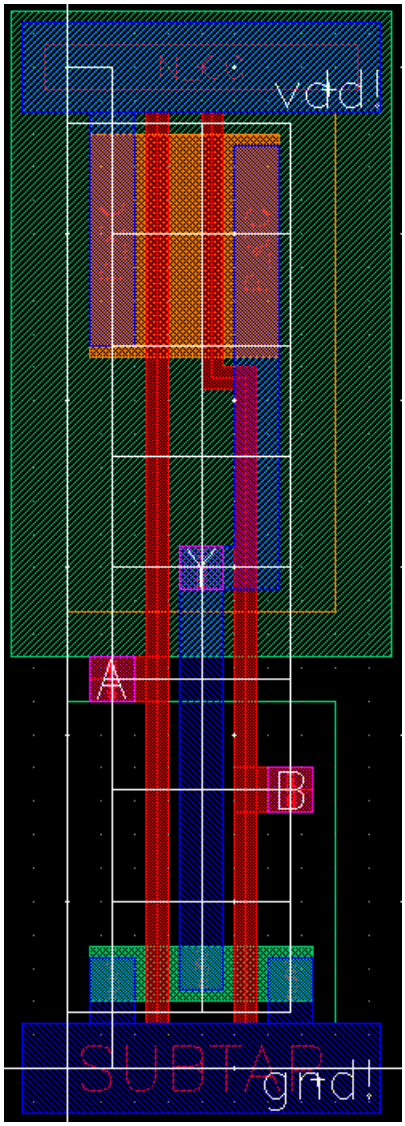

Figure 52: CMOS layout for the NOR2X1 cell.

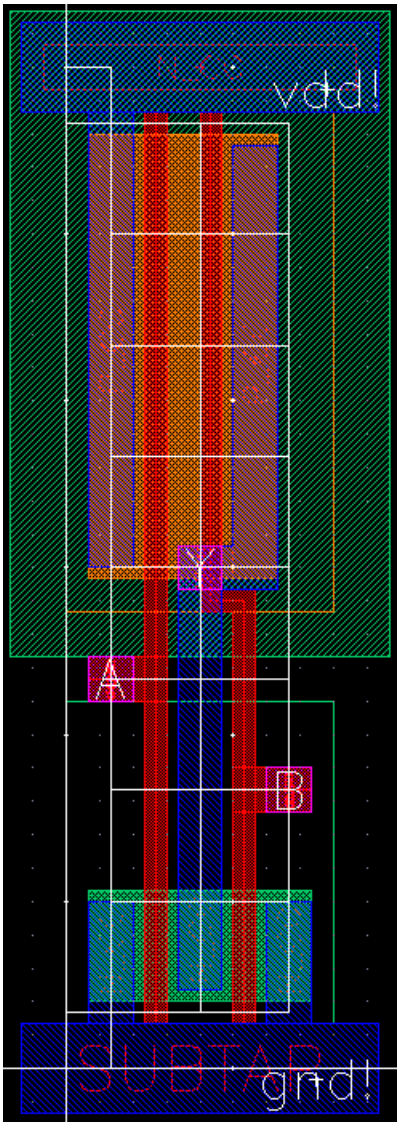

Figure 53: CMOS layout for the NOR2X2 cell.

OAI21

Cell Description:

This is a standard 3 input OR AND INVERT (OAI) cell. This cells functionality is described by the following Boolean equation:

$$Y = \neg((A \vee B) \wedge C)$$

Truth Table:

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Behavioral Verilog:

```
//Verilog HDL for "Lib6710_06", "OAI21X1" "behavioral"
module OAI21X1 ( Y, A, B, C );
  input A;
  input C;
  output Y;
  input B;
  assign Y = ~((A | B) & C);
  specify
  (A => Y) = (1.0, 1.0);
  (B => Y) = (1.0, 1.0);
  (C => Y) = (1.0, 1.0);
  endspecify
endmodule
```

Cell Size:

Drive Strength	Height (µM)	Width (µM)
OAI21X1	27.0	9.6

Performance:

Propagation Delay (Rising Outputs):

Drive Strength	Min. (nS)	Max. (nS)
OAI21X1	0.27968	4.597846

Output Rise Time:

Drive Strength	Min. (nS)	Max. (nS)
OAI21X1	0.225021	3.761913

Propagation Delay (Falling Outputs):

Drive Strength	Min. (nS)	Max. (nS)
OAI21X1	0.275231	3.788826

Output Fall Time:

Drive Strength	Min. (nS)	Max. (nS)
OAI21X1	0.20229	3.002085

Logic Symbol:

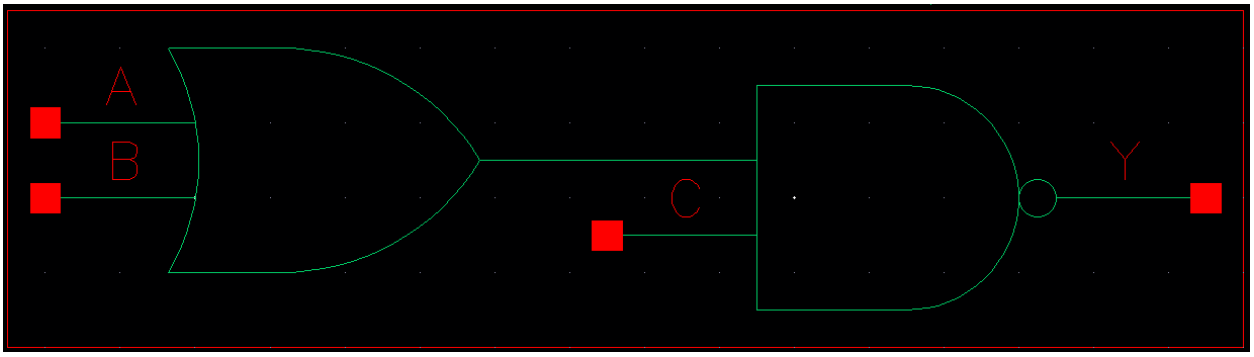

Figure 54: Symbol View for the OAI21 cell

CMOS Schematic:

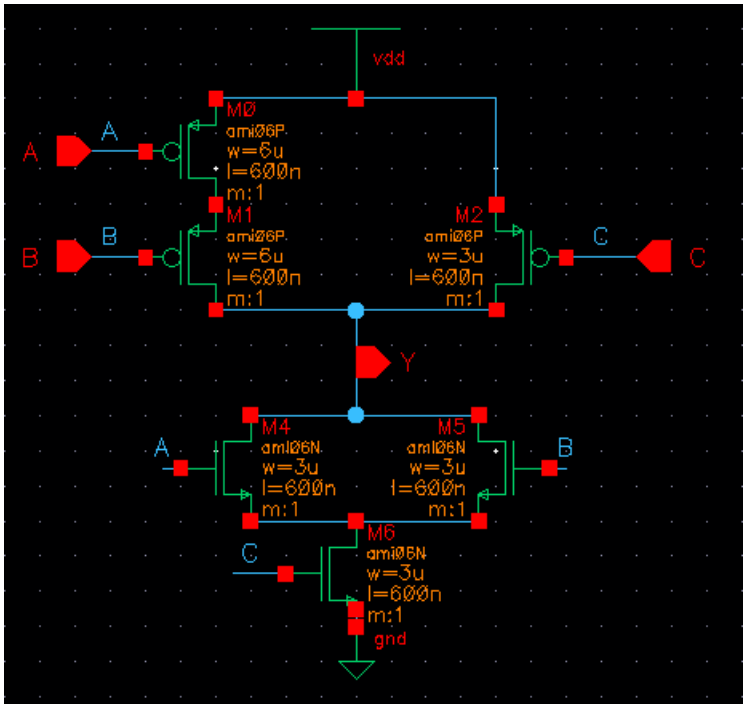

Figure 55: CMOS schematic view for the AOI21X1 cell.

CMOS Layout:

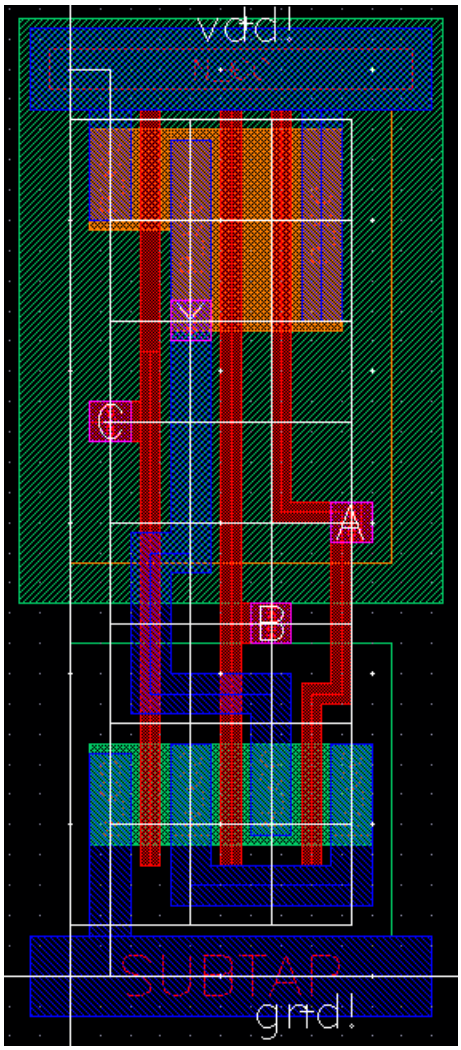

Figure 56: CMOS layout view for the OAI21x1 cell.

OAI22

Cell Description:
This is a standard 4 input OR AND INVERT (OAI) cell. This cells functionality is described by the following Boolean equation:

$$Y = \neg((A \vee B) \wedge (C \vee D))$$

Truth Table:

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Behavioral Verilog:

```
//Verilog HDL for "Lib6710_06", "OAI22X1" "behavioral"
module OAI22X1 ( Y, A, B, C, D );
 input A;
 input C;
 output Y;
 input D;
 input B;
 assign Y = ~((A | B) & (C | D));
 specify
 (A => Y) = (1.0, 1.0);
 (B => Y) = (1.0, 1.0);
 (C => Y) = (1.0, 1.0);
 (D => Y) = (1.0, 1.0);
 endspecify
```

endmodule

Cell Size:

Drive Strength	Height (µM)	Width (µM)
OAI22X1	27.0	12.0

Performance: Propagation Delay (Rising Outputs):

Drive Strength	Min.	Max.
OAI22X1	0.300605	4.006238

Output Rise Time:

Drive Strength	Min.	Max.
OAI22X1	0.256434	3.278998

Propagation Delay (Falling Outputs):

Drive Strength	Min.	Max.
OAI22X1	0.281484	3.527279

Output Fall Time:

Drive Strength	Min.	Max.
OAI22X1	0.205265	2.716359

Logic Symbol:

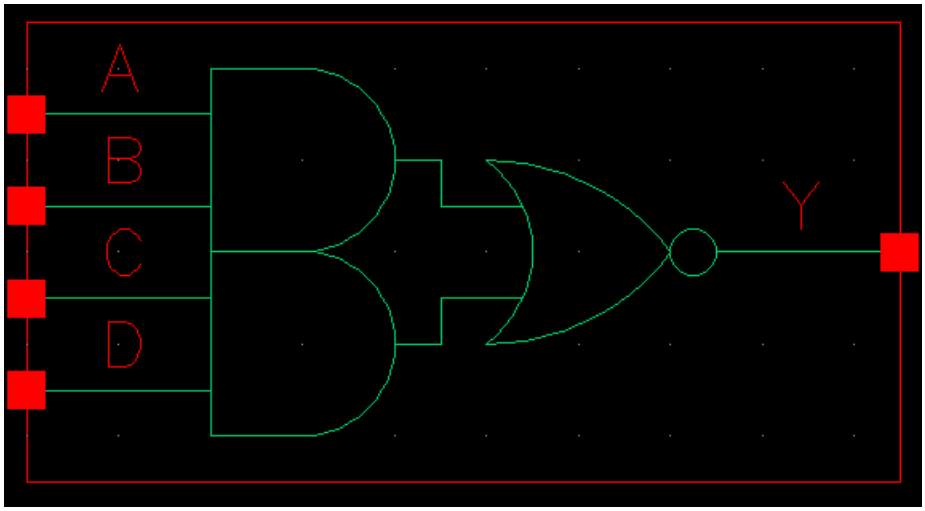

Figure 57: Symbol View for the OAI22 cell.

CMOS Schematic:

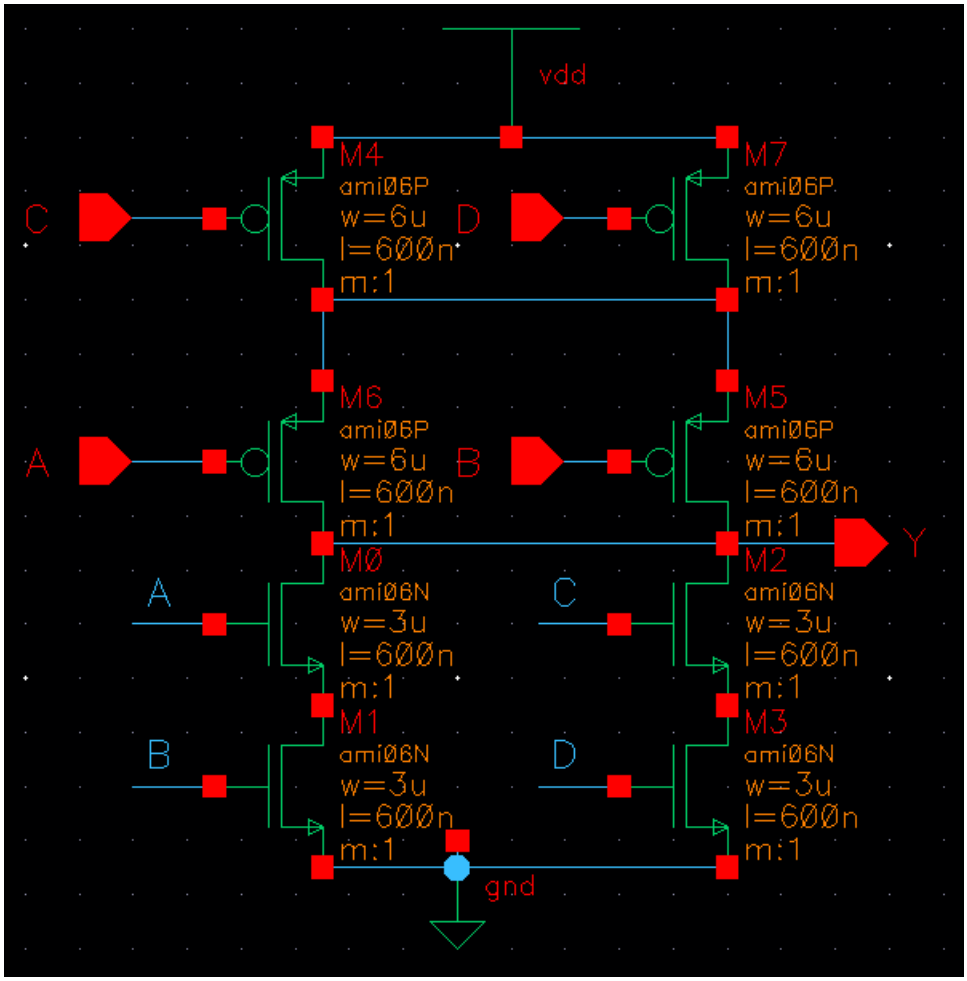

Figure 58: CMOS Schematic for the OAI22x1 cell.

CMOS Layout:

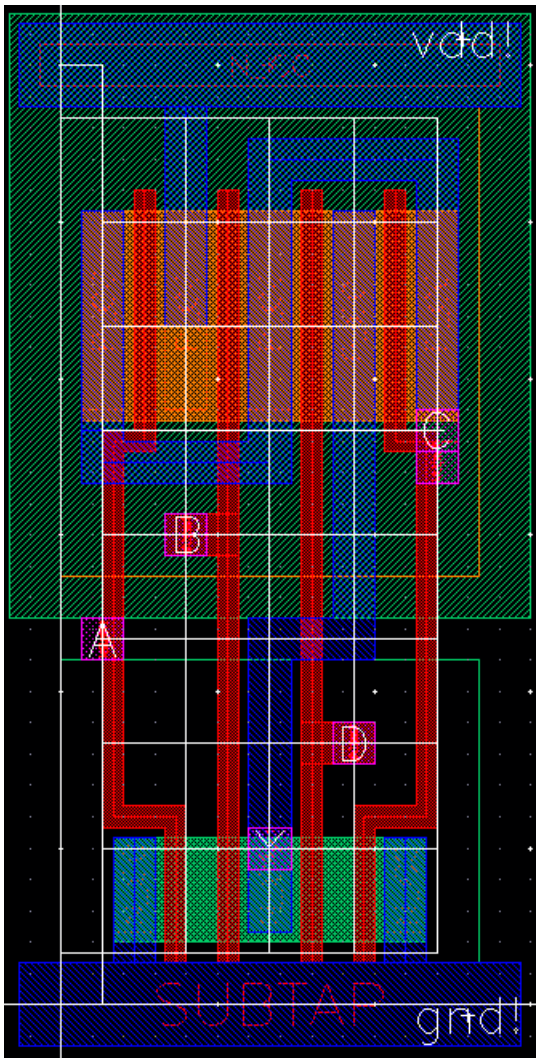

Figure 59: CMOS layout for the OAI22X1 cell.

TIEHI

Cell Description:
This is a standard TIEHI cell. The purpose of this cell is to hardcode a logic high signal. It is described by the following Boolean equation.

$$\boldsymbol{Y = 1}$$

Truth Table:

Y
1

Behavioral Verilog:

Cell Size:

Drive Strength	Height (µM)	Width (µM)
TIEHI	27.0	4.8

Logic Symbol:

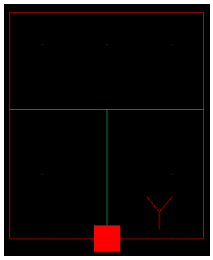

Figure 60: Symbol View for the TIEHI cell.

CMOS Schematic:

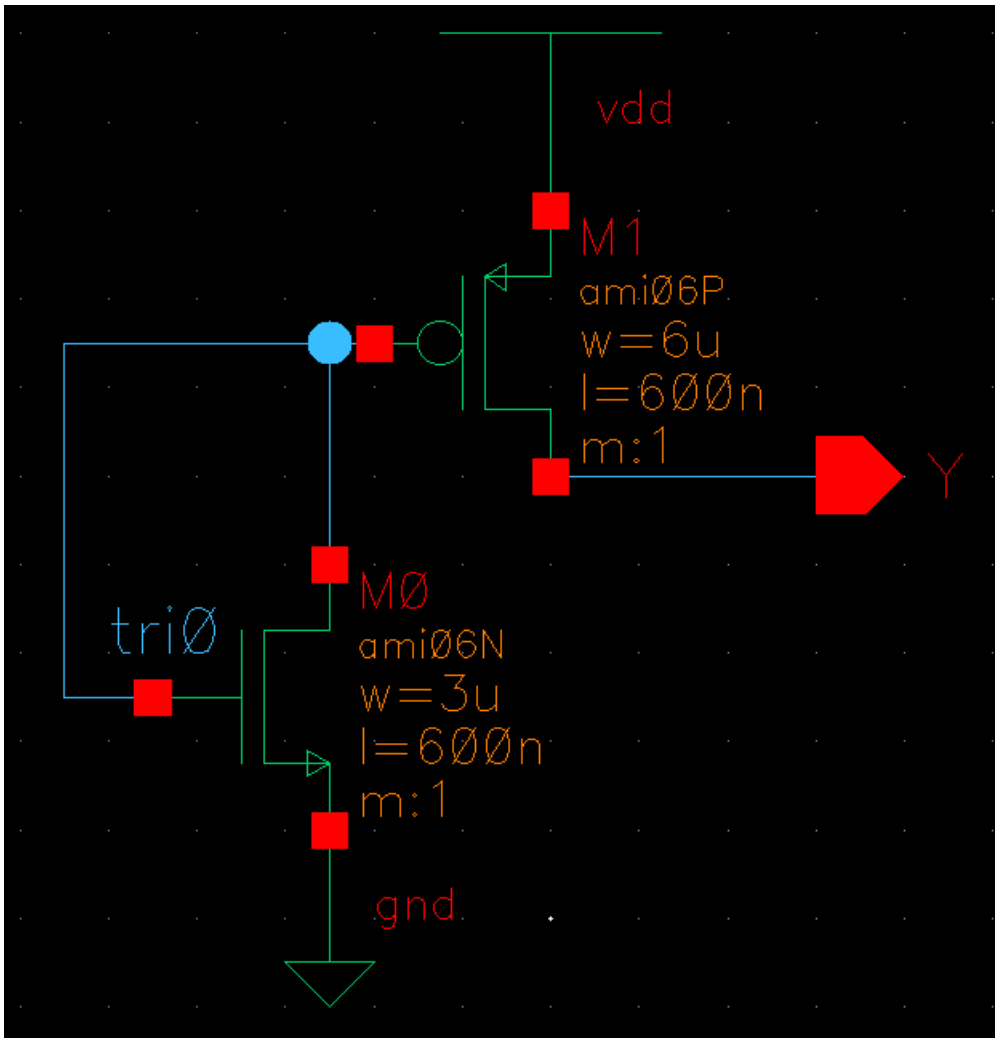

Figure 61: CMOS Schematic for the TIEHI cell.

CMOS Layout:

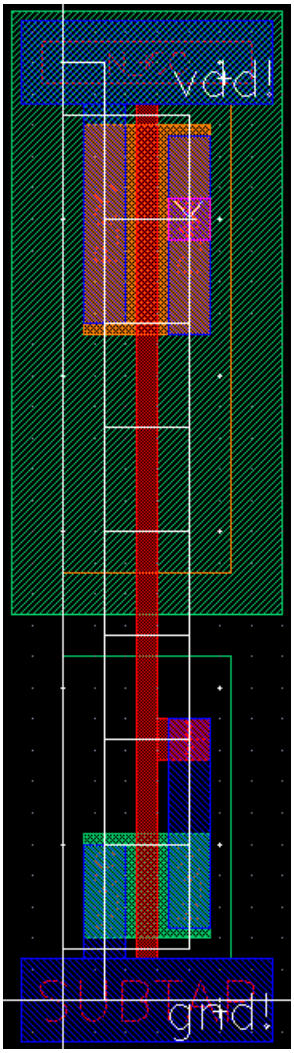

Figure 62: CMOS layout for the TIEHI cell

TIELO

Cell Description:
This is a standard TIELO cell. The purpose of this cell is to hardcode a logic low signal. It is described by the following Boolean equation.

$$Y = 0$$

Truth Table:

Y
0

Behavioral Verilog:

```
//Verilog HDL for "Lib6710_06", "TIELO" "behavioral"
module TIELO ( Y );
  output Y;
  assign Y = 1'b0;
endmodule
```

Cell Size:

Drive Strength	Height (µM)	Width (µM)
TIELO	27.0	4.8

Logic Symbol:

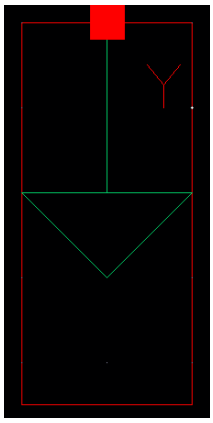

Figure 63: Symbol View for the TIELO cell.

CMOS Schematic:

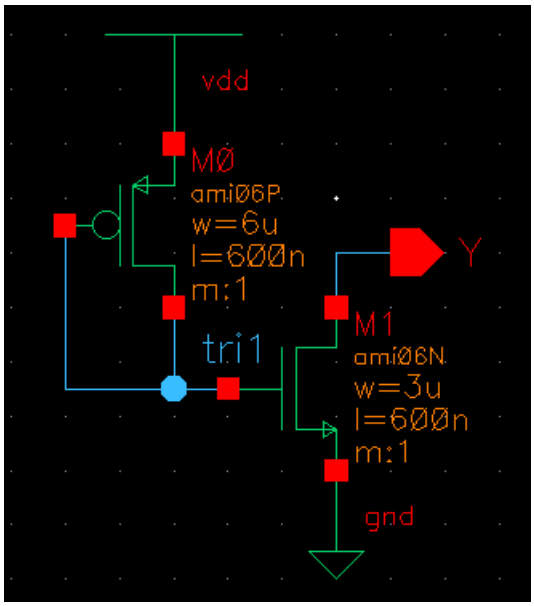

Figure 64:

CMOS Layout:

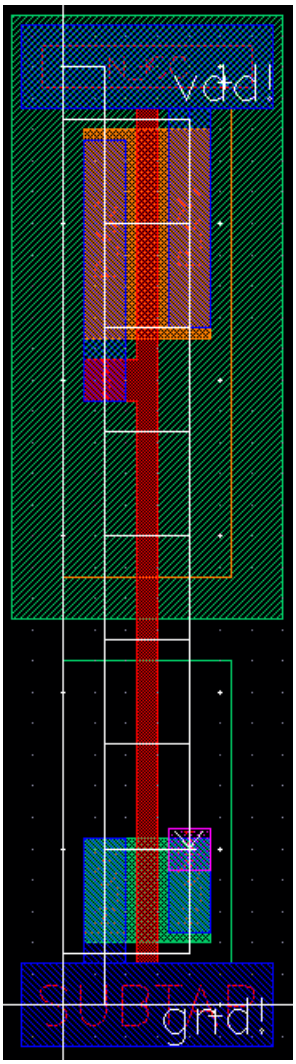

Figure 65: CMOS layout for the TIELO cell

TRINV

Cell Description:
This is a standard tristate inverter cell. This cells functionality is described by the following Boolean equation:

$$Y = (\neg A \wedge \neg P\_EN) \vee \neg(A \wedge N\_EN)$$

Truth Table:

A	P_EN	N_EN	Y
0	0	0	1
0	0	1	1
0	1	0	Z
0	1	1	Z
1	0	0	Z
1	0	1	0
1	1	0	Z
1	1	1	0

Behavioral Verilog:

```
//Verilog HDL for "Lib6710_06", "TRINV" "behavioral"
module TRINV ( Y, A, N_EN, P_EN );
 input A;
 input N_EN;
 output Y;
 input P_EN;
assign Y = (N_EN & ~P_EN) ? ~A : 1'bz;
 specify
 (A => Y) = (1.0, 1.0);
 (N_EN => Y) = (1.0, 1.0);
 (P_EN => Y) = (1.0, 1.0);
 endspecify
endmodule
```

Cell Size:

Drive Strength	Height (µM)	Width (µM)
TRINV	27.0	7.2

Performance:

Propagation Delay (Rising Outputs):

Drive Strength	Min.	Max.
TRINV	0.264876	3.846145

Output Rise Time:

Drive Strength	Min.	Max.
TRINV	0.242767	3.194577

Propagation Delay (Falling Outputs):

Drive Strength	Min.	Max.
TRINV	0.239441	3.677291

Output Fall Time:

Drive Strength	Min.	Max.
TRINV	0.231033	2.994907

Logic Symbol:

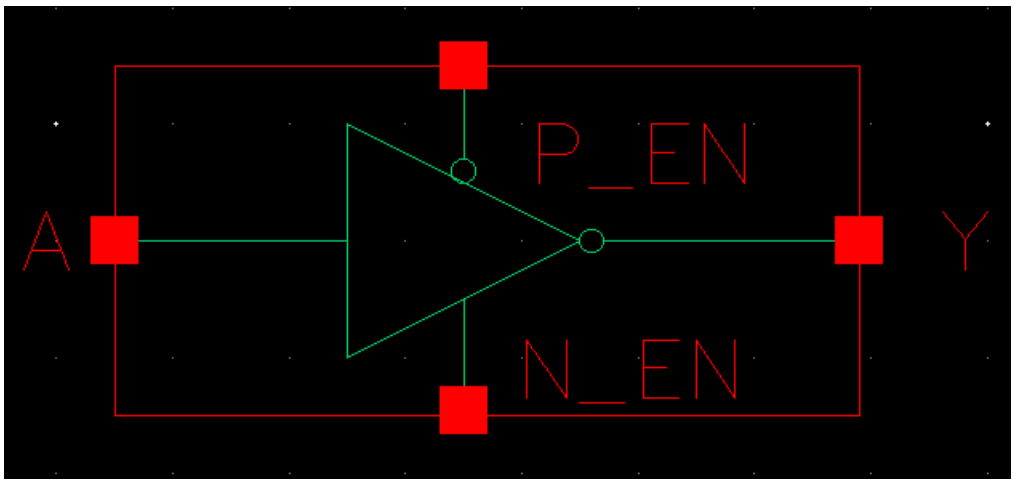

Figure 66: Symbol View for the TRINV cell

CMOS Schematic:

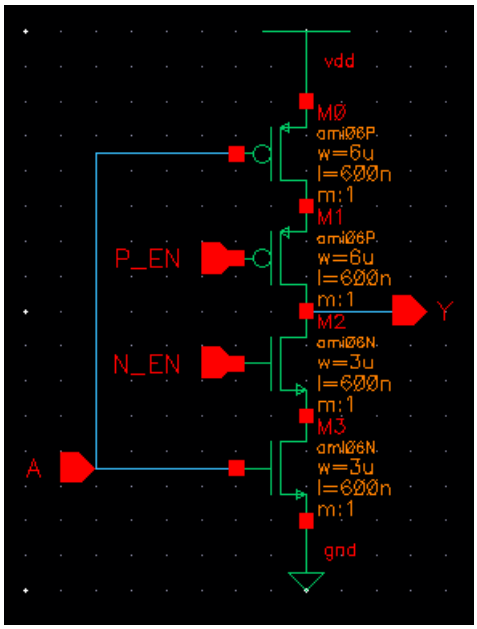

Figure 67: CMOS Schematic for TRINV cell.

CMOS Layout:

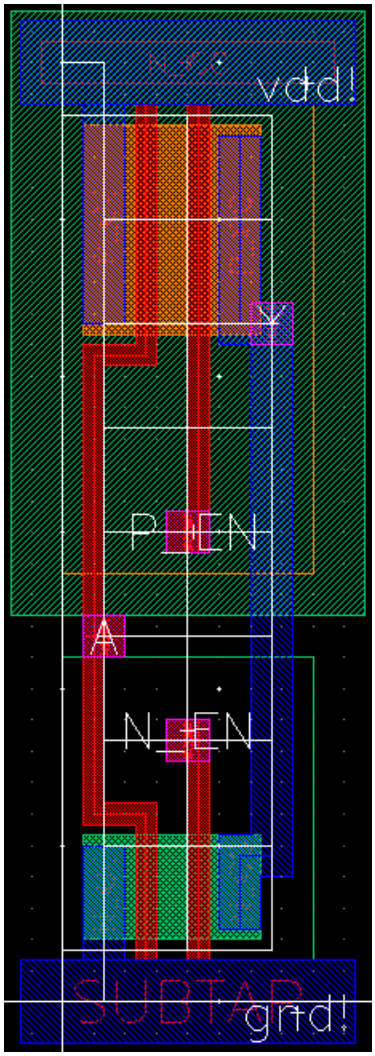

Figure 68: CMOS layout for TRINV cell.

XOR

Cell Description:

This is a standard two input XOR cell with the following Boolean equation.

$$Y = A \oplus B$$

Truth Table:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Behavioral Verilog:

```
//Verilog HDL for "Lib6710_06", "XOR2X1" "behavioral"
module XOR2X1 ( Y, A, B );
  input A;
  output Y;
  input B;
  xor(Y, A, B);
  specify
    (A => Y) = (1.0, 1.0);
    (B => Y) = (1.0, 1.0);
  endspecify
endmodule
```

Cell Size:

Drive Strength	Height (µM)	Width (µM)
XOR2X1	27.0	12.0

Performance:

Propagation Delay (Rising Outputs):

Drive Strength	Min. (nS)	Max. (nS)
XOR2X1	0.309335	0.536119

Output Rise Time:

Drive Strength	Min. (nS)	Max. (nS)
XOR2X1	0.249189	3.189955

Propagation Delay (Falling Outputs):

Drive Strength	Min. (nS)	Max. (nS)
XOR2X1	0.337925	3.873978

Output Fall Time:

Drive Strength	Min. (nS)	Max. (nS)
XOR2X1	0.214332	3.063275

Logic Symbol:

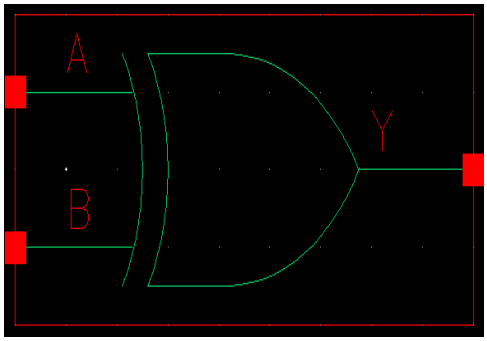

Figure 69: Symbol View for the XOR cell.

CMOS Schematic:

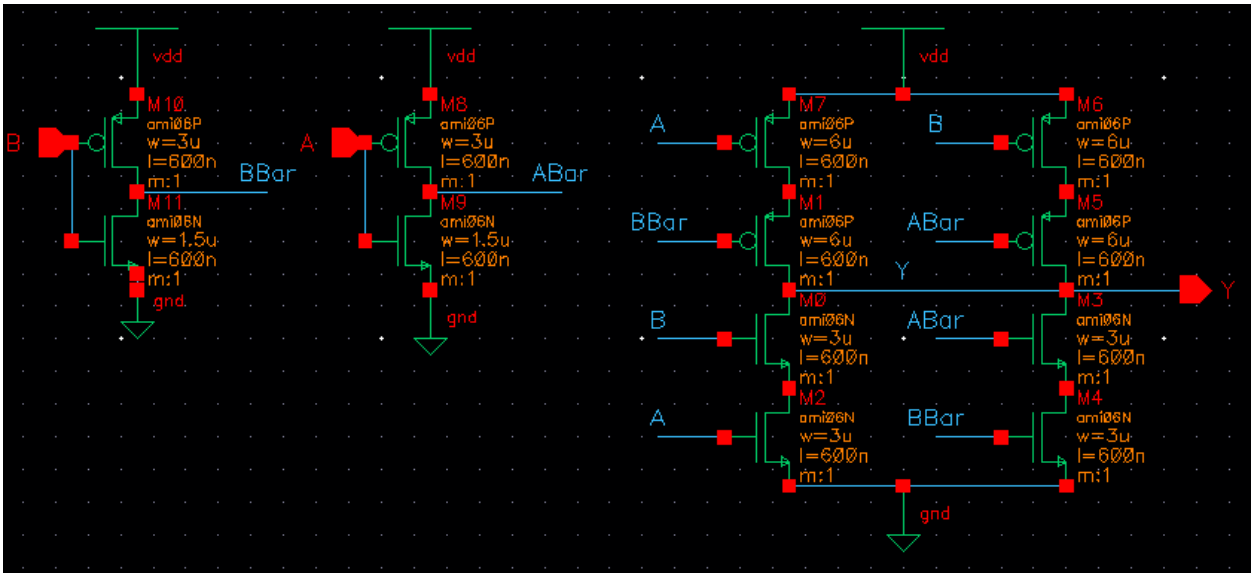

Figure 70: CMOS Schematic for the XOR2X1 cell.

CMOS Layout:

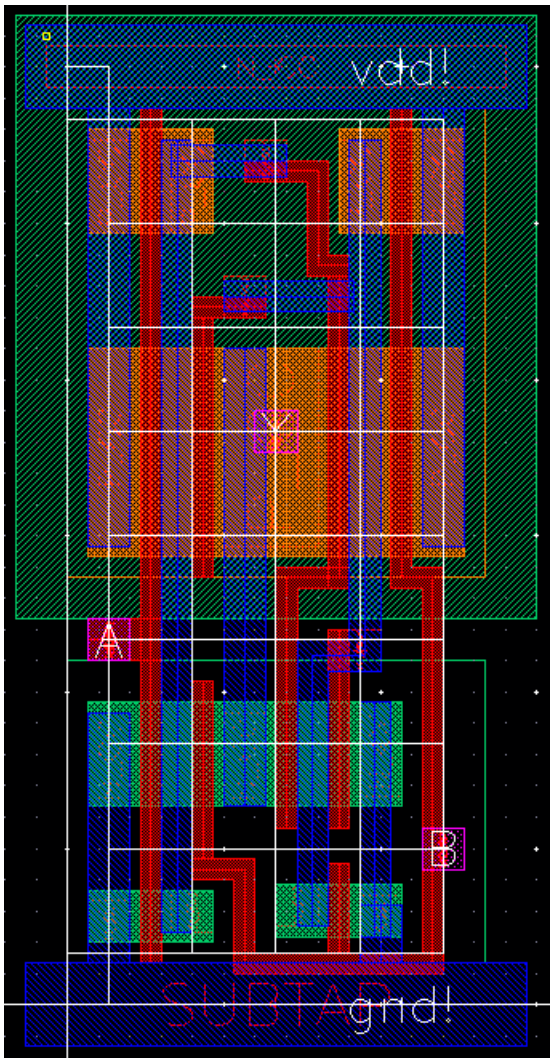

Figure 71: CMOS layout for the Nor2X1 cell.