Project 235 PLD Design

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Design Brief

Client: Netflix

Designers: Thomas Meagher

Problem Statement:

- Netflix needs to display a quote from one of their most popular TV series in their corporate headquarters gift store. They only have one display and need the quote to be displayed asynchronously.

Design Statement:

- I created the message “Friends Dont Lie” on a single seven-segment display using a programmable logic device. Along with that, I used a 4-bit counter and clock pulse to toggle through the states automatically.

Constraints:

- There must be 4 inputs utilized for a total of 16 states shown on your display.
- The display may not be dark for more than 5 states.

Team Deliverables:

- Title Page - name, date, period, project name
- Table of Contents - corresponding sections and page numbers
- Design Brief & Display Definitions - design statement, constraints, summary of display (inputs and outputs)
- Truth Table & Logic Expression - table and algebraic expressions
- Solution - Simulation & Breadboard - images of simulation and breadboard shown clearly, multiple views as necessary, labels and descriptions of final design

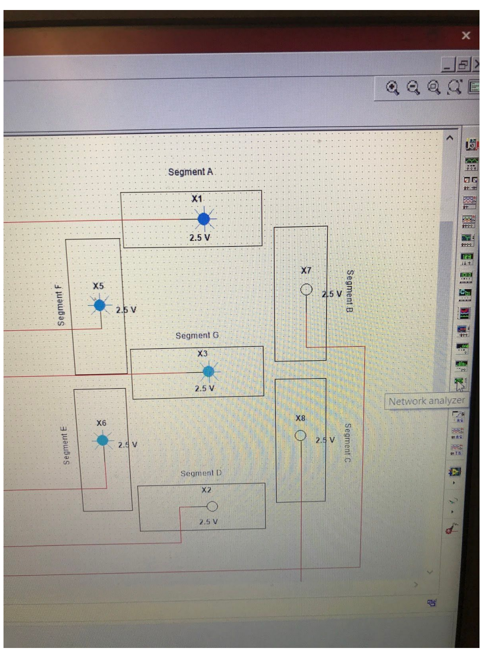
Display Definitions

Inputs:

There are four inputs used for my display: W, X, Y, and Z. During the simplification of the logic expressions I decided to convert the inputs into the letters: A, B, C, and D. Since there were four inputs, there were a total of 16 different possible outputs. The inputs were continuously cycled through to display all 16 outputs.

Outputs:

As I stated before, there were a total of 16 different outputs. And within those 16 different outputs, there were seven segments that made up each display: a, b, c, d, e, f, and g. One of the constraints is that the display may not be dark for more than 5 states. The message I used is “Friends dont Lie” and this phrase consists of 14 letters. Therefore, I only had two states where the display did not light up and I used these states as spaces in between the first and second word and the second and third word. The seven segments for each of the 16 outputs represents the segments that are shown on an SSD. All of outputs for a, b, c, d, e, f, and g in the truth table correspond to the segments on the display.



Segment A corresponds to the top segment. Segment B corresponds to the top right segment. Segment C corresponds to the bottom right segment. Segment D corresponds to the bottom segment. Segment E corresponds to the bottom left segment. Segment F corresponds to the top left segment and Segment G corresponds to the middle segment. For each of the 16 different states, there was a different letter that was displayed on the ssd. And depending on which segments were high and low determined what letter was going to be displayed.

Truth Table

Inputs				Seven Segment Display #1 (Common Cathode)							Display
W	**X**	**Y**	**Z**	**a**	**b**	**c**	**d**	**e**	**f**	**g**	
0	0	0	0	1	0	0	0	1	1	1	F
0	0	0	1	0	0	0	0	1	0	1	r
0	0	1	0	0	0	0	0	1	0	0	i
0	0	1	1	1	0	0	1	1	1	1	E
0	1	0	0	0	0	1	0	1	0	1	n
0	1	0	1	0	1	1	1	1	0	1	d
0	1	1	0	1	0	1	1	0	1	1	S
0	1	1	1	0	0	0	0	0	0	0	N/A
1	0	0	0	0	1	1	1	1	0	1	d
1	0	0	1	0	0	1	1	1	0	1	o
1	0	1	0	0	0	1	0	1	0	1	n
1	0	1	1	0	0	0	1	1	1	1	t
1	1	0	0	0	0	0	0	0	0	0	N/A
1	1	0	1	0	0	0	1	1	1	0	L
1	1	1	0	0	0	0	0	1	0	0	i
1	1	1	1	1	0	0	1	1	1	1	E

Logic Expressions and Simplification

Segment A

Unsimplified: A’B’C’D’ + A’B’CD + A’BCD’ + ABCD

Simplified: A’B’C’D’ + A’B’CD + A’BCD’ + ABCD

Segment B

Unsimplified: A’BC’D + AB’C’D’

Simplified: A’BC’D + AB’C’D’

Segment C

Unsimplified: A’BC’D’ + A’BC’D + A’BCD’ + AB’C’D’ + AB’C’D + AB’CD’

Simplified: A’BC’ + A’BD’ + AB’C’ + AB’D’

Segment D

Unsimplified: A’B’CD + A’BC’D + A’BCD’ + AB’C’D’ + AB’C’D + AB’CD + ABC’D + ABCD

Simplified: A’BCD’ + AB’C’ + B’CD + BC’D + AD

Segment E

Unsimplified: A’B’C’D’ + A’B’C’D + A’B’CD’ + A’B’CD + A’BC’D’ + A’BC’D + AB’C’D’ + AB’C’D + AB’CD’ + AB’CD + ABC’D + ABCD’ + ABCD

Simplified: A’C’ + B’ + C’D + AC

Segment F

Unsimplified: A’B’C’D’ + A’B’CD + A’BCD’ + AB’CD + ABC’D + ABCD

Simplified: A’B’C’D’ + A’BCD’ + B’CD + ABD

Segment G

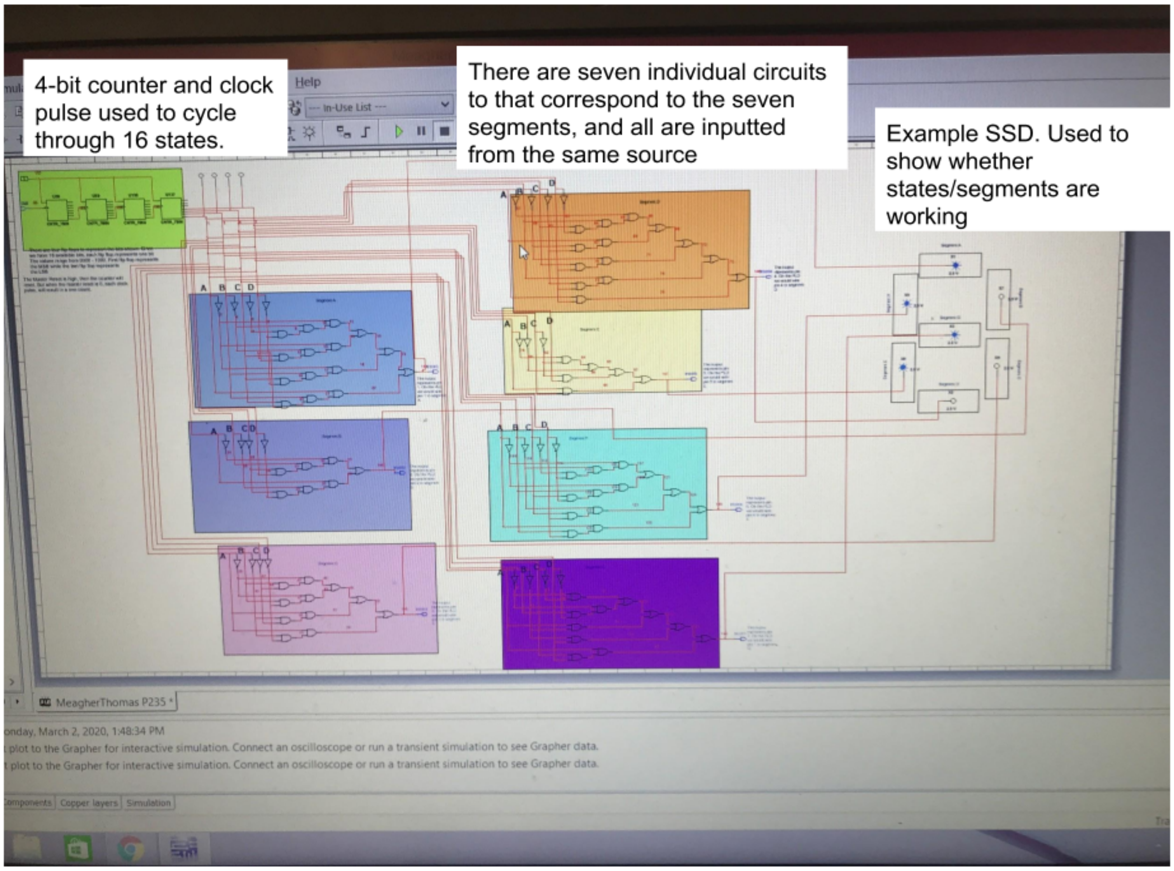
Unsimplified: A’B’C’D’ + A’B’C’D + A’B’CD + A’BC’D’ + A’BC’D + A’BCD’ + AB’C’D’ + AB’C’D + AB’CD’ + AB’CD + ABCD

Simplified: A’C’ + A’BD‘ + AB’ + B’D + ACD

Solution - Description

The final product ended up being a success. To start the process, however, I first brainstormed certain phrases that I could use for this project. I thought of phrases like “merry christmas” and “hello darkness” but there were display letters for m and k. I finally figured out the phrase “Friends dont lie " from one of my favorite TV series, Stranger Things. I created the truth table and then created individual circuits for each segment that could be displayed on the ssd. I used an aoi circuit because it was much easier for me to picture the outcome of the outputs. After creating each individual circuit, I created my 4-bit counter. From advice from my fellow peers, I used four cntr_7bin as my counters. The cntr_7bin has 2 inputs and has multiple outputs. One of the inputs, Master Reset, needs to be kept low or at zero because when Master Reset is 1 or high, it sets all values back to zero. The zero is therefore connected to all four Master Reset pins. The other input is the clock pulse. We connect the clock input into the clock pulse to create the continuous cycle. From there we have an output that is then connected to the next counter’s clock pulse. The last counter has four outputs, though. These four outputs are used to connect the remaining, individual circuits. The four outputs connect to the circuits for a-g and each corresponding output connects to the A, B, C, and D. The individual circuits are now connected to the 4-bit counter and either display a high or low depending on what state it is on. Also, the individual circuits are outputted to different pin numbers. These pin numbers are represented on the PLD. Lastly on the multisim, we had to create our own segment display and place probes connected to the outputs of the segment circuits to test if our display actually works. Once we finished the Multisim, we exported it onto a PLD. We then placed the PLD onto a breadboard and started wiring it. We wired the corresponding pin numbers to their segments, and then grounded both the PLD and the display. Once we were finished wiring, our message was automatically shown on the seven segment display on the bottom of the breadboard.

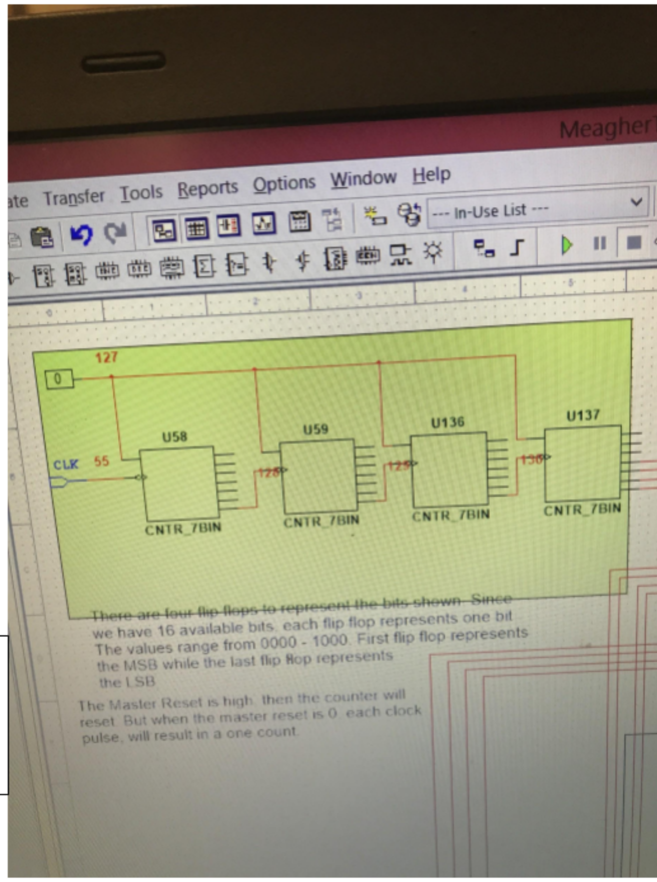
Solution - Simulation

Full Simulation :

4-bit Counter :

The 0 is wired to the MR, so that it does not reset to low

Clock is inserted into clock pulse pin and is outputted from one of the pins into the next clock pulse pin

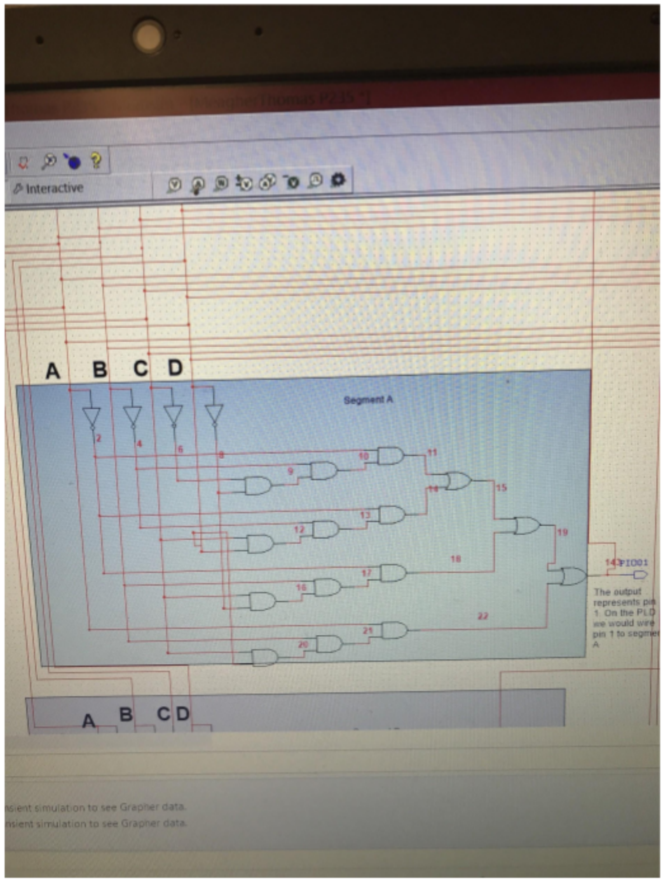
This creates the divide-by-two frequency where the output feeds into the next input.



In the last bit counter, there are 4 outputs pins which are utilized to feed into the A, B, C, and D inputs for the segments

Segment A :

Input values A, B, C, and D are wired from the four ouputs from the 4-bit counter

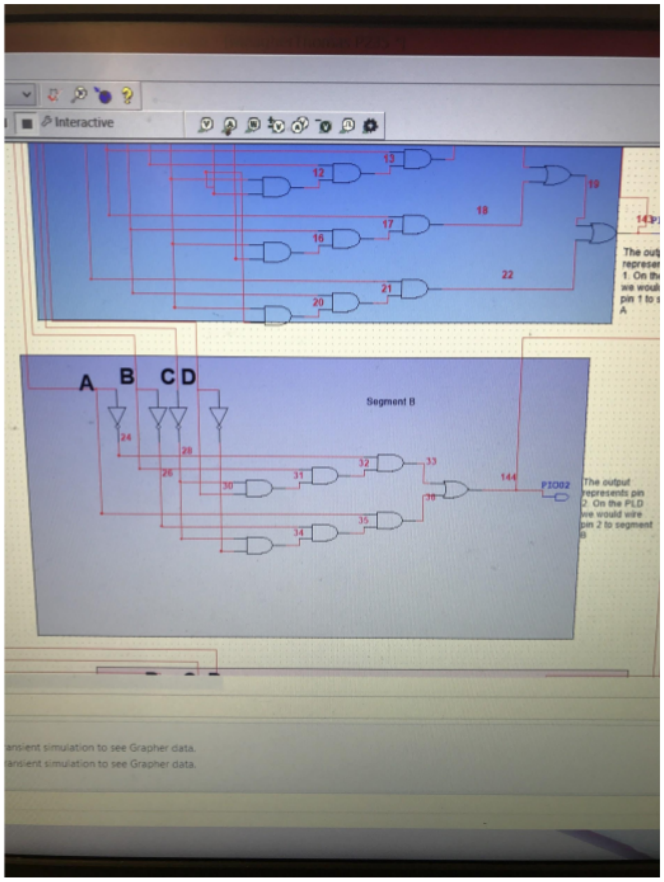


This circuit was created from the truth table “a” column

The output of this circuit is connected to pin 1 on the PLD

Therefore the output will correspond to the top segment of the display

Segment B :



Input values A, B, C, and D are wired from the four outputs from the 4-bit counter

This circuit was created from the truth table “b” column

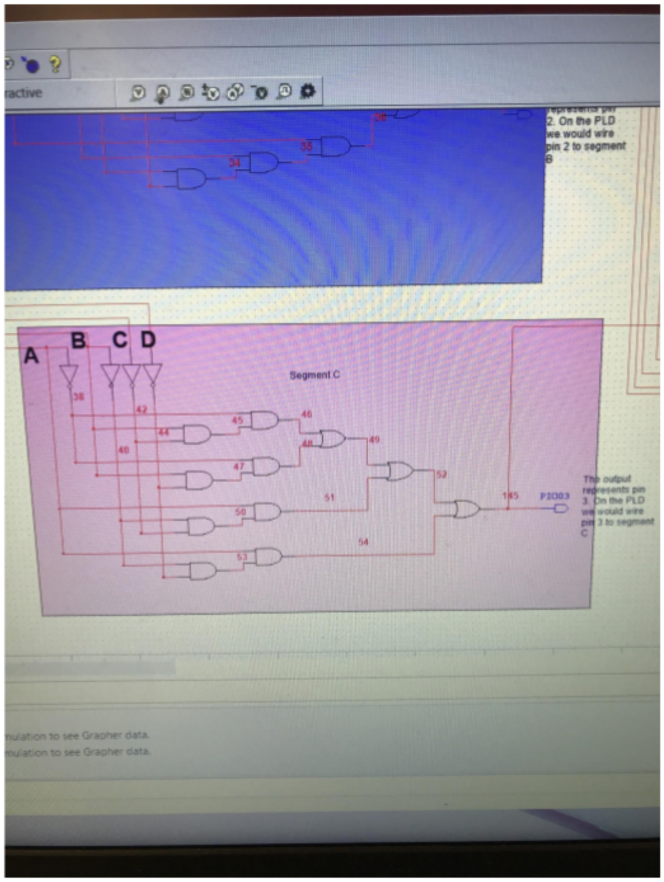
The output of this circuit is connected to pin 2 on the PLD

Therefore the output will correspond to the top right segment of the display

Segment C :

Input values A, B, C, and D are wired from the four outputs from the 4-bit counter

The output of this circuit is connected to pin 3 on the PLD



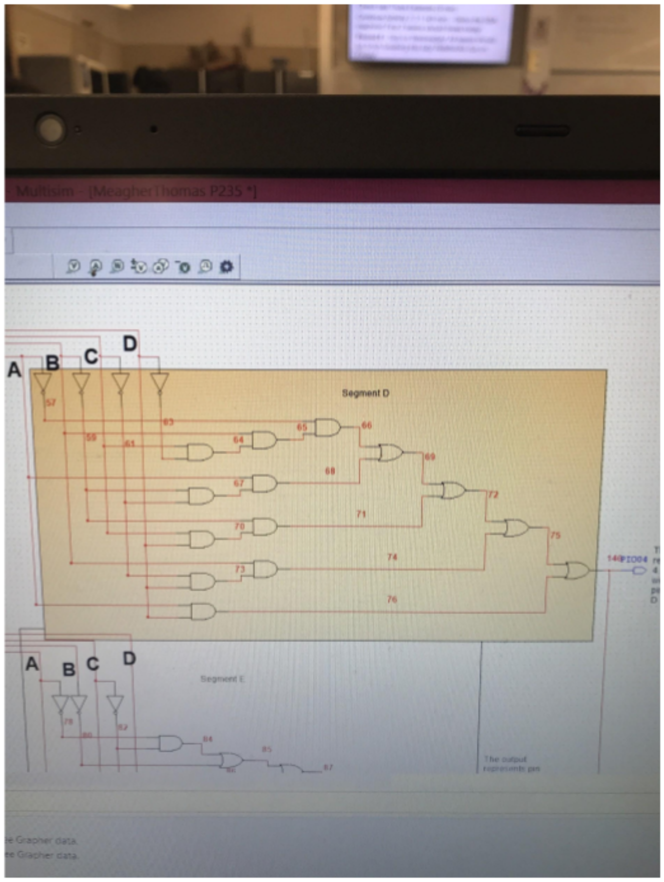
This circuit was created from the truth table "c" column

Therefore the output will correspond to the bottom right segment of the display

Segment D :

Input values A, B, C, and D are wired from the four outputs from the 4-bit counter

The output of this circuit is connected to pin 4 on the PLD



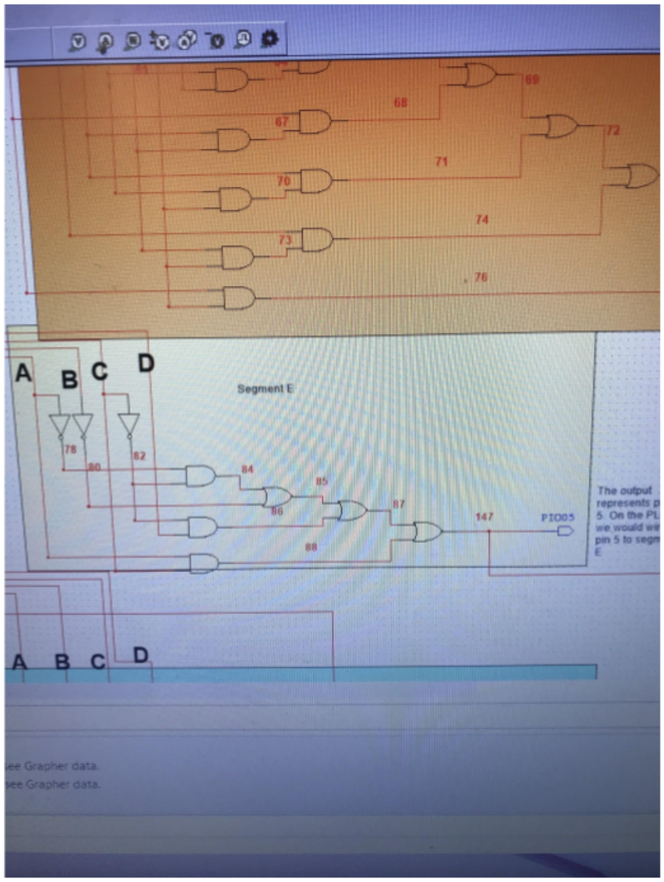
This circuit was created from the truth table "d" column

Therefore the output will correspond to the bottom segment of the display

Segment E :

Input values A, B, C, and D are wired from the four outputs from the 4-bit counter

The output of this circuit is connected to pin 5 on the PLD

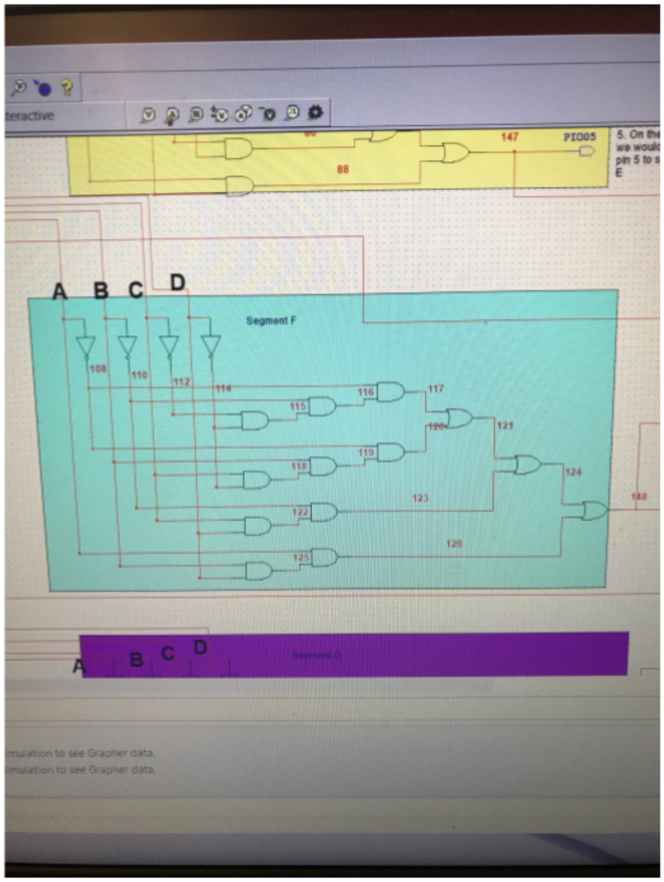


This circuit was created from the truth table “e” column

Therefore the output will correspond to the bottom left segment of the display

Segment F :

Input values A, B, C, and D are wired from the four outputs from the 4-bit counter



This circuit was created from the truth table "f" column

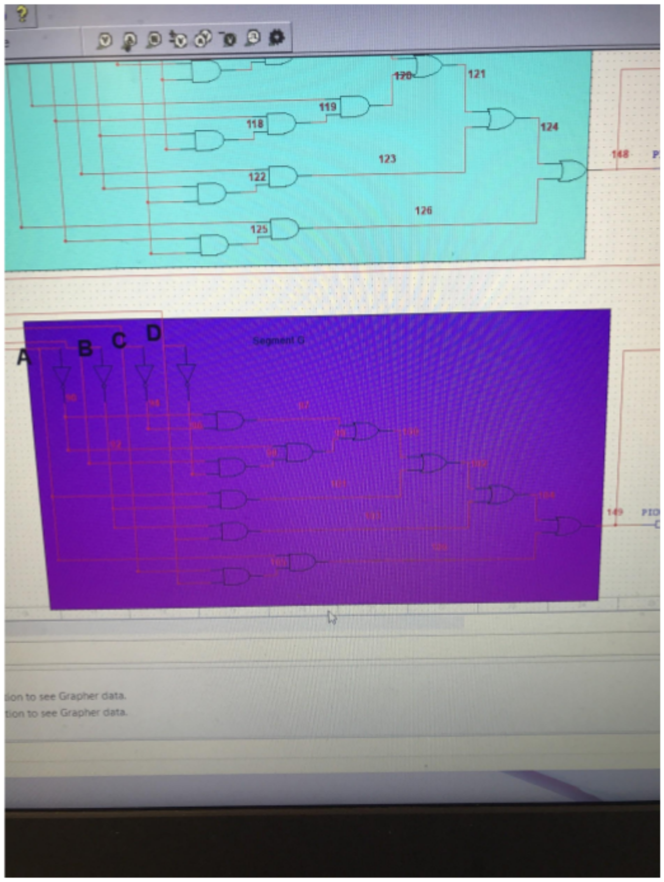
The output of this circuit is connected to pin 6 on the PLD

Therefore the output will correspond to the top left segment of the display

Segment G :

Input values A, B, C, and D are wired from the four outputs from the 4-bit counter

The output of this circuit is connected to pin 7 on the PLD



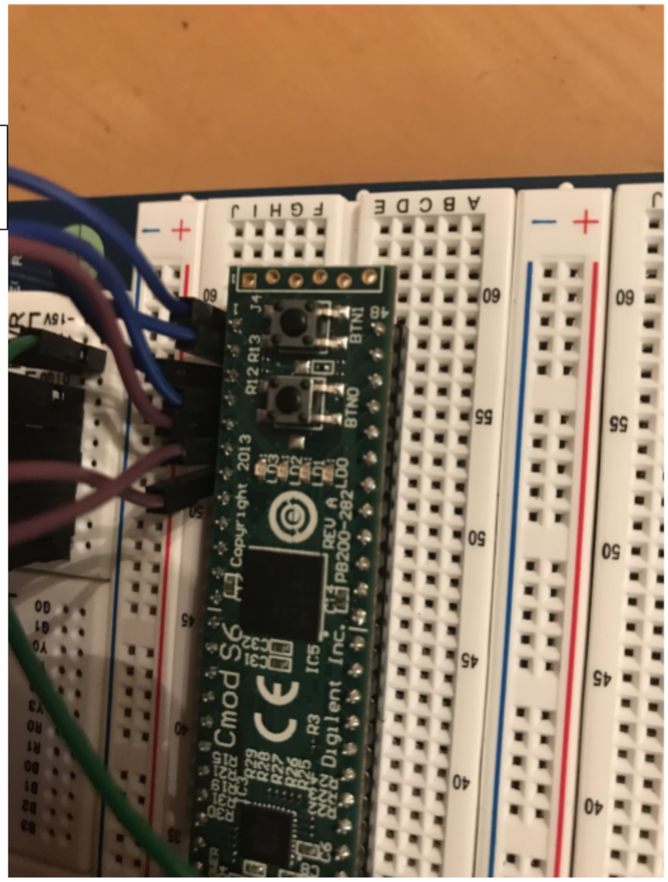
This circuit was created from the truth table “g” column

Therefore the output will correspond to the middle segment of the display

Solution - Breadboard

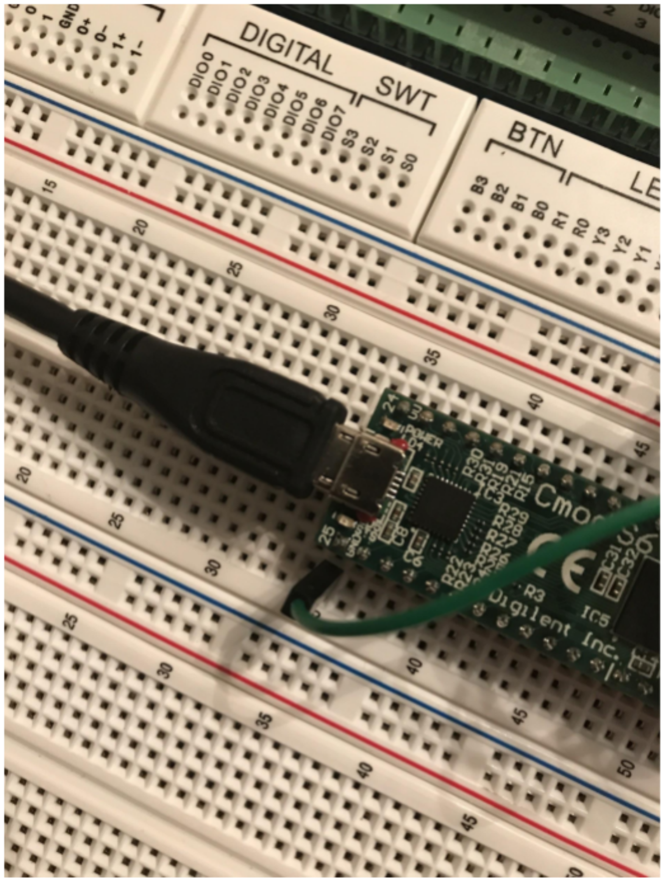
This shows the PLD and the pins that are being used

As you can see there are wires connected to pins 1 - 7



These pins correlate to the outputs of the circuits of the segments

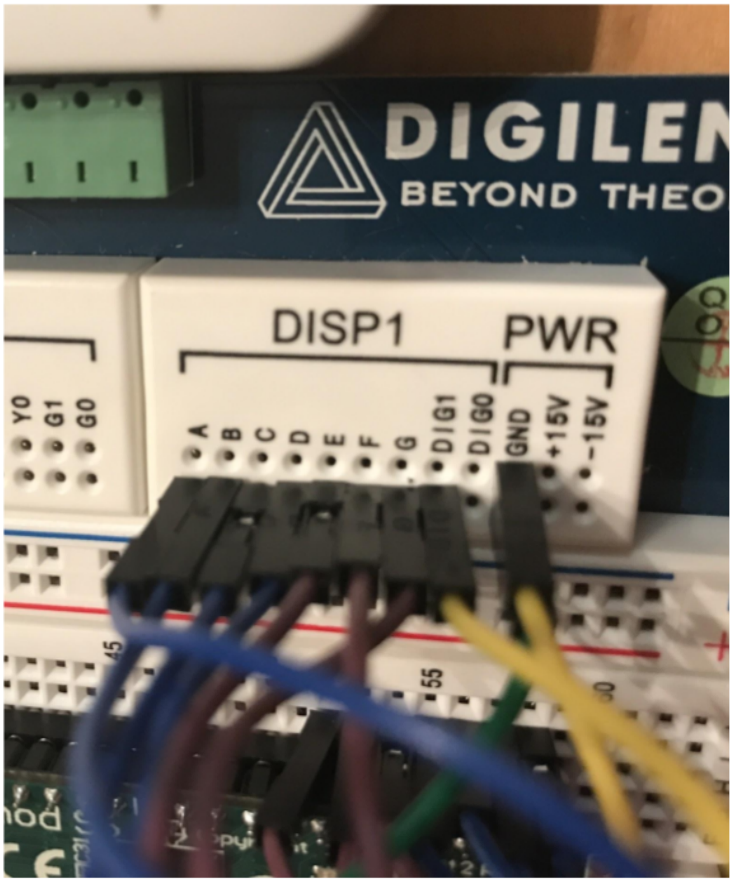
This just shows that we have connected a wire from the ground pin.



The wire leads to the ground hole of the breadboard which allows the PLD to be grounded

Wires from the PLD are being connected to the display on the breadboard.

As you can see the wires are being connected to the display of the breadboard. The DIG1 is grounded to signify that we would used the DIG1 display



A, B, C, D, E, F, and G all represent the different segments of an SSD

As stated from above, we would be using the DIG1 display.

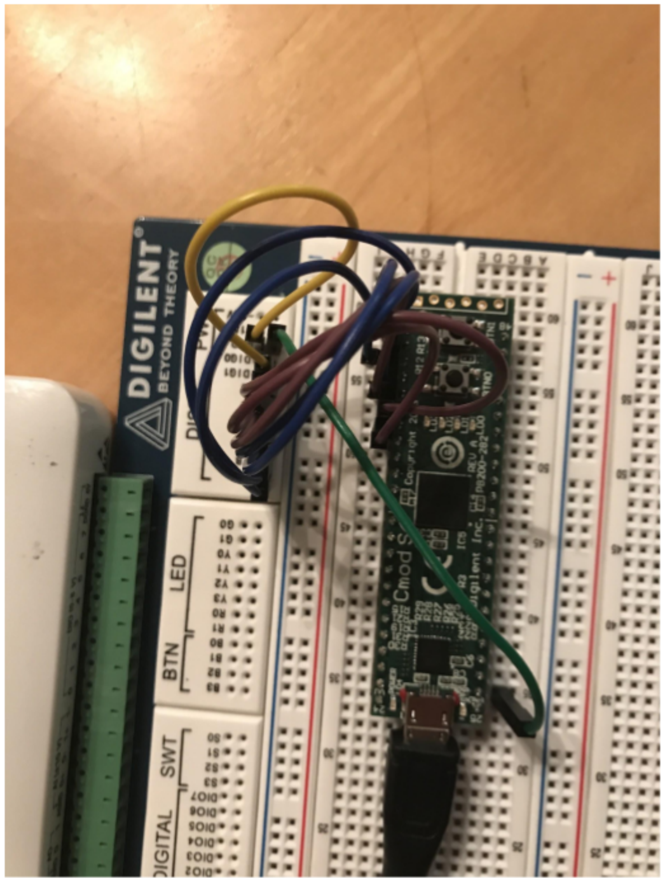
The different letters on the breadboard correspond to the different segments

The display will showcase a letter and will cycle through the other 15 states.

Here is a clear view of the whole breadboard

As you can see, the wires are being connected from the PLD to the breadboard.

The DIG1 pin is connected to the ground as well



Pins 1-7 are being used on the PLD and are connected to a-g. Pin 1 is connected to a. Pin 2 is connected to b. Pin 3 is connected to c. Pin 4 is connected to d. Pin 5 is connected to e. Pin 6 is connected to f. Pin 7 is connected to g.

The ground pin from the PLD is connected to the ground on the breadboard