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FRDM-KL46Z

Revisions

Rev	Description	Date	Approved
A	Initial version		
AX1	1. As per the new FRDM-KL46 pin assignment xls connections changed. 2. Net changed from SWD_CLKto SWD_CLK_TGTMCU in connector J11.2 3. Net name TSI0_CH9/TSI0_CH10 removed from touch interface. 4. Port name and Arduino functions name Text added to the nets. 5. 5V regulator PAD added 6. separate Accelarometer and Magnetometer sensor Freplaced with FXOS8700CQ 7. PPL Released	07-MAR-13	Luis Puebla Palma
AX2	1. As per the FRDM-KL46 new pinout assignement Rev3.xls connections changed. 2. Port name and Arduino functions name Text changed to the nets as per new pin assignment. 3. Arduino connector Ref des changed as per TRD requirement 4. INT1_MAG net removed 5. Test point added in PTE26	14-MAR-13	Luis Puebla Palma
AX3	1. Magnetometer circuit added with same I2C Bus (I2C0_SCL/SDA) 2. Magnetometer interrupt is connected to Accelerometer interrupt 2 through a 0 ohms resistor. 3. Spare buffer U5B input is pulled low using a 0 ohms res.	25-MAR-13	Luis Puebla Palma
AX4	1. FXOS8700CQ replaced with MMA8451Q. NC Pins wired to make compatible with CRST, RST, RSVD1/2 in FXOS8700CQ 2. DNP 0 ohm resistor added between Inertial sensor 3rd pin and GND. 3. DNP 0 ohms resistor added b/w Inertial sensor 16th pin and PTE26	26-MAR-13	Luis Puebla Palma
B	1. DNP Updated 2. RST_K20D50 renamed to RST_K20D50_B 3. A085 Release	28-MAR-13	Luis Puebla Palma
B1	1. D6 - DNP 2. J7 - MOUNT 3. Schematic title changed to FRDM-KL46Z 4. A085 Release	03-MAY-13	Luis Puebla Palma

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ICAP Classification: FCP: FIUO: PUBI: X

Designer: JOHN PAUL FRANKLIN	Drawing Title: FRDM-KL46Z	
Drawn by: JOHN PAUL FRANKLIN	Page Title: TITLE PAGE	
Approved: Luis Puebla Palma	Size C	Document Number SCH-27822 | PDF: SPF-27822 Rev B1
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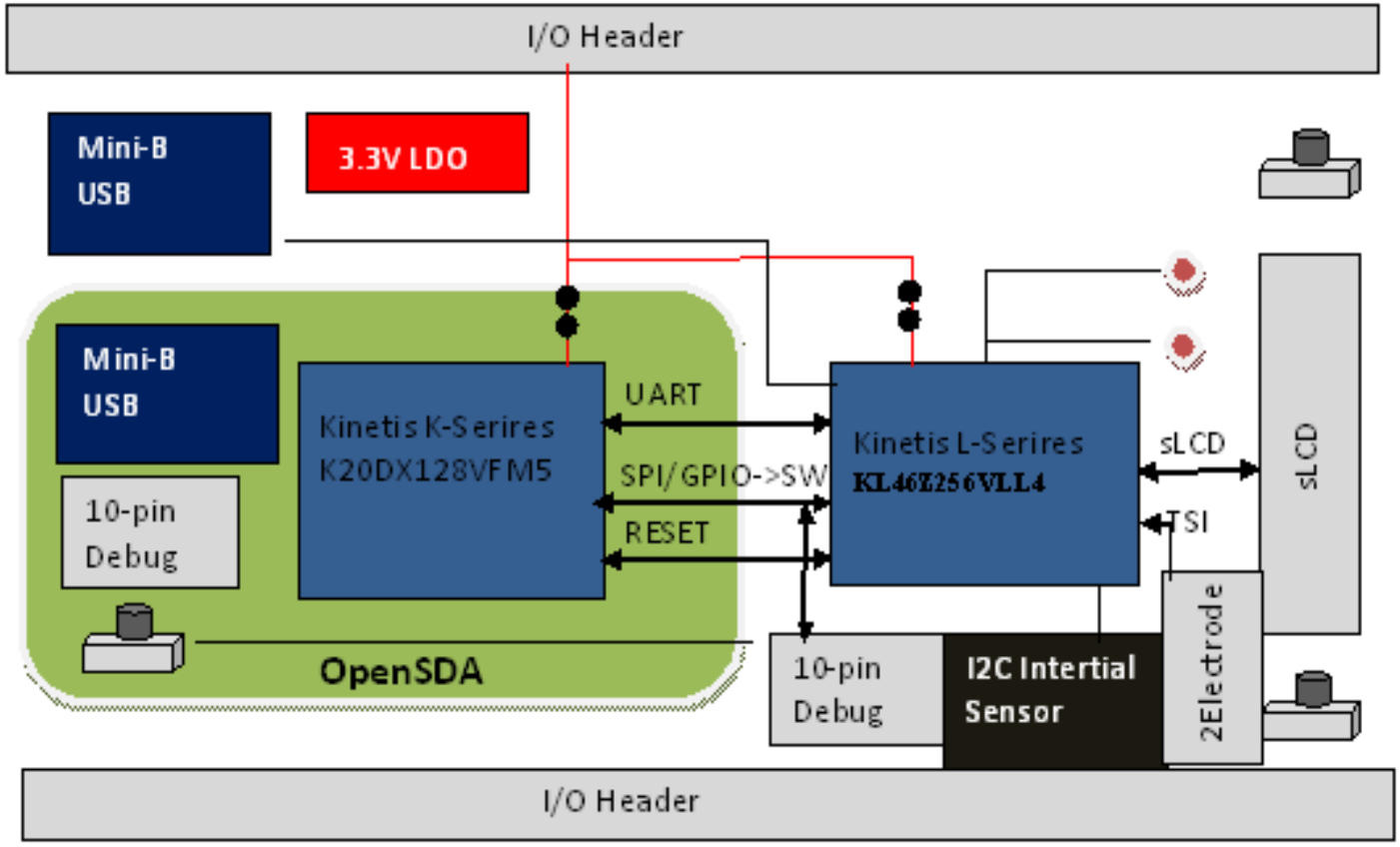
1. Unless Otherwise Specified:
   All resistors are in ohms, 5%, 1/8 Watt
   All capacitors are in uF, 20%, 50V
   All voltages are DC
   All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.



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Drawing Title: **FRDM-KL46Z**

Page Title: **BLOCK DIAGRAM**

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KL46Z Decoupling Caps

Push Buttons

SW1 TL1015AF160QG, C1 1.0UF, GND

SW2 TL1015AF160QG, C32 1.0UF, GND

TSI Capacitive/ Touch Interface

E1, Slider_4

TSI_ELECTRODE1, TSI_ELECTRODE2

SWD CONNECTOR

SHORTING HEADER ON BOTTOM LAYER

Jumper is shorted by a cut-trace on bottom layer. Cutting the trace will effectively isolate the on-board MCU from the OpenSDA debug interface.

J18 HDR 1X2 TH DNP

J11 HDR 2X5 DNP

P3V3_KL46Z, GND

KL25_SWD_CLK, SWD_DIO_TGTMCU, SWD_CLK_TGTMCU [4], RST_K20D50_B [4,5]

USB

KL46_USB_SHLD

J10 CONN USB MINI-B

TP5 DNP, P5V_KL46Z

L2 330 OHM

P5V_KL46_USB_1

KL46_USB_DN, KL46_USB_DP

R10 33, R8 33

USB_DM, USB_DP

KL46_USB_ID, TP9

U3 GSOT05C-GS08

L1 330 OHM

OPTIONAL USB HOST FUNCTIONALITY

KL46_USB_ID, P5V_KL46Z, P5V_SDA

R16 0 DNP

DNP HDR 1X2 TH J16

POPULATE THESE PARTS FOR USB HOST FUNCTIONALITY

ELECTRICAL PROTECTION IS NOT PROVIDED.

USE IT AT YOUR OWN RISK

7 Segment LCD

DS1 LCD-S401M16KR

COM0 LCD-01, COM1 LCD-02, COM2 LCD-03, COM3 LCD-04

1D/1E/1G/1F LCD-05, DP1/1C/1B/1A LCD-06, 2D/2E/2G/2F LCD-07, DP2/2C/2B/2A LCD-08

3D/3E/3G/3F LCD-09, DP3/3C/3B/3A LCD-10, 4D/4E/4G/4F LCD-11, COL/4C/4B/4A LCD-12

LEDs

P3V3

LED1 C D7 A R27 330, LED GREEN

LED2 C D5 A R14 330, LED RED

[4] UART1_RX_TGTMCU, [4] UART1_TX_TGTMCU

R47 1K, R48 1K

J25 D0 D1

KL25_SWD_CLK, [4] SWD_DIO_TGTMCU

EXTAL_8MHZ, XTAL_8MHZ

R31 1.0M, Y1 8MHz, C28 22PF, C26 22PF, GND

RST_K20D50_B

[4] PTC1_SDA, [5] A5

R24 0

[5] A4, SW1

[5] INT1_ACCEL

R20 0

LED1 R11 0, [5] D13

[5] INT2_ACCEL

R41 0

[5] Light_sns, [5] a-A2b

R40 0

U4

PTA0/SWD_CLK/TSI0_CH1/TPM0_CH5
PTA1/TSI0_CH2/UART0_RX/TPM2_CH0
PTA2/TSI0_CH3/UART0_TX/TPM2_CH1
PTA3/SWD_DIO/TSI0_CH4/I2C1_SCL/TPM0_CH0
PTA4/NMI/TSI0_CH5/I2C1_SDA/TPM0_CH1
PTA5/USB_CLKIN/TPM0_CH2/I2S0_TX_BCLK
PTA6/TPM0_CH3
PTA7/TPM0_CH4
PTA12/TPM1_CH0/I2S0_TXD0
PTA13/TPM1_CH1/I2S0_TX_FS
PTA14/SPI0_PCS0/UART0_TX/I2S0_RX_BCLK/I2S0_TXD0
PTA15/SPI0_SCK/UART0_RX/I2S0_RXD0
PTA16/SPI0_MOSI/SPI0_MISO/I2S0_RX_FS/I2S0_RXD0
PTA17/SPI0_MISO/SPI0_MOSI/I2S0_MCLK
PTA18/EXTAL0/UART1_RX/TPM_CLKIN0
PTA19/XTAL0/UART1_TX/TPM_CLKIN1/LPTMR0_ALT1
PTA20/RESET

PTB0/LLWU_P5/LCD_P0/ADC0_SE8/TSI0_CH0/I2C0_SCL/TPM1_CH0
PTB1/LCD_P1/ADC0_SE9/TSI0_CH6/I2C0_SDA/TPM1_CH1
PTB2/LCD_P2/ADC0_SE12/TSI0_CH7/I2C0_SCL/TPM2_CH0
PTB3/LCD_P3/ADC0_SE13/TSI0_CH8/I2C0_SDA/TPM2_CH1
PTB7/LCD_P7
PTB8/LCD_P8/SPI1_PCS0/EXTRG_IN
PTB9/LCD_P9/SPI1_SCK
PTB10/LCD_P10/SPI1_PCS0
PTB11/LCD_P11/SPI1_SCK
PTB16/LCD_P12/TSI0_CH9/SPI1_MOSI/UART0_RX/TPM_CLKIN0/SPI1_MISO
PTB17/LCD_P13/TSI0_CH10/SPI1_MISO/UART0_TX/TPM_CLKIN1/SPI1_MOSI
PTB18/LCD_P14/TSI0_CH11/TPM2_CH0/I2S0_TX_BCLK
PTB19/LCD_P15/TSI0_CH12/TPM2_CH1/I2S0_TX_FS
PTB20/LCD_P16/CMP0_OUT
PTB21/LCD_P17
PTB22/LCD_P18
PTB23/LCD_P19

PTC0/LCD_P20/ADC0_SE14/TSI0_CH13/EXTRG_IN/AUDIOUSB_SOF_OUT/CMP0_OUT/I2S0_TXD0
PTC1/LLWU_P6/RTC_CLKIN/LCD_P21/ADC0_SE15/TSI0_CH14/I2C1_SCL/TPM0_CH0/I2S0_TXD0
PTC2/LCD_P22/ADC0_SE11/TSI0_CH15/I2C1_SDA/TPM0_CH1/I2S0_TX_FS
PTC3/LLWU_P7/LCD_P23/UART1_RX/TPM0_CH2/CLKOUT/I2S0_TX_BCLK
PTC4/LLWU_P8/LCD_P24/SPI0_PCS0/UART1_TX/TPM0_CH3/I2S0_MCLK
PTC5/LLWU_P9/LCD_P25/SPI0_SCK/LPTMR0_ALT2/I2S0_RXD0/CMP0_OUT
PTC6/LLWU_P10/LCD_P26/CMP0_IN0/SPI0_MOSI/EXTRG_IN/I2S0_RX_BCLK/SPI0_MISO/I2S0_MCLK
PTC7/CLD_P27/CMP0_IN1/SPI0_MISO/AUDIOUSB_SOF_OUT/I2S0_RX_FS/SPI0_MOSI
PTC8/LCD_P28/CMP0_IN2/I2C0_SCL/TPM0_CH4/I2S0_MCLK
PTC9/LCD_P29/CMP0_IN3/I2C0_SDA/TPM0_CH5/I2S0_RX_BCLK
PTC10/LCD_P30/I2C1_SCL/I2S0_RX_FS
PTC11/LCD_P31/I2C1_SDA/I2S0_RXD0
PTC12/LCD_P32/TPM_CLKIN0
PTC13/LCD_P33/TPM_CLKIN1
PTC16/LCD_P36
PTC17/LCD_P37
PTC18/LCD_P38

PTD0/LCD_P40/SPI0_PCS0/TPM0_CH0
PTD1/LCD_P41/ADC0_SE5B/SPI0_SCK/TPM0_CH1
PTD2/LCD_P42/SPI0_MOSI/UART2_RX/TPM0_CH2/SPI0_MISO
PTD3/LCD_P43/SPI0_MISO/UART2_TX/TPM0_CH3/SPI0_MOSI
PTD4/LLWU_P14/LCD_P44/SPI1_PCS0/UART2_RX/TPM0_CH4
PTD5/LCD_P45/ADC0_SE6B/SPI1_SCK/UART2_TX/TPM0_CH5
PTD6/LLWU_P15/LCD_P46/ADC0_SE7B/SPI1_MOSI/UART0_RX/SPI1_MISO
PTD7/LCD_P47/SPI1_MISO/UART0_TX/SPI1_MOSI

PTE0/LCD_P48/SPI1_MISO/UART1_TX/RTC_CLKOUT/CMP0_OUT/I2C1_SDA
PTE1/LCD_P49/SPI1_MOSI/UART1_RX/SPI1_MISO/I2C1_SCL
PTE2/LCD_P50/SPI1_SCK
PTE3/LCD_P51/SPI1_MISO/SPI1_MOSI
PTE4/LCD_P52/SPI1_PCS0
PTE5/LCD_P53
PTE6/LCD_P54/I2S0_MCLK/AUDIOUSB_SOF_OUT
PTE16/LCD_P55/ADC0_DP1/ADC0_SE1/SPI0_PCS0/UART2_TX/TPM_CLKIN0
PTE17/LCD_P56/ADC0_DM1/ADC0_SE5A/SPI0_SCK/UART2_RX/TPM_CLKIN1/LPTMR0_ALT3
PTE18/LCD_P57/ADC0_DP2/ADC0_SE2/SPI0_MOSI/I2C0_SDA/SPI0_MISO
PTE19/LCD_P58/ADC0_DM2/ADC0_SE6A/SPI0_MISO/I2C0_SCL/SPI0_MOSI
PTE20/LCD_P59/ADC0_DP0/ADC0_SE0/TPM1_CH0/UART0_TX
PTE21/LCD_P60/ADC0_DM0/ADC0_SE4A/TPM1_CH1/UART0_RX
PTE22/ADC0_DP3/ADC0_SE3/TPM2_CH0/UART2_TX
PTE23/ADC0_DM3/ADC0_SE7A/TPM2_CH1/UART2_RX
PTE24/TPM0_CH0/I2C0_SCL
PTE25/TPM0_CH1/I2C0_SDA
PTE26/TPM0_CH5/RTC_CLKOUT/USB_CLKIN
PTE29/CMP0_IN5/ADC0_SE4B/TPM0_CH2/TPM_CLKIN0
PTE30/DAC0_OUT/ADC0_SE23/CMP0_IN4/TPM0_CH3/TPM_CLKIN1
PTE31/TPM0_CH4

USB_DP, USB_DM

USB0_DP
USB0_DM

MKL46Z256VLL4

P3V3_KL46Z: C7 1.0UF, C23 0.1UF, C9 1.0UF, C18 0.1UF, C19 1.0UF, C22 0.1UF, GND

VDD1 8, VDD2 30, VDD3 48

P3V3_KL46Z, C12 0.1UF, GND

VDDA 22

KL46Z_REGIN

VREGIN 13

J7 HDR 1X2 TH

P5V_KL46Z, R13 0, AREF [5]

P3V3_KL46Z, R17 0, R18 1K DNP

VREFH 23, VREFL 24

C15 0.1UF, GND

CAD NOTE: Place these capacitors near their respective CPU pin (VREFH to VREFL and VDDA to VSSA)

D6 DNP 3.0V

VLL1 77, VLL2 76, VLL3 75

TP10, TP12

VLL1/LCD_P5/PTC21, VLL2/LCD_P4/PTC20

J12 HDR 1X2 TH DNP

TP23, P3V3_KL46Z, C14 0.1UF, C16 0.1UF

VCAP1 79, VCAP2 78

VCAP1/LCD_P39/PTC23, VCAP2/LCD_P6/PTC22

C13 0.1UF

TP11

VOUT33 12

C11 2.2UF, GND

VSS1 9, VSS2 29, VSS3 49, VSS4 74, GND

VSSA 25, GND

ICAP Classification: FCP: ___ FIUO: PUBI: X

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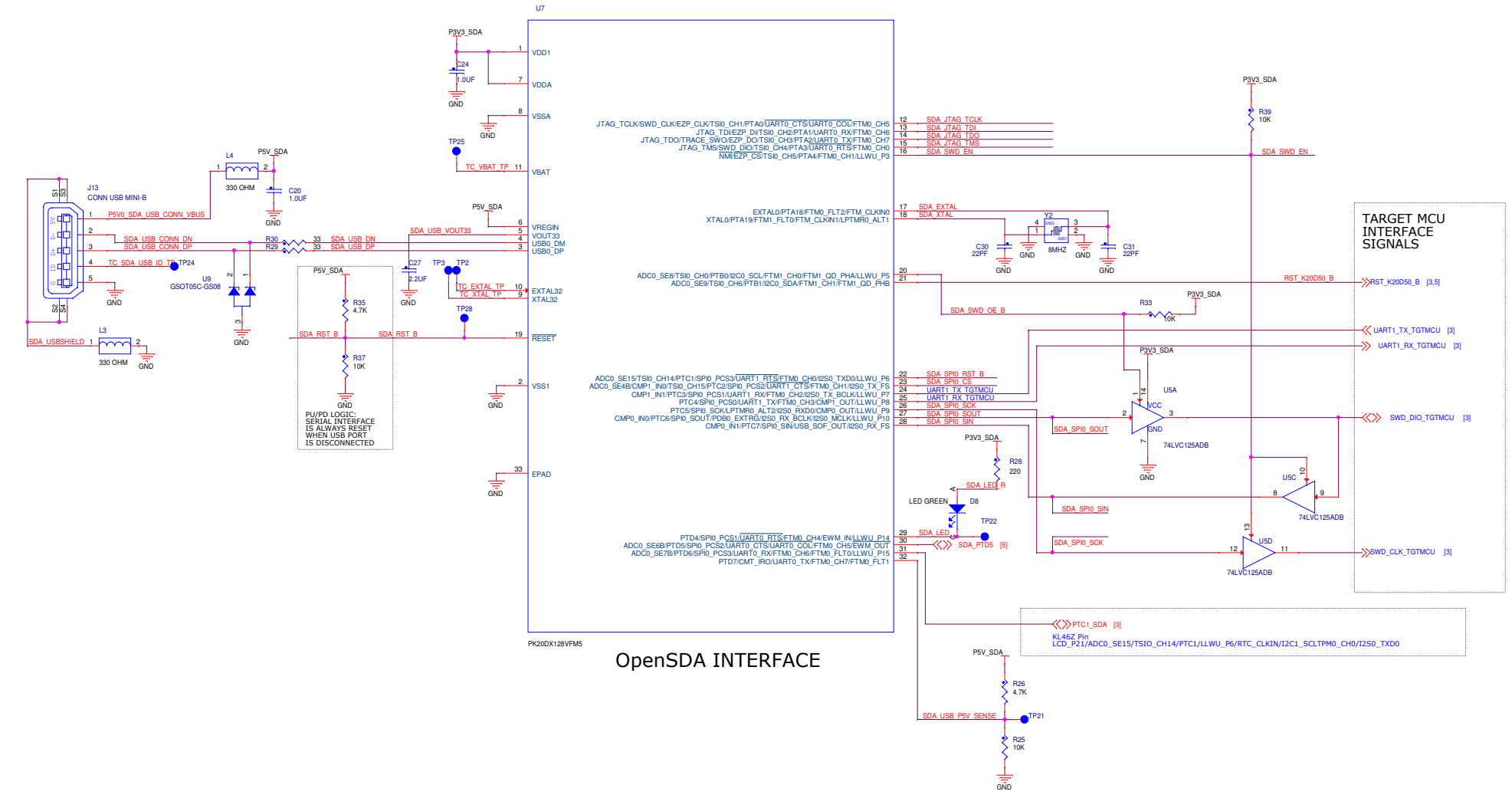

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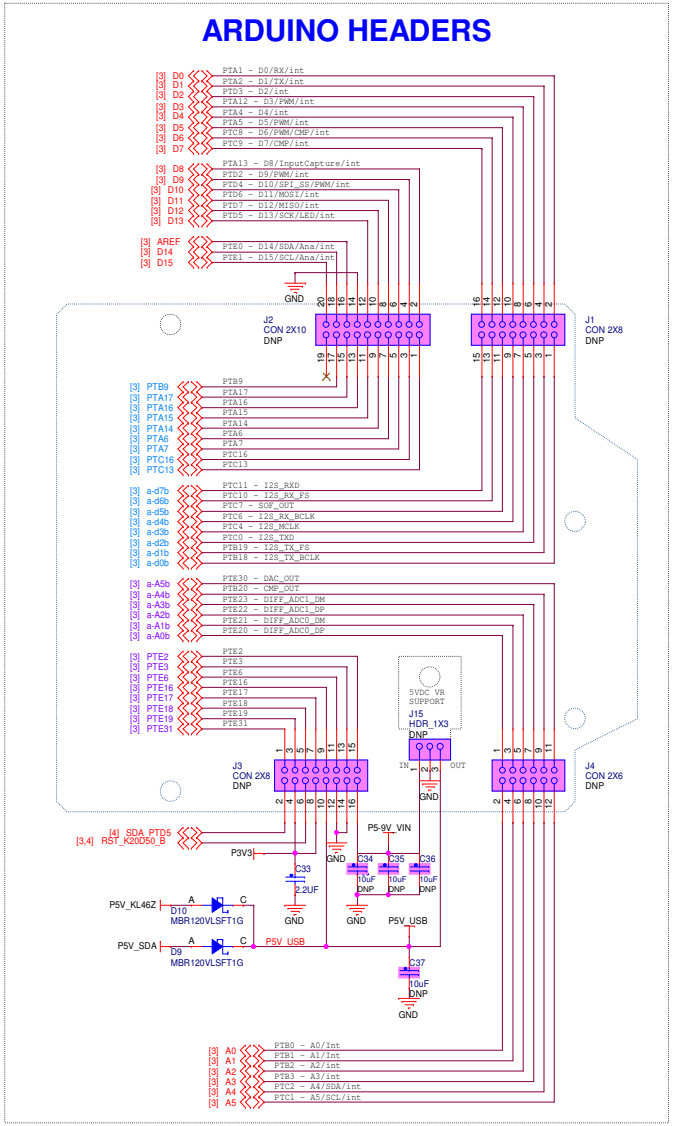
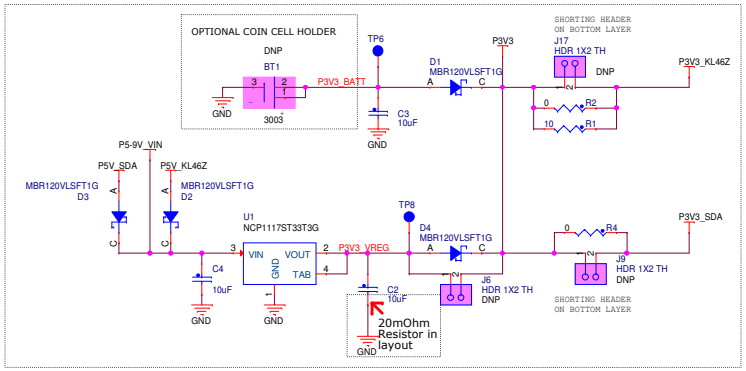
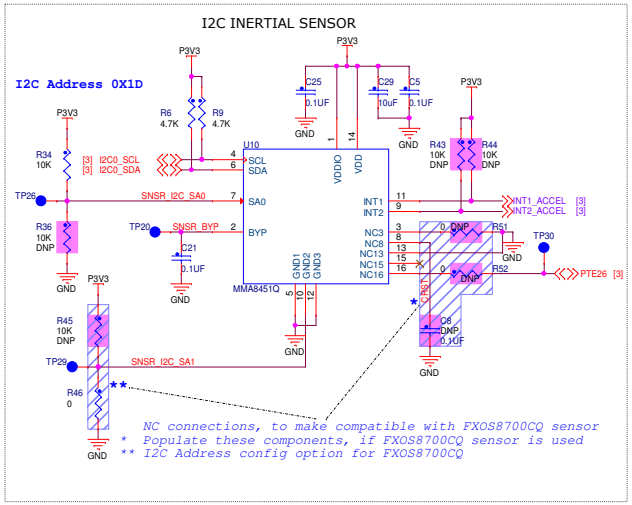
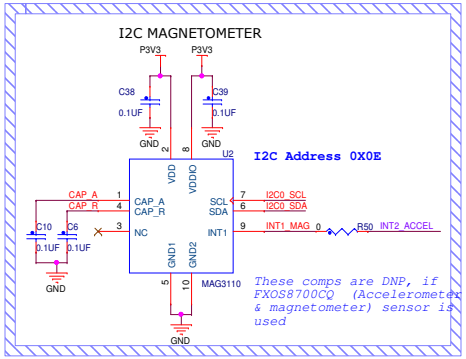
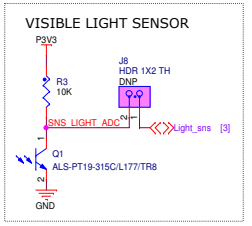
ARDUINO HEADERS

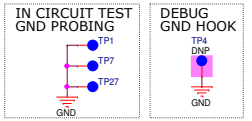












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