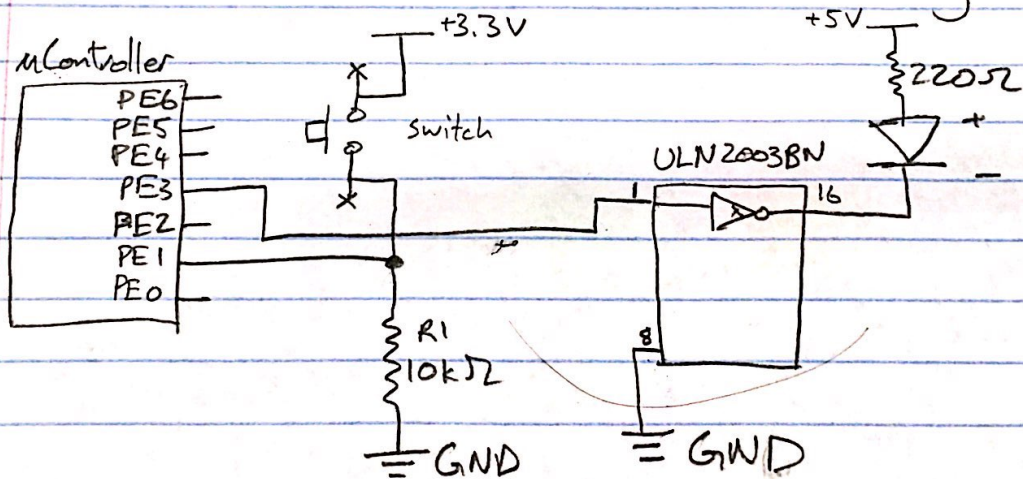


Lab 3 Table

Parameter	Value	Units
Resistance of 10k Ω resistor	9850	Ω
Supply Voltage $V_{+3.3}$	3.3	V
Switch not Pressed		
Input Voltage V_{PE1}	0.0035	V
Resistor Current	0	mA
Switch Pressed		
Input Voltage V_{PE1}	3.3	V
Resistor Current	0.33	mA

	Resistance of 220Ω	216Ω
	5 V Power	5.14 V
Out = 0	V_{PE2} into ULN2003B	0 V
	ULN2003B Out, pin 16 V_k	3.6 V
	LED a^+ , V_{a^+} , anode	5.14 V
	LED Voltage	1.54 V
	LED Current (off)	0 mA calculated & measured
Out = 1	V_{PE2} into ULN2003B	3.229 V
	Pin 16 V_k	0.716 V
	LED anode V_{a^+}	2.602 V
	LED voltage	1.886 V
	LED Current (on)	11.75 mA calculated 11.56 mA measured

Lab 3 Circuit Diagram



Value

0x004B250D
0x00000000
0x00000010
0x00000014
0x00000000
0x00000001
0x000002AC
0x00000004
0x20000030
0x00000284
0x400243FC
0x400253FC
0x00000000
0x20000478
0x0000039D
0x0000047E
0x21000000

Thread

Privileged

MSP

100302498

1.25378543

Logic Analyzer

Setup... Load... Save... ?

Min Time 0 s

Max Time 1.253781 s

Grid 0.1 s

Zoom In Out All

Min/Max Auto Undo

Update Screen Stop Clear

Transition Prev Next

Jump to Code Trace

Signal Info Show Cycles

Amplitude Cursor

4.4082 ms

0.650408 s

1.002408 s, d: 0.352 s

Disassembly

Logic Analyzer

main.s Startup.s

207 LDR R1,=SaveLink

208 LDR LR,[R1]

209 BX LR

210

211

212 delay

213 dloop

214 SUBS R0,#1

215 BNE dloop

216 BX LR

217

218 ALIGN ; make sure the end of th

219 END ; end of file

220

221

TexaS Lab3

Port F Hardware

TM4C123

SW1 PF3 PF4 PF0

SW2

PF1 PF2 LED LED

Port F Registers

DATA: 0x11 PUR: 0x11 LOCK: 0x00

DIR: 0x00 PDR: 0x00 CR: 0x1F

DEN: 0x10 RCGCGPIO: 0x00000039 Clock enabled

Memory 1

Address: 0x2000030

0x02000030: 00000000 00000000 00000000 00000000
0x02000050: 00000000 00000000 00000000 00000000
0x02000070: 00000000 00000000 00000000 00000000
0x02000090: 00000000 00000000 00000000 00000000
0x020000B0: 00000000 00000000 00000000 00000000
0x020000D0: 00000000 00000000 00000000 00000000
0x020000F0: 00000000 00000000 00000000 00000000
0x02000110: 00000000 00000000 00000000 00000000

Call Stack + Locals Watch 1 Memory 1

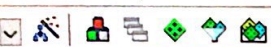
Simulation

211

defined line number

0x00000008) >> 3
0x00000008) >> 3 & 0x8) >> 3
0x00000004) >> 2 & 0x4) >> 2
0x00000008) >> 3 & 0x8) >> 3

BreakEnable BreakKill BreakList BreakSet BreakAccess COVERAGE COVTOFILE



main.s Startup.s

```

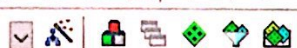
28 ;      TIP: debugging the breathing LED algorithm using the real board.
29 ; PortE device registers
30 GPIO_PORTE_DATA_R EQU 0x400243FC
31 GPIO_PORTE_DIR_R  EQU 0x40024400
32 GPIO_PORTE_AFSEL_R EQU 0x40024420
33 GPIO_PORTE_DEN_R  EQU 0x4002451C
34 ; PortF device registers
35 GPIO_PORTF_DATA_R EQU 0x400253FC
36 GPIO_PORTF_DIR_R  EQU 0x40025400
37 GPIO_PORTF_AFSEL_R EQU 0x40025420
38 GPIO_PORTF_PUR_R   EQU 0x40025510
39 GPIO_PORTF_DEN_R   EQU 0x4002551C
40 GPIO_PORTF_LOCK_R  EQU 0x40025520
41 GPIO_PORTF_CR_R    EQU 0x40025524
42 GPIO_LOCK_KEY      EQU 0x4C4F434B ; Unlocks the GPIO_CR register
43 SYSTCL_RCGCGPIO_R EQU 0x400FE608
44
45
46     IMPORT TExaS_Init
47     THUMB
48     AREA    DATA, ALIGN=2
49 ;global variables go here
50 Index SPACE 4
51 Index2 SPACE 4
52 SaveLink SPACE 4
53     AREA    |.text|, CODE, READONLY, ALIGN=2
54     THUMB
55     EXPORT  Start
56 CArr DCD 2000000, 4670000, 3300000, 3300000, 4670000, 2000000, 5950000, 660000, 660000, 5950000, 3000000, 7000000,
57 Breath DCD 15000/2, 135000/2, 45000/2, 105000/2, 75000/2, 75000/2, 105000/2, 45000/2, 135000/2, 15000/2
58 Start
59 ; TExaS_Init sets bus clock at 80 MHz

```

```

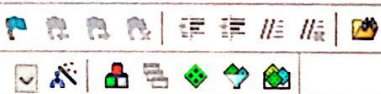
55      EXPORT Start
56 CArr DCD 2000000, 4670000, 3300000, 3300000, 4670000, 2000000, 5950000, 660000, 660000, 5950000 ;3000000,
57 Breath DCD 15000/2, 135000/2, 45000/2, 105000/2, 75000/2, 75000/2, 105000/2, 45000/2, 135000/2, 15000/2
58 Start
59 ; TExaS_Init sets bus clock at 80 MHz
60 BL TExaS_Init ; voltmeter, scope on PD3
61 LDR R0,=SYSCCTL_RCGCGPIO_R ;turn on Port E and Port F clock
62 LDR R1,[R0]
63 ORR R1,#0x30
64 STR R1,[R0]
65 NOP
66 NOP
67 NOP
68 NOP
69 LDR R0,=GPIO_PORTE_DIR_R ;Set PE1 as input, PE3 as output
70 LDR R1,[R0]
71 ORR R1,#0x08
72 BIC R1,#0x02
73 STR R1,[R0]
74 LDR R0,=GPIO_PORTF_DIR_R ;Set PF4 as input
75 LDR R1,[R0]
76 BIC R1,#0x10
77 STR R1,[R0]
78 LDR R0,=GPIO_PORTE_DEN_R ;Digitally enable PE1 and PE3
79 LDR R1,[R0]
80 ORR R1,#0x0A
81 STR R1,[R0]
82 LDR R0,=GPIO_PORTF_DEN_R ;Digitally enable PF4
83 LDR R1,[R0]
84 ORR R1,#0x10
85 STR R1,[R0]
86 LDR R0,=GPIO_PORTF_LOCK_R

```

main.s Startup.s

```
88     STR R1,[R0]
89     LDR R0,=GPIO_PORTF_CR_R
90     LDR R1,[R0]
91     ORR R1,#0xFF
92     STR R1,[R0]
93     LDR R0,=GPIO_PORTF_PUR_R      ;Set Pull up resistor for PF4
94     LDR R1,[R0]
95     ORR R1,#0x11
96     STR R1,[R0]
97     LDR R8,=Index
98     MOV R1,#0
99     STR R1,[R8]
100    STR R1,[R8,#4]
101    LDR R9,=CArr
102    LDR R6,=Breath
103    LDR R10,=GPIO_PORTE_DATA_R      ;Reserved Regs, R0-count R8-Index R9-Array R10-PortE R6-Breath R11-PortF R12-Index
104    LDR R11,=GPIO_PORTF_DATA_R
105    CPSIE I      ; TExaS voltmeter, scope runs on interrupts
106    loop
107    LDR R1,[R10]
108    BL  check
109    MOV R5,#1
110    MOV R12,#0
111    BL  breathingstr
112    LDR R1,[R10]
113    ORR R1,#0x08
114    STR R1,[R10]
115    LDR R7,[R8]
116    LDR R0,[R9,R7]
117    BL  delay
118    LDR R1,[R10]
119    BIC R1,#0x08
```

main.s Startup.s

```
118    LDR R1, [R10]
119    BIC R1, #0x08
120    STR R1, [R10]
121    LDR R7, [R8]
122    ADD R7, #4
123    STR R7, [R8]
124    LDR R0, [R9, R7]
125    BL delay
126    LDR R7, [R8]
127    SUB R7, #4
128    STR R7, [R8]
129    LDR R0, [R9, R7]
130    B   loop
131
132 check
133    AND R2, R1, #0x02
134    LSR R2, #1
135    CMP R2, #1
136    BNE skip
137    LDR R7, [R8]
138    CMP R7, #32
139    BEQ redo
140    ADD R7, #8
141    STR R7, [R8]
142    B   skip
143 redo
144    SUB R7, #32
145    STR R7, [R8]
146 skip
147    LDR R1, [R10]
148    AND R2, R1, #0x02
149    CMP R2, #0
```

I

```

145     STR R7, [R8]
146 skip
147     LDR R1, [R10]
148     AND R2, R1, #0x02
149     CMP R2, #0
150     BNE skip
151     BX LR
152
153 breathingr
154     LDR R1, =SaveLink
155     STR LR, [R1]
156 breathing
157     LDR R1, [R11]
158     AND R2, R1, #0x10
159     CMP R2, #0x10
160     BEQ done
161
162     MOV R2, #12
163 sameduty
164     LDR R1, [R10]
165     ORR R1, #0x08
166     STR R1, [R10]
167     LDR R7, [R8, #4]
168     LDR R0, [R6, R7]
169     BL delay
170     LDR R1, [R10]
171     BIC R1, #0x08
172     STR R1, [R10]
173     LDR R7, [R8, #4]
174     ADD R7, #4
175     STR R7, [R8, #4]
176     LDR R0, [R6, R7]

```

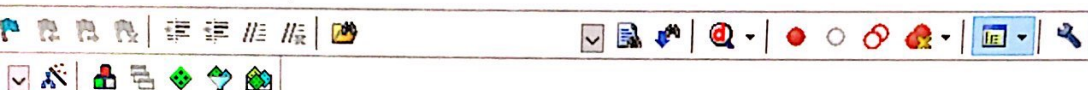
I



main.s Startup.s

```
169 BL delay
170 LDR R1,[R10]
171 BIC R1,#0x08
172 STR R1,[R10]
173 LDR R7,[R8,#4]
174 ADD R7,#4
175 STR R7,[R8,#4]
176 LDR R0,[R6,R7]
177 BL delay
178 LDR R7,[R8,#4]
179 SUB R7,#4
180 STR R7,[R8,#4]
181 SUBS R2,#1
182 BNE sameduty
183 CMP R5,#1
184 BEQ continue
185 LDR R7,[R8,#4]
186 CMP R7,#32
187 BEQ setmask
188 CMP R7,#0
189 BEQ setmask
190 CMP R12,#1
191 BEQ subtract
192 BNE continue
193 setmask
194 EOR R12,#1
195 CMP R12,#1
196 BNE continue
197 subtract
198 SUB R7,#8
199 STR R7,[R8,#4]
200 R breathing
```

I



main.s Startup.s

```
191     BEQ subtract
192     BNE continue
193 setmask
194     EOR R12,#1
195     CMP R12,#1
196     BNE continue
197 subtract
198     SUB R7,#8
199     STR R7,[R8,#4]
200     B breathing
201 continue
202     BIC R5,#1
203     ADD R7,#8
204     STR R7,[R8,#4]
205     B breathing
206 done
207     LDR R1,=SaveLink
208     LDR LR,[R1]
209     BX LR
210
211
212 delay
213 dloop
214     SUBS R0,#1
215     BNE dloop
216     BX LR
217
218     ALIGN      ; make sure the end of this section is aligned
219     END        ; end of file
220
221
```