**Tendayi Kamucheka**
Ph.D. Candidate
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## Summary

Highly motivated and results-driven professional with a proven track record in delivering solutions across various technologies in business and research settings. Background in software and hardware development with strong skills in machine learning compiler design, FPGA accelerator design, post-quantum cryptography, GPU high-performance computing, and web development. Committed to delivering excellence and exceeding expectations in every task.

## Education

- **University of Arkansas** — Fayetteville, AR
  *Doctor of Philosophy Computer Engineering* — *Jan. 2019 – May. 2026 (Expected)*
- **University of Arkansas** — Fayetteville, AR
  *Master of Science Computer Engineering* — *Jan. 2019 – May. 2026 (cf.)*
- **Nanjing University of Aeronautics & Astronautics** — Nanjing, China
  *Bachelor of Engineering in Software Engineering* — *Sept. 2012 – July. 2016*

## Research

- **Compiler Design**
  *Compiler for Machine Learning models on FPGA* — *ANTLR4, LLVM, MLIR, C++, Verilog*
  - **Compiler Driven HW/SW Co-Design of Deep Learning Accelerators *(Fall 2022 - Current)***:
    - Developed a functional simulator for a custom FPGA-based SIMD accelerators.
    - Developed RISC-V-like ISA, assembly language, and assembler as a compilation target for custom accelerators.
    - Designed performance characterization benchmark for FPGA PIM overlays
    - Designed Treesitter grammar and plugin for syntax highlighting of assembly language in Neovim.
    - Implemented dialects in MLIR tailored for 2-D SIMD array accelerators.
    - Implemented RTL clock domain crossing logic and read-write channel FIFO buffering based on AXI Stream for custom accelerator.
    - Actively developing a compiler for deep learning models in ONNX format targeting custom accelerators on FPGA and ASICs. (Ph.D. Dissertation Topic)
- **FPGA Functional Testing**
  *Vendor independent functional testing and counterfeit hardware detection* — *Verilog, VHDL, Python, Linux*
  - **CIFT - Independent Functional Testing, Path Delay Project *(Summer 2022)***:
    - Designed and implemented Verilog/VHDL slice-level functional tests for Xilinx 7-series devices.
    - Implemented IP-level parameterized Slice (LOC) targeting and custom (LUT-to-FF) signal routing.
- **FPGA RTL Design**
  *Quantum computer resistant cryptography* — *C/C++, Verilog, Python, JavaScript, Linux*
  - **NIST Post Quantum Cryptography Standardization Process *(Summer 2020 - 2022)***:
    - Evaluated candidate post-quantum cryptography algorithms against power analysis side-channel-assisted attacks.
    - Implemented reference and dual rail masked side-channel-resistant RTL designs for CRYSTALS-Kyber on Virtex-7 devices.
    - Modified Xilinx FPGA development board PCBs to add probe leads for current measurement with an oscilloscope.
    - Created software for automating power trace collection on oscilloscope and Differential Power Analysis using Python over UART and Ethernet VISA protocols.
    - Supported future project development with training and mentoring for new graduate students.

- **GPU Accelerated High-Performance Computing**
  *Leveraging graphics processing units for parallel computation* *C/C++, CUDA, R, Matlab, Linux*
  - **Computational Electromagnetics *(Spring 2019 - Summer 2020)***:
    - Created a software library in C++ for finite-difference time-domain electromagnetic simulations.
    - Implemented C++ code for antenna simulations using the Acceleware FDTD library.
  - **Statistical Learning *(Fall 2019)***:
    - Created an R package for simulating particle systems using Sequential Monte Carlo and Markov Chains.
    - Implemented parallel algorithms for learning statistical distributions of data streams on CUDA GPUs.
    - Applications: Statistical learning for weather system predictions, pattern predictions (e.g. wildfire path prediction)
  - **Distributed Computing *(Aug 2016 - Dec 2017)***:
    - Deployed volunteer-based distributed computing server using Berkeley Open Infrastructure for Network Computing (BOINC).
    - Implemented rainbow-table-based password recovery server applications using BOINC distributed infrastructure.
    - Developed distributed client CUDA GPU applications for password recovery.

## Experience

- **University of Arkansas** Fayetteville, AR
  *Senior Graduate Assistant* *Jan 2019 - Present*
  - **Research Assistant**: FPGA RTL Design, Compilers, & High Performance Computing
  - **Teaching Assistant**: Embedded Systems, Computer Organization & Database Management Systems

- **University of Southern California - Information Sciences Institute** Arlington, VA
  *Visiting Research Assistant* *May 2022 - August 2022*
  - **CIFT - Independent FPGA Functional Testing, Path Delay Project**: FPGA RTL Design

- **Purple Lite Media** Nanjing, China
  *Founder, Software Engineer* *September 2016 - March 2018*
  - **Description**: Established a dynamic startup specializing in web development and social media marketing, catering to expatriate entrepreneurs engaged in export ventures within China. Our flagship offerings revolved around custom information systems for client relations and inventory logistics. We implemented secure private cloud storage and email infrastructure while crafting compelling social media branding strategies and executing targeted marketing campaigns.
  - **Roles**:
    - Managed a team of 3 software developers and 2 content creators.
    - Served as the principal developer and solution architect on software development projects.
    - Responsible for project management activities including milestone planning, task assignments, tracking, and delivery.
  - **Technologies Experience**:
    - **Web Frameworks:** WordPress, React, and Ruby On Rails
    - **Automated Email:** Mailgun
    - **Hosting:** Heroku, DigitalOcean, and HostGator
    - **DNS/CDN:** CloudFlare
    - **CI/CD:** GitHub and Capistrano

- **Fullbright Tutors South Africa - Private Tutoring Company** Pretoria, South Africa
  *Software Engineer (Remote)* *2012 - 2015*
  - **Web Developer**:
    * Designed and deployed Drupal, WordPress, and Ruby on Rails websites.
    * Implemented a management information system for clientele, course offerings, scheduling, and tutor/student matching.
    * Implemented landing pages for professional training programs aimed at the Pretoria local government.
    * Implemented a double-blind peer-review e-journal platform.

- **Lifemark Computers** Harare, Zimbabwe
  *Computer Technician* *2011 - 2012*
  - **Computer Repair**: Performed desktop/laptop computer repair and maintenance.
  - **Network Installation**: Installed indoor and outdoor Wi-Fi and Wi-Max networking solutions for customers in rural Zimbabwe
  - **Hardware Installation**: Designed and installed classroom computer networks with teaching servers and thin client student terminals.

- **Scotehcorp Micro-finance Company** Harare, Zimbabwe
  *Software Developer* *2010 - 2011*
  - **Clientele Management Information System**: Developed a custom customer relations management (CRM) application with MS Access and VB.Net. for handling the processing of microloan lending for an average of 200 monthly customers.
  - **API Integration**: Implemented API integration with the Zimbabwe Salary Services Bureau to process automatic payroll deductions for government employee clientele.

## Publications

- Kabir, M. A., Fredricks, N., **Kamucheka, T.**, Mandebi, J., Huang, M., Bakos, J. D., & Andrews, D. (2025). DA-VinCi: A Deep-Learning Accelerator Overlay Using In-Memory Computing. ACM Transactions on Reconfigurable Technology and Systems, 18(4), 1-38.

- **Kamucheka, T.**, & Andrews, D. (2024, May). Ph. D. Project: A Compiler-Driven Approach to HW/SW Co-Design of Deep-Learning Accelerators. In 2024 IEEE 32nd Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM) (pp. 237-238). IEEE.

- Kabir, M. A., **Kamucheka, T.**, Fredricks, N., Mandebi, J., Bakos, J., Huang, M., & Andrews, D. (2024, September). IMAGine: An In-Memory Accelerated GEMV Engine Overlay. In 2024 34th International Conference on Field-Programmable Logic and Applications (FPL) (pp. 220-226). IEEE.

- Kabir, M. A., **Kamucheka, T.**, Fredricks, N., Mandebi, J., Bakos, J., Huang, M., & Andrews, D. (2024, May). The BRAM is the Limit: Shattering Myths, Shaping Standards, and Building Scalable PIM Accelerators. In 2024 IEEE 32nd Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM) (pp. 223-223). IEEE.

- **Kamucheka, T.**, Nelson, A., Andrews, D., & Huang, M. (2022, December). A masked pure-hardware implementation of Kyber cryptographic algorithm. In 2022 International Conference on Field-Programmable Technology (ICFPT) (pp. 1-1). IEEE.

- **Kamucheka, T.**, Fahr, M., Teague, T., Nelson, A., Andrews, D., & Huang, M. (2021). Power-based side-channel attack analysis on PQC algorithms. Cryptology ePrint Archive.

- **Kamucheka, T.**, Gui, Z., Huang, M., Churchill, H., & El-Shenawee, M. (2020, July). Benchmark of Acceleware vs. XFdtd for Field Simulations of Microstrip Patch Antenna. In 2020 International Applied Computational Electromagnetics Society Symposium (ACES) (pp. 1-2). IEEE.

## Awards

- **University Of Arkansas**:
  - Reginald R. "Barney" & Jameson A. Baxter Graduate Fellowship. (2022, 2023)
  - Dept. of Electrical Engineering & Computer Science Scholarship. (2022, 2023)
- **Nanjing University of Aeronautics & Astronautics**:
  - Nanjing Municipal Government Scholarship. (2015, 2016)
  - Nanjing University of Aeronautics & Astronautics Scholarship. (2016)

## Extracurricular

- **Leisure Activities**:
  - An avid fisherman - I enjoy saltwater fishing.
  - Hobby PCB circuit design - I designed a Raspberry Pi-based 3D printed infotainment system for Android Auto Calling/Navigation, audio DAC integration, and OBD data display.
- **Free Geek Arkansas**: Volunteered to help re-purpose and recycle e-waste.
- **IEEE-HKN Sigma Phi Chapter**: Active member. Former Vice President (2022-2023)