Introduction to CSED311 Lab

Sanghwan Jang
jsh710101@postech.ac.kr

Lab Information

- TAs:
  - Sangyoun Kwak (ksy109@postech.ac.kr)
  - Sanghwan Jang (jsh710101@postech.ac.kr)
  - Byounghoon So (sbh4728@postech.ac.kr)
  - Jaejun Ha (dreamline91@postech.ac.kr)

- POVIS LMS as the default lab homepage
  - Announcements, Materials, Experiments, etc.

Lab Coverage

- Verilog (Lab 0-2)
  - Hardware Description Language
  - ModelSim: Design & Simulation Tool
- CPU Design in Verilog (Lab 3-7)
  - Register
  - Datapath
  - Control Unit
  - Pipelined CPU
  - Cache
  - DMA
- Advanced cache replacement policy (Lab 8)

Lab 8: Advanced Cache Replacement Policy

- You will evaluate a high-performance cache replacement policy called RRIP (Re-Reference Interval Prediction)
  - Paper: Jaleel et al., "High performance cache replacement using re-reference interval prediction (RRIP)," ISCA'10
- Read the paper and implement & evaluate SRRIP-HP policy on a C++-based simulator
  - More information on the simulator available at https://crc2.ece.tamu.edu/
  - Please use the simulator and traces that will be made available on LMS
- Extra points
  - +5% if you also implement DRRIP
  - Another +5% if you also implement TA-DRRIP

Lab Schedule

Week	Date	Topic
1	2/19	Lab 0: Lab Introduction
2	2/26	Lab 1: Verilog Introduction
3	3/5	Lab 2: RTL Design (Vending Machine)
4	3/12	Lab 3: Single-Cycle CPU
5	3/19	Lab 4: Multi-Cycle CPU
6	3/26	-
7	4/2	Lab 5: Pipelined CPU
8	4/9	MIDTERM EXAM
9	4/16	-
10	4/23	Lab 6: Cache
11	4/30	-
12	5/7	Lab 7: DMA
13	5/14	Lab 8: Cache Replacement Policy
14	5/21	-
15	5/28	-
16	6/4	FINAL EXAM

Grading

- Overall (100%)
  - Midterm Exam: 25%
  - Final Exam: 25%
  - Labs: 35%
  - HW: 8%
  - Quiz (or paper critique): 7%

- **Labs (35%)**
  - Report: 20%
  - Demonstration: 80%

Lab score allocation:

Lab	Score weight (%)
Lab 1 (ALU)	1
Lab 2 (Vending machine)	4
Lab 3 (Single-cycle CPU)	10
Lab 4 (Multi-cycle CPU)	20
Lab 5 (Pipelined CPU)	30
Lab 6 (Cache)	15
Lab 7 (DMA)	5
Lab 8 (Advanced cache replacement policy)	15
Total	**100**

Rule

- Each team has 1-day late submission token
  - You can submit 1-day late without any penalty.
  - If you want to use it, let the TA know at the time of submission.
- Score deduction for late submission (when the token is not used)
  - 1 day late → -10%
  - 2 days late → -20%
  - 3 days late → -50%
  - 4+ days late → zero score
    (and you may still need to finish it for the next lab)
- **Cheating**
  - 'F' grade (NO EXCEPTION)

Timetable

- Hand in the report for the previous experiment
  - 1 min
- Lab Quiz
  - 5 mins
- Explanation of the next experiment
  - 20 mins
- Demonstration for the previous experiment
  - ? mins

Group

- Make a group
  - 2 people in 1 group
  - For 1-person group: 10% additional points for lab session
  - Send an e-mail to TA until 2/24 (Sun) 23:59
    - Sanghwan Jang (jsh710101@postech.ac.kr)
  - If you don’t send the e-mail, team member will be randomly assigned